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# Power MOSFETs

ON Semiconductor™

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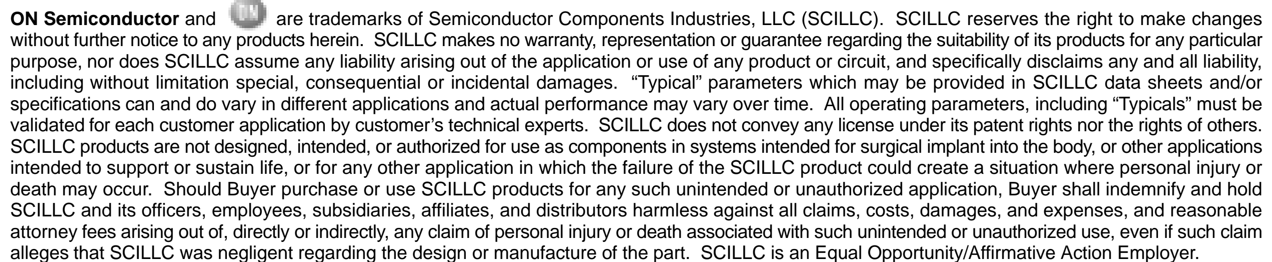
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| MTP50N06VL | Power MOSFET 42 Amps, 60 Volts, Logic Level N–Channel TO–220 | 1255 |
| MTP50P03HDL | Power MOSFET 50 Amps, 30 Volts, Logic Level P–Channel TO–220 | 1261 |
| MTP52N06V | Power MOSFET 52 Amps, 60 Volts N–Channel TO–220 | 1268 |
| MTP52N06VL | Power MOSFET 52 Amps, 60 Volts, Logic Level N–Channel TO–220 | 1274 |
| MTP5P06V | Power MOSFET 5 Amps, 60 Volts P–Channel TO–220 | 1280 |
| MTP60N06HD | Power MOSFET 60 Amps, 60 Volts N–Channel TO–220 | 1286 |
| MTP6P20E | Power MOSFET 6 Amps, 200 Volts P–Channel TO–220 | 1293 |
| MTP75N03HDL | Power MOSFET 75 Amps, 25 Volts, Logic Level N–Channel TO–220 | 1299 |
| MTP75N05HD | Power MOSFET 75 Amps, 50 Volts N–Channel TO–220 | 1306 |
| MTP75N06HD | Power MOSFET 75 Amps, 60 Volts N–Channel TO–220 | 1313 |
| MTP7N20E | Power MOSFET 7 Amps, 200 Volts N–Channel TO–220 | 1320 |
| MTSF1P02HD | Power MOSFET 1 Amp, 20 Volts P–Channel Micro8™ | 1326 |
| MTSF3N02HD | Power MOSFET 3 Amps, 20 Volts N–Channel Micro8™ | 1337 |
| MTSF3N03HD | Power MOSFET 3 Amps, 30 Volts N–Channel Micro8™ | 1348 |
| MTW32N20E | Power MOSFET 32 Amps, 200 Volts N–Channel TO–247 | 1359 |
| MTW32N25E | Power MOSFET 32 Amps, 250 Volts N–Channel TO–247 | 1365 |
| MTW35N15E | Power MOSFET 35 Amps, 150 Volts N–Channel TO–247 | 1371 |
| MTW45N10E | Power MOSFET 45 Amps, 100 Volts N–Channel TO–247 | 1377 |
| MTY55N20E | Power MOSFET 55 Amps, 200 Volts N–Channel TO–264 | 1383 |
| VN0300L | Small Signal MOSFET 200 mAmps, 60 Volts N–Channel TO–92 | 1389 |
| VN2222LL | Small Signal MOSFET 150 mAmps, 60 Volts N–Channel TO–92 | 1391 |
| VN2406L | Small Signal MOSFET 200 mAmps, 240 Volts N–Channel TO–92 | 1394 |
| VN2410L | Small Signal MOSFET 200 mAmps, 240 Volts N–Channel TO–92 | 1396 |

# Power MOSFET Selector Guide

**Table 1. ChipFET – Case 1206A**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.5 V (Ω) | 1.8 V (Ω) | $I_D$ (cont) Amps (Note 8.) | Device (Note 3.) | $P_D$ (Notes 1. & 2.) (Watts) Max | Configuration | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 30 | 0.035 | 0.055 | – | – | 6.7 | ***NTHS5402T1*** | 1.3 | Single N–Channel | 95 |
| | 0.085 | 0.143 | – | – | 3.9 | ***NTHD5902T1*** | 1.1 | Dual N–Channel | 80 |
| 20 | – | 0.03 | 0.045 | – | 7.2 | ***NTHS5404T1*** | 1.3 | Single N–Channel | 106 |
| | – | 0.075 | 0.0134 | – | 4.2 | ***NTHD5904T1*** | 1.1 | Dual N–Channel | 90 |
| | – | 0.060 (Note 7.) | 0.083 | – | 5.3 | ***NTHS5441T1*** | 1.3 | Single P–Channel | 109 |
| | – | 0.065 | 0.110 | – | 4.7 | ***NTHS5443T1*** | 1.3 | Single P–Channel | 112 |
| | – | 0.155 | 0.260 | – | 2.9 | ***NTHD5903T1*** | 1.1 | Dual P–Channel | 85 |
| 8 | – | 0.035 | 0.047 | 0.062 | 7.1 | ***NTHS5445T1*** | 1.3 | Single P–Channel | 114 |
| | | 0.09 | 0.13 | 0.18 | 4.1 | ***NTHD5905T1*** | 1.1 | Dual P–Channel | 95 |

**Table 2. SO-8 (MiniMOS™) – Case 751–06**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 4.) | $P_D$ (Notes 1. & 2.) (Watts) Max | Configuration (Note 6.) | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 60 | – | 0.130 (Note 5.) | – | – | 3.3 | ***MMDF3N06VLR2*** | 2.0 | Dual N–Channel | 540 |
| | 0.100 | 0.200 | – | – | 3.3 | ***MMDF3N06HDR2*** | 2.0 | Dual N–Channel | 531 |
| 50 | 0.300 | 0.500 | – | – | 1.5 | ***MMDF1N05ER2*** | 2.0 | Dual N–Channel | 399 |
| 40 | 0.080 | 0.100 | – | – | 3.4 | ***MMDF3N04HDR2*** | 2.0 | Dual N–Channel | 521 |
| 30 | 0.030 | 0.039 | – | – | 7.0 | ***MMSF1308R2*** | 2.5 | Single N–Channel | 681 |
| | 0.015 | 0.019 | – | – | 10.0 | ***MMSF1310R2*** | 2.5 | Single N–Channel | 689 |
| | 0.0125 | 0.020 | – | – | 11.5 | ***MMSF3300R2*** | 2.5 | Single N–Channel | 705 |
| | 0.040 | 0.050 | – | – | 6.5 | ***MMSF5N03HDR2*** | 2.5 | Single N–Channel | 733 |
| | 0.028 | 0.040 | – | – | 8.2 | ***MMSF7N03HDR2*** | 2.5 | Single N–Channel | 742 |
| | 0.085 | 0.115 | – | – | 3.05 | ***NTMS3P03R2*** | 2.5 | Single P–Channel | 150 |
| | 0.070 | 0.075 | – | – | 4.1 | ***MMDF3N03HDR2*** | 2.0 | Dual N–Channel | 512 |
| | 0.035 | 0.050 | – | – | 6.0 | ***MMDF6N03HDR2*** | 2.0 | Dual N–Channel | 560 |
| | 0.085 | 0.125 | – | – | 3.05 | ***NTMD3P03R2*** | 2.0 | Dual P–Channel | 120 |
| | 0.070/0.200 | 0.075/0.300 | – | – | 4.1 | ***MMDF2C03HDR2*** | 2.0 | Complementary | 439 |
| 25 | 0.100/0.210 | 0.160/0.375 | – | – | 3.0/2.0 | ***MMDF1300R2*** | 1.8 | Complementary | 396 |
| 20 | 0.025 | 0.040 | – | – | 8.2 | ***MMSF5N02HDR2*** | 2.5 | Single N–Channel | 724 |
| | – | 0.045 | 0.055 | – | 4.0 | ***NTMS4N01R2*** | 2.5 | Single N–Channel | 157 |
| | 0.250 | 0.400 | – | – | 2.5 | ***MMSF2P02ER2*** | 2.5 | Single P–Channel | 697 |
| | 0.075 | 0.095 | – | – | 5.6 | ***MMSF3P02HDR2*** | 2.5 | Single P–Channel | 715 |
| | – | 0.033 | – | 0.048 | 5.4 | ***NTMS5P02R2*** | 2.5 | Single P–Channel | 171 |
| | – | 0.014 | – | 0.020 | 10.0 | ***NTMS10P02R2*** | 2.5 | Single P–Channel | 143 |

1. $T_C$ = 25°C
2. See Data Sheet for Applicable Mounting Configuration.
3. Available in Tape and Reel only. T1 suffix = 3000 per reel.
4. Available in Tape and Reel only. R2 suffix = 2500 per reel.
5. $V_{GS}$ = 5.0 V
6. Data for all Complementary Devices listed as Nch/Pch.
7. $V_{GS}$ = 3.6 V
8. t ≤ 5 sec

Devices listed in ***bold, italic*** are ON Semiconductor preferred devices.

**Table 2. SO-8 (MiniMOS™) – Case 751–06** (continued)

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 11.) | $P_D$ (Notes 9. & 10.) (Watts) Max | Configuration (Note 12.) | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 20 | 0.100 | 0.200 | – | – | 3.6 | ***MMDF2N02ER2*** | 2.0 | Dual N–Channel | 451 |
| | – | 0.035 | 0.048 | 0.049 | 6.5 | ***NTMD6N02R2*** | 2.0 | Dual N–Channel | 127 |
| | 0.090 | 0.100 | – | – | 3.8 | ***MMDF3N02HDR2*** | 2.0 | Dual N–Channel | 503 |
| | 0.250 | 0.400 | – | – | 2.5 | ***MMDF2P02ER2*** | 2.0 | Dual P–Channel | 477 |
| | 0.160 | 0.180 | – | – | 3.3 | ***MMDF2P02HDR2*** | 2.0 | Dual P–Channel | 485 |
| | – | 0.033 | – | 0.050 | 7.8 | ***NTMD6P02R2*** | 2.0 | Dual P–Channel | 120 |
| | 0.100/0.250 | 0.200/0.400 | – | – | 3.6 | ***MMDF2C02ER2*** | 2.0 | Complementary | 416 |
| | 0.090/0.160 | 0.100/0.180 | – | – | 3.8 | ***MMDF2C02HDR2*** | 2.0 | Complementary | 427 |
| | – | 0.024/0.074 | – | – | 7.0 | ***NTMD7C02R2*** | 2.0 | Complementary | 141 |
| 12 | – | 0.045 | 0.055 | – | 5.1 | ***NTMS4P01R2*** | 2.5 | Single P–Channel | 164 |
| | – | 0.180 | 0.220 | – | 3.4 | ***MMDF2P01HDR2*** | 2.0 | Dual P–Channel | 468 |
| | – | 0.045/0.180 | – | – | 5.2 | ***MMDF2C01HDR2*** | 2.0 | Complementary | 404 |

**Table 3. SO–8 FETKY™ — Case 751–06**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 11.) | $P_D$ (Notes 9. & 10.) (Watts) Max | Configuration | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 30 | 0.035 | 0.050 | – | – | 6.0 | ***MMDFS6N303R2*** | 2.0 | Dual N–Channel/ Schottky | 589 |
| | 0.085 | 0.125 | – | – | 3.05 | ***NTMSD3P303R2*** | 2.0 | Dual P–Channel/ Schottky | 198 |
| 20 | 0.160 | 0.180 | – | – | 3.3 | ***MMDFS2P102R2*** | 2.0 | Dual P–Channel/ Schottky | 579 |
| | – | 0.090 | 0.130 | 0.15 | 2.4 | ***NTMSD2P102LR2*** | 2.0 | Dual P–Channel/ Schottky | 178 |
| | 0.085 | 0.125 | – | – | 3.0 | ***NTMSD3P102R2*** | 2.0 | Dual P–Channel/ Schottky | 188 |

**Table 4. EZFET™ – SO–8 Power MOSFETs with Zener Gate Protection – Case 751–06**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 11.) | $P_D$ (Notes 9. & 10.) (Watts) Max | Configuration | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 50 | 0.3 | – | – | – | 2.0 | ***MMDF2N05ZR2*** | 2.0 | Dual N–Channel | 459 |
| 30 | 0.03 | 0.04 | – | – | 7.5 | ***MMSF7N03ZR2*** | 2.5 | Single N–Channel | 751 |
| | 0.013 | 0.018 | – | – | 10 | ***MMSF10N03ZR2*** | 1.6 | Single N–Channel | 671 |
| 20 | – | 0.015 | 0.019 | – | 10 | ***MMSF10N02ZR2*** | 2.5 | Single N–Channel | 662 |
| | – | 0.04 | 0.05 | – | 5.0 | ***MMDF5N02ZR2*** | 2.0 | Dual N–Channel | 551 |
| | – | 0.027 | – | 0.035 | 7.0 | ***MMDF7N02ZR2*** | 2.0 | Dual N–Channel | 569 |

9. $T_C$ = 25°C
10. See Data Sheet for Applicable Mounting Configuration.
11. Available in Tape and Reel only. R2 suffix = 2500 per reel.
12. Data for all Complementary Devices listed as Nch/Pch.

# Power MOSFET Selector Guide (continued)

**Table 5. Micro8™ – Case 846A–02**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 15.) | $P_D$ (Notes 13. & 14.) (Watts) Max | Configuration | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 60 | 0.22 | 0.26 | – | – | 1.5 | ***MTDF2N06HDR2*** | 1.25 | Dual N–Channel | 1115 |
| 30 | 0.04 | 0.06 | – | – | 5.7 | ***MTSF3N03HDR2*** | 1.79 | Single N–Channel | 1348 |
| | 0.085 | 0.135 | – | – | 2.5 | ***NTTS2P03R2*** | 1.79 | Single P–Channel | 255 |
| | 0.12 | 0.16 | – | – | 2.0 | ***MTDF1N03HDR2*** | 1.25 | Dual N–Channel | 1104 |
| 20 | – | 0.04 | 0.05 | – | 6.1 | ***MTSF3N02HDR2*** | 1.79 | Single N–Channel | 1337 |
| | – | 0.16 | 0.19 | – | 1.8 | ***MTSF1P02HDR2*** | 1.8 | Single P–Channel | 1326 |
| | – | 0.09 | 0.13 | – | 2.4 | ***NTTS2P02R2R2*** | 0.78 | Single P–Channel | 248 |
| | – | 0.12 | 0.16 | – | 2.8 | ***MTDF1N02HDR2*** | 1.25 | Dual N–Channel | 1093 |
| | – | 0.16 | 0.25 | – | 1.45 | ***NTTD1P02R2*** | 1.25 | Dual P–Channel | 234 |
| | – | 0.090 | 0.130 | – | 2.4 | ***NTTD2P02R2*** | 1.25 | Dual P–Channel | 241 |

**Table 6. SOT-223 – Case 318E–04**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 5.0 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 16.) | $P_D$ (Notes 13. & 14.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|---|
| **N–Channel** | | | | | | | | |
| 240 | 6.0 | – | – | 10 | 0.7 | ***MMFT2406T1/T3*** | 1.5 | 605 |
| 200 | 14 | – | – | – | 0.25 | ***MMFT107T1/T3*** | 0.8 | 599 |
| 60 | 0.13 | – | – | – | 1.7 | ***MMFT3055VT1/T3*** | 2.0 | 628 |
| | – | 0.14 | – | – | 1.5 | ***MMFT3055VLT1/T3*** | 2.0 | 637 |
| | 1.7 | – | – | – | 0.3 | ***MMFT960T1*** | 0.8 | 656 |
| 20 | – | 0.15 | – | – | 1.6 | ***MMFT2N02ELT1*** | 0.8 | 619 |
| **P–Channel** | | | | | | | | |
| 60 | 0.3 | – | – | – | 1.2 | ***MMFT2955ET1/T3*** | 0.8 | 610 |
| 30 | 0.1 | – | – | – | 5.2 | ***MMFT5P03HDT3*** | 3.13 | 646 |

**Table 7. TSOP–6 – Case 318G–02**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 17.) | $P_D$ (Notes 13. & 14.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|---|
| **N–Channel** | | | | | | | | |
| 30 | 0.065 | 0.095 | – | – | 4.2 | ***MGSF3454VT1*** | 2.0 | 349 |
| 20 | – | 0.07 | – | 0.095 | 4.0 | ***MGSF3442VT1*** | 2.0 | 344 |
| | – | 0.045 | – | 0.055 | 5.8 | ***NTGS3446T1*** | 1.6 | 73 |
| **P–Channel** | | | | | | | | |
| 30 | 0.100 | 0.170 | – | – | 3.5 | ***NTGS3455T1*** | 2.0 | 76 |
| 20 | – | 0.09 | – | 0.135 | 3.3 | ***NTGS3441T1*** | 2.0 | 61 |
| | – | 0.065 | 0.090 | 0.100 | 4.4 | ***NTGS3443T1*** | 2.0 | 67 |
| | 0.175 | 0.28 | – | – | 1.3 | ***MGSF2P02HDT1*** | 2.0 | 336 |
| 12 | – | .075 | .095 | – | 3.3 | ***NTGS3433T1*** | 2.0 | 57 |

13. $T_C$ = 25°C
14. See Data Sheet for Applicable Mounting Configuration.
15. Available in Tape and Reel only. R2 suffix = 4000 per reel.
16. Available in Tape and Reel only. T1 suffix = 1000 per reel, T3 suffix = 4000 per reel.
17. Available in Tape and Reel only. T1 suffix = 3000 per reel.

# Power MOSFET Selector Guide (continued)

**Table 8. TSSOP–8 – Case 318G–02**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 20.) | $P_D$ (Notes 18. & 19.) (Watts) Max | Configuration | Page No. |
|---|---|---|---|---|---|---|---|---|---|
| 20 | – | 0.03 (Note 23.) | – | 0.04 | 5.8 | ***NTQD6866R2*** | 1.6 | Dual N–Channel | 230 |
| | – | 0.020 | 0.027 | – | 6.2 | ***NTQS6463R2*** | 1.05 | Single P–Channel | 232 |

**Table 9. SOT–23 – Case 318–08**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.5 V (Ω) | $I_D$ (cont) Amps | Device (Note 21.) | $P_D$ (Notes 18. & 19.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N–Channel** | | | | | | | |
| 100 | 6.0 | – | – | 0.17 | ***BSS123LT1/T3*** | 0.225 | 280 |
| 60 | 5.0 | – | – | 0.50 | ***MMBF170LT1/T3*** | 0.225 | 384 |
| | 7.5 | – | – | 0.115 | ***2N7002LT1/T3*** | 0.225 | 267 |
| 50 | – | 3.5 @ 5.0 V | 7.0 @ 2.75 | 0.20 | ***BSS138LT1/T3*** | 0.225 | 284 |
| 30 | 0.1 | 0.145 | – | 0.75 | ***MGSF1N03LT1*** | 0.4 | 324 |
| 20 | 0.09 | 0.13 | – | 0.75 | ***MGSF1N02LT1*** | 0.4 | 320 |
| | 1.0 | 1.4 | – | 0.3 | ***MMBF0201NLT1*** | 0.225 | 372 |
| | – | 0.085 | 0.115 | 0.75 | ***MGSF1N02ELT1*** | 0.4 | 316 |
| **P–Channel** | | | | | | | |
| 50 | – | 10 @ 5.0 V | – | 0.13 | ***BSS84LT1*** | 0.225 | 289 |
| 20 | – | 0.26 | 0.5 | 0.75 | ***MGSF1P02ELT1*** | 0.4 | 328 |
| | 0.35 | 0.5 | – | 0.75 | ***MGSF1P02LT1*** | 0.4 | 332 |
| | 1.4 | 3.5 | – | 0.3 | ***MMBF0202PLT1*** | 0.225 | 377 |

**Table 10. SC–70 / SOT–323 – Case 419–02**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device (Note 22.) | $P_D$ (Notes 18. & 19.) (Watts) Max | $V_{GS}$ (Volts) Min | Page No. |
|---|---|---|---|---|---|---|---|---|
| **N–Channel** | | | | | | | | |
| 30 | – | 50 | – | 0.10 | ***MMBF1374T1*** | 0.10 | 1.0 | 382 |
| 20 | 1.0 | 1.4 | – | 0.30 | ***MMBF2201NT1*** | 0.15 | 1.0 | 388 |
| **P–Channel** | | | | | | | | |
| 20 | 2.2 | 3.5 | – | 0.30 | ***MMBF2202PT1*** | 0.15 | 1.0 | 392 |

**Table 11. SC–88 / SOT–363 – Case 419B–01**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device (Note 22.) | $P_D$ (Notes 18. & 19.) (Watts) Max | $V_{GS}$ (Volts) Min | Page No. |
|---|---|---|---|---|---|---|---|---|
| **N–Channel** | | | | | | | | |
| 20 | 10 | – | – | 0.1 | ***NTUD01N02*** | 0.15 | 0.5 | 262 |

18. $T_C$ = 25°C
19. See Data Sheet for Applicable Mounting Configuration.
20. Available in Tape and Reel only. R2 suffix = 4000 per reel.
21. Available in Tape and Reel only. T1 suffix = 3000 per reel, T3 suffix = 10,000 per reel.
22. Available in Tape and Reel only. T1 suffix = 3000 per reel.
23. $V_{GS}$ = 4.0 V

**Table 12. DPAK – Case 369A–13 (TO–252)**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 5.0 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device (Note 26.) | $P_D$ (Notes 24. & 25.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 200 | 1.2 | – | – | 4.0 | ***MTD4N20E*** | 40 | 1048 |
| | 0.07 | – | | 6.0 | ***MTD6N20E*** | 50 | 1066 |
| 100 | 0.25 | – | – | 9.0 | ***MTD9N10E*** | 40 | 1084 |
| 60 | 0.094 | – | – | 12 | ***NTD3055–094*** | 36 | 35 |
| | – | 0.104 | – | 12 | ***NTD3055L104*** | 36 | 37 |
| | 0.15 | – | – | 12 | ***MTD3055V*** | 48 | 1019 |
| | – | 0.18 | – | 12 | ***MTD3055VL*** | 48 | 1028 |
| | 0.12 | – | – | 15 | ***MTD15N06V*** | 55 | 942 |
| | – | 0.085 | – | 15 | ***MTD15N06VL*** | 60 | 951 |
| | 0.045 | – | – | 20 | ***MTD20N06HD*** | 40 | 970 |
| | – | 0.045 | – | 20 | ***MTD20N06HDL*** | 40 | 980 |
| | 0.046 | – | – | 20 | ***NTD20N06*** | 60 | 33 |
| | 0.026 | – | – | 32 | ***NTD32N06*** | 60 | 39 |
| | – | 0.028 | – | 32 | ***NTD32N06L*** | 60 | 44 |
| 30 | – | 0.035 | – | 20 | ***MTD20N03HDL*** | 74 | 960 |
| | 0.022 | – | – | 20 | ***MTD1302*** | 74 | 932 |
| | – | 0.027 | – | 20 | ***NTD20N03L27*** | 74 | 29 |
| | 0.010 | 0.013 | – | 20 | ***NTD4302*** | 62 | 49 |
| | 0.010 | – | – | 30 | ***MTD3302*** | 96 | 1037 |
| **P-Channel** | | | | | | | |
| 100 | 0.66 | – | – | 6.0 | ***MTD6P10E*** | 50 | 1075 |
| 60 | 0.45 | – | – | 5.0 | ***MTD5P06V*** | 40 | 1057 |
| | 0.20 | – | – | 12 | ***MTD2955V*** | 60 | 1010 |
| | – | 0.175 | – | 15 | ***MTD20P06HDL*** | 72 | 1000 |
| 30 | – | 0.099 | – | 19 | ***MTD20P03HDL*** | 75 | 990 |

24. $T_C$ = 25°C
25. See Data Sheet for Applicable Mounting Configuration.
26. Also available in Tape and Reel. T4 suffix = 2500 per reel.

**Table 13. D2PAK – Case 418B–03 (TO–264)**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 5.0 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device (Note 29.) | $P_D$ (Notes 27. & 28.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 200 | 0.16 | – | – | 20 | ***MTB20N20E*** | 125 | 772 |
| 150 | 0.07 | – | – | 29 | ***MTB29N15E*** | 125 | 790 |
| 100 | 0.04 | – | – | 40 | ***MTB40N10E*** | 169 | 825 |
| 60 | 0.04 | – | – | 32 | ***MTB36N06V*** | 90 | 816 |
| | – | 0.05 | – | 30 | ***MTB30N06VL*** | 90 | 798 |
| | 0.026 | – | – | 45 | ***NTB45N06*** | 120 | 210 |
| | – | 0.028 | – | 45 | ***NTB45N06L*** | 120 | 215 |
| | 0.028 | – | – | 42 | ***MTB50N06V*** | 125 | 834 |
| | – | 0.032 | – | 42 | ***MTB50N06VL*** | 125 | 843 |
| | 0.022 | – | – | 52 | ***MTB52N06V*** | 165 | 862 |
| | – | 0.025 | – | 52 | ***MTB52N06VL*** | 188 | 871 |
| | 0.016 | – | – | 55 | ***MTB55N06Z*** | 136 | 880 |
| | 0.014 | – | – | 60 | ***MTB60N06HD*** | 125 | 895 |
| | 0.010 | – | – | 75 | ***MTB75N06HD*** | 125 | 922 |
| 50 | 0.0095 | – | – | 75 | ***MTB75N05HD*** | 125 | 915 |
| | – | 0.014 | – | 60 | ***MTB60N05HDL*** | 150 | 885 |
| 30 | 0.0065 | – | – | 75 | ***MTB1306*** | 150 | 765 |
| | 0.0065 | – | – | 75 | ***NTB75N03–06*** | 150 | 220 |
| | – | 0.009 | – | 75 | ***NTB75N03L09*** | 150 | 225 |
| 25 | – | 0.009 | – | 75 | ***MTB75N03HDL*** | 125 | 905 |
| **P-Channel** | | | | | | | |
| 60 | 0.12 | – | – | 23 | ***MTB23P06V*** | 90 | 781 |
| | 0.08 | – | – | 30 | ***MTB30P06V*** | 125 | 807 |
| 30 | – | 0.025 | – | 50 | ***MTB50P03HDL*** | 125 | 852 |

27. $T_C$ = 25°C
28. See Data Sheet for Applicable Mounting Configuration.
29. Also available in Tape and Reel. T4 suffix = 800 per reel.

# Power MOSFET Selector Guide (continued)

**Table 14. TO-220AB – Case 221A–09**

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 5.0 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device | $P_D$ (Note NO TAG) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 200 | 0.70 | – | – | 7.0 | ***MTP7N20E*** | 50 | 1320 |
| | 0.16 | – | – | 20 | ***MTP20N20E*** | 125 | 1175 |
| 150 | 0.07 | – | – | 29 | ***MTP29N15E*** | 125 | 1199 |
| | 0.13 | – | – | 20 | ***MTP20N15E*** | 112 | 1173 |
| 100 | 0.25 | – | – | 10 | ***MTP10N10E*** | 75 | 1123 |
| | 0.07 | – | – | 27 | ***MTP27N10E*** | 104 | 1187 |
| | 0.04 | – | – | 40 | ***MTP40N10E*** | 169 | 1243 |
| | – | 0.22 | – | 10 | ***MTP10N10EL*** | 40 | 1130 |
| 60 | 0.150 | – | – | 12 | ***MTP3055V*** | 48 | 1213 |
| | – | 0.18 | – | 12 | ***MTP3055VL*** | 48 | 1219 |
| | 0.12 | – | – | 15 | ***MTP15N06V*** | 55 | 1155 |
| | – | 0.085 | – | 15 | ***MTP15N06VL*** | 60 | 1161 |
| | 0.085 | – | – | 20 | ***MTP20N06V*** | 60 | 1167 |
| | 0.046 | – | – | 27 | ***NTP27N06*** | 74 | 208 |
| | 0.04 | – | – | 32 | ***MTP36N06V*** | 90 | 1237 |
| | – | 0.05 | – | 30 | ***MTP30N06VL*** | 90 | 1225 |
| | 0.026 | – | – | 45 | ***NTP45N06*** | 120 | 210 |
| | – | 0.028 | – | 45 | ***NTP45N06L*** | 120 | 215 |
| | 0.028 | – | – | 42 | ***MTP50N06V*** | 125 | 1249 |
| | – | 0.032 | – | 42 | ***MTP50N06VL*** | 125 | 1255 |
| | 0.022 | – | – | 52 | ***MTP52N06V*** | 165 | 1268 |
| | – | 0.025 | – | 52 | ***MTP52N06VL*** | 165 | 1274 |
| | 0.014 | – | – | 60 | ***MTP60N06HD*** | 150 | 1286 |
| | 0.01 | – | – | 75 | ***MTP75N06HD*** | 150 | 1313 |
| 50 | 0.0095 | – | – | 75 | ***MTP75N05HD*** | 150 | 1306 |
| 30 | 0.022 | 0.029 | – | 42 | ***MTP1302*** | 74 | 1141 |
| | 0.0065 | 0.0085 | – | 75 | ***MTP1306*** | 150 | 1148 |
| | 0.0065 | – | – | 75 | ***NTP75N03–06*** | 150 | 220 |
| | – | 0.009 | – | 75 | ***NTP75N03L09*** | 150 | 225 |
| 25 | – | 0.009 | – | 75 | ***MTP75N03HDL*** | 150 | 1299 |
| **P-Channel** | | | | | | | |
| 500 | 6.0 | – | – | 2.0 | ***MTP2P50E*** | 75 | 1207 |
| 200 | 1.0 | – | – | 6.0 | ***MTP6P20E*** | 75 | 1293 |
| 100 | 0.30 | – | – | 12 | ***MTP12P10*** | 75 | 1136 |
| 60 | 0.45 | – | – | 5.0 | ***MTP5P06V*** | 40 | 1280 |
| | 0.20 | – | – | 12 | ***MTP2955V*** | 60 | 1193 |
| | 0.12 | – | – | 23 | ***MTP23P06V*** | 90 | 1181 |
| | 0.08 | – | – | 30 | ***MTP30P06V*** | 125 | 1231 |
| 30 | – | 0.025 | – | 50 | ***MTP50P03HDL*** | 125 | 1261 |

30. $T_C$ = 25°C

# Power MOSFET Selector Guide (continued)

### Table 15. TO-247 (Isolated Mounting Hole) – Case 340K–01

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device | $P_D$ (Note 31.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 250 | 0.08 | – | – | 32 | ***MTW32N25E*** | 250 | 1365 |
| 200 | 0.075 | – | – | 32 | ***MTW32N20E*** | 180 | 1359 |
| 150 | 0.05 | – | – | 35 | ***MTW35N15E*** | 180 | 1371 |
| 100 | 0.035 | – | – | 45 | ***MTW45N10E*** | 180 | 1377 |

### Table 16. TO-264 – Case 340G–02

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device | $P_D$ (Note 31.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 200 | 0.028 | – | – | 55 | ***MTY55N20E*** | 300 | 1383 |

### Table 17. SMARTDISCRETES™

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 5.0 V (Ω) | 2.7 V (Ω) | Function | Device | $P_D$ (Notes 31. & 32.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **TO-220AB** | | | | | | | |
| 62 (Clamped) | – | 0.75 | – | Current Limit, ESD | ***MLP1N06CL*** | 40 | 360 |
| | – | 0.40 | – | Current Limit, ESD | ***MLP2N06CL*** | 40 | 366 |
| **DPAK** | | | | | | | |
| 62 (Clamped) | – | 0.75 | – | Current Limit, ESD | ***MLD1N06CLT4*** (Note 33.) | 40 | 354 |
| **D2PAK – 5 Lead** | | | | | | | |
| 40 V | – | 0.02 | – | Temp Sense, ESD, Overvoltage Protect | ***NIB6404–5L*** | 115 | 23 |
| **SO–8** | | | | | | | |
| 30 V | 0.05 | – | – | Current Mirror, ESD Protect | ***NIMD6302R2*** (Note 34.) | 20 | 27 |

31. $T_C$ = 25°C
32. See Data Sheet for Applicable Mounting Configuration.
33. Available in Tape and Reel only. T4 suffix = 2500 per reel.
34. Available in Tape and Reel only. R2 suffix = 2500 per reel.

### Table 18. TO-92

| $V_{(BR)DSS}$ (Volts) Min | Max $R_{DS(on)}$ @ $V_{GS}$ 10 V (Ω) | 4.5 V (Ω) | 2.7 V (Ω) | $I_D$ (cont) Amps | Device | $P_D$ (Note 35.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **N-Channel** | | | | | | | |
| 240 | 10 | – | 10 @ 2.5 V | 0.2 | ***VN2410L*** | 0.35 | 1396 |
| | 6.0 | – | 10 @ 2.5 V | 0.2 | ***VN2406L*** | 0.35 | 1394 |
| 200 | – | 8.0 @ 2.8 V | 10 @ 2.5 V | 0.25 | ***BS108*** | 0.35 | 275 |
| | 14 | – | 28 @ 2.6 V | 0.25 | ***BS107*** | 0.35 | 271 |
| | 6.0 | – | – | 0.25 | ***BS107A*** | 0.35 | 271 |
| 90 | 2.0 | – | – | 2.0 | ***MPF990*** | 1.0 | 761 |
| 60 | 7.5 | – | – | 0.15 | ***VN2222LL*** | 0.4 | 1391 |
| | 5.0 | – | – | 0.5 | ***BS170*** | 0.35 | 277 |
| | 5.0 | 6.0 | – | 0.2 | ***2N7000*** | 0.35 | 264 |
| | 1.7 | – | – | 2.0 | ***MPF960*** | 1.0 | 761 |
| | 1.2 | 3.3 @ 5 V | – | 0.2 | ***VN0300L*** | 0.35 | 1389 |
| 35 | 1.4 | – | – | 2.0 | ***MPF930*** | 1.0 | 761 |
| | 1.4 | – | – | 2.0 | ***MPF930A*** | 1.0 | 761 |

### Table 19. Ignition IGBTs – Insulated Gate Bipolar Transistors

| $V_{(BR)CES}$ (Volts) Min | Max $V_{CE(on)}$ @ $V_{GE}$ 4.0 V $I_C$ = 6.0 A | 4.5 V $I_C$ = 10 A | $I_C$ (pulse) Amps | $I_C$ (cont) Amps | Device | $P_D$ (Notes 35. & 36.) (Watts) Max | Page No. |
|---|---|---|---|---|---|---|---|
| **TO-220AB** | | | | | | | |
| 400 V (Clamped) | 1.6 | 1.9 | 50 | 15 | ***MGP15N40CL*** | 150 | 301 |
| 350 V (Clamped) | 1.6 | 1.9 | 50 | 15 | ***MGP15N35CL*** | 150 | 293 |
| | 1.6 | 1.8 | 50 | 19 | ***MGP19N35CL*** | 166 | 309 |
| **$D^2PAK$** | | | | | | | |
| 400 V (Clamped) | 1.6 | 1.9 | 50 | 15 | ***MGB15N40CLT4*** (Note 37.) | 150 | 301 |
| 350 V (Clamped) | 1.6 | 1.9 | 50 | 15 | ***MGB15N35CLT4*** (Note 37.) | 150 | 293 |
| | 1.6 | 1.8 | 50 | 19 | ***MGB19N35CLT4*** (Note 37.) | 166 | 309 |
| **DPAK** | | | | | | | |
| 410 V (Clamped) | 1.7 | 2.1 | 50 | 15 | ***NGD15N41CLT4*** (Note 38.) | 96 | 21 |

35. $T_C$ = 25°C
36. See Data Sheet for Applicable Mounting Configuration.
37. Available in Tape and Reel only. T4 suffix = 800 per reel.
38. Available in Tape and Reel only. T4 suffix = 2500 per reel.

# CHAPTER 1
# MOSFET Data Sheets

# NGD15N41CL

*Product Preview*

# Ignition IGBT
# 15 Amps, 410 Volts

## N–Channel DPAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

- Ideal for Coil–on–Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Cell Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Short–Circuit Withstand Capability
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor ($R_G$) and Gate–Emitter Resistor ($R_{GE}$)

**MAXIMUM RATINGS** ($-55°C \le T_J \le 175°C$ unless otherwise noted)

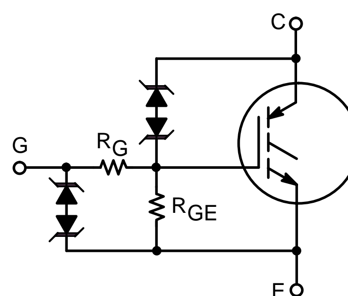
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CES}$ | 440 | $V_{DC}$ |
| Collector–Gate Voltage | $V_{CER}$ | 440 | $V_{DC}$ |
| Gate–Emitter Voltage | $V_{GE}$ | 15 | $V_{DC}$ |
| Collector Current–Continuous @ $T_C = 25°C$ | $I_C$ | 15 | $A_{DC}$ |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

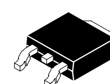
**ON Semiconductor™**

**http://onsemi.com**

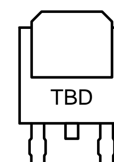
**15 AMPS**
**410 VOLTS**
**$V_{CE(on)}$ @ 10 A = 2.1 V MAX**




**MARKING DIAGRAM**



**DPAK**
**CASE 369A**
**STYLE 2**




TBD = Specific Device Code

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NGD15N41CL | DPAK | 75 Units/Rail |
| NGD15N41CLT4 | DPAK | 2500/Tape & Reel |

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**UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS** ($-55°C \le T_J \le 175°C$)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Collector–to–Emitter Avalanche Energy<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5 V, Pk $I_L$ = 16 A, L = 1.8 mH, Starting $T_J$ = 25°C<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5 V, Pk $I_L$ = 15 A, L = 1.8 mH, Starting $T_J$ = 150°C | $E_{AS}$ | <br>225<br>200 | mJ |

**THERMAL CHARACTERISTICS**

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Ambient | DPAK | $R_{\theta JA}$ | 100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | | $T_L$ | 275 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Collector–Emitter Clamp Voltage | $BV_{CES}$ | $I_C$ = 2 mA<br>$T_J$ = –40°C to 175°C | 380 | 410 | 440 | $V_{DC}$ |
| Zero Gate Voltage Collector Current | $I_{CES}$ | $V_{CE}$ = 300 V,<br>$V_{GE}$ = 0, $T_J$ = 25°C | – | – | 40 | μ$A_{DC}$ |
| | | $V_{CE}$ = 300 V,<br>$V_{GE}$ = 0, $T_J$ = 150°C | – | – | 200 | |
| Reverse Collector–Emitter Leakage Current | $I_{ECS}$ | $V_{CE}$ = –24 V | – | – | 1.0 | mA |
| Gate–Emitter Clamp Voltage | $BV_{GES}$ | $I_G$ = 5 mA | 10 | – | 16 | $V_{DC}$ |
| Gate Resistor (Optional) | $R_G$ | – | – | 70 | – | Ω |
| Gate Emitter Resistor (Optional) | $R_{GE}$ | – | 10 | – | 26 | kΩ |
| **ON CHARACTERISTICS*** | | | | | | |
| Gate Threshold Voltage | $V_{GE(th)}$ | $I_C$ = 1 mA<br>$V_{GE}$ = $V_{CE}$ | 1.0 | 1.4 | 2.1 | $V_{DC}$ |
| Threshold Temperature Coefficient (Negative) | – | – | – | 4.4 | – | mV/°C |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 6 A, $V_{GE}$ = 4 V | – | – | 1.8 | $V_{DC}$ |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 10 A,<br>$V_{GE}$ = 4.5 V,<br>$T_J$ = 150°C | – | – | 2.1 | $V_{DC}$ |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{CC}$ = 15 V | – | 700 | – | pF |
| Output Capacitance | $C_{OSS}$ | $V_{GE}$ = 0 V | – | 60 | – | |
| Transfer Capacitance | $C_{RSS}$ | f = 1 MHz | – | 6.0 | – | |
| **SWITCHING CHARACTERISTICS*** | | | | | | |
| Turn–Off Delay Time | $t_{d(off)}$ | $V_{CC}$ = 300 V,<br>$I_C$ = 10 A | – | 4.0 | – | μSec |
| Fall Time | $t_f$ | $R_G$ = 1 kΩ,<br>L = 300 μH | – | 10 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{CC}$ = 10 V,<br>$I_C$ = 6.5 A | – | 1.0 | – | μSec |
| Rise Time | $t_r$ | $R_G$ = 1 kΩ,<br>$R_L$ = 1 Ω | – | 4.0 | – | |

*Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

# NIB6404-5L

**Preferred Device**

*Product Preview*

# SMARTDISCRETES™
# 52 Amps, 40 Volts
## Self Protected with Temperature Sense
## N–Channel $D^2PAK$

**ON Semiconductor™**

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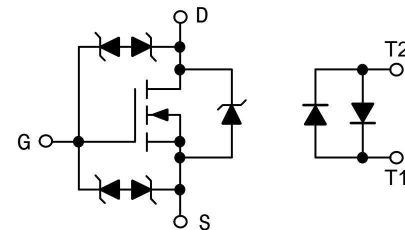
**52 AMPERES**
**40 VOLTS**
**$R_{DS(on)}$ = 20 mΩ**

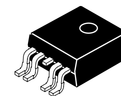



SMARTDISCRETES devices are an advanced series of Power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on–resistance per silicon area while incorporating additional features such as clamp diodes. They are capable of withstanding high energy in the avalanche and commutation modes. The avalanche energy is specified to eliminate guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

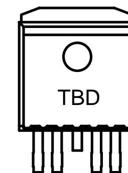
This new SMARTDISCRETES device features integrated Gate–to–Source diodes for ESD protection, and Gate–to–Drain clamp for overvoltage protection. Also, this device integrates a sense diode for temperature monitoring.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Overvoltage Protection
- Temperature Sense Diode
- ESD Human Body Model Discharge Sensitivity Class 3

**MARKING DIAGRAM**



**$D^2PAK$**
**CASE 936D**
**PLASTIC**




TBD = Specific Device Code

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 40 | Vdc |
| Drain–to–Gate Voltage | $V_{DGR}$ | 40 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 10 | Vdc |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C (Note 1.) ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_{L(pk)}$ = 25 A, L = 1.4 mH, $R_G$ = 10 kΩ) | $E_{AS}$ | 450 | mJ |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 140°C<br>– Single Pulse ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>52<br>25<br>200 | Adc |
| Total Power Dissipation (t ≤ 10 seconds)<br>Linear Derating Factor | $P_D$ @ $T_A$ = 25°C | 115<br>0.76 | W<br>W/°C |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.3<br>80 | °C/W |

1. Measured while surface mounted to an FR4 board using the minimum recommended pad size. Typical value is 64°C/W.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NIB6404–5L | $D^2PAK$ | TBD |

**Preferred** devices are recommended choices for future use and best overall value.

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**February, 2001 – Rev. 1**
Publication Order Number:
**NIB6404–5L/D**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 2.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc, –55°C < $T_J$ < 175°C)<br>Temperature Coefficient (Negative) | | $V_{(BR)DSS}$ | <br>40<br>– | <br>51<br>7.0 | <br>55<br>– | Vdc<br><br>mV/°C |
| Gate–to–Source Clamp Voltage (Note 2.)<br>($V_{GS}$ = 0 Vdc, $I_G$ = 20 µAdc) | | $V_{(BR)GSS}$ | 10 | 13 | 20 | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 35 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 35 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>–<br>– | <br>1.1<br>0.2<br>4.0 | <br>100<br>2.0<br>20 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | 0.02 | 1.0 | µAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Note 2.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.7<br>4.5 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 2.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 20 Adc) | | $R_{DS(on)}$ | – | 18 | 20 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 10 Adc) (Note 2.) | | $g_{FS}$ | TBD | 34 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1720 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 525 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 120 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 32 Vdc, $I_D$ = 25 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 10 Ω) (Note 2.) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 263 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 149 | – | |
| Fall Time | | $t_f$ | – | 345 | – | |
| Gate Charge | ($V_{DS}$ = 32 Vdc, $I_D$ = 25 Adc, $V_{GS}$ = 5.0 Vdc) (Note 2.) | $Q_T$ | – | 29 | – | nC |
| | | $Q_1$ | – | 6.0 | – | |
| | | $Q_2$ | – | 16 | – | |
| | | $Q_3$ | – | 2.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.876<br>0.746 | 1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 25 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) (Note 2.) | $t_{rr}$ | – | 60 | – | ns |
| | | $t_a$ | – | 29 | – | |
| | | $t_b$ | – | 32 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 80 | – | pC |
| **TEMPERATURE SENSE DIODE CHARACTERISTICS** | | | | | | |
| Forward (Reverse) On–Voltage | ($I_{F(R)}$ = 250 µAdc) (Note 2.)<br>($I_{F(R)}$ = 250 µAdc, $T_J$ = 125°C) | $V_{AC(ACR)}$ | 715<br>– | 743<br>570 | 775<br>– | mVdc |
| Temperature Coefficient (Negative) | $I_{F(R)}$ = 250 µAdc, $T_J$ = 160°C | $V_{FTC}$ | 1.57 | 1.71 | 1.85 | mV/°C |
| Forward Voltage Hysteresis | $I_{F(R)}$ = 125 µAdc to 250 µAdc | $V_{hys}$ | 25 | 37 | 50 | mVdc |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

## TYPICAL ELECTRICAL CHARACTERISTICS

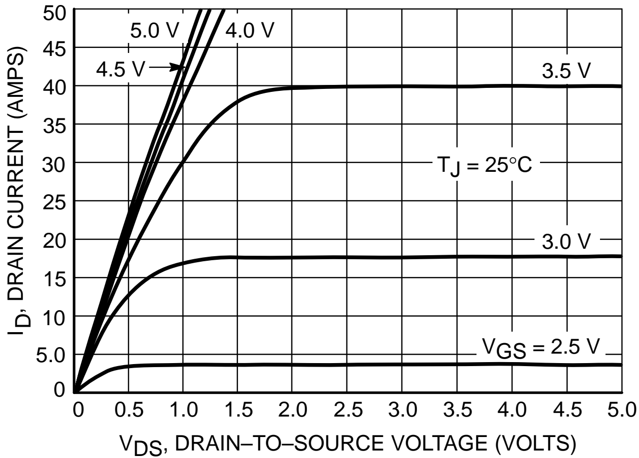



**Figure 1. On–Region Characteristics**

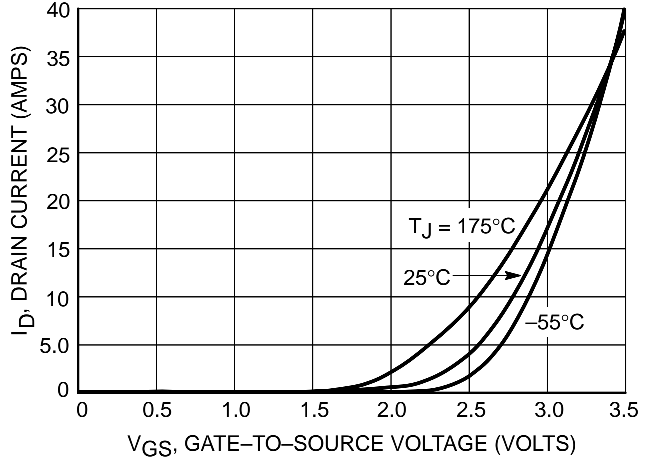



**Figure 2. Transfer Characteristics**

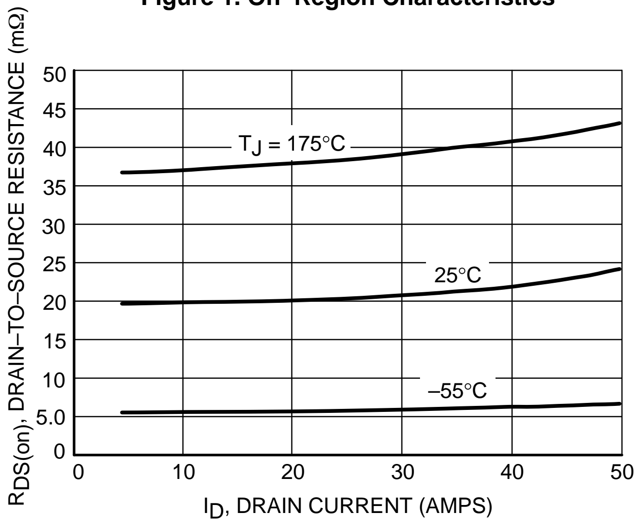



**Figure 3. On–Resistance versus Drain Current and Temperature**

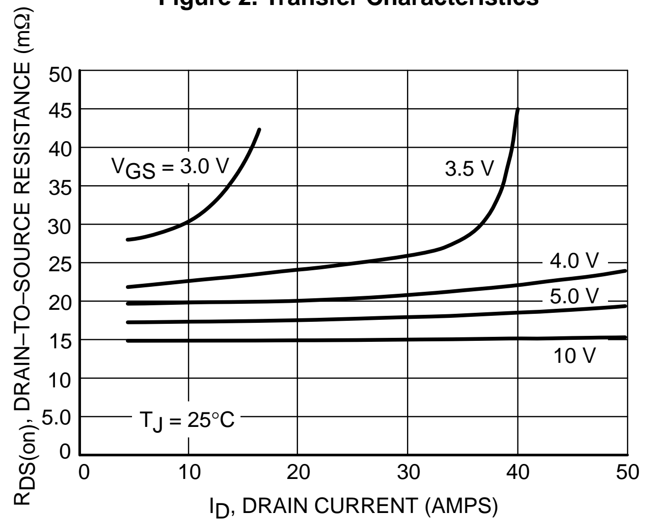



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

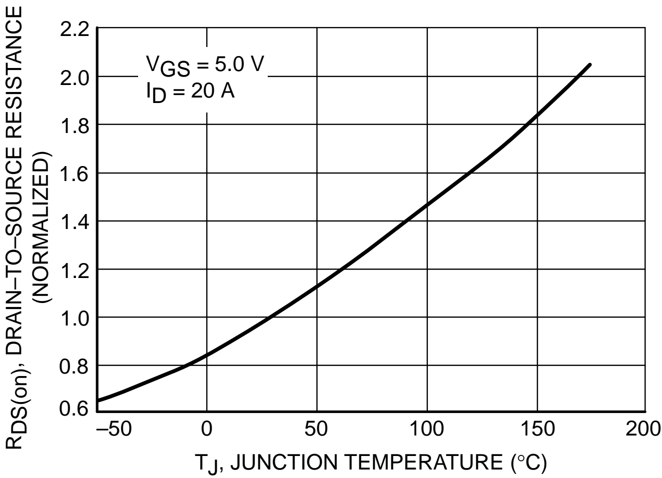



**Figure 5. On–Resistance Variation with Temperature**

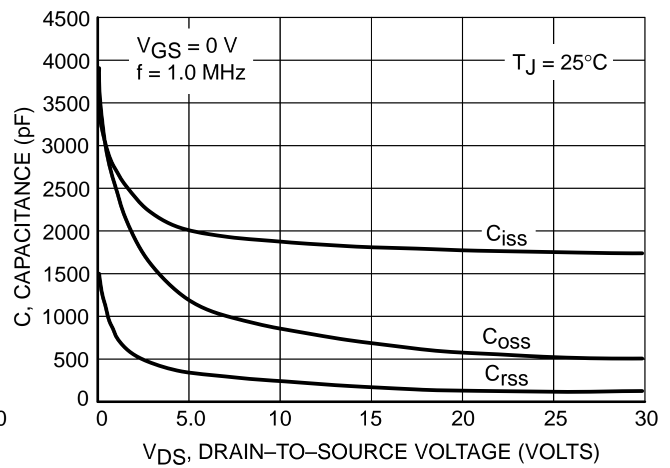



**Figure 6. Capacitance Variation**

## TYPICAL ELECTRICAL CHARACTERISTICS

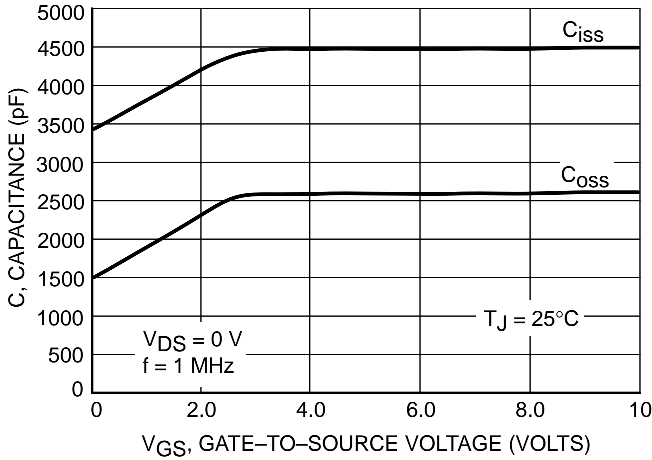



**Figure 7. Capacitance Variation**

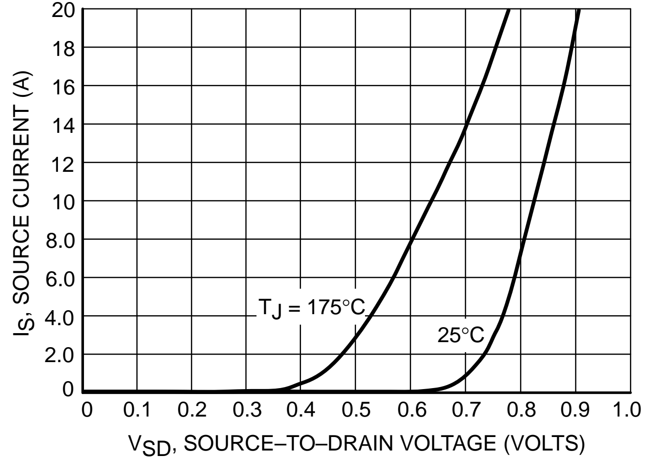



**Figure 8. Diode Forward Voltage versus Current**

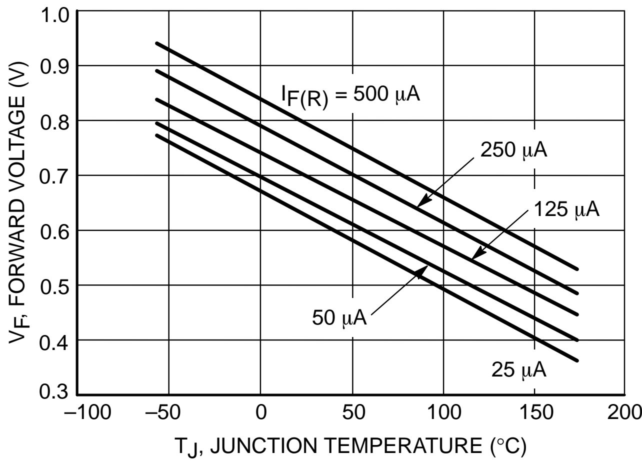



**Figure 9. Sense Diode Forward Voltage Variation with Temperature**

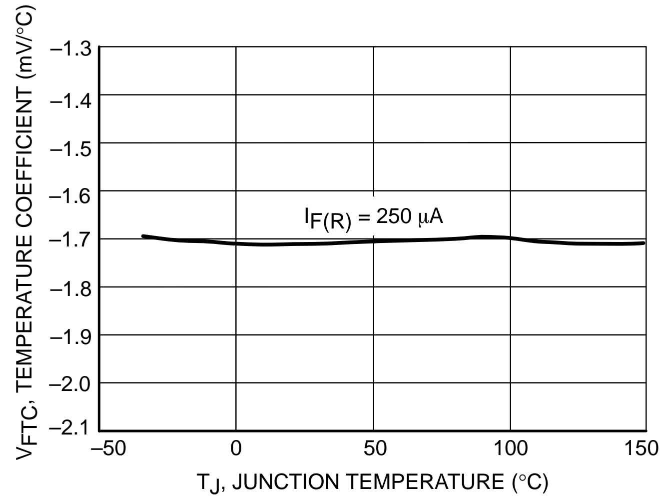



**Figure 10. Sense Diode Temperature Coefficient Variation with Temperature**

# NIMD6302R2

*Product Preview*

## SMARTDISCRETES™
## 5 Amps, 30 Volts
### Self Protected with Current Sense

### N–Channel SO–8, Dual

SMARTDISCRETES devices are an advanced series of Power MOSFETs which utilize ON Semiconductor's latest MOSFET technology process to achieve the lowest possible on–resistance per silicon area while incorporating smart features. They are capable of withstanding high energy in the avalanche and commutation modes. The avalanche energy is specified to eliminate guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

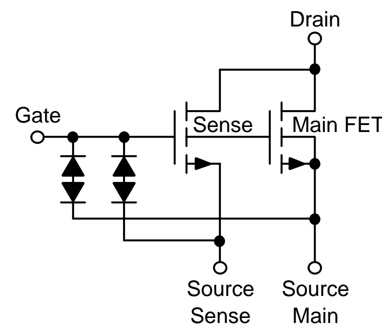
This new SMARTDISCRETES device features an integrated Gate–to–Source clamp for ESD protection. Also, this device features a sense FET for current monitoring.

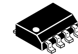
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Current Sense FET
- ESD Protected, Main FET and SENSEFET

ON Semiconductor™

http://onsemi.com

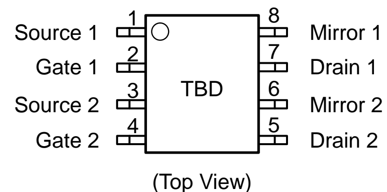
**5.0 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 50 mΩ**



**SOIC–8**
**CASE 751**
**STYLE 19**

**MARKING DIAGRAM**




(Top View)

TBD = Specific Device Code

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NIMD6302R2 | SOIC–8 | TBD |

### ABSOLUTE MAXIMUM RATINGS

Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in this specification is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

**MAIN MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 16 | Vdc |
| Single Pulse Drain–to–Source Avalanche Energy (Note 1.) ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $V_{DS}$ = 20 Vdc, $I_L$ = 15 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 250 | mJ |
| Drain Current | | | |
| – Continuous @ $T_A$ = 25°C | $I_D$ | 6.5 | Adc |
| – Continuous @ $T_A$ = 100°C (Note 1.) | $I_D$ | 4.4 | Adc |
| – Single Pulse ($t_p \leq$ 10 µs) | $I_{DM}$ | 33 | Apk |
| Maximum Power Dissipation ($T_A$ = 25°C) | $P_D$ | TBD | W |

1. Switching characteristics are independent of operating junction temperatures

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**MAIN MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 30 | 35 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 30 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = 12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | 22 | 32 | μAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | – | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 5.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Note 2.) ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc, $T_J$ @ 25°C) | | $R_{DS(on)}$ | – | – | 50 | mΩ |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc, $T_J$ @ 125°C) | | | – | – | TBD | |
| Forward Transconductance (Note 2.) ($V_{DS}$ = 6.0 Vdc, $I_D$ = 15 Adc) | | $g_{FS}$ | – | 7.4 | – | mhos |
| ($V_{DS}$ = 15 Vdc, $I_D$ = 15 Adc) | | | – | 5.5 | – | |
| **DYNAMIC CHARACTERISTICS** (Note 3.) | | | | | | |
| Input Capacitance | ($V_{DS}$ = 6.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 380 | 600 | pF |
| Output Capacitance | | $C_{oss}$ | – | 272 | 350 | |
| Transfer Capacitance | | $C_{rss}$ | – | 93 | 200 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | – | 8.4 | – | ns |
| Rise Time | | $t_r$ | – | 24 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 18 | – | |
| Fall Time | | $t_f$ | – | 5.0 | – | |
| Gate Charge | ($V_{DS}$ = 6.0 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 11.3 | – | nC |
| | | $Q_1$ | – | 2.8 | – | |
| | | $Q_2$ | – | 1.9 | – | |
| | | $Q_3$ | – | 2.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.76 | – | Vdc |
| Forward On–Voltage (Notes 2., 3.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.62 | – | |
| Reverse Recovery Time (Note 3.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 24.7 | – | ns |
| | | $t_a$ | – | 13 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge (Note 3.) | | $Q_{RR}$ | – | 0.018 | – | μC |
| **MIRROR MOSFET CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) | | | | | | |
| Main/Mirror MOSFET Current Ratio | ($V_{DS}$ = 6.0 Vdc, $I_{Dmain}$ = 25 mA) | $I_{RAT}$ | 192 | 200 | 208 | – |
| | ($V_{DS}$ = 6.0 Vdc, $I_{Dmain}$ = 25 mA, $T_A$ = 125°C) | | 192 | 200 | 208 | |
| Main/Mirror Current Ratio Variation versus Current and Temperature | ($V_{DS}$ = 6.0 Vdc, $I_{Dmain}$ = 25 mA, $T_A$ = 25 to 125°C) | $I_{\Delta RAT}$ | –7.5 | ±3.0 | +7.5 | % |
| Gate–Body Leakage Current | $V_{DS}$ = 0 Vdc, $V_{GS}$ = 3.0 Vdc | $I_{GSS}$ | – | – | 100 | nAdc |

2. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
3. Switching characteristics are independent of operating junction temperatures.

# NTD20N03L27

## Power MOSFET 20 Amps, 30 Volts

### N–Channel DPAK

**ON Semiconductor™**

**http://onsemi.com**

**20 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 27 mΩ**

This logic level vertical power MOSFET is a general purpose part that provides the "best of design" available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain–to–source diode has a ideal fast but soft recovery.

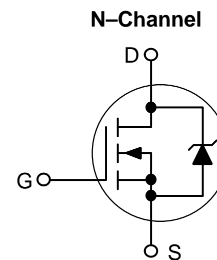
**Features**

- Ultra–Low $R_{DS(on)}$, single base, advanced technology
- SPICE parameters available
- Diode is characterized for use in bridge circuits
- $I_{DSS}$ and $V_{DS(on)}$ specified at elevated temperatures
- High Avalanche Energy Specified
- ESD JEDAC rated HBM Class 1, MM Class A, CDM Class 0

**Typical Applications**

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTD20N03L in many applications

**N–Channel**

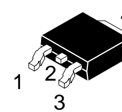



**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

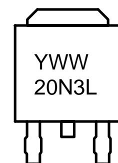
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>± 20<br>± 24 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>20<br>16<br>60 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note 1.) | $P_D$ | 74<br>0.6<br>1.75 | Watts<br>W/°C<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5 Vdc, L = 1.0 mH, $I_{L(pk)}$ = 24 A, $V_{DS}$ = 34 Vdc) | $E_{AS}$ | 288 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size and repetitive rating; pulse width limited by maximum junction temperature.

**MARKING DIAGRAM**

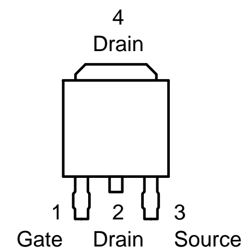



**CASE 369A**
**DPAK**
**STYLE 2**




20N3L = Device Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD20N03L27 | DPAK | 75 Units/Rail |
| NTD20N03L27–1 | DPAK | 75 Units/Rail |
| NTD20N03L27T4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 2.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 30<br>– | –<br>43 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ =150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Note 2.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.6<br>5.0 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 2.)<br>($V_{GS}$ = 4.0 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | –<br>– | 28<br>23 | 31<br>27 | mΩ |
| Static Drain–to–Source On–Resistance (Note 2.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 10 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 0.48<br>0.40 | 0.54<br>– | Vdc |
| Forward Transconductance (Note 2.) ($V_{DS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | – | 21 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1005 | 1260 | pF |
| Output Capacitance | | $C_{oss}$ | – | 271 | 420 | |
| Transfer Capacitance | | $C_{rss}$ | – | 87 | 112 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 20 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) (Note 2.) | $t_{d(on)}$ | – | 17 | 25 | ns |
| Rise Time | | $t_r$ | – | 137 | 160 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 38 | 45 | |
| Fall Time | | $t_f$ | – | 31 | 40 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc) (Note 2.) | $Q_T$ | – | 13.8 | 18.9 | nC |
| | | $Q_1$ | – | 2.8 | – | |
| | | $Q_2$ | – | 6.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.0<br>0.9 | 1.15<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ =15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 23 | – | ns |
| | | $t_a$ | – | 13 | – | |
| | | $t_b$ | – | 10 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.017 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

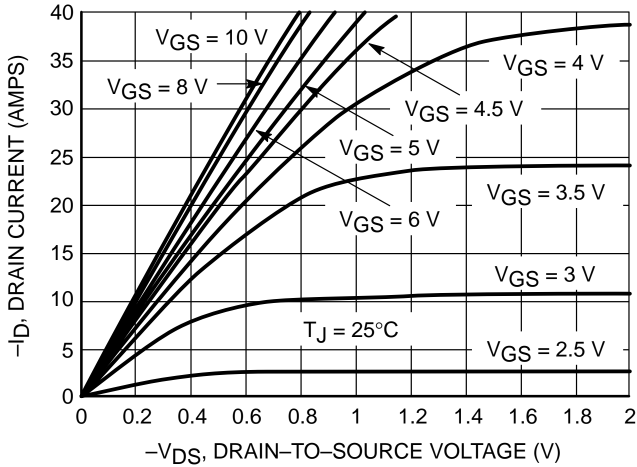


**Figure 1. On–Region Characteristics**

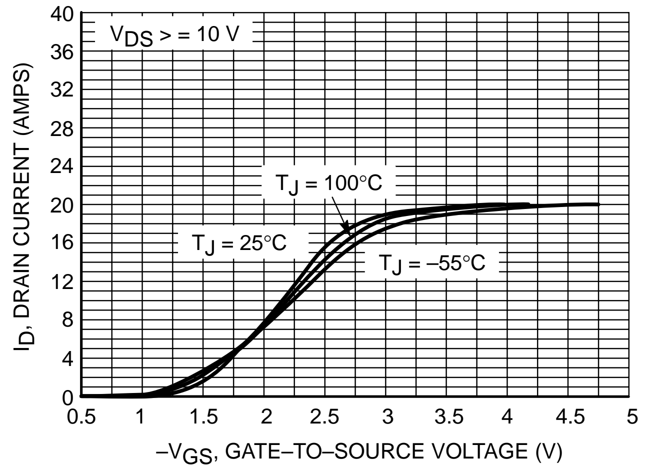


**Figure 2. Transfer Characteristics**

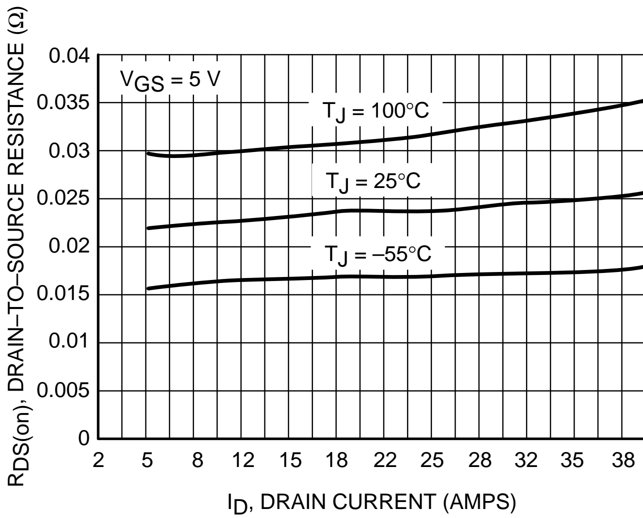


**Figure 3. On–Resistance vs. Drain Current and Temperature**

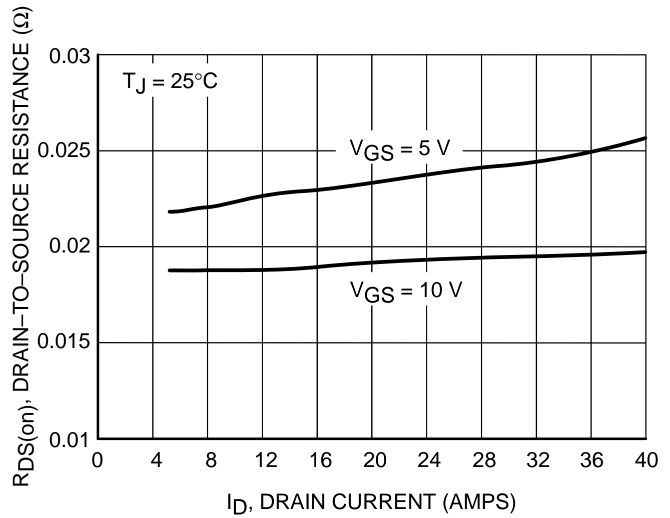


**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

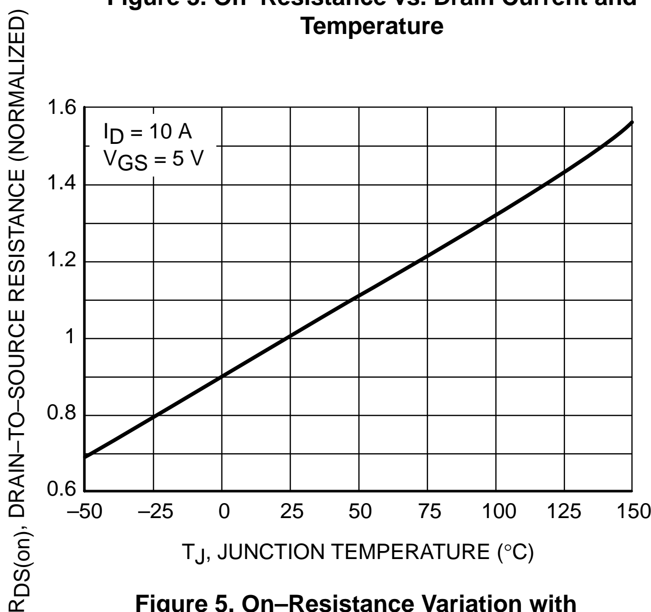


**Figure 5. On–Resistance Variation with Temperature**

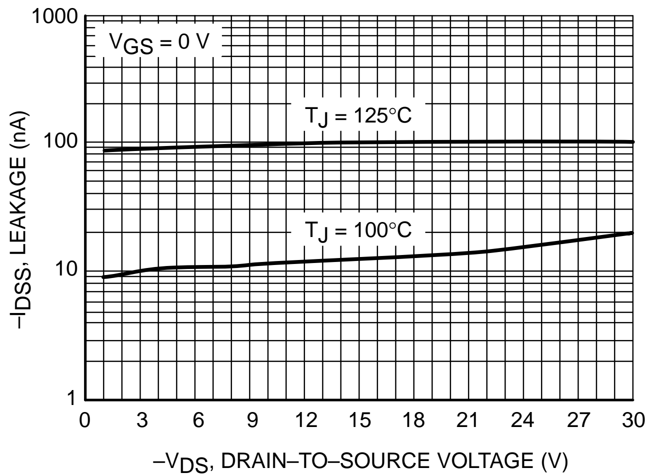


**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

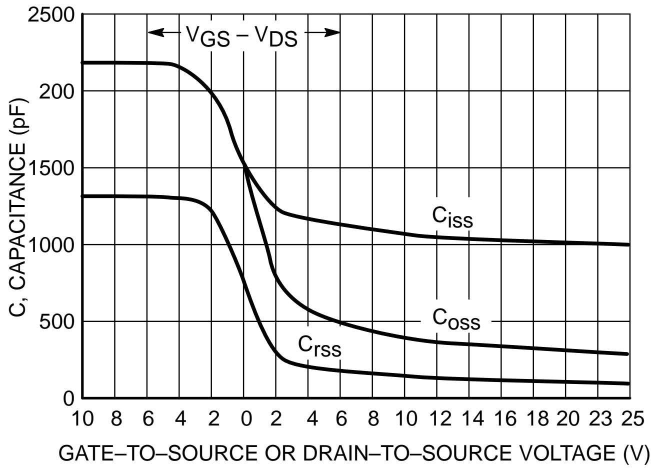


**Figure 7. Capacitance Variation**

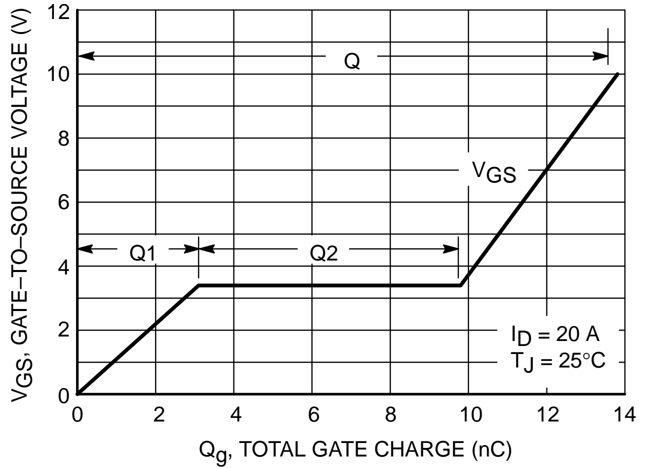


**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

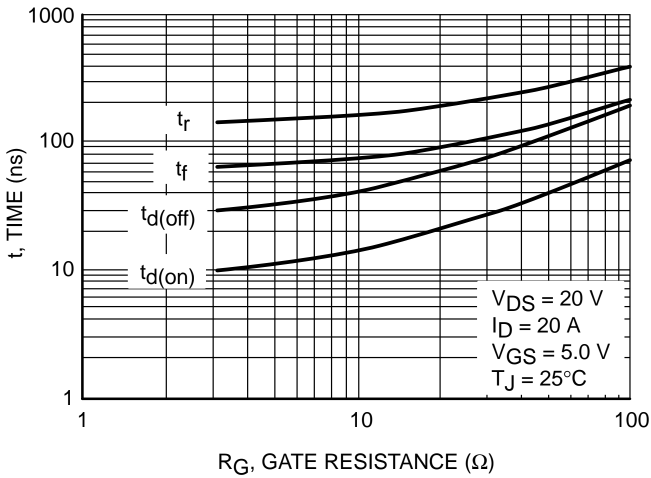


**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

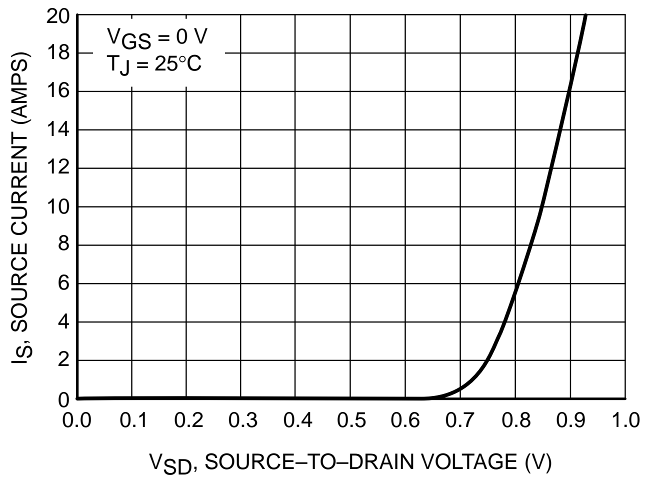


**Figure 10. Diode Forward Voltage vs. Current**

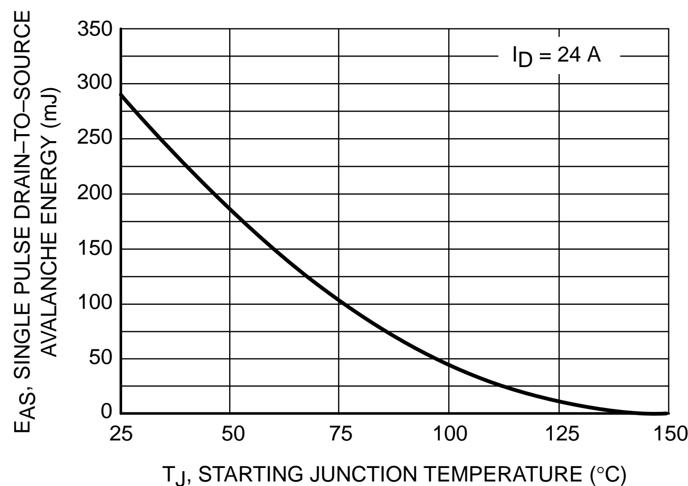


**Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature**

# NTD20N06

*Advance Information*

## Power MOSFET
## 20 Amps, 60 Volts
### N–Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Lower and Tighter $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

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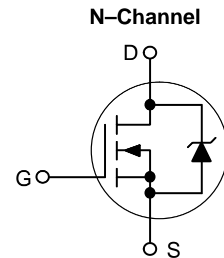
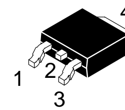
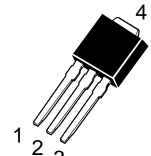
**20 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 46 mΩ**

**N–Channel**




**CASE 369A**
**DPAK**
**(Bent Lead)**
**STYLE 2**




**CASE 369**
**DPAK**
**(Straight Lead)**
**STYLE 2**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

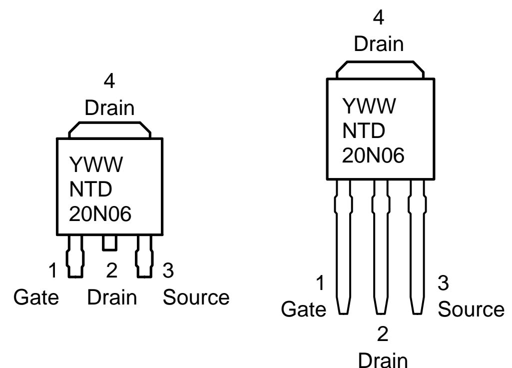
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>± 20<br>± 30 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>20<br>10<br>60 | Adc<br><br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 60<br>0.40<br>1.88<br>1.36 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, L = 1.0 mH, $I_L$(pk) = 18.4 A, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 170 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.)<br>– Junction–to–Ambient (Note 2.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.5<br>80<br>110 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 $in^2$).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

NTD20N06 = Device Code
Y = Year
WW = Work Week

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD20N06 | DPAK | 75 Units/Rail |
| NTD20N06–1 | DPAK Straight Lead | 75 Units/Rail |
| NTD20N06T4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 3.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | 71.7<br>79.4 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.91<br>6.9 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 3.) ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 37.5 | 46 | mΩ |
| Static Drain–to–Source On–Voltage (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 0.78<br>1.57 | 1.10<br>– | Vdc |
| Forward Transconductance (Note 3.) ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | – | 13.2 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 725 | 1015 | pF |
| Output Capacitance | | $C_{oss}$ | – | 213 | 300 | |
| Transfer Capacitance | | $C_{rss}$ | – | 58 | 120 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 3.) | $t_{d(on)}$ | – | 9.5 | 20 | ns |
| Rise Time | | $t_r$ | – | 60.5 | 120 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27.1 | 60 | |
| Fall Time | | $t_f$ | – | 37.1 | 80 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) (Note 3.) | $Q_T$ | – | 21.2 | 30 | nC |
| | | $Q_1$ | – | 5.6 | – | |
| | | $Q_2$ | – | 7.3 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 3.)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.0<br>0.87 | 1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3.) | $t_{rr}$ | – | 42.9 | – | ns |
| | | $t_a$ | – | 33 | – | |
| | | $t_b$ | – | 9.9 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.084 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

# NTD3055-094

*Advance Information*

# Power MOSFET
# 12 Amps, 60 Volts
## N–Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

### Features

- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower and Tighter $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±20<br>±30 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>12<br>10<br>45 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 48<br>0.32<br>2.1<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, L = 1.0 mH<br>$I_{L(pk)}$ = 11 A, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 61 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.)<br>– Junction–to–Ambient (Note 2.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>71.4<br>100 | <br>°C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in$^2$).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in$^2$).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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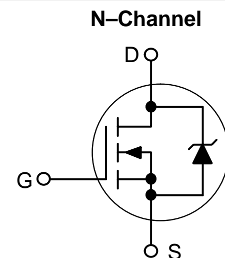
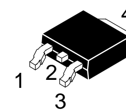
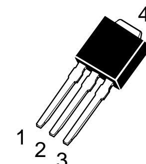
**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 94 mΩ**

**N–Channel**



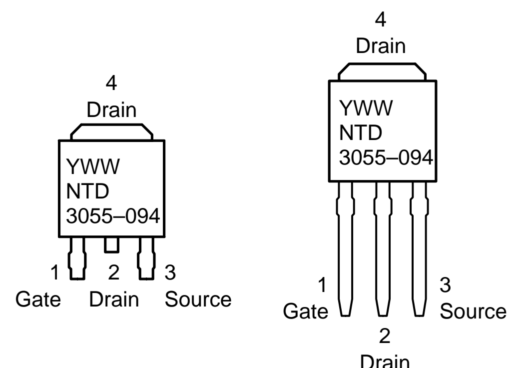

**CASE 369A**
**DPAK**
**(Bent Lead)**
**STYLE 2**




**CASE 369**
**DPAK**
**(Straight Lead)**
**STYLE 2**

NTD3055–094 = Device Code
Y = Year
WW = Work Week

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD3055–094 | DPAK | 75 Units/Rail |
| NTD3055–094–1 | DPAK Straight Lead | 75 Units/Rail |
| NTD3055–094T4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 3.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | 68 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 54.4 | – | mV/°C |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 2.9 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 6.3 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Note 3.) ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 84 | 94 | mOhm |
| Static Drain–to–Source On–Voltage (Note 3.) | | $V_{DS(on)}$ | | | | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 12 Adc) | | | – | 0.85 | 1.35 | |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc, $T_J$ = 150°C) | | | – | 0.77 | – | |
| Forward Transconductance (Note 3.) ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | – | 6.7 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 323 | 450 | pF |
| Output Capacitance | | $C_{oss}$ | – | 107 | 150 | |
| Transfer Capacitance | | $C_{rss}$ | – | 34 | 70 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 3.) | $t_{d(on)}$ | – | 7.7 | 15 | ns |
| Rise Time | | $t_r$ | – | 32.3 | 70 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 25.2 | 50 | |
| Fall Time | | $t_f$ | – | 23.9 | 50 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) (Note 3.) | $Q_T$ | – | 10.9 | 20 | nC |
| | | $Q_1$ | – | 3.1 | – | |
| | | $Q_2$ | – | 4.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc) (Note 3.) | $V_{SD}$ | – | 0.94 | 1.15 | Vdc |
| | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 0.82 | – | |
| Reverse Recovery Time | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3.) | $t_{rr}$ | – | 33.1 | – | ns |
| | | $t_a$ | – | 24 | – | |
| | | $t_b$ | – | 8.9 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.047 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

# NTD3055L104

ON Semiconductor™

http://onsemi.com

## *Advance Information*
# Power MOSFET
# 12 Amps, 60 Volts, Logic Level
## N–Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

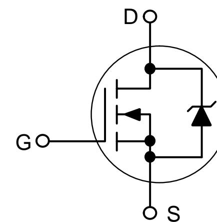
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Tighter $V_{SD}$ Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

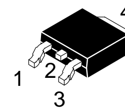
**Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

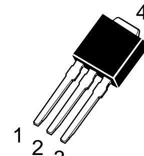
**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 104 mΩ**

N–Channel




CASE 369A
DPAK
(Bent Lead)
STYLE 2




CASE 369
DPAK
(Straight Lead)
STYLE 2

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

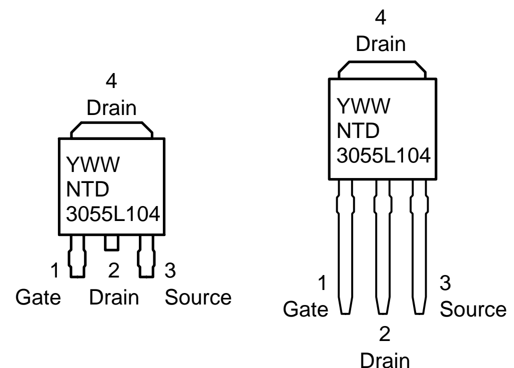
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±15<br>±20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>12<br>10<br>45 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 48<br>0.32<br>2.1<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, L = 1.0 mH $I_{L(pk)}$ = 11 A, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 61 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.)<br>– Junction–to–Ambient (Note 2.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>71.4<br>100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 $in^2$).

This document contains information on a new product. Specifications and information herein are subject to change without notice.

NTD3055L104 = Device Code
Y = Year
WW = Work Week

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD3055L104 | DPAK | 75 Units/Rail |
| NTD3055L104–1 | DPAK Straight Lead | 75 Units/Rail |
| NTD3055L104T4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 3.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | 70 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 62.9 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.6 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.2 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Note 3.) ($V_{GS}$ = 5.0 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 89 | 104 | mOhm |
| Static Drain–to–Source On–Voltage (Note 3.) ($V_{GS}$ = 5.0 Vdc, $I_D$ = 12 Adc) | | $V_{DS(on)}$ | – | 0.98 | 1.50 | Vdc |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 6.0 Adc, $T_J$ = 150°C) | | | – | 0.86 | – | |
| Forward Transconductance (Note 3.) ($V_{DS}$ = 8.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | – | 9.1 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 316 | 440 | pF |
| Output Capacitance | | $C_{oss}$ | – | 105 | 150 | |
| Transfer Capacitance | | $C_{rss}$ | – | 35 | 70 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) (Note 3.) | $t_{d(on)}$ | – | 9.2 | 20 | ns |
| Rise Time | | $t_r$ | – | 104 | 210 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 19 | 40 | |
| Fall Time | | $t_f$ | – | 40.5 | 80 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5.0 Vdc) (Note 3.) | $Q_T$ | – | 7.4 | 20 | nC |
| | | $Q_1$ | – | 2.0 | – | |
| | | $Q_2$ | – | 4.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc) (Note 3.) | $V_{SD}$ | – | 0.95 | 1.2 | Vdc |
| | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 0.82 | – | |
| Reverse Recovery Time | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3.) | $t_{rr}$ | – | 35 | – | ns |
| | | $t_a$ | – | 21 | – | |
| | | $t_b$ | – | 14 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.04 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

# NTD32N06

**ON Semiconductor™**

**http://onsemi.com**

## Power MOSFET 32 Amps, 60 Volts

### N–Channel DPAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

- Smaller Package than MTB36N06V
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Total Gate Charge
- Lower and Tighter $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

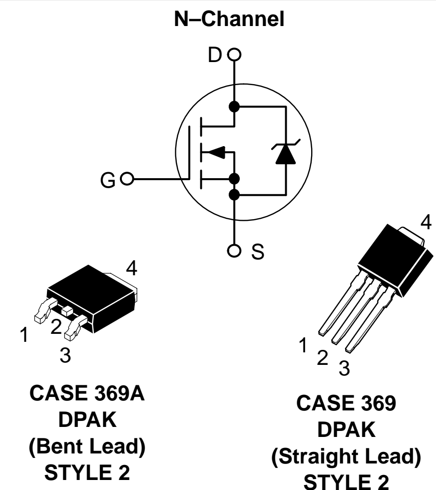
- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>± 20<br>± 30 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>32<br>22<br>90 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 93.75<br>0.625<br>2.88<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C (Note 3.)<br>($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, L = 1.0 mH, $I_{L(pk)}$ = 25 A, $V_{DS}$ = 60 Vdc, $R_G$ = 25 Ω) | $E_{AS}$ | 313 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.)<br>– Junction–to–Ambient (Note 2.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.6<br>52<br>100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

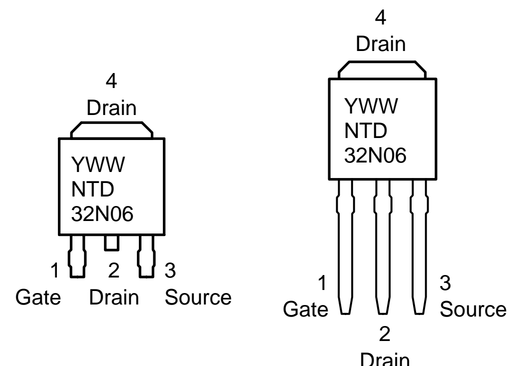
1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in$^2$).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in$^2$).
3. Repetitive rating; pulse width limited by maximum junction temperature.

**32 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 26 mΩ**




| | |
|---|---|
| NTD32N06 | = Device Code |
| Y | = Year |
| WW | = Work Week |
| T | = MOSFET |

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD32N06 | DPAK | 75 Units/Rail |
| NTD32N06–1 | DPAK Straight Lead | 75 Units/Rail |
| NTD32N06T4 | DPAK | 2500 Tape & Reel |

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March, 2001 – Rev. 1

Publication Order Number:
NTD32N06/D

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 4.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | 70<br>41.6 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage (Note 4.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>7.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 4.) ($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 21 | 26 | mOhm |
| Static Drain–to–Source On–Voltage (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 32 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>–<br>– | 0.417<br>0.680<br>0.633 | 0.62<br>–<br>– | Vdc |
| Forward Transconductance (Note 4.) ($V_{DS}$ = 6 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | – | 21.1 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1231 | 1725 | pF |
| Output Capacitance | | $C_{oss}$ | – | 346 | 485 | |
| Transfer Capacitance | | $C_{rss}$ | – | 77 | 160 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 4.) | $t_{d(on)}$ | – | 10 | 25 | ns |
| Rise Time | | $t_r$ | – | 84 | 180 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 31 | 70 | |
| Fall Time | | $t_f$ | – | 93 | 200 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) (Note 4.) | $Q_T$ | – | 33 | 60 | nC |
| | | $Q_1$ | – | 6.0 | – | |
| | | $Q_2$ | – | 15 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>–<br>– | 0.89<br>0.96<br>0.75 | 1.0<br>–<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4.) | $t_{rr}$ | – | 52 | – | ns |
| | | $t_a$ | – | 37 | – | |
| | | $t_b$ | – | 14.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.095 | – | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

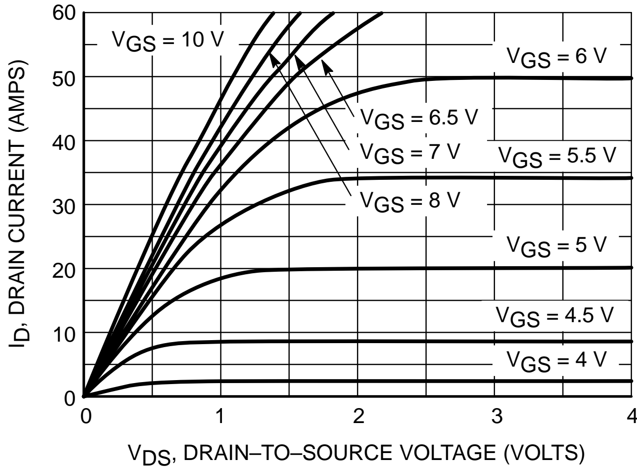


**Figure 1. On–Region Characteristics**

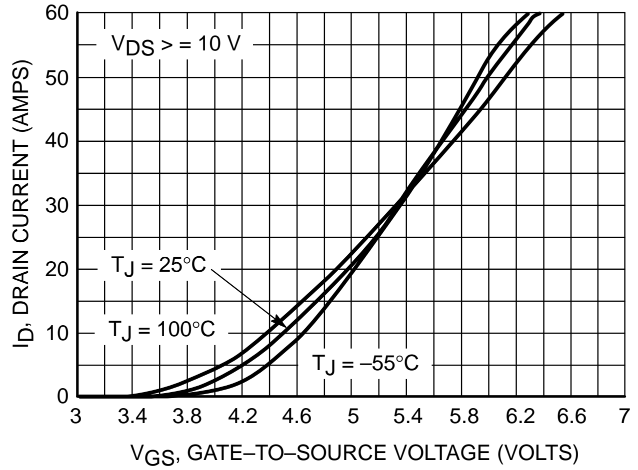


**Figure 2. Transfer Characteristics**

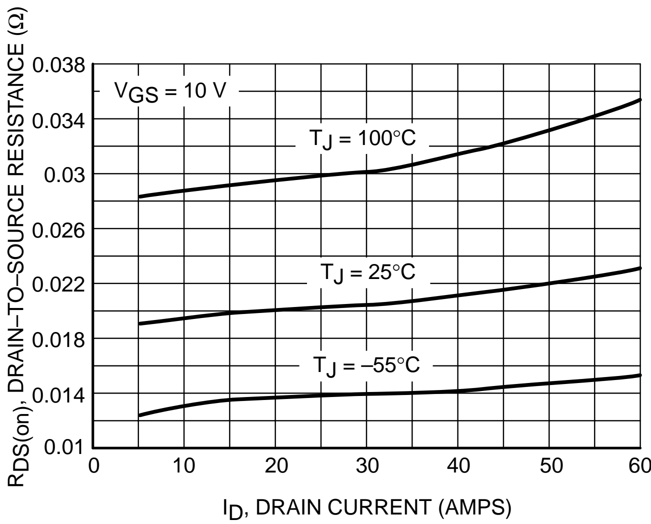


**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

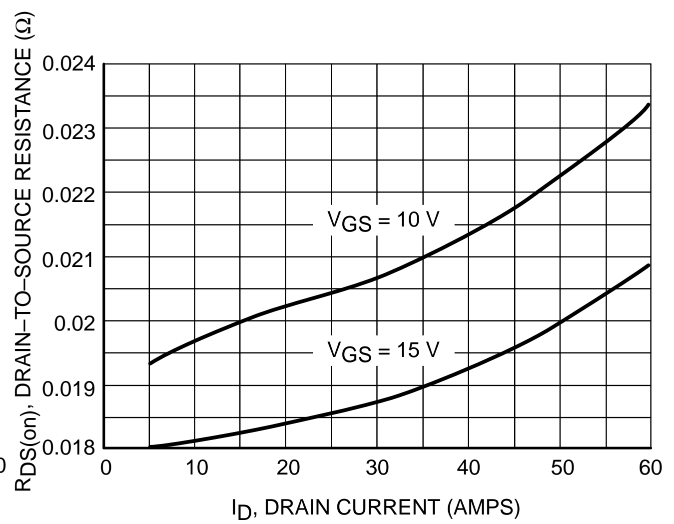


**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

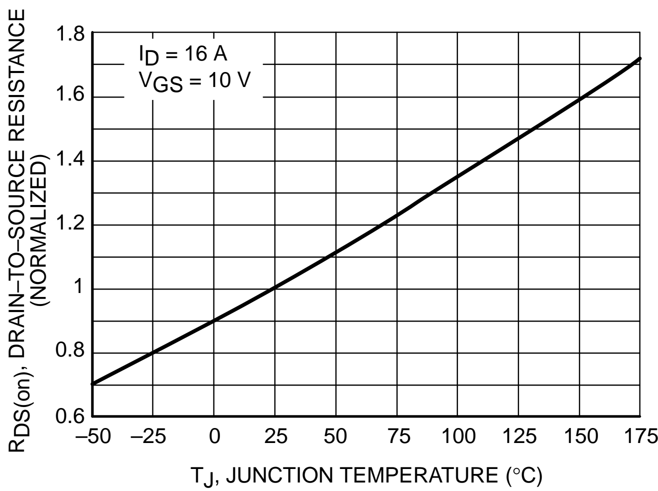


**Figure 5. On–Resistance Variation with Temperature**

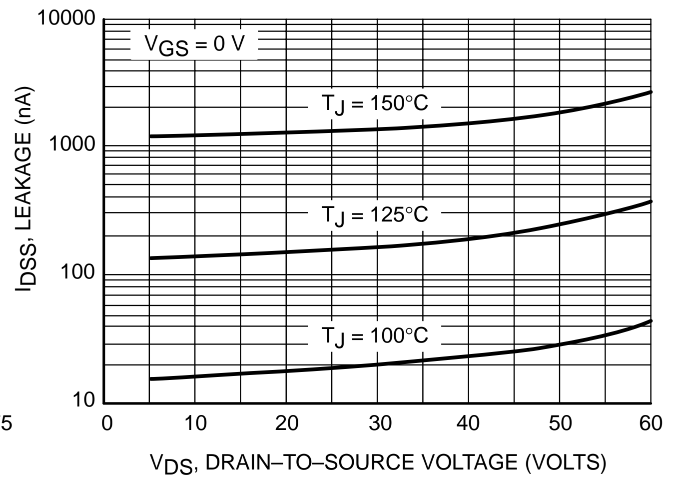


**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

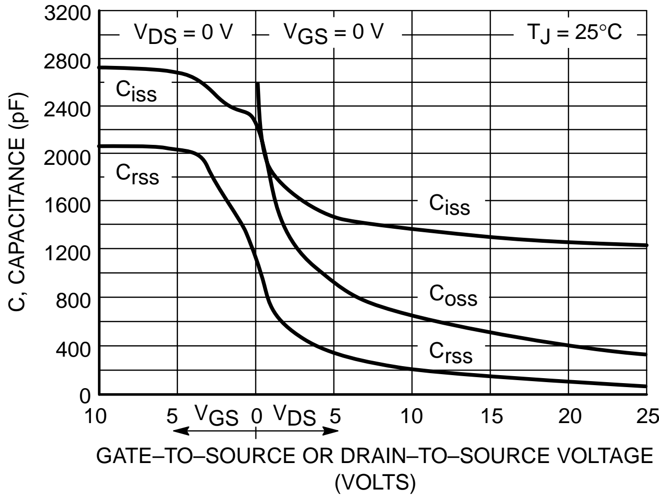


**Figure 7. Capacitance Variation**

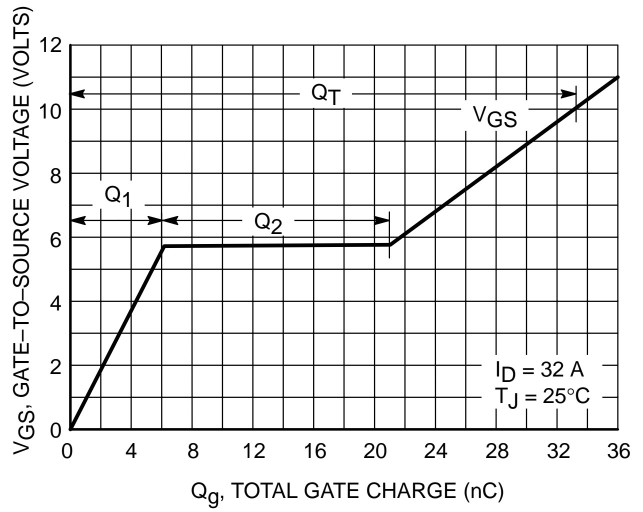


**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

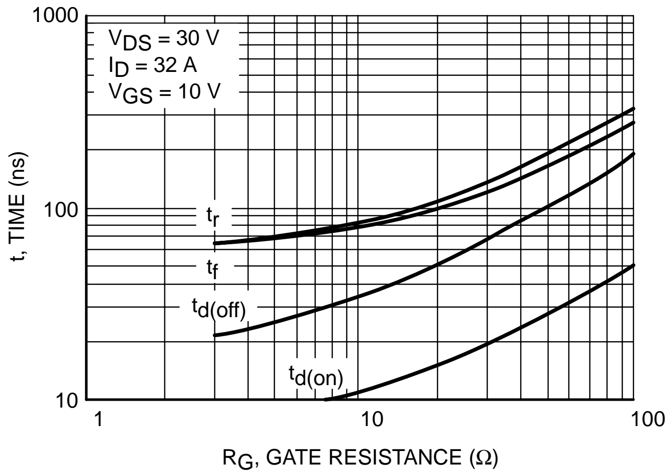


**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

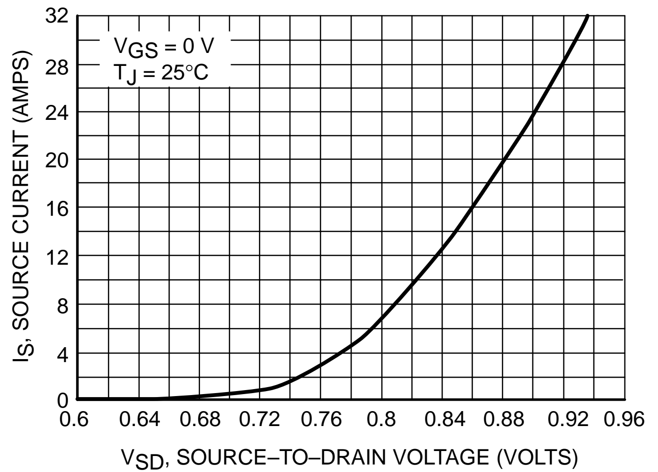


**Figure 10. Diode Forward Voltage vs. Current**

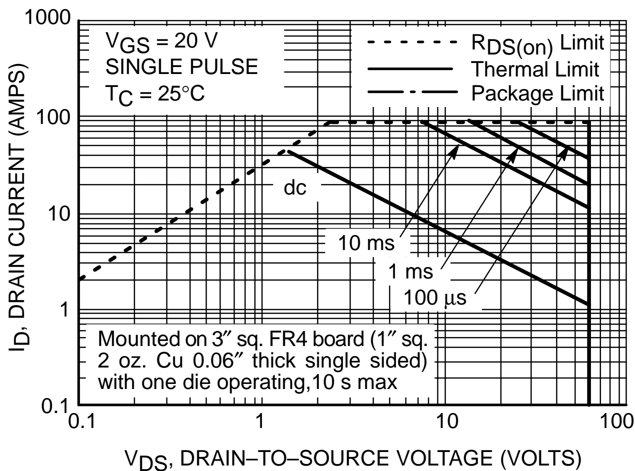


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

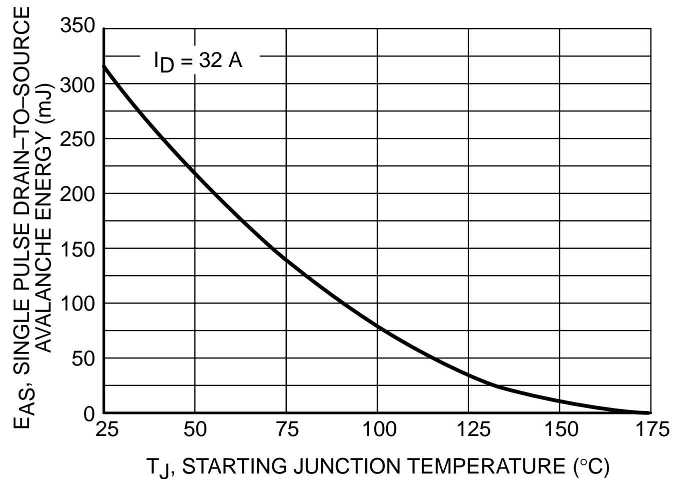


**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

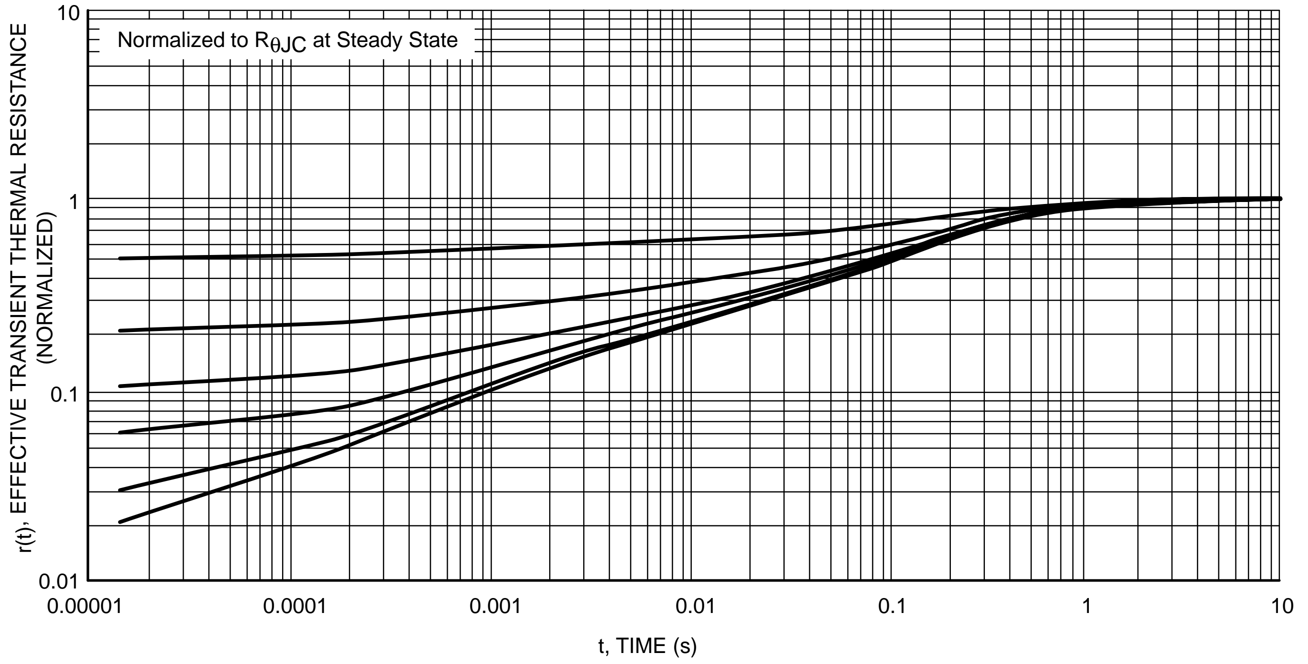


**Figure 13. Thermal Response**

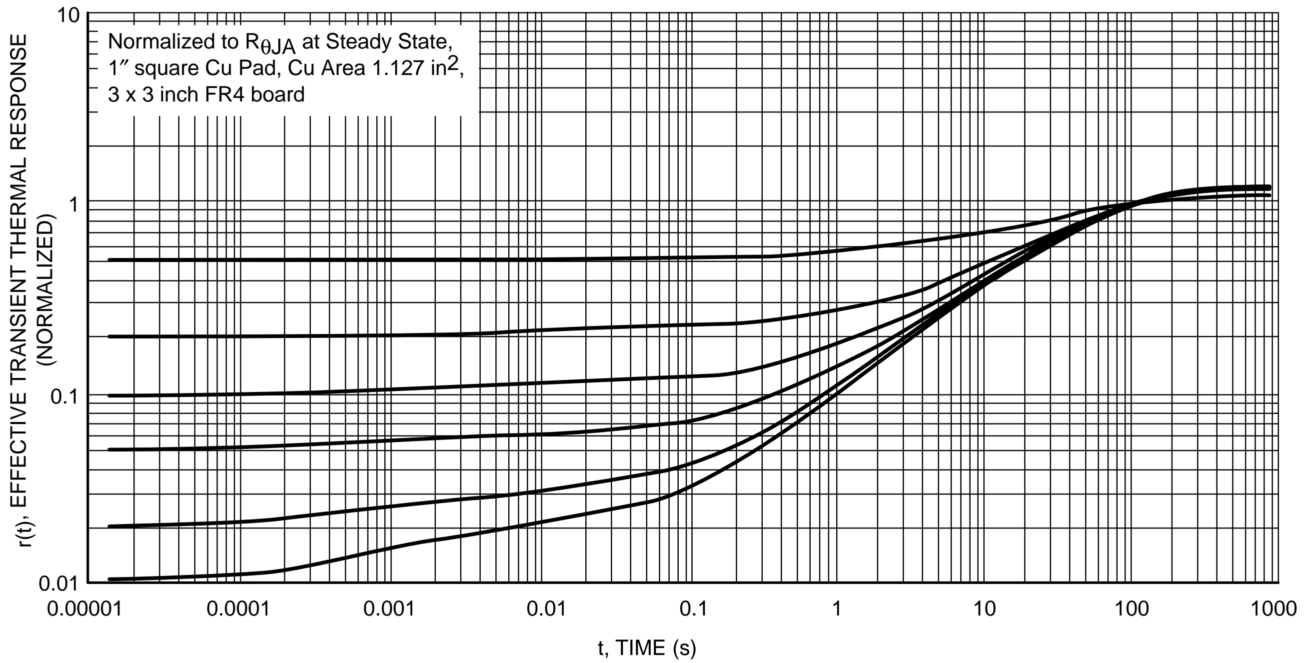


**Figure 14. Thermal Response**

# NTD32N06L

## Power MOSFET
## 32 Amps, 60 Volts, Logic Level
### N–Channel DPAK

**ON Semiconductor**™

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Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

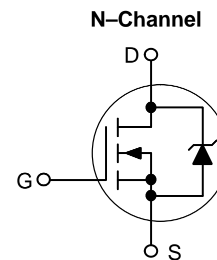
- Smaller Package than MTB30N06VL
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Total Gate Charge
- Lower and Tighter $V_{SD}$
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

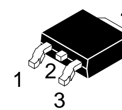
- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**32 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

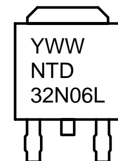
**N–Channel**




**MARKING DIAGRAM**

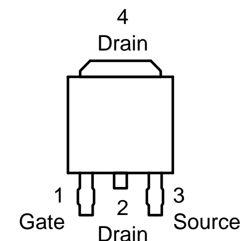



**CASE 369A**
**DPAK**
**STYLE 2**




NTD32N06L = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±15<br>±20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>32<br>22<br>90 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 93.75<br>0.625<br>2.88<br>1.5 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C (Note 3.)<br>($V_{DD}$ = 50 Vdc, $V_{GS}$ = 5 Vdc, L = 1.0 mH, $I_{L(pk)}$ = 25 A, $V_{DS}$ = 60 Vdc, $R_G$ = 25 Ω) | $E_{AS}$ | 313 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1.)<br>– Junction–to–Ambient (Note 2.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.6<br>52<br>100 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in$^2$).
2. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in$^2$).
3. Repetitive rating; pulse width limited by maximum junction temperature.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD32N06L | DPAK | 75 Units/Rail |
| NTD32N06L–1 | DPAK | 75 Units/Rail |
| NTD32N06LT4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 4.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | 70<br>62 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage (Note 4.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.7<br>4.8 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 4.) ($V_{GS}$ = 5 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 23.7 | 28 | mOhm |
| Static Drain–to–Source On–Resistance (Note 4.)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 32 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 16 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>–<br>– | 0.48<br>0.78<br>0.61 | 0.67<br>–<br>– | Vdc |
| Forward Transconductance (Note 4.) ($V_{DS}$ = 6 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | – | 27 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1214 | 1700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 343 | 480 | |
| Transfer Capacitance | | $C_{rss}$ | – | 87 | 180 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) (Note 4.) | $t_{d(on)}$ | – | 12.8 | 30 | ns |
| Rise Time | | $t_r$ | – | 221 | 450 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 37 | 80 | |
| Fall Time | | $t_f$ | – | 128 | 260 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 5 Vdc) (Note 4.) | $Q_T$ | – | 23 | 50 | nC |
| | | $Q_1$ | – | 4.5 | – | |
| | | $Q_2$ | – | 14 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>–<br>– | 0.89<br>0.95<br>0.74 | 1.0<br>–<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4.) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 31 | – | |
| | | $t_b$ | – | 25 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.093 | – | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.

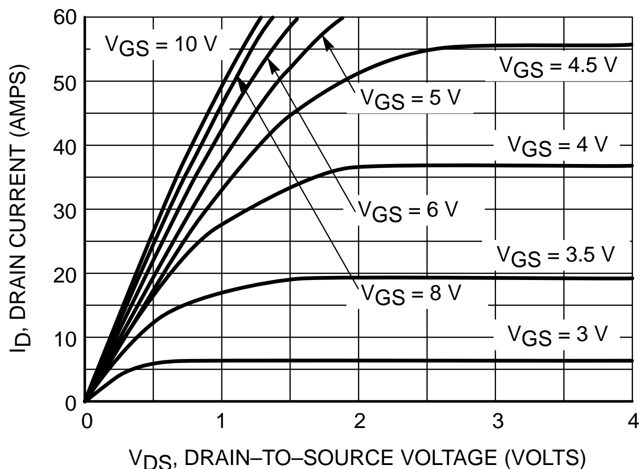



**Figure 1. On–Region Characteristics**

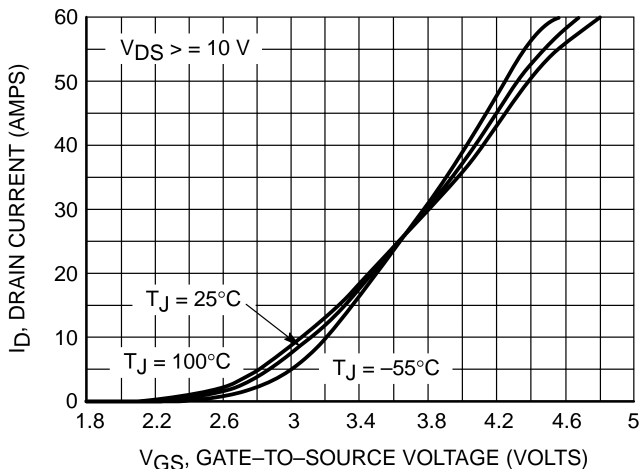



**Figure 2. Transfer Characteristics**

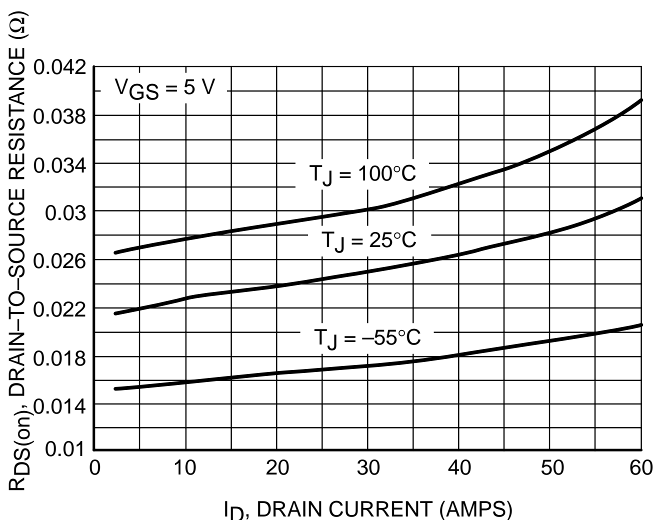



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

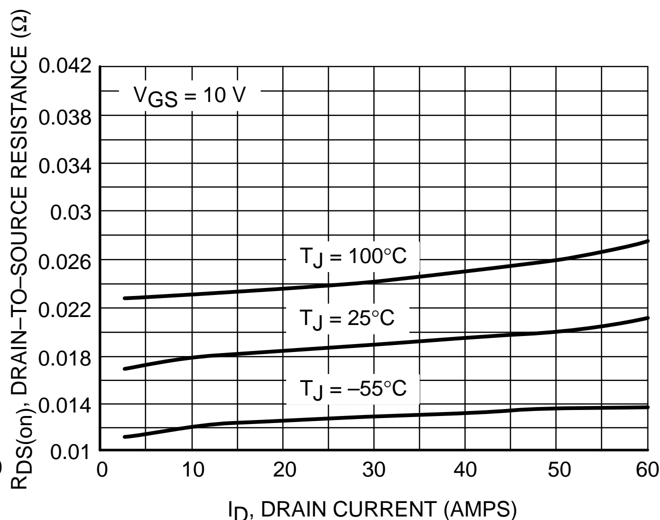



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

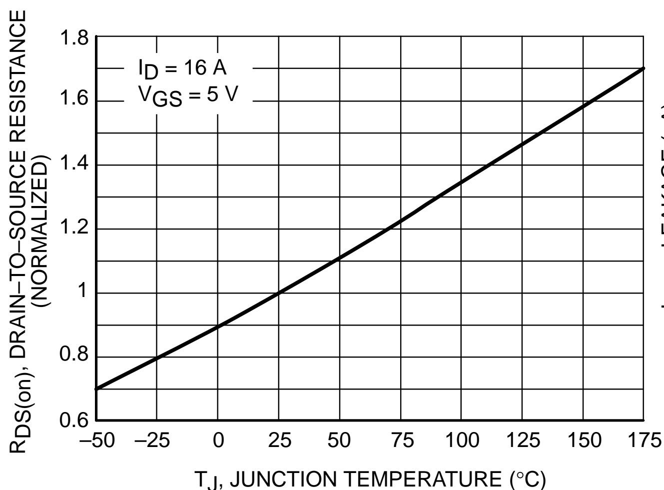



**Figure 5. On–Resistance Variation with Temperature**

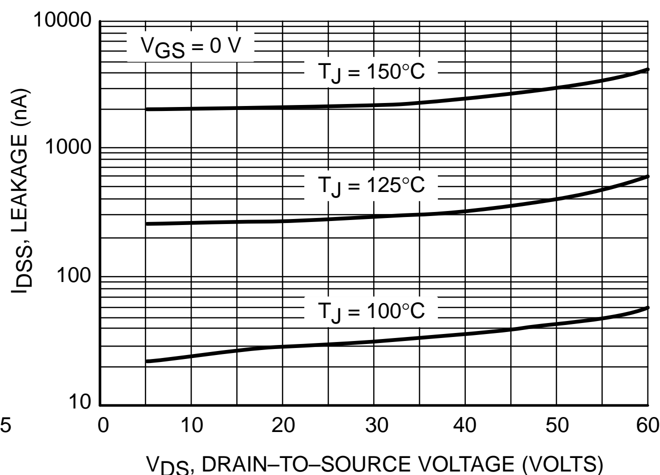



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

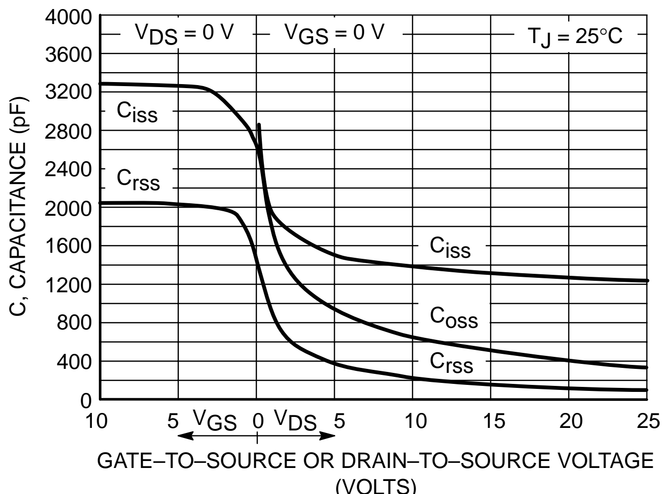



**Figure 7. Capacitance Variation**

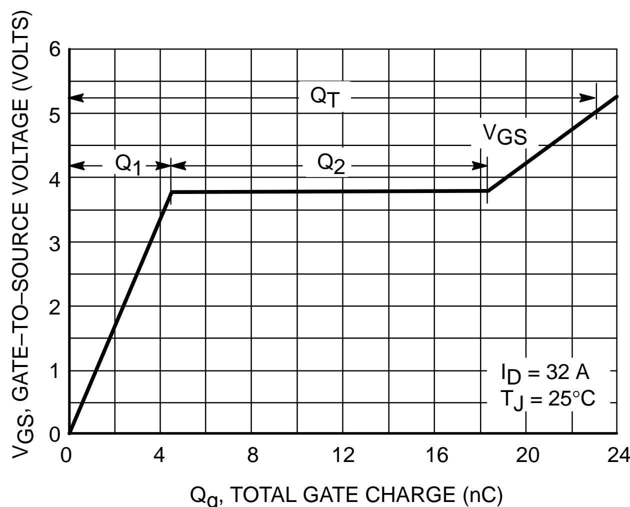



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

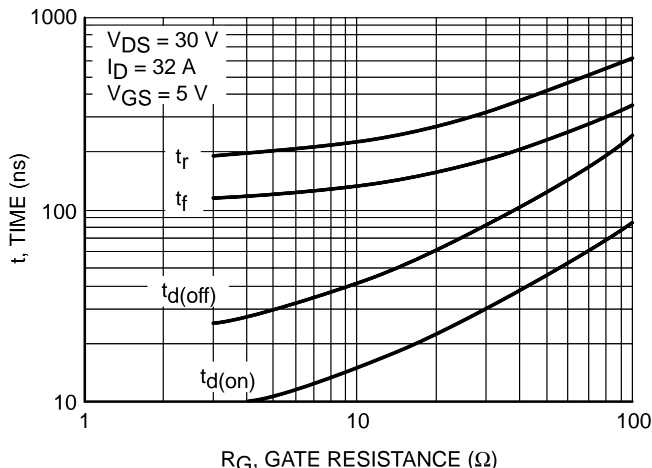



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

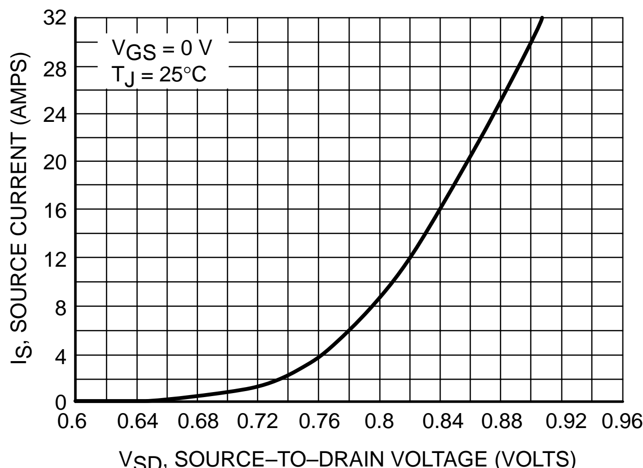



**Figure 10. Diode Forward Voltage vs. Current**

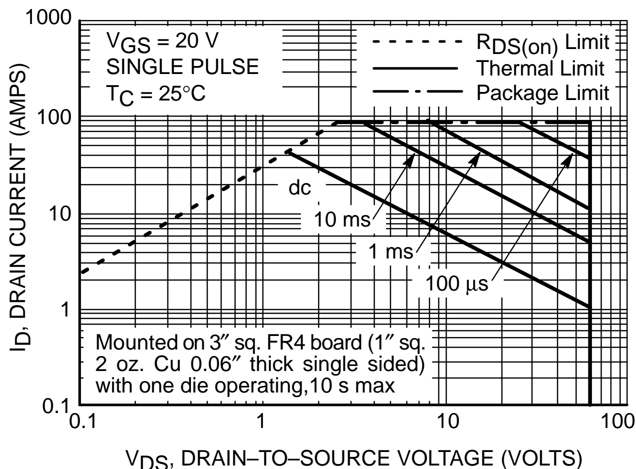



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

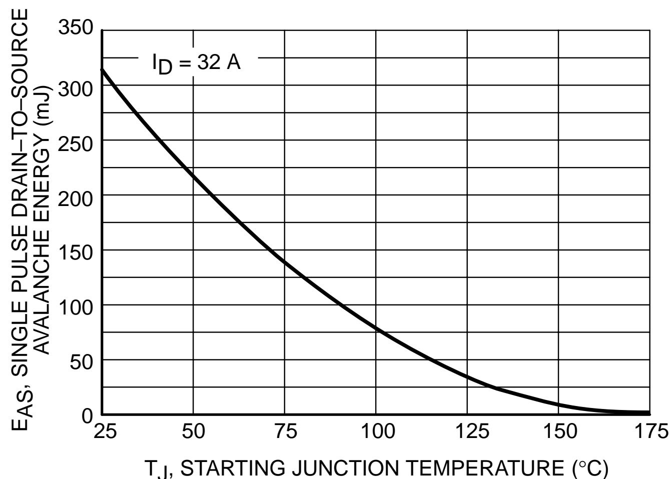



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

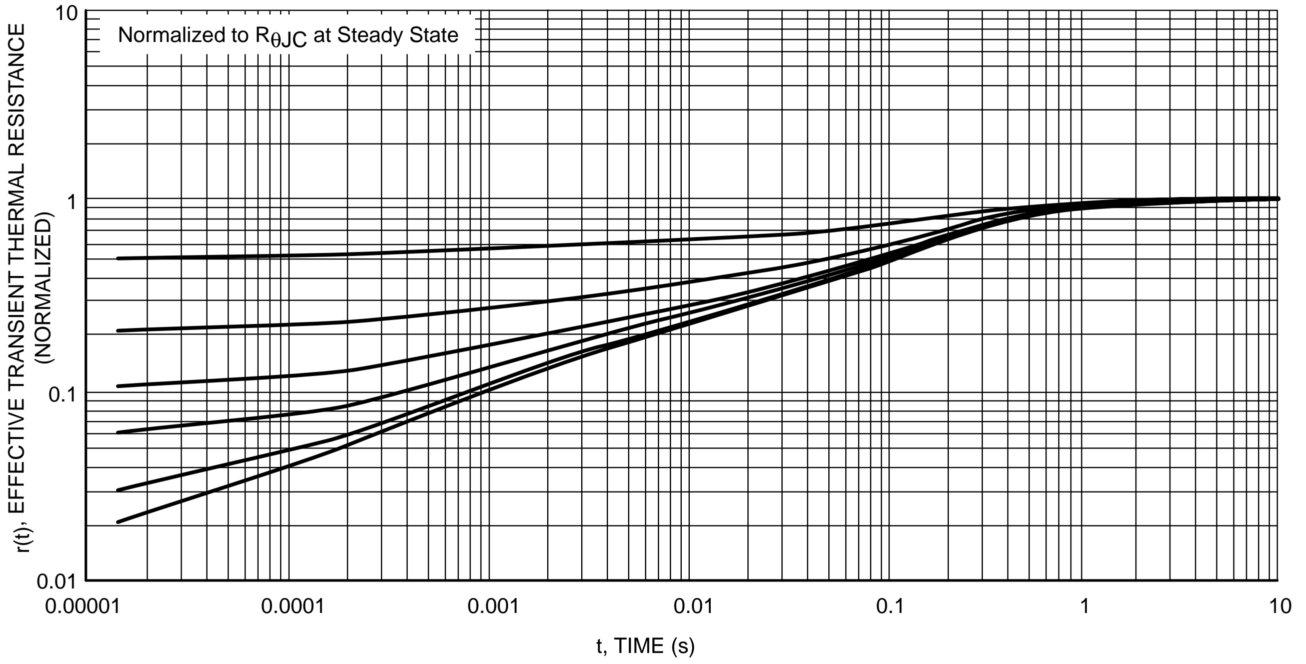



Figure 13. Thermal Response

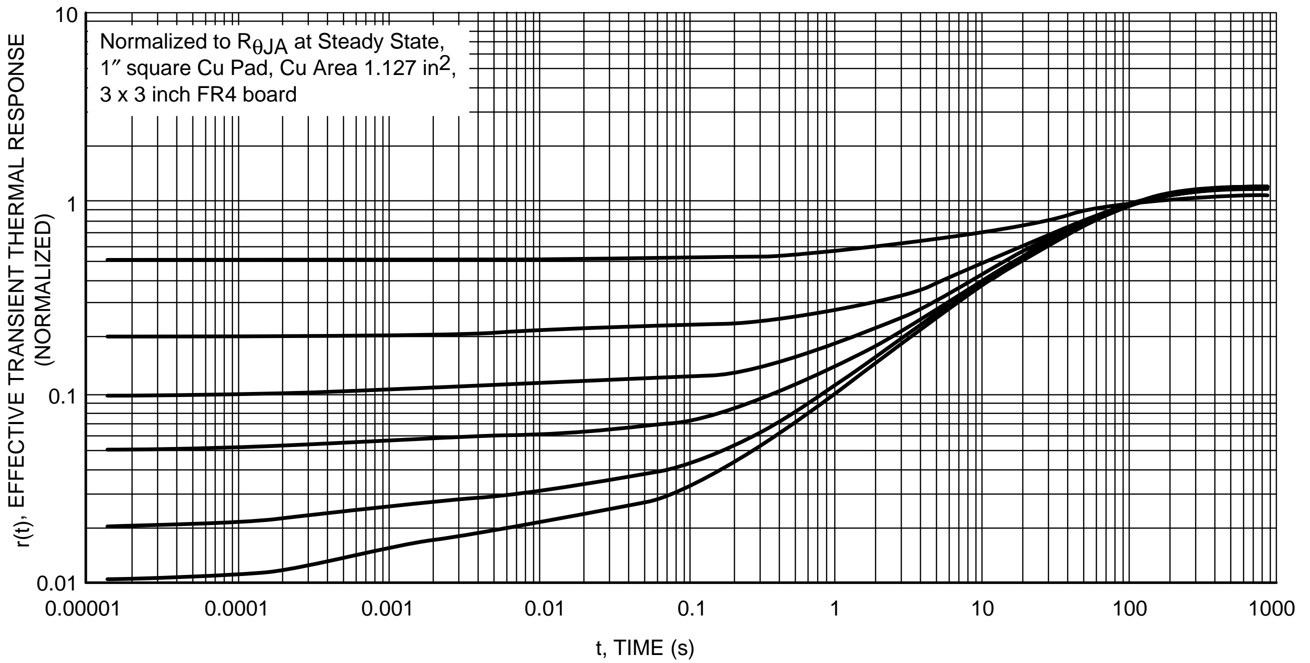



Figure 14. Thermal Response

# NTD4302

## Power MOSFET 18.5 Amps, 30 Volts

### N–Channel DPAK

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- $I_{DSS}$ Specified at Elevated Temperature
- SO–8 Mounting Information Provided

**Applications**

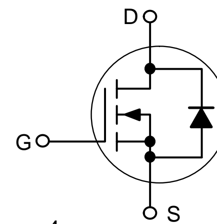
- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery Powered Products: i.e., Computers, Printers, Cellular and Cordless Telephones, and PCMCIA Cards

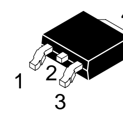
**ON Semiconductor™**

**http://onsemi.com**

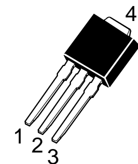
**18.5 AMPERES**
**30 VOLTS**
**10 mΩ @ $V_{GS}$ = 10 V**

**N–Channel**



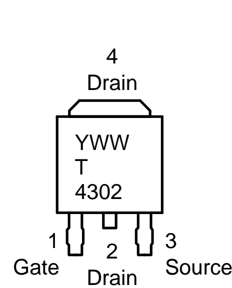



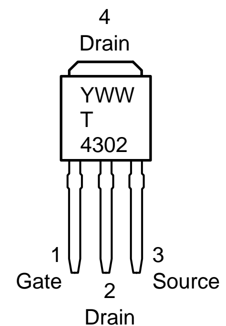

**CASE 369A**
**DPAK**
**(Bend Lead)**
**STYLE 2**




**CASE 369**
**DPAK**
**(Straight Lead)**
**STYLE 2**

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




4302 = Device Code
Y = Year
WW = Work Week
T = MOSFET

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTD4302 | DPAK | 75 Units/Rail |
| NTD4302–1 | DPAK Straight Lead | 75 Units/Rail |
| NTD4302T4 | DPAK | 2500 Tape & Reel |

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March, 2001 – Rev. 1
Publication Order Number:
NTD4302/D

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Thermal Resistance<br>– Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Pulsed Drain Current (Note 5.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>1.3<br>96<br>30<br>90 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Thermal Resistance<br>– Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 5.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>25<br>5.0<br>18.5<br>11.5<br>60 | <br>°C/W<br>Watts<br>Amps<br>Amps<br>Amps |
| Thermal Resistance<br>– Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 5.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>67<br>1.87<br>11.3<br>7.1<br>36 | <br>°C/W<br>Watts<br>Amps<br>Amps<br>Amps |
| Thermal Resistance<br>– Junction–to–Ambient (Note 4.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 5.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>120<br>1.04<br>8.4<br>5.3<br>28 | <br>°C/W<br>Watts<br>Amps<br>Amps<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 17 Apk, L = 5.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 722 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on Heat Sink, Steady State.
2. Mounted on 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Time ≤ 10 seconds.
3. Mounted on 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Steady State.
4. Minimum FR–4 or G–10 PCB, Steady State.
5. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μA) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Positive Temperature Coefficient | | | – | 25 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = 30 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{GS}$ = 0 Vdc, $V_{DS}$ = 30 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.9 | 3.0 | Vdc |
| Negative Temperature Coefficient | | | – | –3.8 | – | |
| Static Drain–Source On–State Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 18.5 Adc) | | $R_{DS(on)}$ | – | 0.0078 | 0.010 | Ω |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | | – | 0.0078 | 0.010 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | | – | 0.010 | 0.013 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 10 Adc) | | gFS | – | 20 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2050 | 2400 | pF |
| Output Capacitance | | $C_{oss}$ | – | 640 | 800 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 225 | 310 | |
| **SWITCHING CHARACTERISTICS** (Note 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 15 | 25 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 85 | 130 | |
| Fall Time | | $t_f$ | – | 55 | 90 | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 2.5 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 13 | 20 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 55 | 90 | |
| Fall Time | | $t_f$ | – | 40 | 75 | |
| Turn–On Delay Time | ($V_{DD}$ = 24 Vdc, $I_D$ = 18.5 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 2.5 Ω) | $t_{d(on)}$ | – | 15 | – | ns |
| Rise Time | | $t_r$ | – | 25 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 40 | – | |
| Fall Time | | $t_f$ | – | 58 | – | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 55 | 80 | nC |
| | | $Q_{gs}$ (Q1) | – | 5.5 | – | |
| | | $Q_{gd}$ (Q2) | – | 15 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc) | | $V_{SD}$ | – | 0.75 | 1.0 | Vdc |
| ($I_S$ = 18.5 Adc, $V_{GS}$ = 0 Vdc) | | | – | 0.88 | – | |
| ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | 0.65 | – | |
| Reverse Recovery Time | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 39 | 65 | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 19 | – | |
| Reverse Recovery Stored Charge | | $Q_{rr}$ | – | 0.043 | – | μC |

6. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperature.

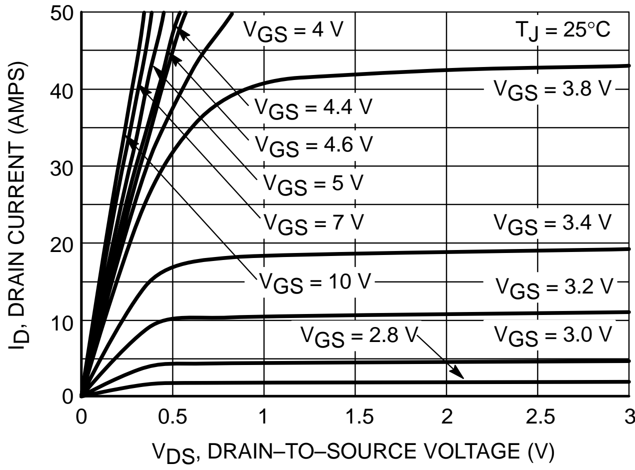



**Figure 1. On–Region Characteristics**

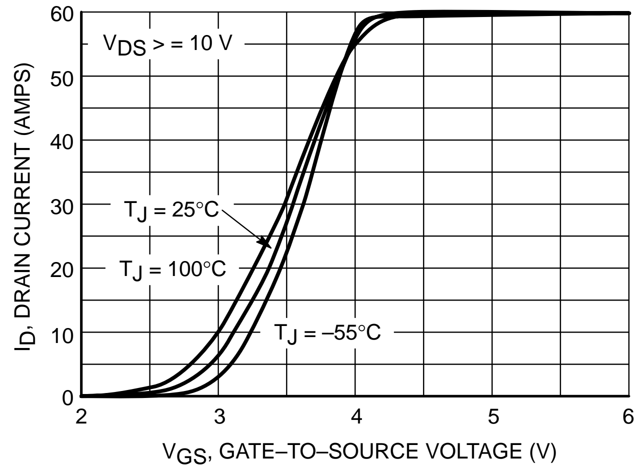



**Figure 2. Transfer Characteristics**

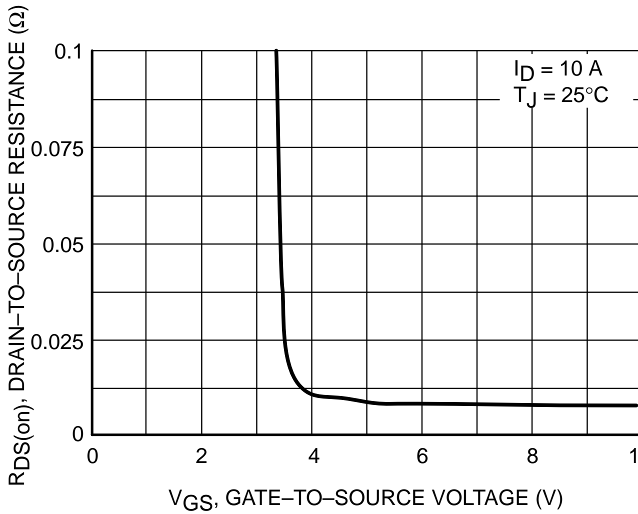



**Figure 3. On–Resistance vs. Gate–To–Source Voltage**

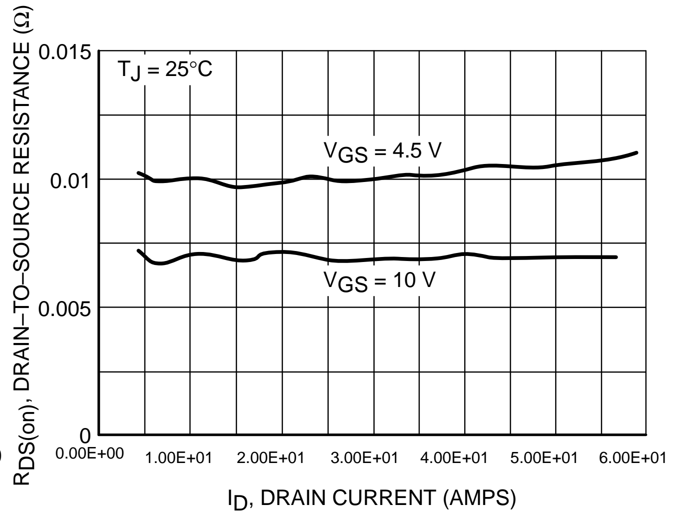



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

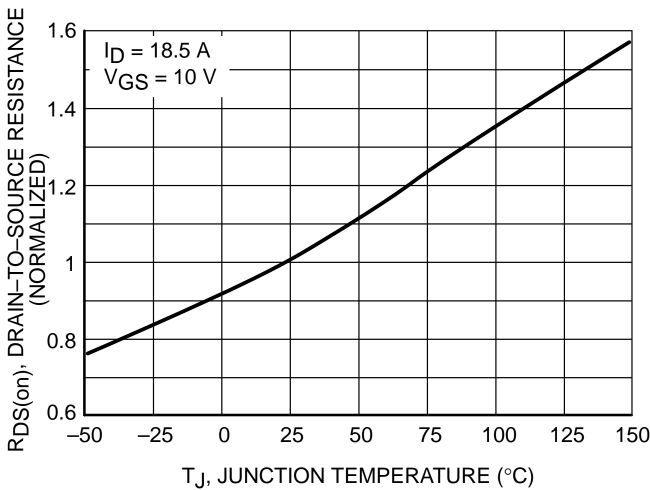



**Figure 5. On–Resistance Variation with Temperature**

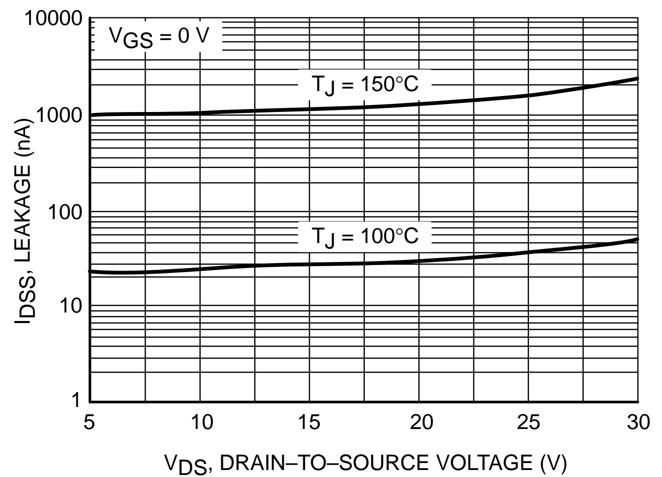



**Figure 6. Drain–To–Source Leakage Current vs. Voltage**

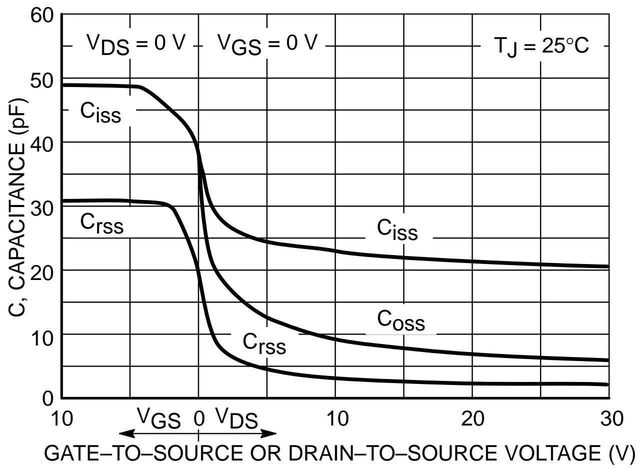



**Figure 7. Capacitance Variation**

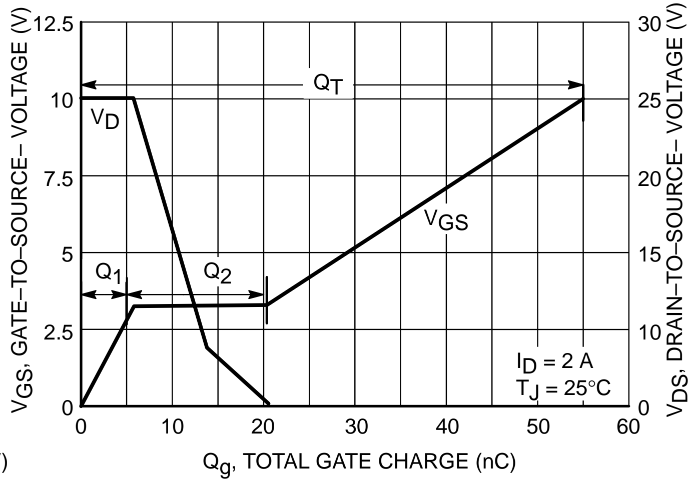



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

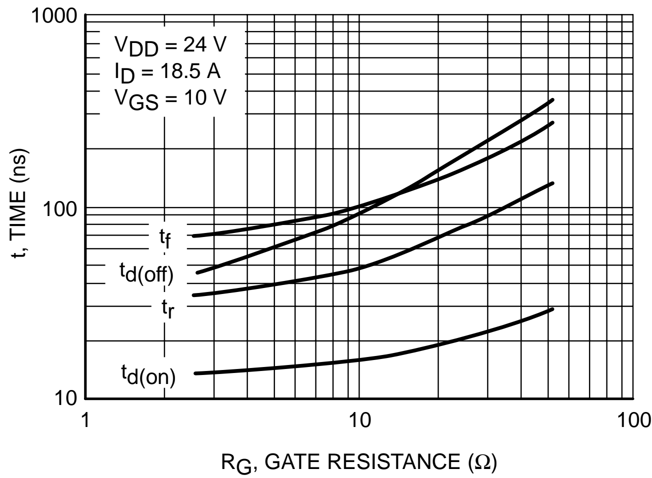



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

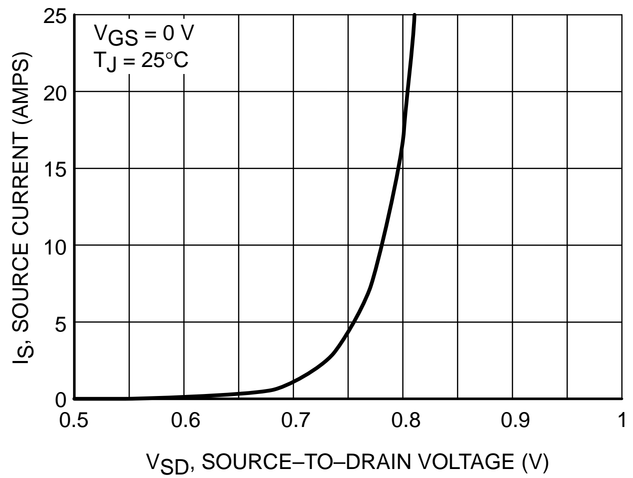



**Figure 10. Diode Forward Voltage vs. Current**

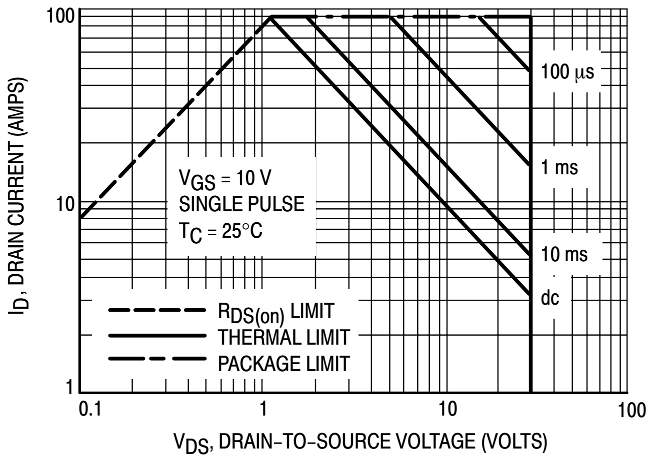



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

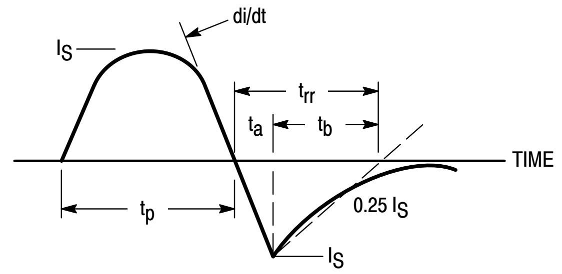



**Figure 12. Diode Reverse Recovery Waveform**

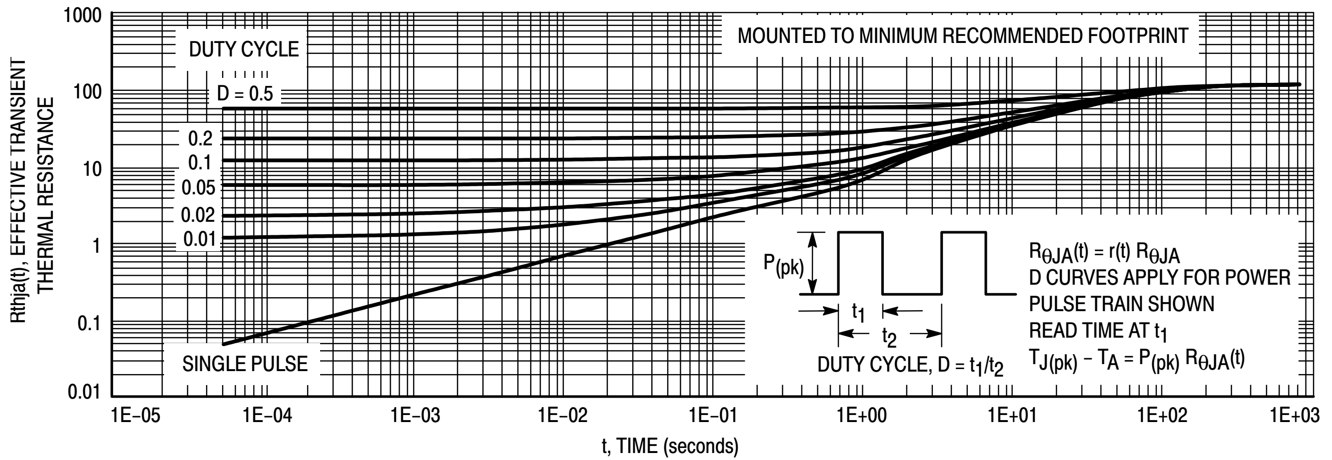
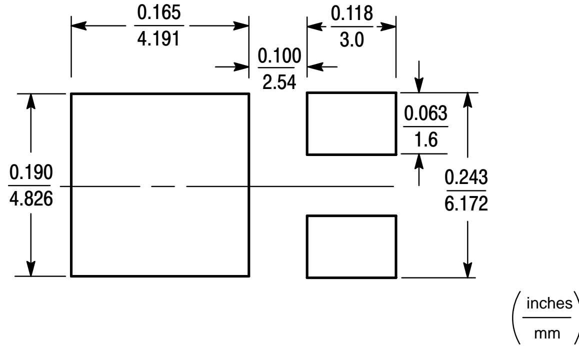



**Figure 13. Thermal Response – Various Duty Cycles**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 14 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

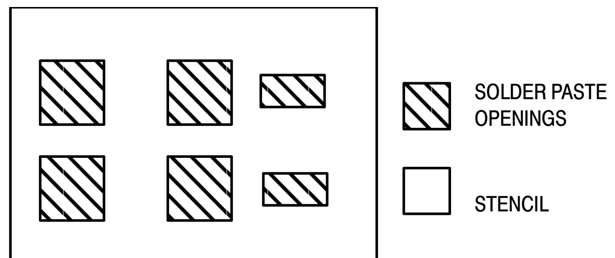



**Figure 14. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

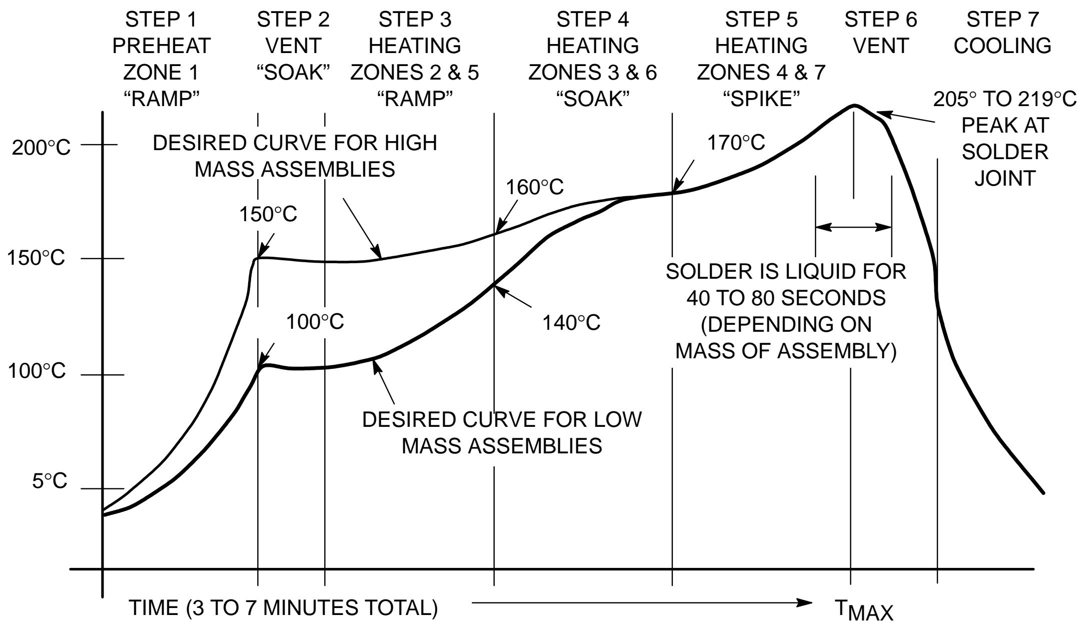



**Figure 15. Typical Solder Heating Profile**

# NTGS3433T1

*Product Preview*

# MOSFET -3.3 Amps, -12 Volts

## P–Channel TSOP–6

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP–6 Surface Mount Package

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –12 | Volts |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Volts |
| Thermal Resistance<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS)<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$<br>$P_d$<br>$I_D$ | <br>62.5<br>2.0<br>–3.3<br><br>–20<br>1.0<br>–2.35 | <br>°C/W<br>Watts<br>Amps<br><br>Amps<br>Watts<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS)<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$<br>$P_d$<br>$I_D$ | <br>128<br>1.0<br><br>–2.35<br>–14<br>0.5<br>–1.65 | <br>°C/W<br>Watts<br><br>Amps<br>Amps<br>Watts<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes for 10 Seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), t < 5.0 seconds.
2. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), operating to steady state.

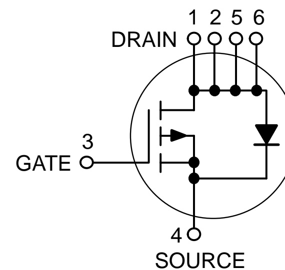
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ON Semiconductor™**

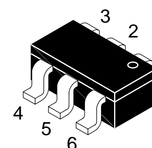
**http://onsemi.com**

**–3.3 AMPERES**
**–12 VOLTS**
**75 mΩ @ $V_{GS}$ = –4.5 V**

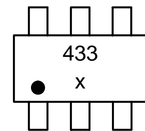
**P–Channel**




**MARKING DIAGRAM**

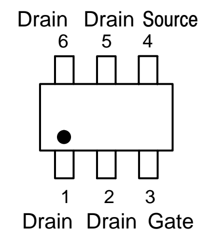



**TSOP–6**
**CASE 318G**
**STYLE 1**




433 = Device Code
x = Date Code

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTGS3433T1 | TSOP–6 | 3000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Notes 3. & 4.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –10 μA) | | $V_{(BR)DSS}$ | –12 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –8 Vdc, $T_J$ = 25°C) ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –8 Vdc, $T_J$ = 70°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–5.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –0.50 | –0.70 | –1.50 | Vdc |
| Static Drain–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –3.3 Adc) ($V_{GS}$ = –2.5 Vdc, $I_D$ = –2.9 Adc) | | $R_{DS(on)}$ | –<br>– | 0.055<br>0.075 | 0.075<br>0.095 | Ω |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –3.3 Adc) | | $g_{FS}$ | – | 7.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Total Gate Charge | ($V_{DS}$ = –10 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –3.3 Adc) | $Q_{tot}$ | – | 7.0 | 15 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 3.5 | – | |
| Input Capacitance | ($V_{DS}$ = –5.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 450 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 200 | – | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –4.5 Vdc, $R_g$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | 30 | ns |
| Rise Time | | $t_r$ | – | 20 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 110 | 120 | |
| Fall Time | | $t_f$ | – | 100 | 115 | |
| Reverse Recovery Time | ($I_S$ = –1.7 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 30 | – | ns |
| **BODY–DRAIN DIODE RATINGS** | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.80 | –1.5 | Vdc |
| Diode Forward On–Voltage | ($I_S$ = –3.3 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.90 | – | Vdc |

3. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.
4. Class 1 ESD rated – Handling precautions to protect against electrostatic discharge is mandatory.

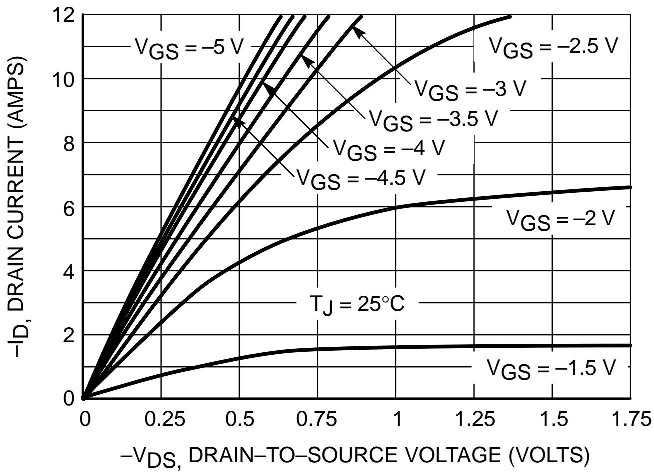


**Figure 1. On–Region Characteristics**

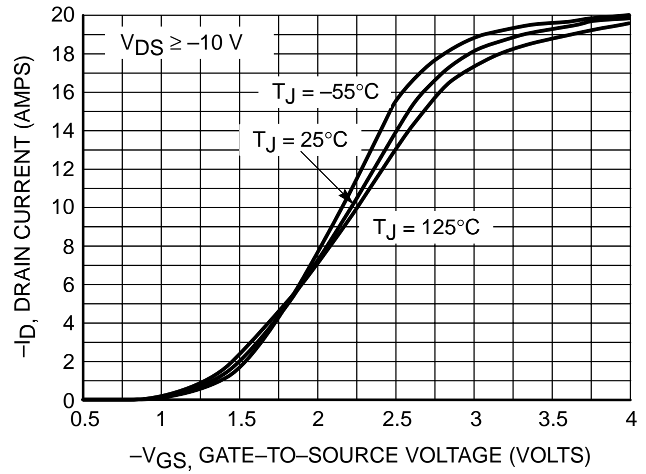


**Figure 2. Transfer Characteristics**

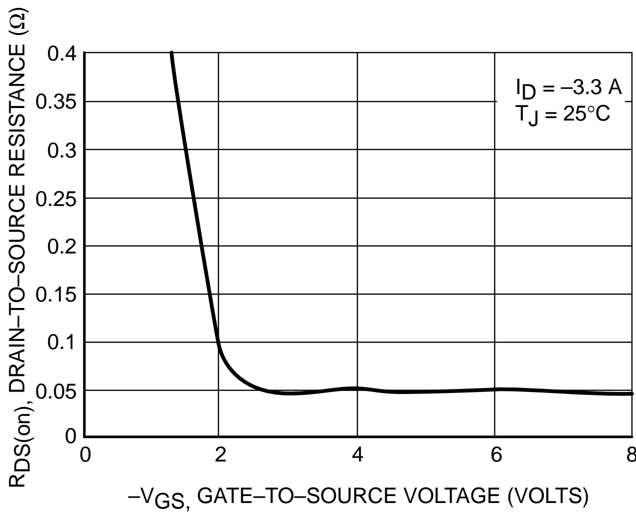


**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

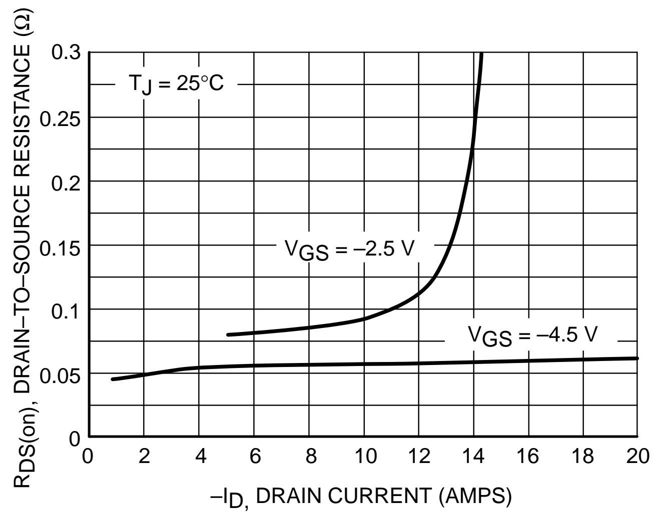


**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

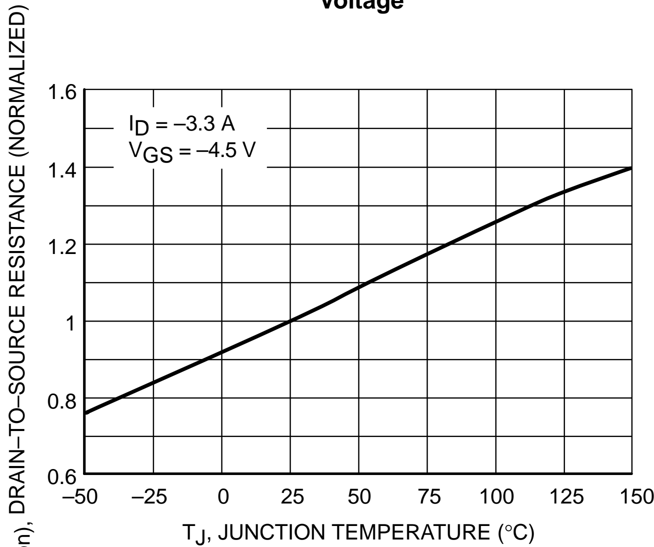


**Figure 5. On–Resistance Variation with Temperature**

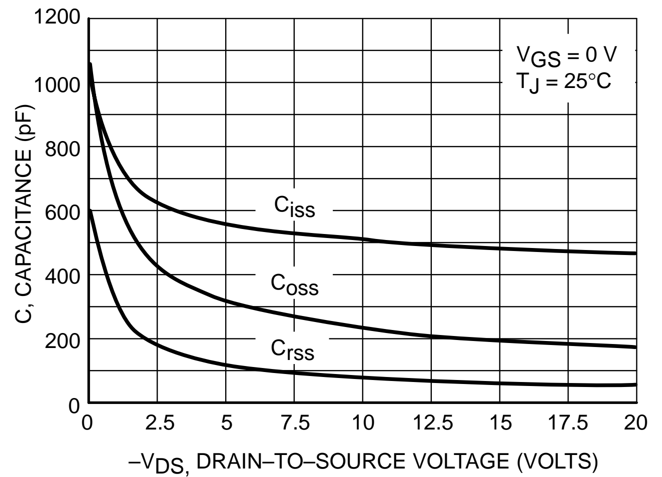


**Figure 6. Capacitance Variation**

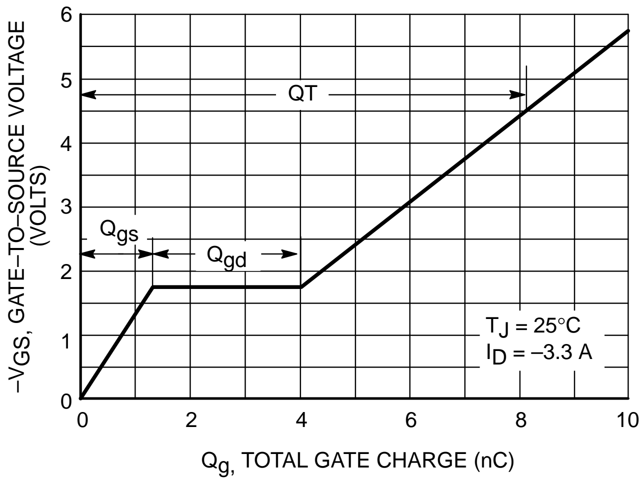


Figure 7. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

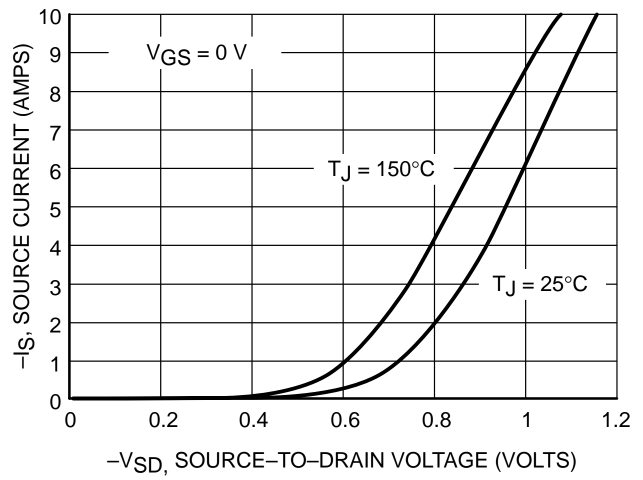


Figure 8. Diode Forward Voltage vs. Current

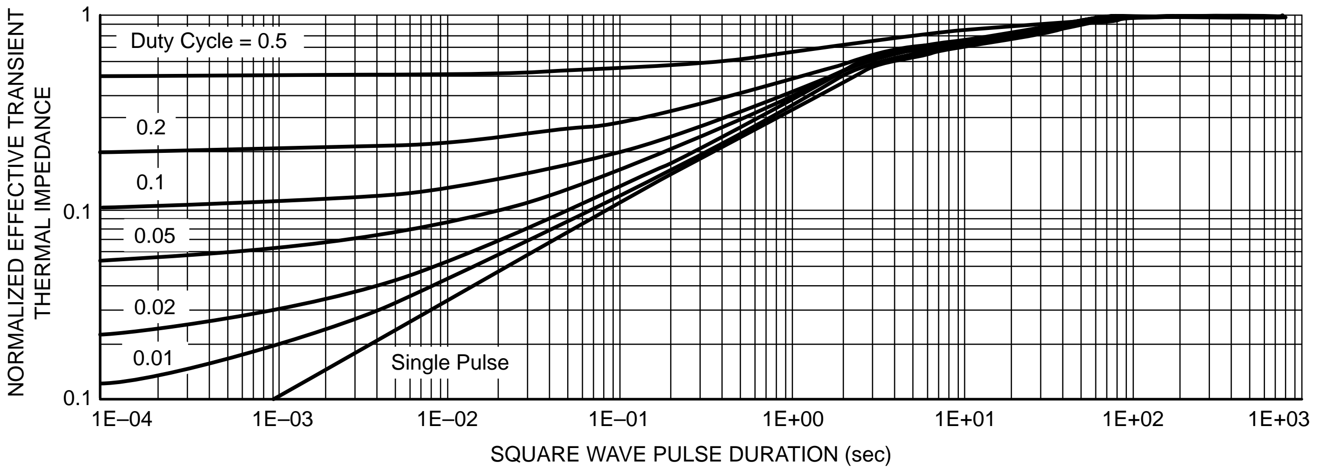


Figure 9. Normalized Thermal Transient Impedance, Junction–to–Ambient

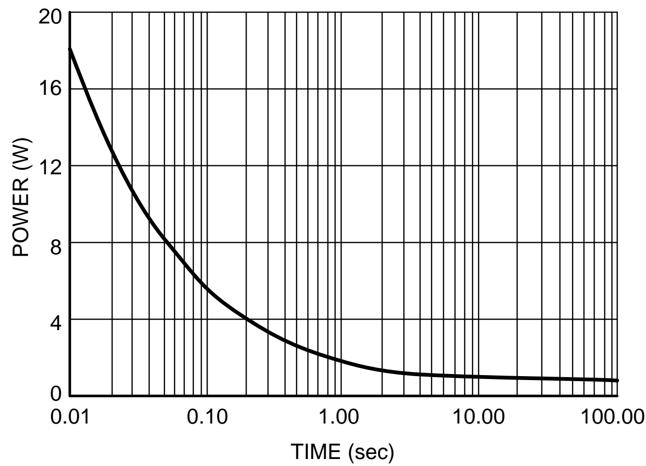


Figure 10. Single Pulse Power

# NTGS3441T1

## Power MOSFET 1 Amp, 20 Volts

### P–Channel TSOP–6

**ON Semiconductor™**

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**1 AMPERE**
**20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ**

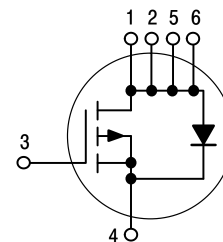
**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP–6 Surface Mount Package

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

**P–Channel**

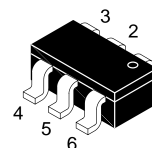



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

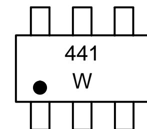
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | Volts |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Volts |
| Thermal Resistance<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>244<br>0.5<br>–1.65<br>–10 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>128<br>1.0<br>–2.35<br>–14 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>62.5<br>2.0<br>–3.3<br>–20 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes for 10 Seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10PCB, operating to steady state.
2. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), operating to steady state.
3. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), t < 5.0 seconds.

**MARKING DIAGRAM**

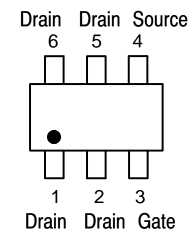



**TSOP–6**
**CASE 318G**
**STYLE 1**




441 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTGS3441T1 | TSOP–6 | 3000 Tape & Reel |

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November, 2000 – Rev. 1

Publication Order Number:
NTGS3441T1/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Notes 4. & 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –10 μA) | | $V_{(BR)DSS}$ | –20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –1.0 | μAdc |
| ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 70°C) | | | – | – | –5.0 | |
| Gate–Body Leakage Current ($V_{GS}$ = –8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –0.45 | –1.05 | –1.50 | Vdc |
| Static Drain–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –3.3 Adc) | | $R_{DS(on)}$ | – | 0.069 | 0.090 | Ω |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –2.9 Adc) | | | – | 0.117 | 0.135 | |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –3.3 Adc) | | $g_{FS}$ | – | 6.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –5.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 480 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 265 | – | pF |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 100 | – | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –20 Vdc, $I_D$ = –1.6 Adc, $V_{GS}$ = –4.5 Vdc, $R_g$ = 6.0 Ω) | $t_{d(on)}$ | – | 13 | 25 | ns |
| Rise Time | | $t_r$ | – | 23.5 | 45 | ns |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27 | 50 | ns |
| Fall Time | | $t_f$ | – | 24 | 45 | ns |
| Total Gate Charge | ($V_{DS}$ = –10 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –3.3 Adc) | $Q_{tot}$ | – | 6.2 | 14 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.3 | – | nC |
| Gate–Drain Charge | | $Q_{gd}$ | – | 2.5 | – | nC |
| **BODY–DRAIN DIODE RATINGS** | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.6 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.88 | –1.2 | Vdc |
| Diode Forward On–Voltage | ($I_S$ = –3.3 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.98 | – | Vdc |
| Reverse Recovery Time | ($I_S$ = –1.6 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 30 | 60 | ns |

4. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.
5. Handling precautions to protect against electrostatic discharge is mandatory.

## TYPICAL ELECTRICAL CHARACTERISTICS

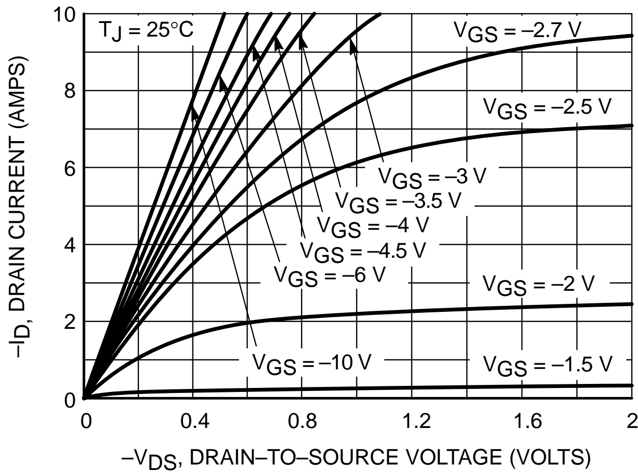



**Figure 1. On–Region Characteristics**

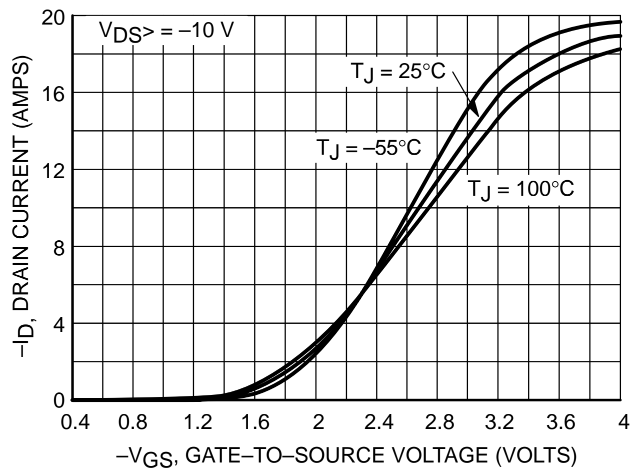



**Figure 2. Transfer Characteristics**

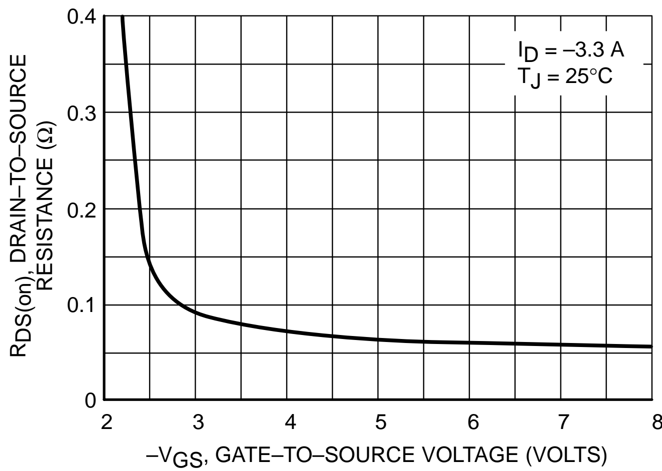



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

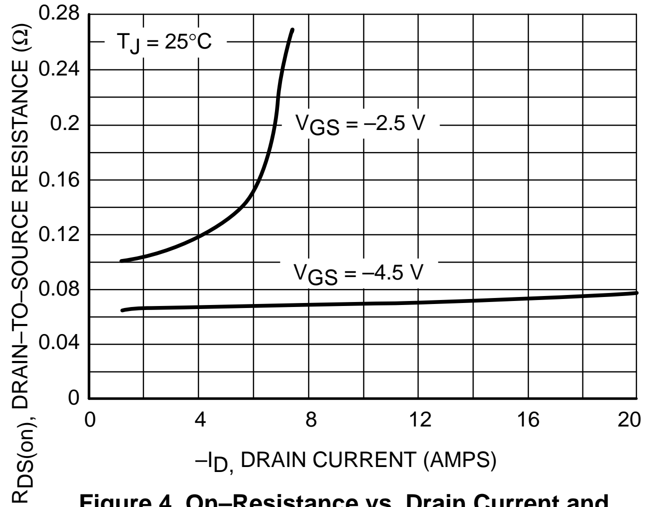



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

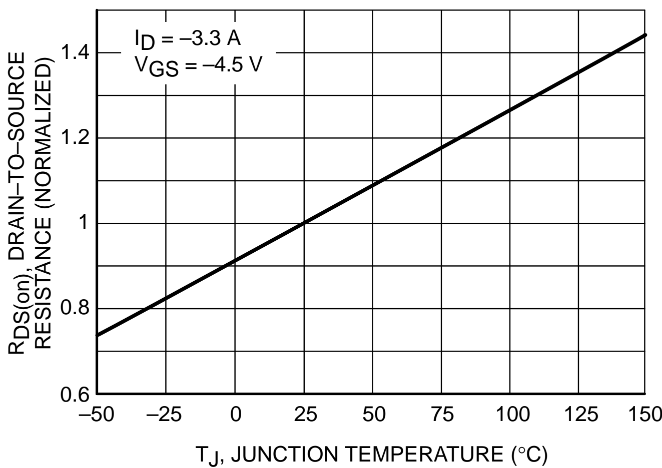



**Figure 5. On–Resistance Variation with Temperature**

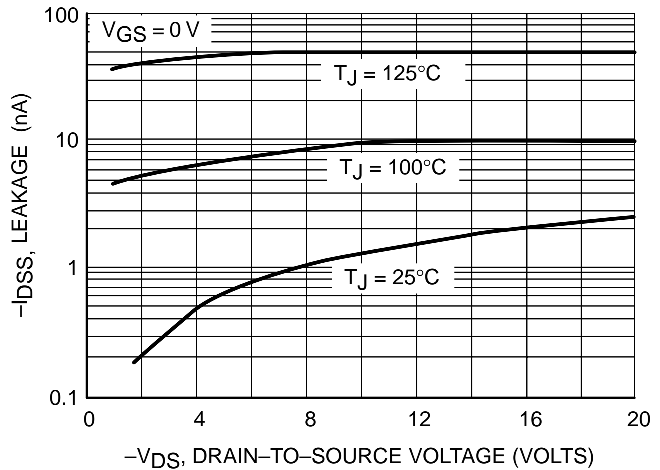



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS

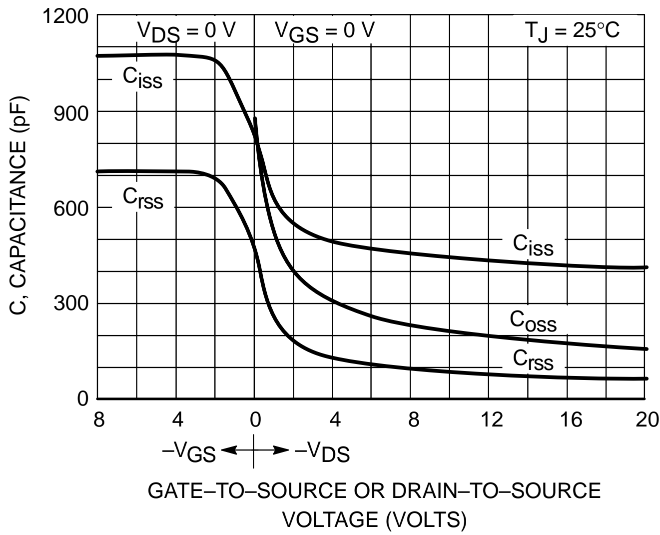



**Figure 7. Capacitance Variation**

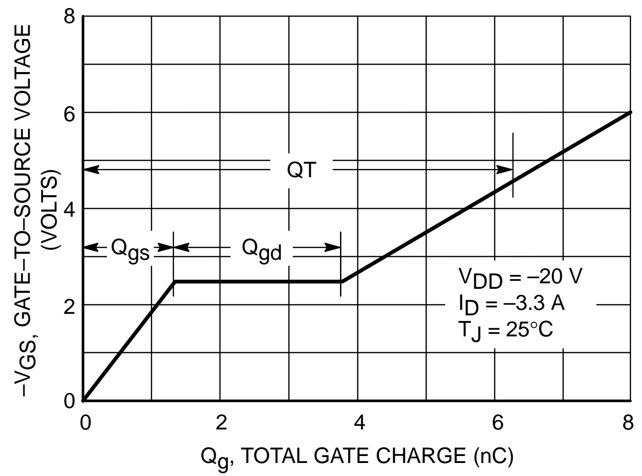



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

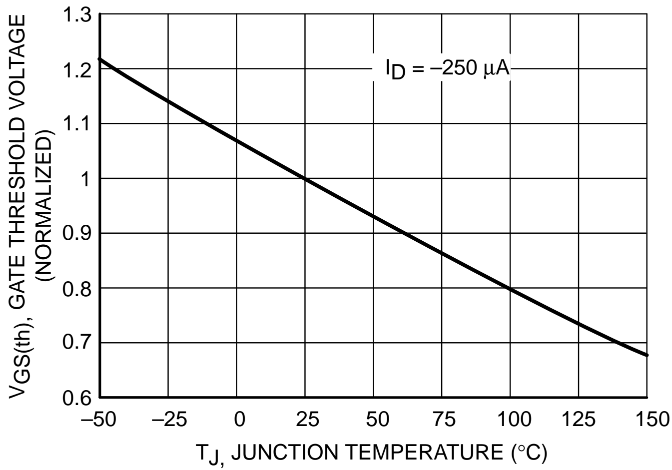



**Figure 9. Gate Threshold Voltage Variation with Temperature**

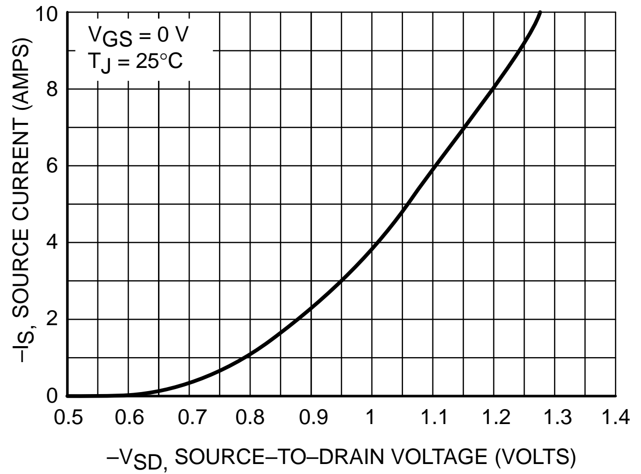



**Figure 10. Diode Forward Voltage vs. Current**

## TYPICAL ELECTRICAL CHARACTERISTICS

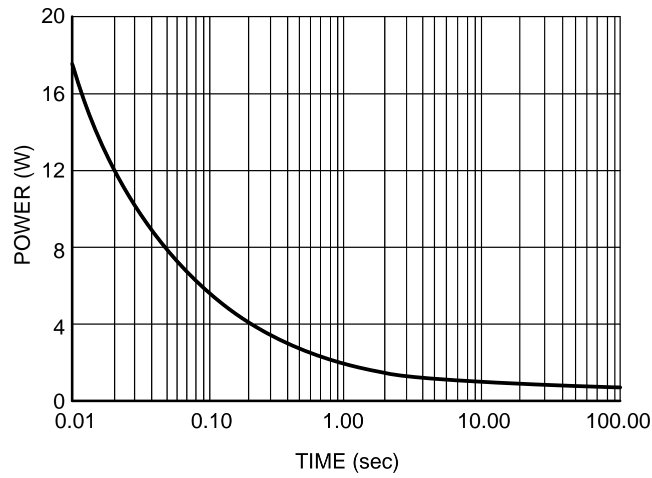



**Figure 11. Single Pulse Power**

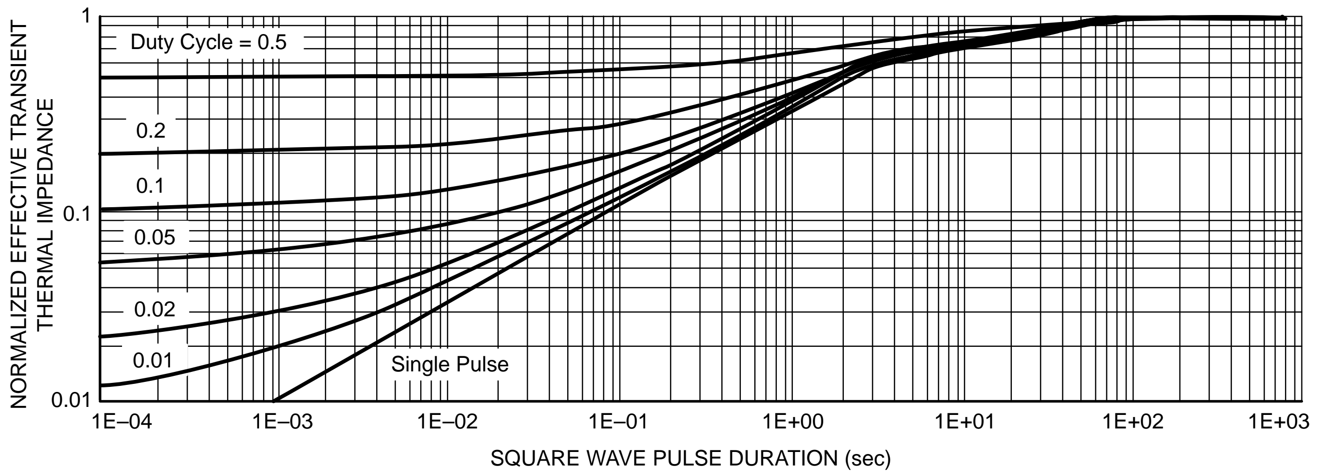
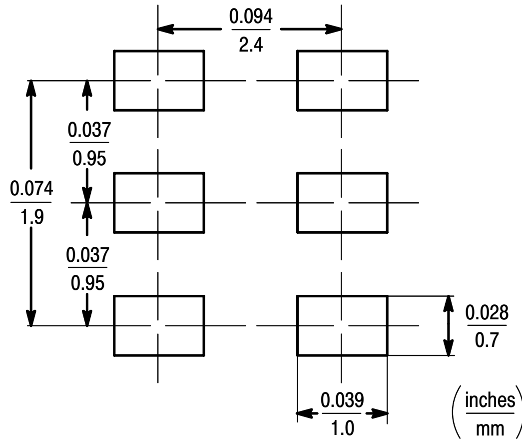



**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Ambient**

# INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# NTGS3443T1

## Power MOSFET 2 Amps, 20 Volts

### P–Channel TSOP–6

**ON Semiconductor™**

http://onsemi.com

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP6 Surface Mount Package

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

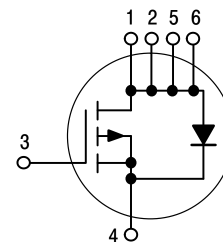
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | Volts |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Volts |
| Thermal Resistance<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>244<br>0.5<br>–2.2<br>–10 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>128<br>1.0<br>–3.1<br>–14 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current – Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 μS) | <br>$R_{\theta JA}$<br>$P_d$<br>$I_D$<br>$I_{DM}$ | <br>62.5<br>2.0<br>–4.4<br>–20 | <br>°C/W<br>Watts<br>Amps<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes for 10 Seconds | $T_L$ | 260 | °C |

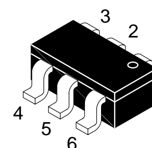
1. Minimum FR–4 or G–10PCB, operating to steady state.
2. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), operating to steady state.
3. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), t < 5.0 seconds.

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 65 mΩ**

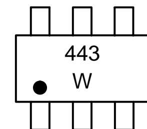
**P–Channel**




**MARKING DIAGRAM**

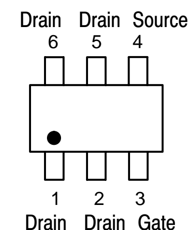



**TSOP–6**
**CASE 318G**
**STYLE 1**




443 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTGS3443T1 | TSOP–6 | 3000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Notes 4. & 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –10 μA) | | $V_{(BR)DSS}$ | –20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –1.0 | μAdc |
| ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 70°C) | | | – | – | –5.0 | |
| Gate–Body Leakage Current ($V_{GS}$ = –12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –0.60 | –0.95 | –1.50 | Vdc |
| Static Drain–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –4.4 Adc) | | $R_{DS(on)}$ | – | 0.058 | 0.065 | Ω |
| ($V_{GS}$ = –2.7 Vdc, $I_D$ = –3.7 Adc) | | | – | 0.082 | 0.090 | |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –3.5 Adc) | | | – | 0.092 | 0.100 | |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –4.4 Adc) | | $g_{FS}$ | – | 8.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –5.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 565 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 320 | – | pF |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 120 | – | pF |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –20 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –4.5 Vdc, $R_g$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | 25 | ns |
| Rise Time | | $t_r$ | – | 18 | 45 | ns |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 50 | ns |
| Fall Time | | $t_f$ | – | 31 | 50 | ns |
| Total Gate Charge | ($V_{DS}$ = –10 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –4.4 Adc) | $Q_{tot}$ | – | 7.5 | 15 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.4 | – | nC |
| Gate–Drain Charge | | $Q_{gd}$ | – | 2.9 | – | nC |
| **BODY–DRAIN DIODE RATINGS** | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.83 | –1.2 | Vdc |
| Reverse Recovery Time | ($I_S$ = –1.7 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 30 | – | ns |

4. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.
5. Handling precautions to protect against electrostatic discharge is mandatory.

## TYPICAL ELECTRICAL CHARACTERISTICS

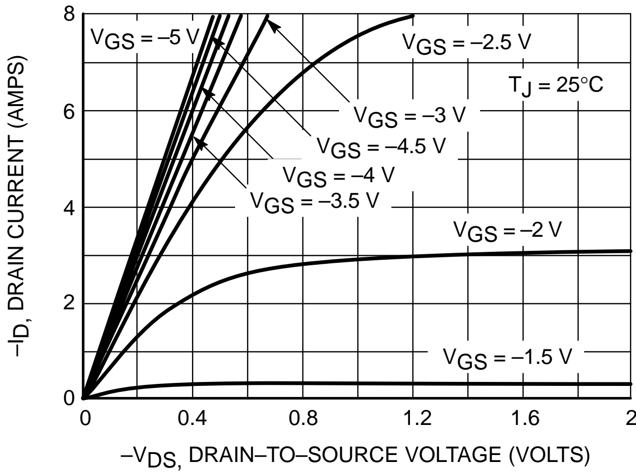



**Figure 1. On−Region Characteristics**

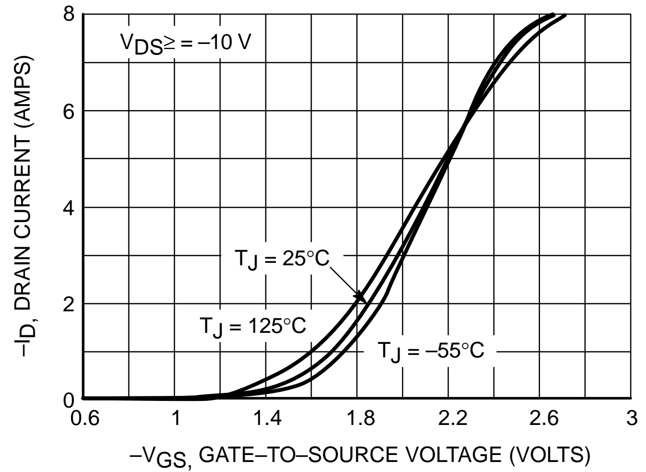



**Figure 2. Transfer Characteristics**

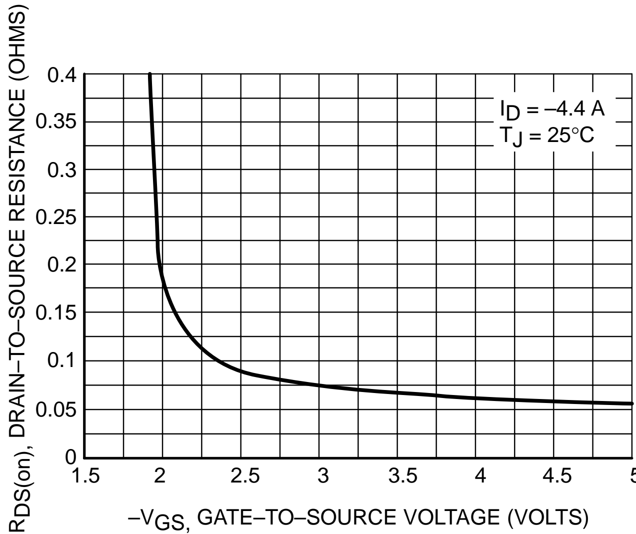



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

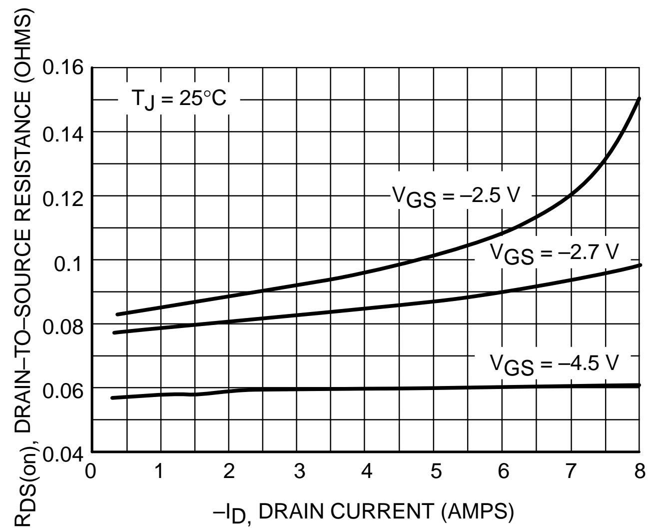



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

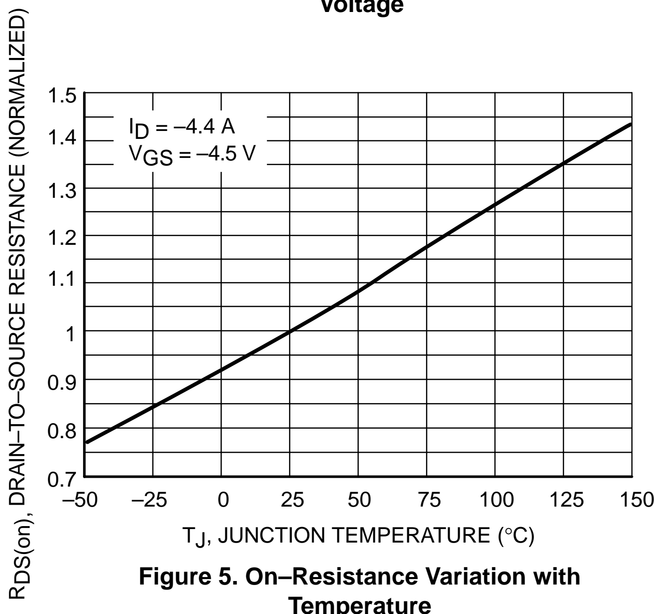



**Figure 5. On−Resistance Variation with Temperature**

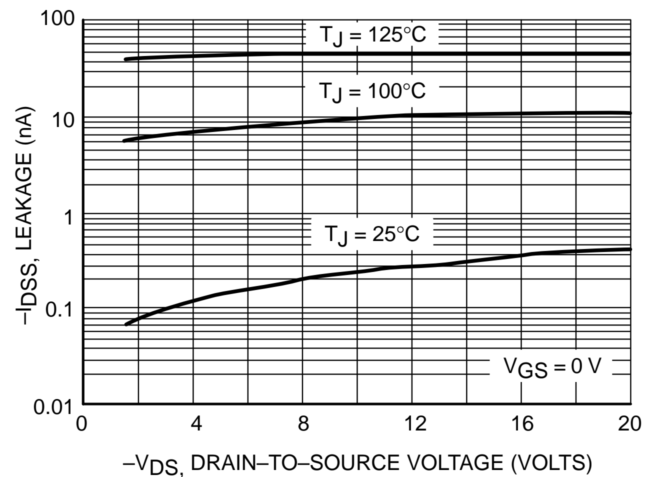



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

## TYPICAL ELECTRICAL CHARACTERISTICS

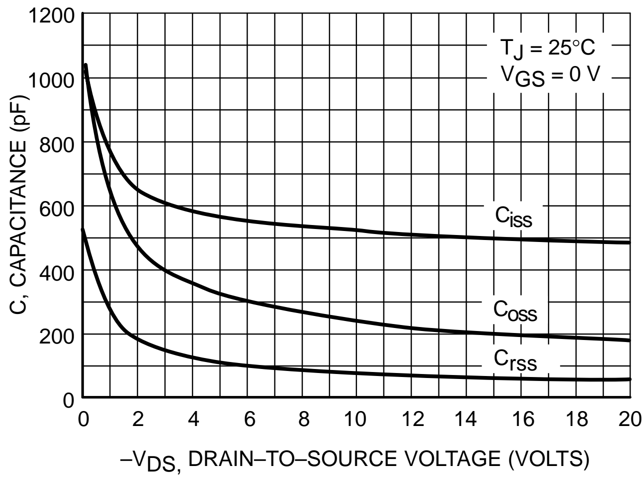



**Figure 7. Capacitance Variation**

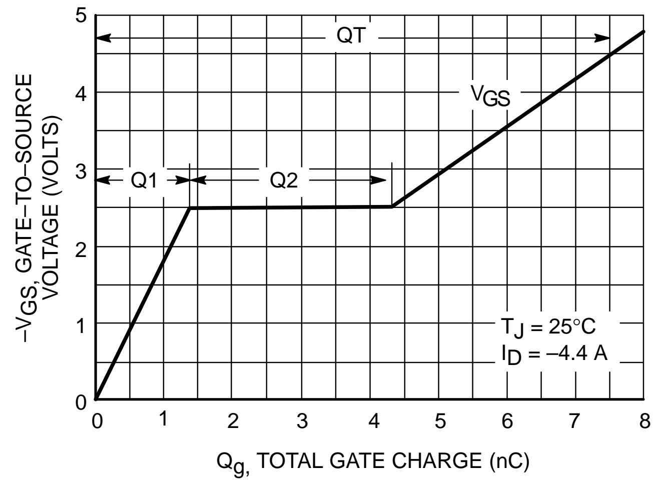



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

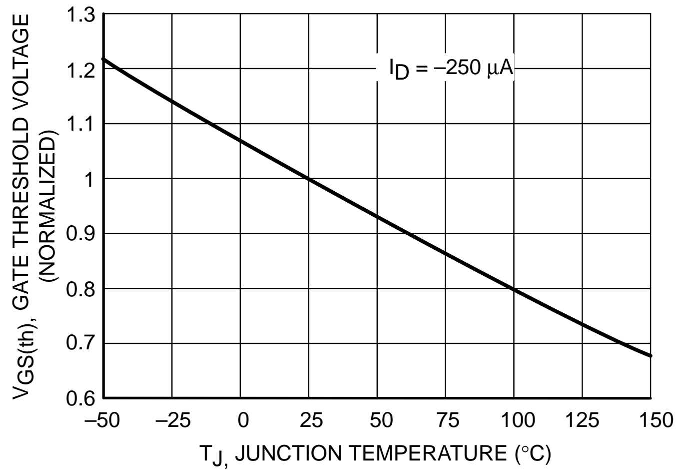



**Figure 9. Gate Threshold Voltage Variation with Temperature**

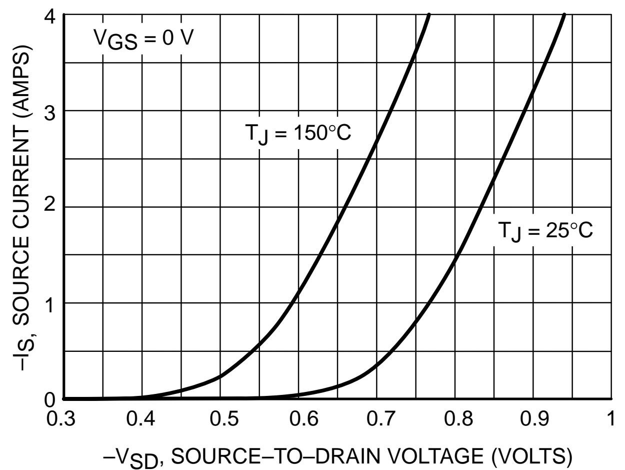



**Figure 10. Diode Forward Voltage vs. Current**

## TYPICAL ELECTRICAL CHARACTERISTICS

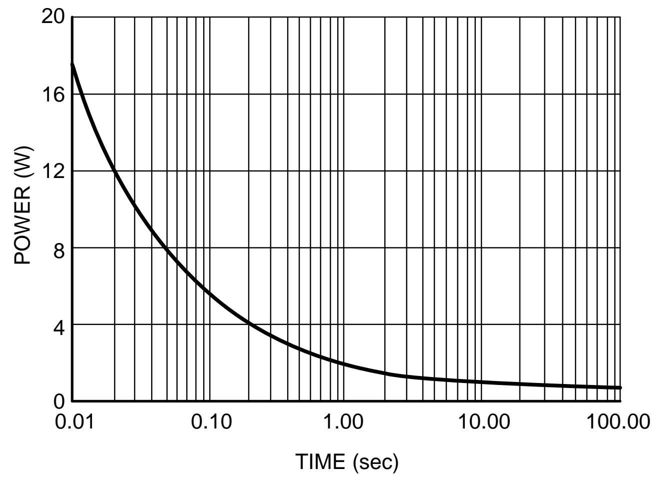



**Figure 11. Single Pulse Power**

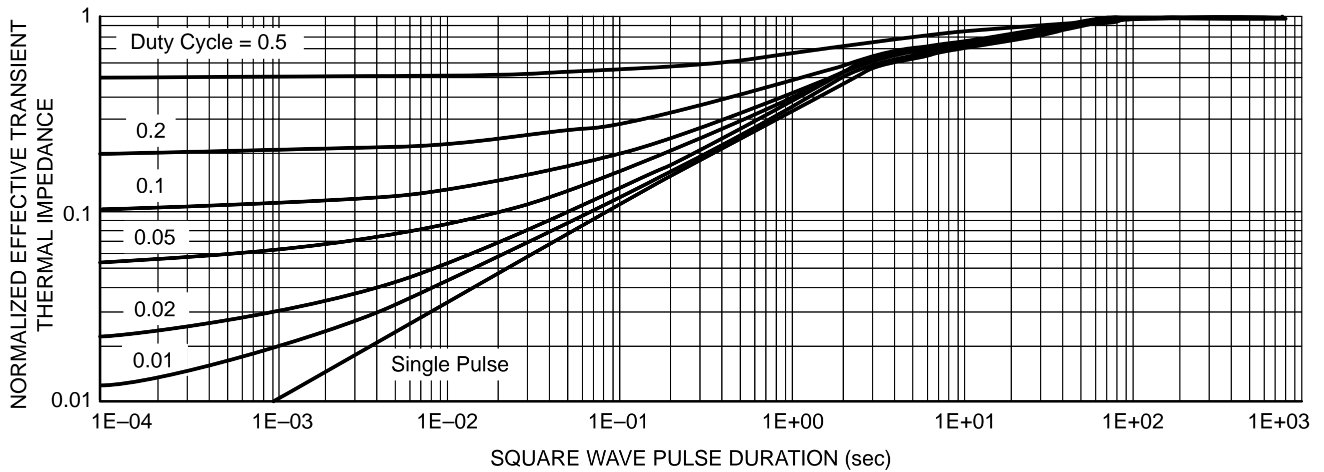
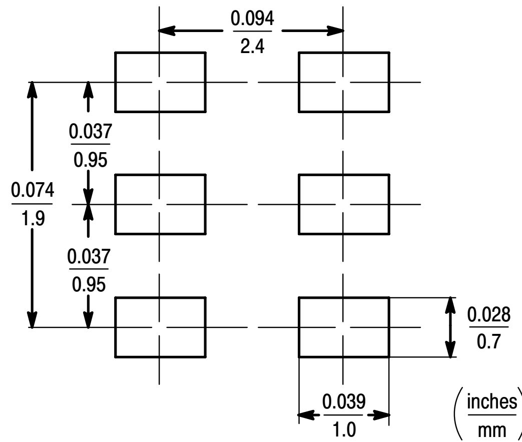



**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Ambient**

## INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# NTGS3446T1

ON Semiconductor™

http://onsemi.com

## Power MOSFET 5.3 Amps, 20 Volts

### N–Channel TSOP–6

**Features**

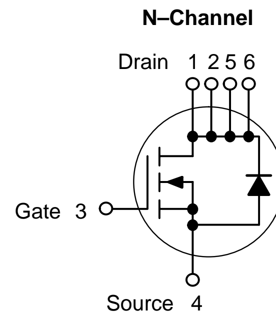
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- $I_{DSS}$ Specified at Elevated Temperature

**Applications**

- Power Management in portable and battery–powered products, i.e. computers, printers, PCMCIA cards, cellular and cordless
- Lithium Ion Battery Applications
- Notebook PC

**5.3 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 45 mΩ**

**N–Channel**

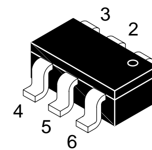



**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

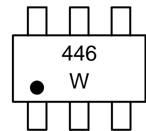
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–Source Voltage – Continuous | $V_{GS}$ | 12 | Vdc |
| Thermal Resistance<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p$ < 10 μs) | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$ | <br>62.5<br>2.0<br><br>5.3<br>25 | <br>°C/W<br>Watts<br><br>Amps<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p$ < 10 μs) | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$ | <br>128<br>1.0<br><br>3.7<br>20 | <br>°C/W<br>Watts<br><br>Amps<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), t < 5.0 seconds.
2. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), operating to steady state.

**MARKING DIAGRAM**

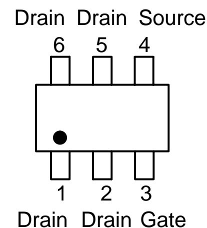



**TSOP–6**
**CASE 318G**
**STYLE 1**




446 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTGS3446T1 | TSOP–6 | 3000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 22 | – | mV/°C |
| Zero Gate Voltage Collector Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | µAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 85°C) | | | – | – | 25 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±12 Vdc, $V_{DS}$ = 0) | | $I_{GSS(f)}$ | – | – | 100 | nAdc |
| | | $I_{GSS(r)}$ | – | – | –100 | |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage $I_D$ = 0.25 mA, $V_{DS}$ = $V_{GS}$ | | $V_{GS(th)}$ | 0.6 | 0.85 | 1.2 | Vdc |
| Temperature Coefficient (Negative) | | | – | –2.5 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.3 Adc) | | $R_{DS(on)}$ | – | 36 | 45 | mΩ |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 4.4 Adc) | | | – | 44 | 55 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 5.3 Adc) | | $g_{FS}$ | – | 12 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 510 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | 350 | |
| Transfer Capacitance | | $C_{rss}$ | – | 60 | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 9.0 | 16 | ns |
| Rise Time | | $t_r$ | – | 12 | 20 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | 60 | |
| Fall Time | | $t_f$ | – | 20 | 35 | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 5.3 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 8.0 | 15 | nC |
| | | $Q_{gs}$ | – | 2.0 | – | |
| | | $Q_{gd}$ | – | 2.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 3.) | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.74 | 1.1 | Vdc |
| | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 85°C) | | – | 0.66 | – | |
| Reverse Recovery Time | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 20 | – | ns |
| | | $t_a$ | – | 11 | – | |
| | | $t_b$ | – | 9.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.01 | – | µC |

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

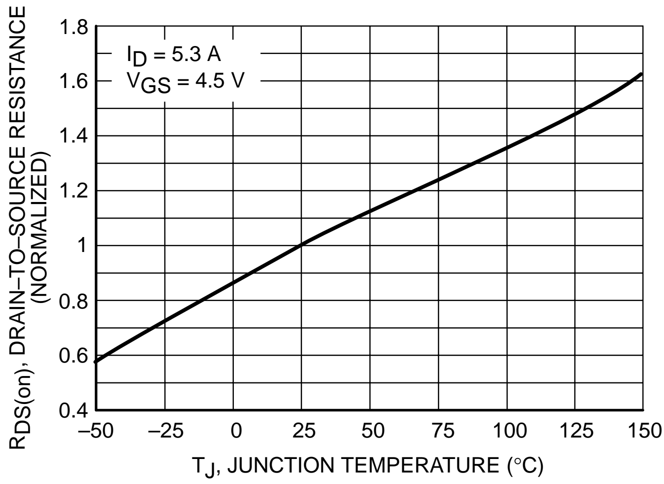


**Figure 1. On–Resistance Variation with Temperature**

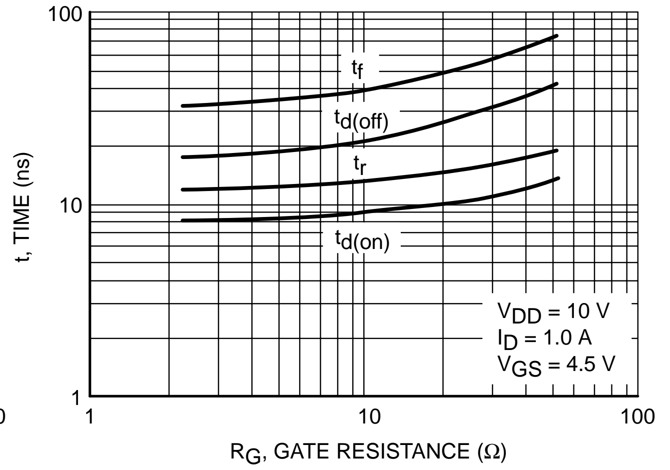


**Figure 2. Resistive Switching Time Variation vs. Gate Resistance**

# NTGS3455T1

*Product Preview*

## MOSFET -3.5 Amps, -30 Volts

### P–Channel TSOP–6

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature TSOP–6 Surface Mount Package

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones, and PCMCIA Cards

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –30 | Volts |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20.0 | Volts |
| Thermal Resistance<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 µS)<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$<br>$P_d$<br>$I_D$ | <br>62.5<br>2.0<br>–3.5<br><br>–20<br>1.0<br>–2.5 | <br>°C/W<br>Watts<br>Amps<br><br>Amps<br>Watts<br>Amps |
| Thermal Resistance<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($T_p$ < 10 µS)<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current | <br>$R_{\theta JA}$<br>$P_d$<br><br>$I_D$<br>$I_{DM}$<br>$P_d$<br>$I_D$ | <br>128<br>1.0<br><br>–2.5<br>–14<br>0.5<br>–1.75 | <br>°C/W<br>Watts<br><br>Amps<br>Amps<br>Watts<br>Amps |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes for 10 Seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), t < 5.0 seconds.
2. Mounted onto a 2″ square FR–4 board (1″ sq. 2 oz. cu. 0.06″ thick single sided), operating to steady state.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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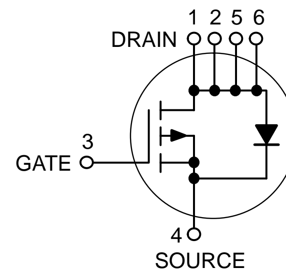
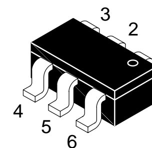
**–3.5 AMPERES**
**–30 VOLTS**
**100 mΩ @ $V_{GS}$ = –10 V**

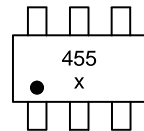
**P–Channel**




**MARKING DIAGRAM**

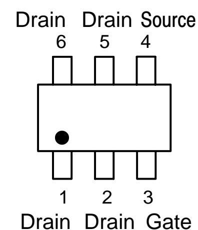



**TSOP–6**
**CASE 318G**
**STYLE 1**




455 = Device Code
x = Date Code

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTGS3455T1 | TSOP–6 | 3000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Notes 3. & 4.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –10 μA) | | $V_{(BR)DSS}$ | –30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –30 Vdc, $T_J$ = 25°C) ($V_{GS}$ = 0 Vdc, $V_{DS}$ = –30 Vdc, $T_J$ = 70°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–5.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –20.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +20.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –1.0 | –1.87 | –3.0 | Vdc |
| Static Drain–Source On–State Resistance ($V_{GS}$ = –10 Vdc, $I_D$ = –3.5 Adc) ($V_{GS}$ = –4.5 Vdc, $I_D$ = –2.7 Adc) | | $R_{DS(on)}$ | –<br>– | 0.094<br>0.144 | 0.100<br>0.170 | Ω |
| Forward Transconductance ($V_{DS}$ = –15 Vdc, $I_D$ = –3.5 Adc) | | $g_{FS}$ | – | 6.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Total Gate Charge | ($V_{DS}$ = –15 Vdc, $V_{GS}$ = –10 Vdc, $I_D$ = –3.5 Adc) | $Q_{tot}$ | – | 9.0 | 13 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 2.0 | – | |
| Input Capacitance | ($V_{DS}$ = –5.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 480 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 220 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 60 | – | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –20 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –10 Vdc, $R_g$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 15 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 20 | 35 | |
| Fall Time | | $t_f$ | – | 10 | 20 | |
| Reverse Recovery Time | ($I_S$ = –1.7 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 30 | – | ns |
| **BODY–DRAIN DIODE RATINGS** | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –0.90 | –1.2 | Vdc |
| Diode Forward On–Voltage | ($I_S$ = –3.5 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | –1.0 | – | Vdc |

3. Indicates Pulse Test: P.W. = 300 μsec max, Duty Cycle = 2%.
4. Class 1 ESD rated – Handling precautions to protect against electrostatic discharge is mandatory.

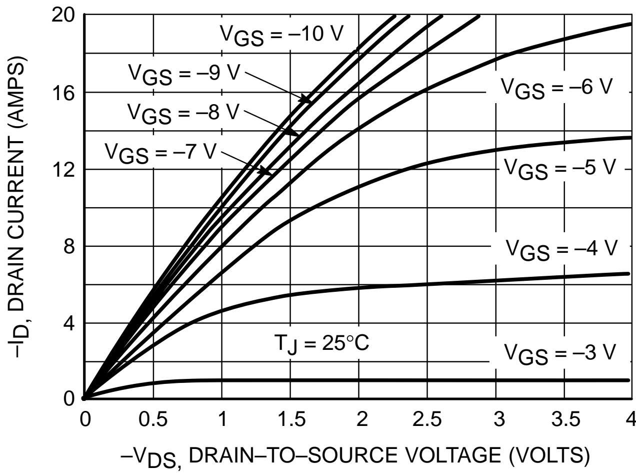


**Figure 1. On–Region Characteristics**

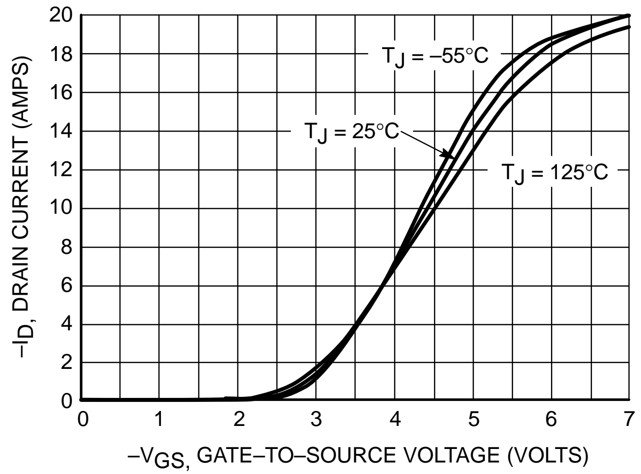


**Figure 2. Transfer Characteristics**

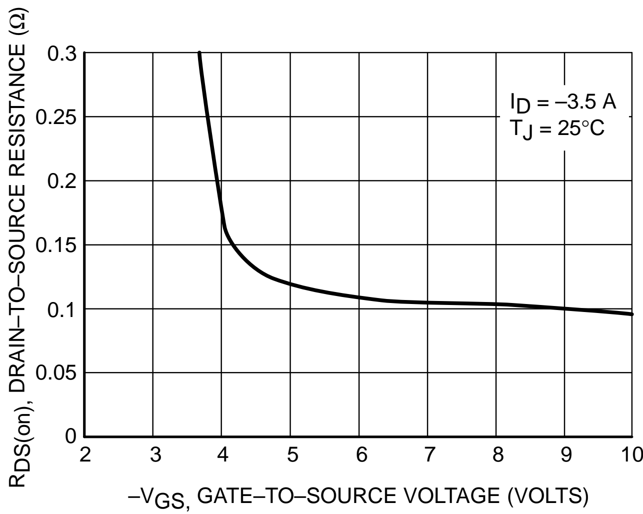


**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

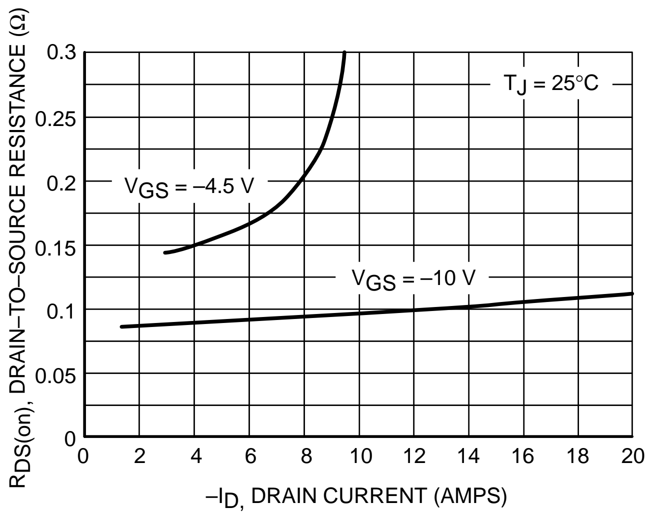


**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

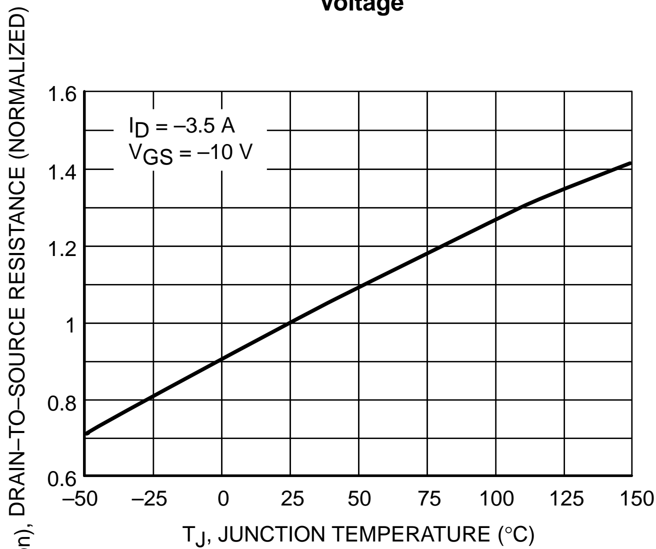


**Figure 5. On–Resistance Variation with Temperature**

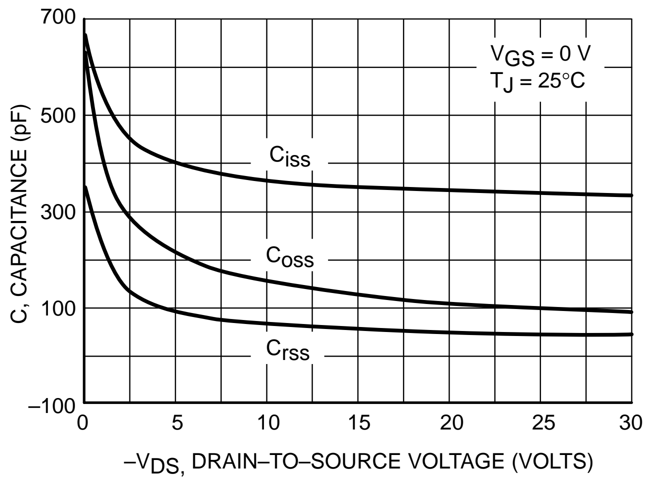


**Figure 6. Capacitance Variation**

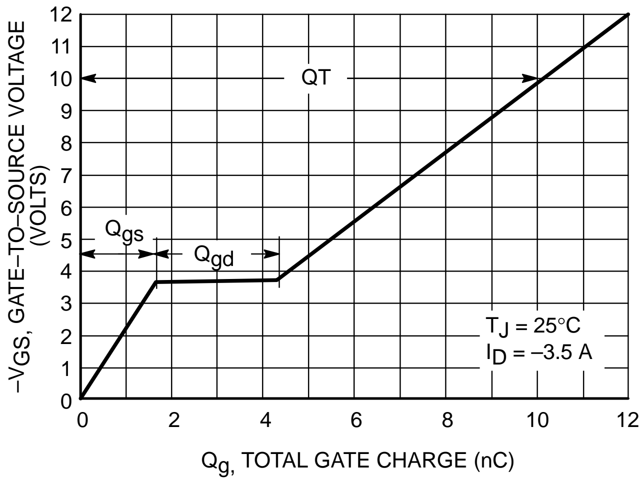


**Figure 7. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

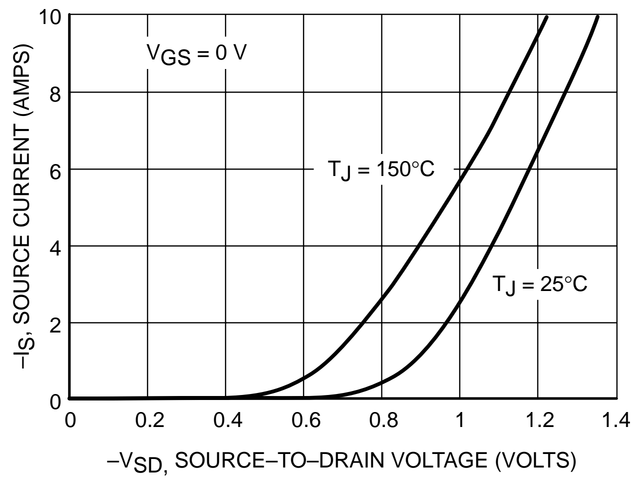


**Figure 8. Diode Forward Voltage vs. Current**

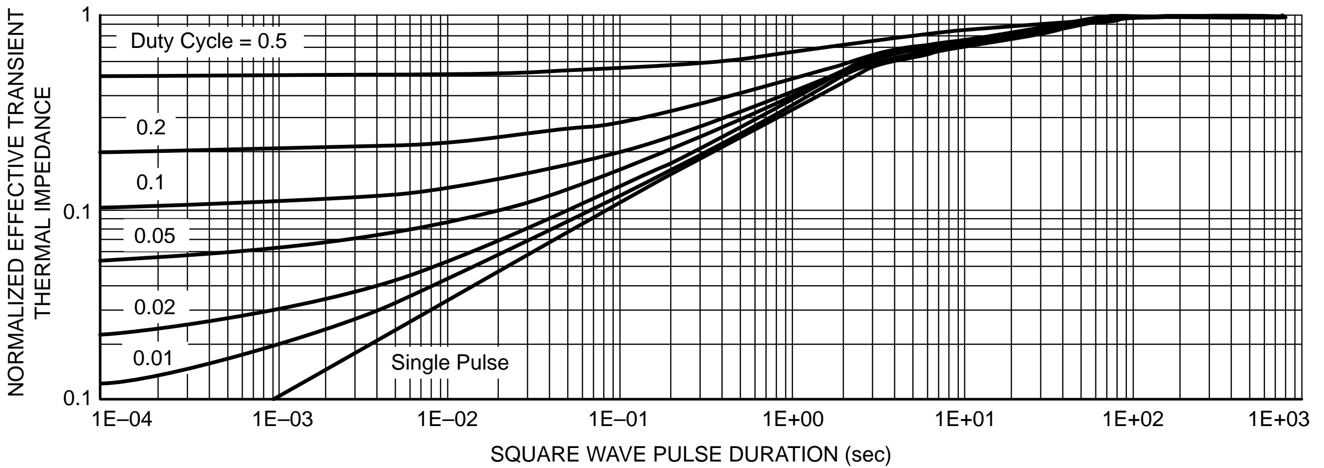


**Figure 9. Normalized Thermal Transient Impedance, Junction–to–Ambient**

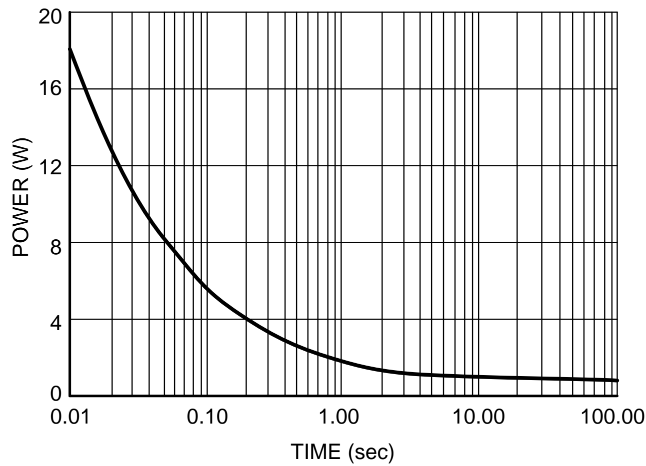


**Figure 10. Single Pulse Power**

# NTHD5902T1

*Product Preview*

## Dual N-Channel 30 V (D-S) MOSFET

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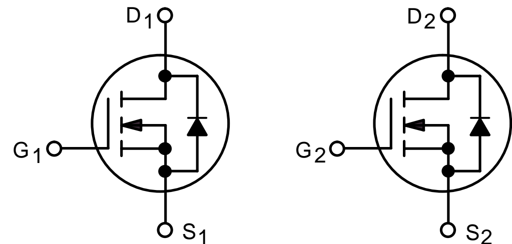
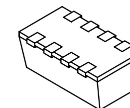
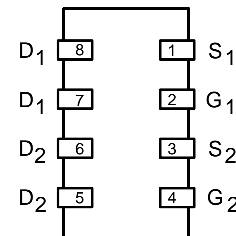



**N–Channel MOSFET** **N–Channel MOSFET**

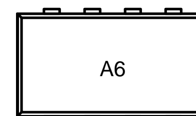


**ChipFET**
**CASE 1206A**
**STYLE 2**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A6 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| 30 | 0.085 @ $V_{GS}$ = 10 V | ±3.9 |
| | 0.143 @ $V_{GS}$ = 4.5 V | ±3.0 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 30 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±20 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.) $T_A$ = 25°C / $T_A$ = 85°C | $I_D$ | ±3.9 / ±2.8 | ±2.9 / ±2.1 | A |
| Pulsed Drain Current | $I_{DM}$ | ±10 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | 1.8 | 0.9 | A |
| Maximum Power Dissipation (Note 1.) $T_A$ = 25°C / $T_A$ = 85°C | $P_D$ | 2.1 / 1.1 | 1.1 / 0.6 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHD5902T1 | ChipFET | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.) | $R_{thJA}$ | | | °C/W |
| t ≤ 5 sec | | 50 | 60 | |
| Steady State | | 90 | 110 | |
| Maximum Junction–to–Foot<br>Steady State | $R_{thJF}$ | 30 | 40 | °C/W |

### ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 μA | 1.0 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1.0 | μA |
| | | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | 5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≥ 5.0 V, $V_{GS}$ = 10 V | 10 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 2.9 A | – | 0.072 | 0.085 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 2.2 A | – | 0.120 | 0.143 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = 15 V, $I_D$ = 2.9 A | – | 20 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = 0.9 A, $V_{GS}$ = 0 V | – | 0.8 | 1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_D$ = 2.9 A | – | 5.0 | 7.5 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 0.8 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 1.0 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $R_L$ = 15 Ω, $I_D$ ≅ 1.0 A, $V_{GEN}$ = 10 V, $R_G$ = 6 Ω | – | 7.0 | 11 | ns |
| Rise Time | $t_r$ | | – | 12 | 18 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 12 | 18 | |
| Fall Time | $t_f$ | | – | 7.0 | 11 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 0.9 A, di/dt = 100 A/μs | – | 40 | 80 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

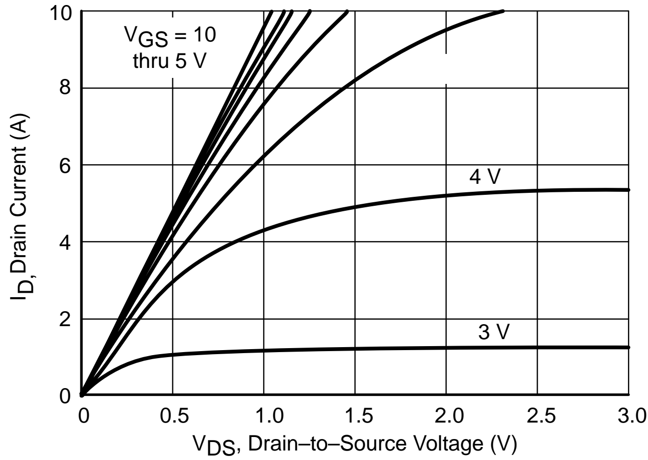


**Figure 1. Output Characteristics**

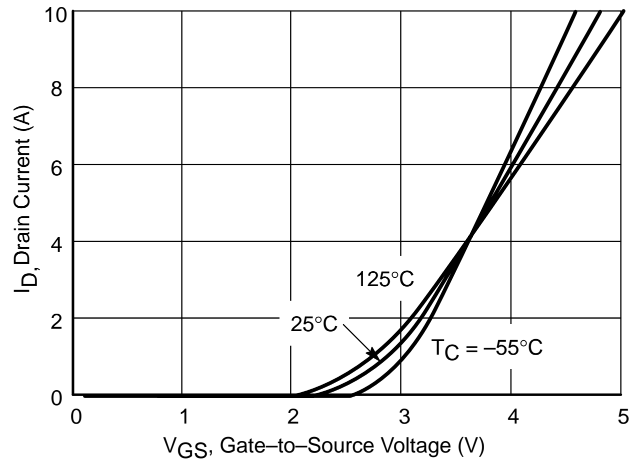


**Figure 2. Transfer Characteristics**

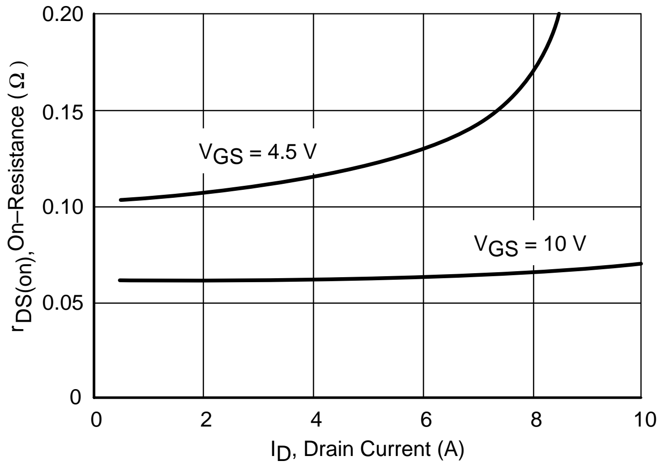


**Figure 3. On–Resistance vs. Drain Current**

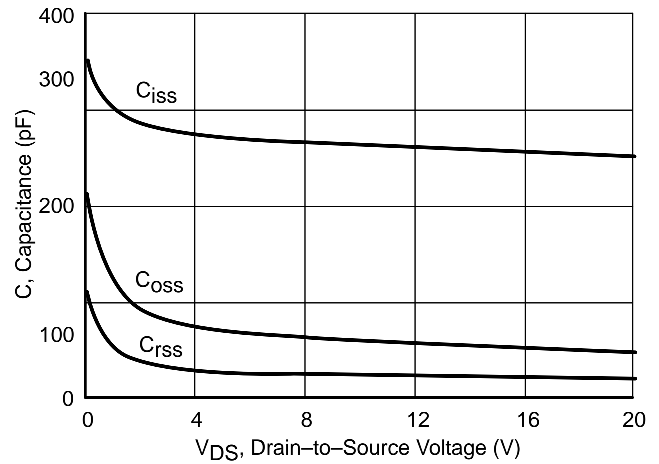


**Figure 4. Capacitance**

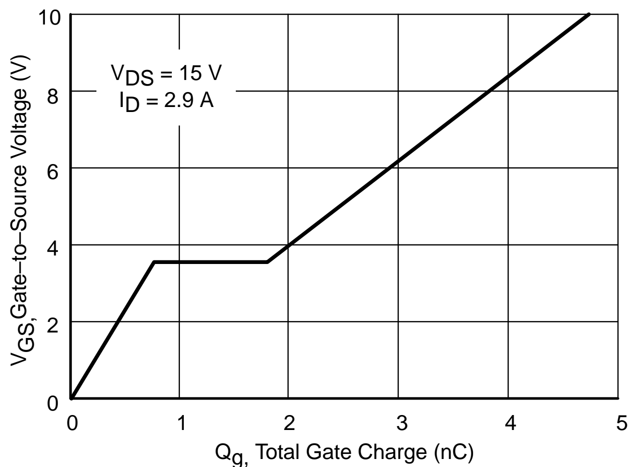


**Figure 5. Gate Charge**

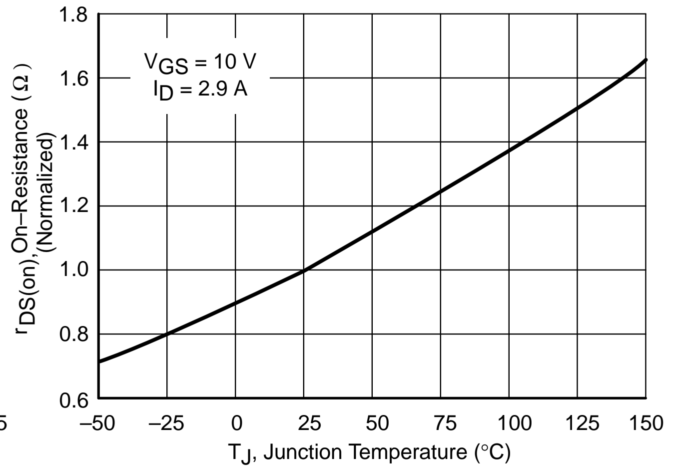


**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

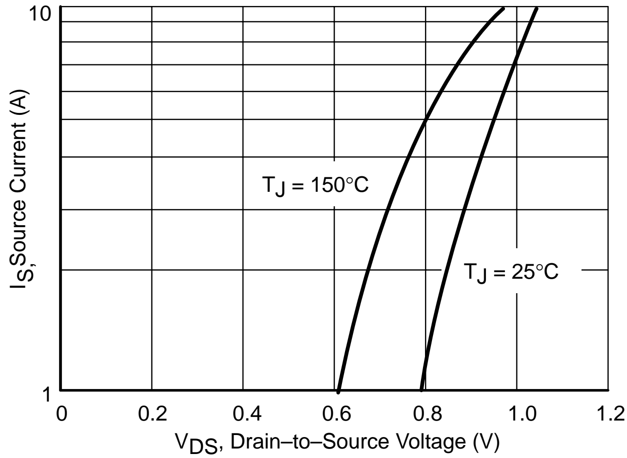


**Figure 7. Source–Drain Diode Forward Voltage**

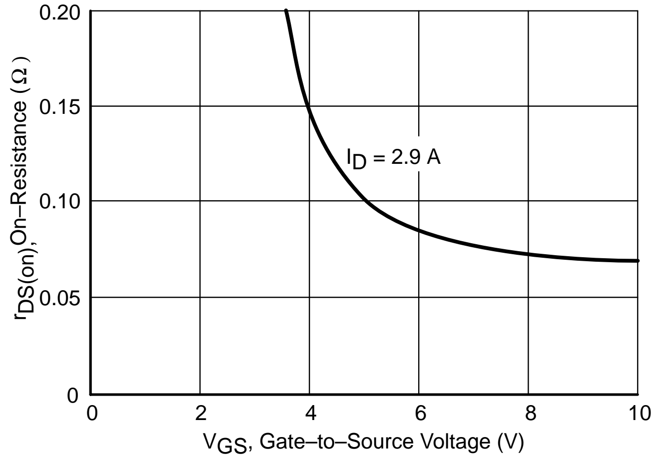


**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

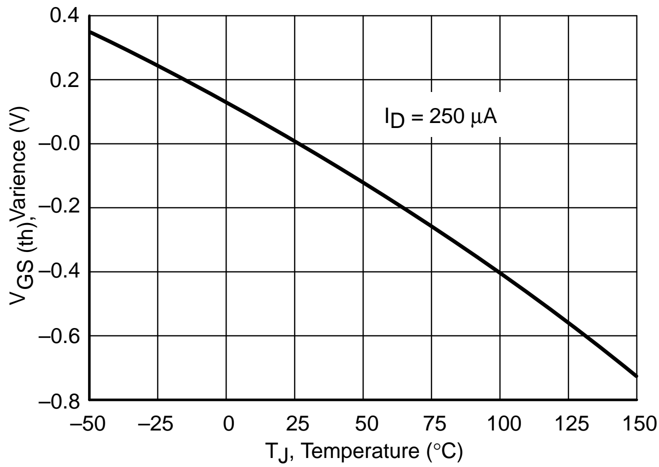


**Figure 9. Threshold Voltage**

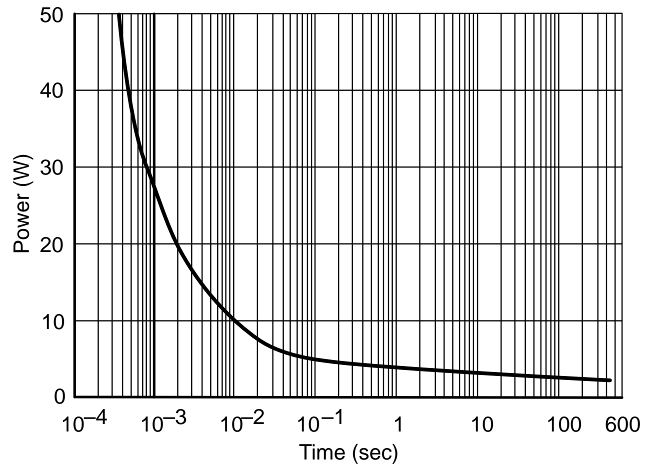


**Figure 10. Single Pulse Power**

## TYPICAL ELECTRICAL CHARACTERISTICS

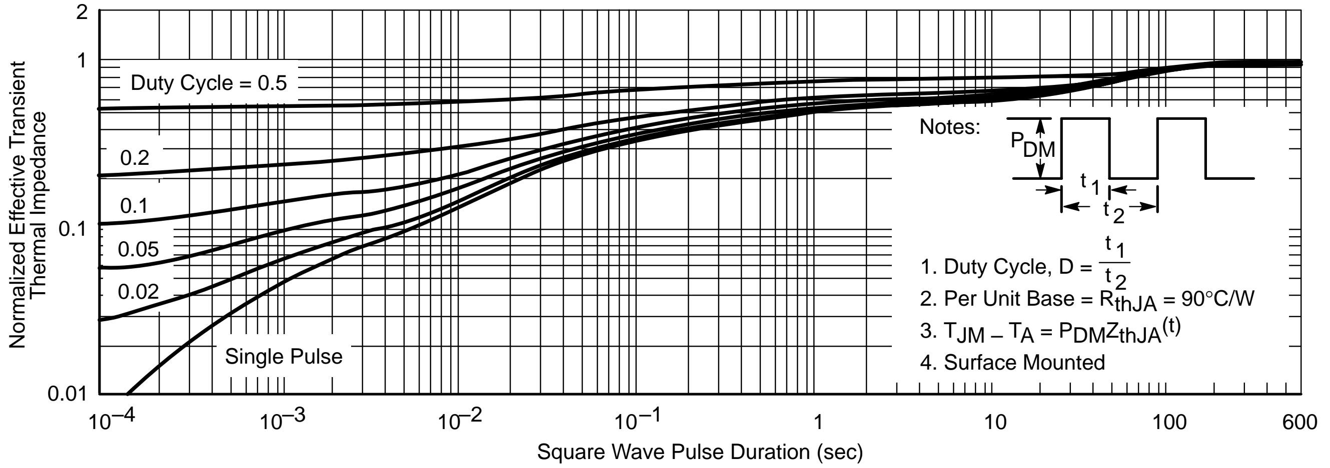


**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

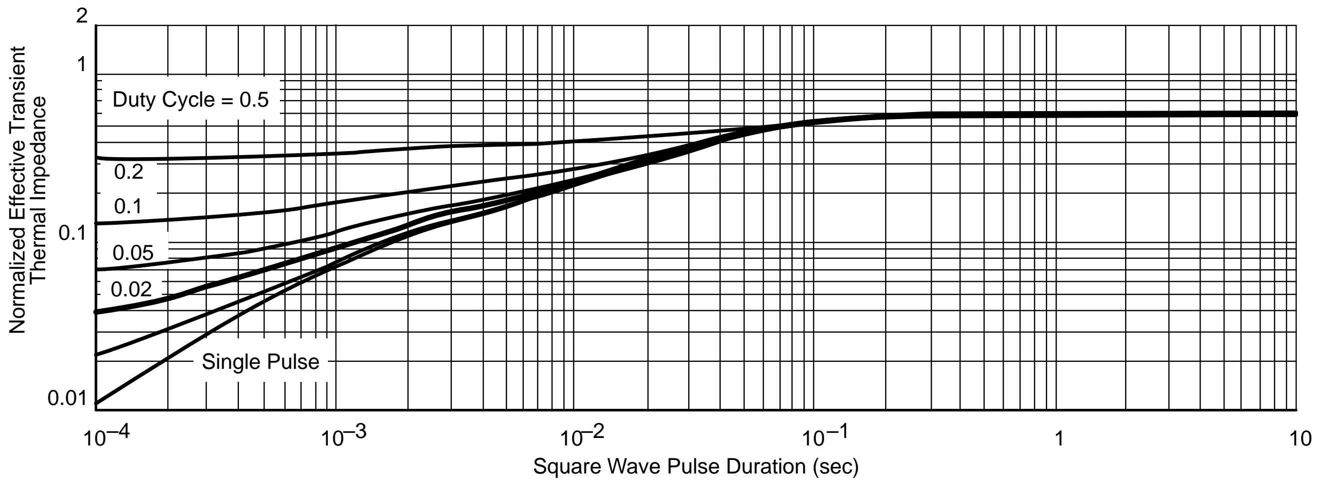


**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

# NTHD5903T1

*Product Preview*

# Dual P-Channel 2.5 V (G-S) MOSFET

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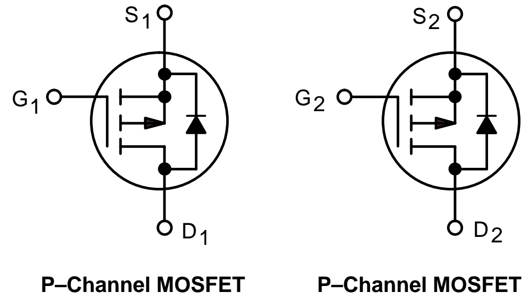
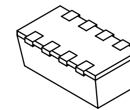
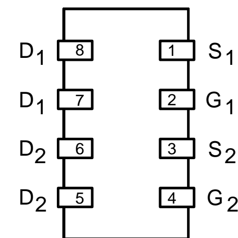



**P–Channel MOSFET** **P–Channel MOSFET**

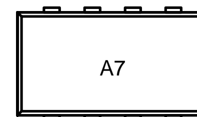


**ChipFET**
**CASE 1206A**
**STYLE 2**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A7 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –20 | 0.155 @ $V_{GS}$ = –4.5 V | ± 2.9 |
| | 0.180 @ $V_{GS}$ = –3.6 V | ± 2.7 |
| | 0.260 @ $V_{GS}$ = –2.5 V | ± 2.2 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ± 12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.) | $I_D$ | | | A |
| $T_A$ = 25°C | | ± 2.9 | ± 2.1 | |
| $T_A$ = 85°C | | ± 2.1 | ± 1.5 | |
| Pulsed Drain Current | $I_{DM}$ | ± 10 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | –1.8 | –0.9 | A |
| Maximum Power Dissipation (Note 1.) | $P_D$ | | | W |
| $T_A$ = 25°C | | 2.1 | 1.1 | |
| $T_A$ = 85°C | | 1.1 | 0.6 | |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHD5903T1 | ChipFET | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.) | $R_{thJA}$ | | | °C/W |
| $t \leq 5$ sec | | 50 | 60 | |
| Steady State | | 90 | 110 | |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 30 | 40 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = –250 μA | –0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 12 V | – | – | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | – | – | –1.0 | μA |
| | | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | –5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS} \leq$ –5.0 V, $V_{GS}$ = –4.5 V | –10 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = –4.5 V, $I_D$ = –2.1 A | – | 0.130 | 0.155 | Ω |
| | | $V_{GS}$ = –3.6 V, $I_D$ = –2.0 A | – | 0.150 | 0.180 | |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –1.7 A | – | 0.215 | 0.260 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = –10 V, $I_D$ = –2.1 A | – | 5.0 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = –0.9 A, $V_{GS}$ = 0 V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –2.1 A | – | 3.0 | 6.0 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 0.9 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 0.6 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –10 V, $R_L$ = 10 Ω, $I_D \cong$ –1.0 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | – | 13 | 20 | ns |
| Rise Time | $t_r$ | | – | 35 | 55 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 25 | 40 | |
| Fall Time | $t_f$ | | – | 25 | 40 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –0.9 A, di/dt = 100 A/μs | – | 40 | 80 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

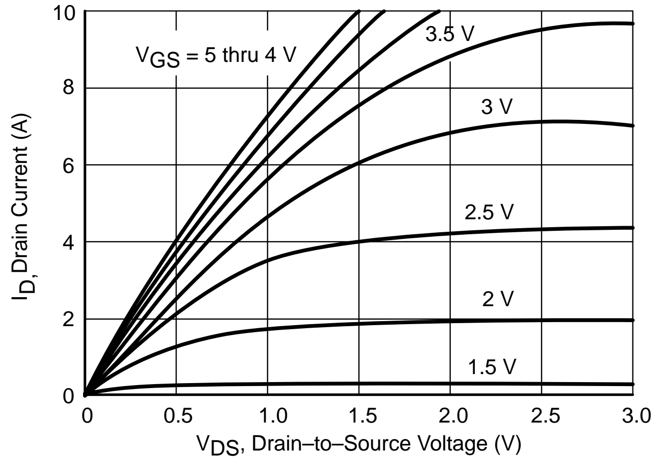


**Figure 1. Output Characteristics**

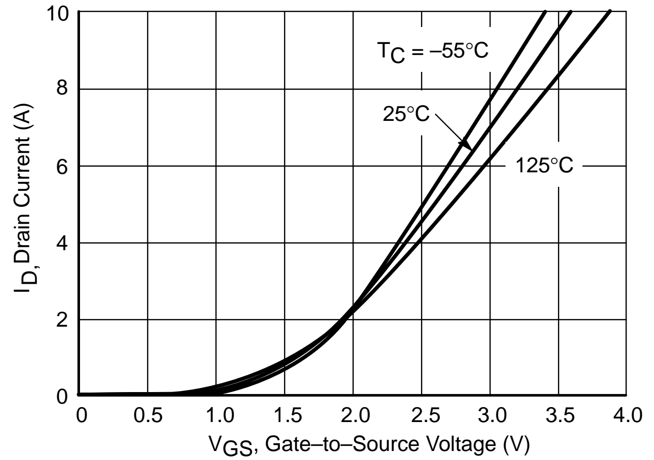


**Figure 2. Transfer Characteristics**

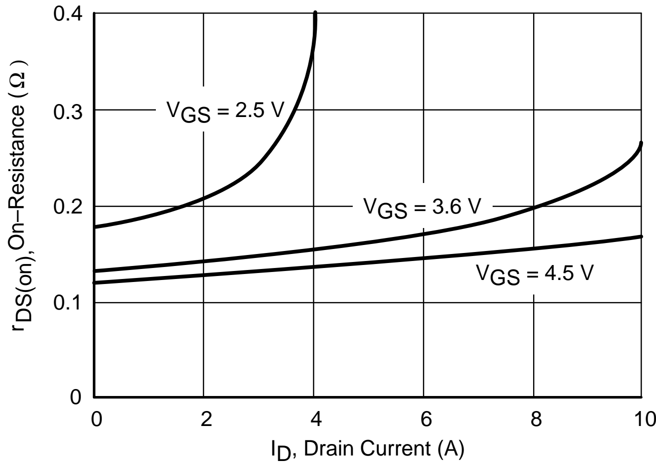


**Figure 3. On–Resistance vs. Drain Current**

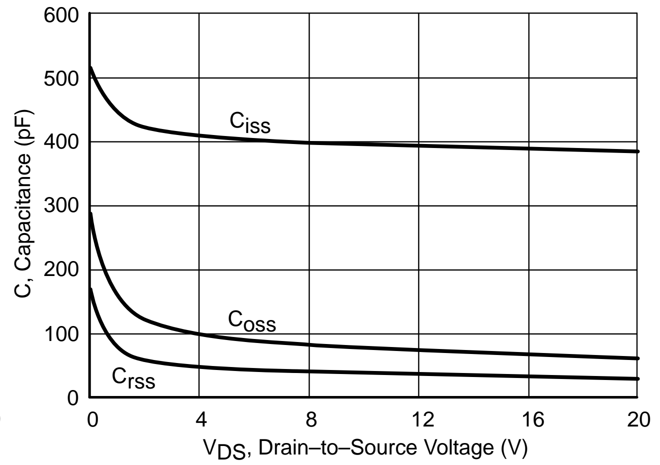


**Figure 4. Capacitance**

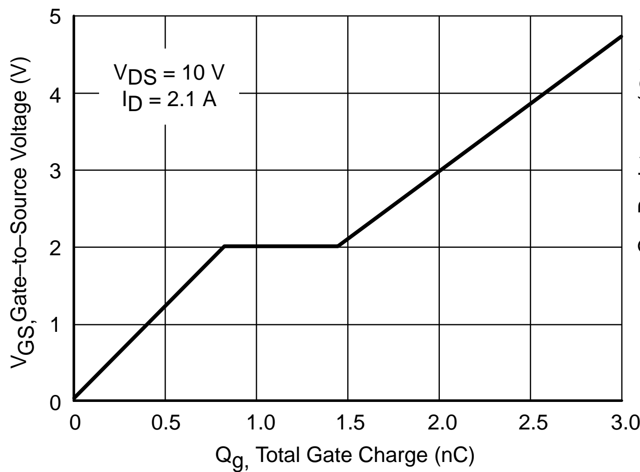


**Figure 5. Gate Charge**

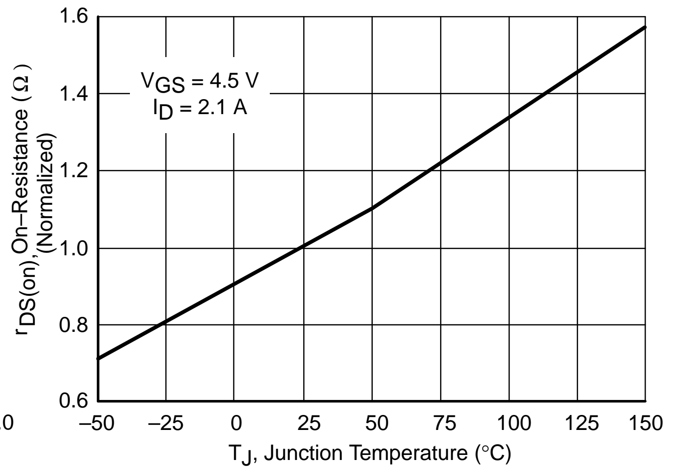


**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

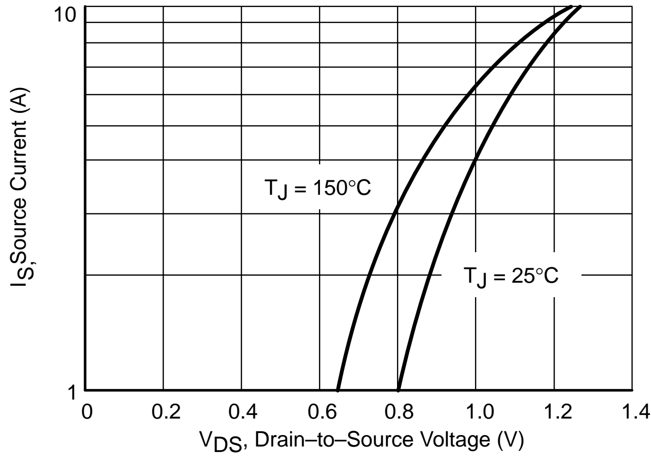


**Figure 7. Source–Drain Diode Forward Voltage**

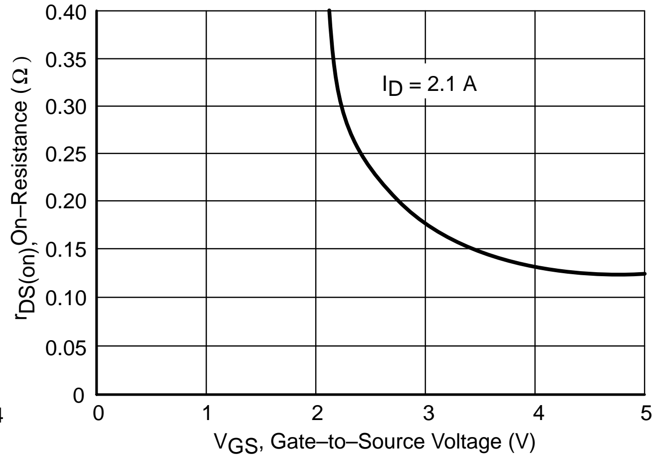


**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

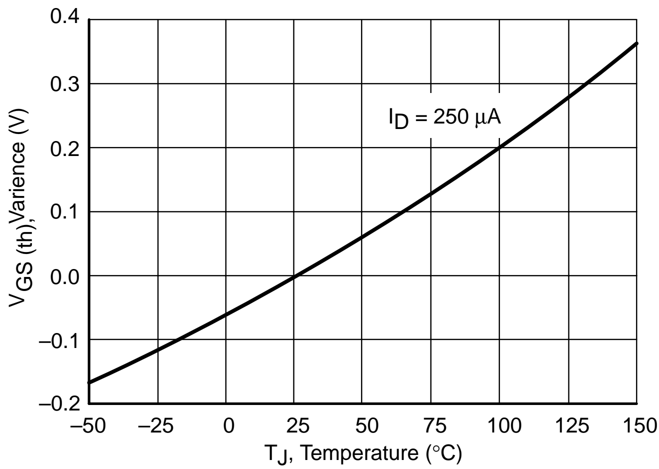


**Figure 9. Threshold Voltage**

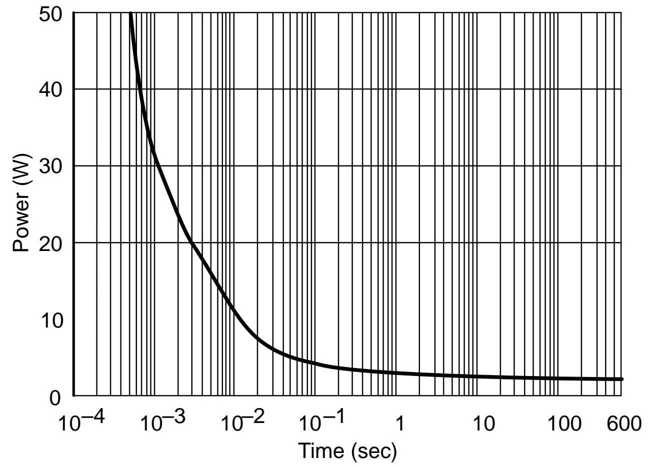


**Figure 10. Single Pulse Power**

## TYPICAL ELECTRICAL CHARACTERISTICS

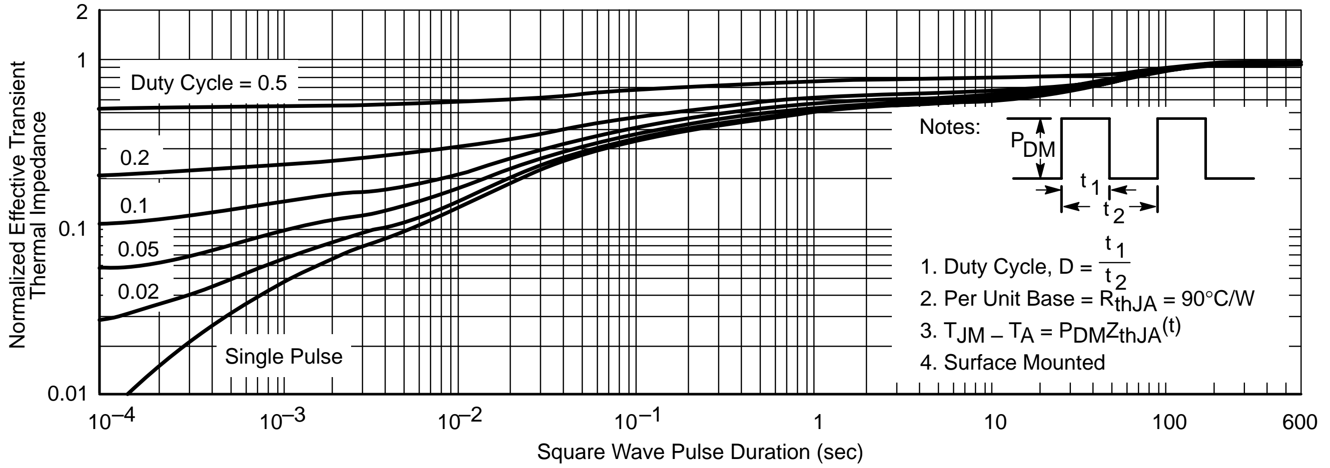


**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

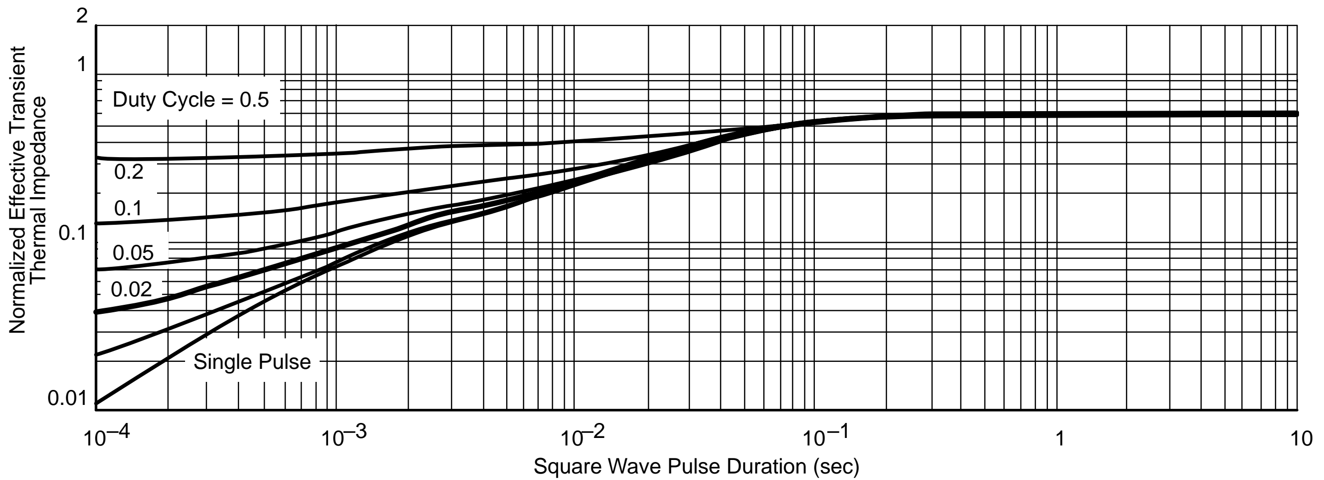


**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

# NTHD5904T1

*Product Preview*

## Dual N-Channel 2.5 V (G-S) MOSFET

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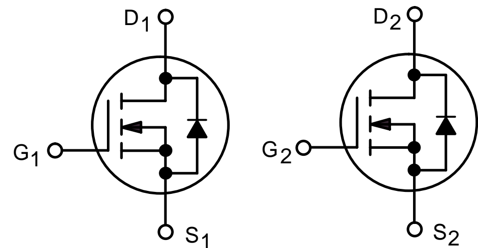
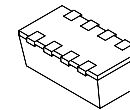
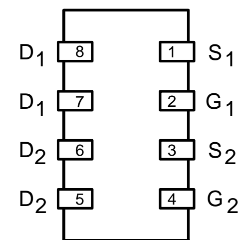



N–Channel MOSFET N–Channel MOSFET

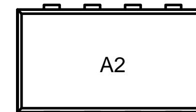


ChipFET
CASE 1206A
STYLE 2

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A2 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| 20 | 0.075 @ $V_{GS}$ = 4.5 V | ±4.2 |
| | 0.134 @ $V_{GS}$ = 2.5 V | ±3.1 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±4.2<br>±3.0 | <br>±3.1<br>±2.2 | A |
| Pulsed Drain Current | $I_{DM}$ | ±10 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | 1.8 | 0.9 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.1<br>1.1 | <br>1.1<br>0.6 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHD5904T1 | ChipFET | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.)<br>$t \leq 5$ sec<br>Steady State | $R_{thJA}$ | <br>50<br>90 | <br>60<br>110 | °C/W |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 30 | 40 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 μA | 0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | – | – | 1.0 | μA |
| | | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | 5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS} \geq$ 5.0 V, $V_{GS}$ = 4.5 V | 10 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 3.1 A | – | 0.065 | 0.075 | Ω |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 2.3 A | – | 0.115 | 0.143 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 3.1 A | – | 8.0 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = 0.9 A, $V_{GS}$ = 0 V | – | 0.8 | 1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 3.1 A | – | 4.0 | 6.0 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 0.6 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 1.3 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 10 Ω, $I_D \cong$ 1.0 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 Ω | – | 12 | 18 | ns |
| Rise Time | $t_r$ | | – | 35 | 55 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 19 | 30 | |
| Fall Time | $t_f$ | | – | 9.0 | 15 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 0.9 A, di/dt = 100 A/μs | – | 40 | 80 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

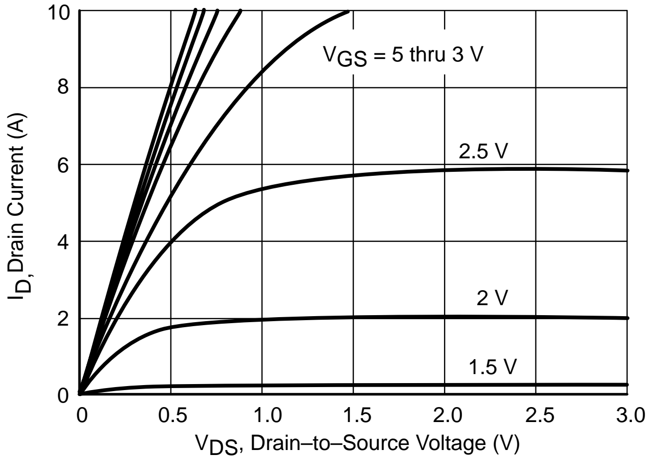


**Figure 1. Output Characteristics**

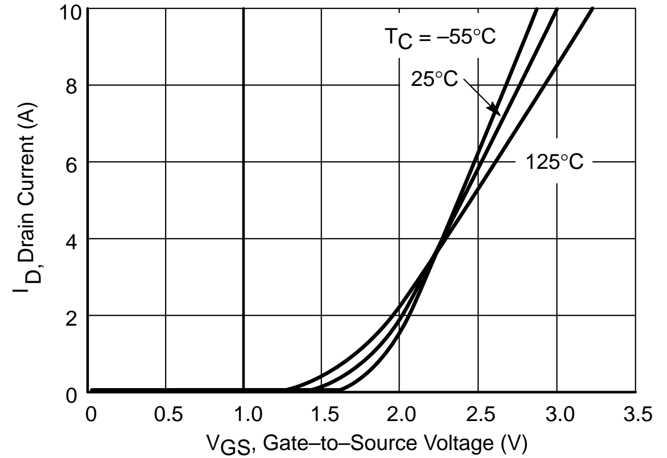


**Figure 2. Transfer Characteristics**

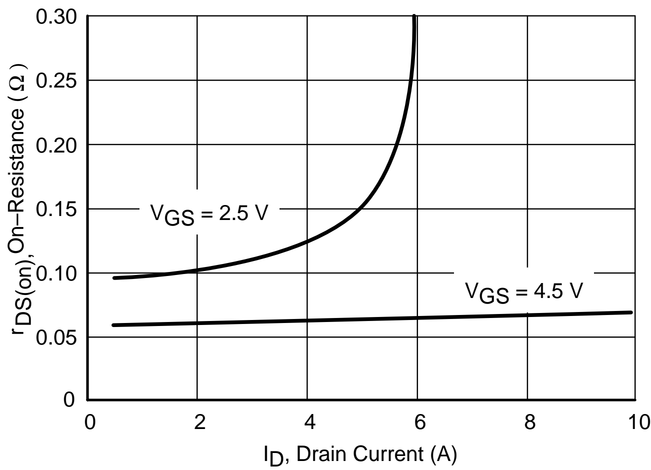


**Figure 3. On–Resistance vs. Drain Current**

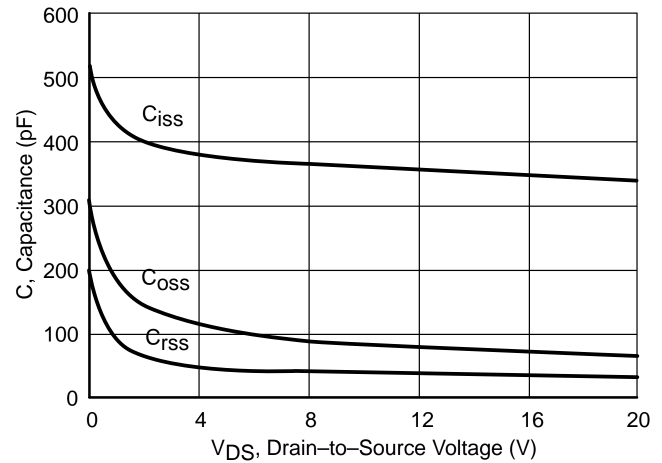


**Figure 4. Capacitance**

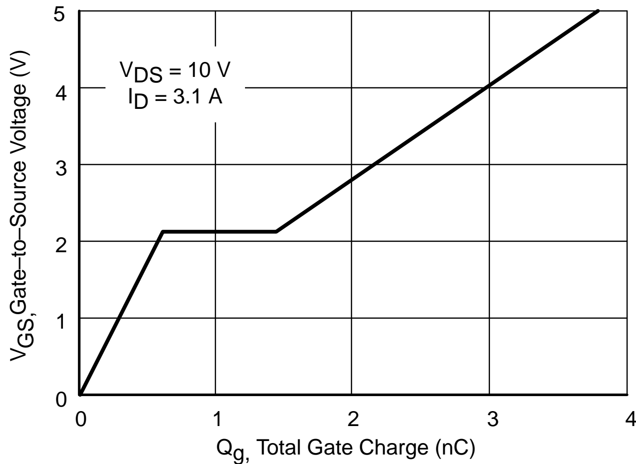


**Figure 5. Gate Charge**

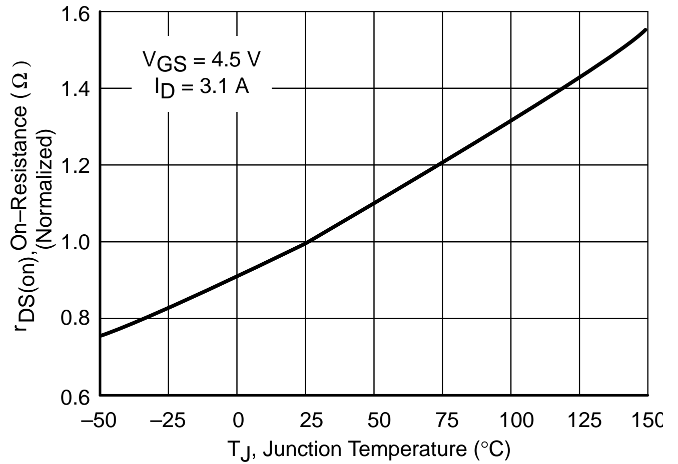


**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

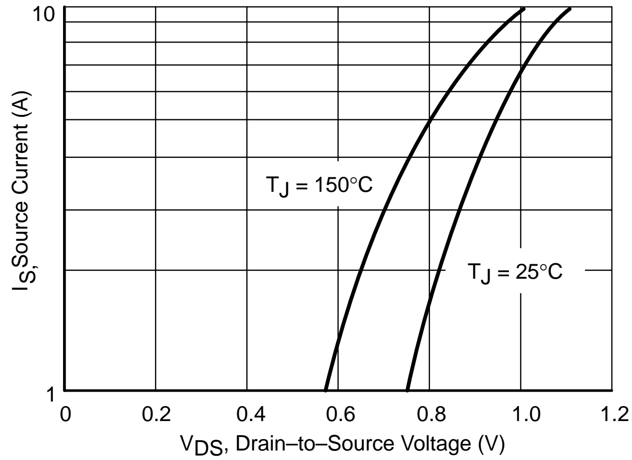


**Figure 7. Source–Drain Diode Forward Voltage**

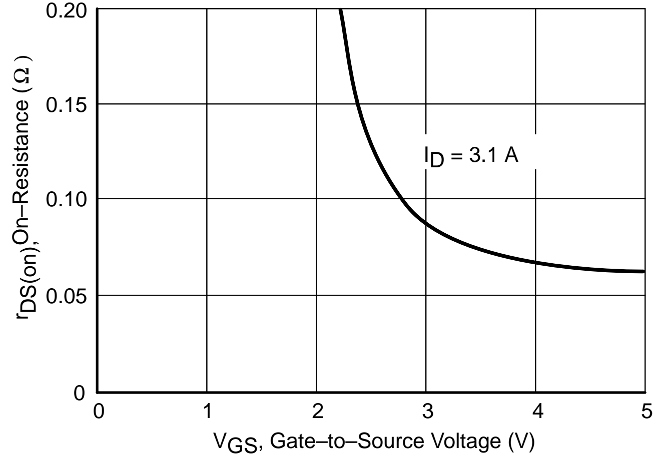


**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

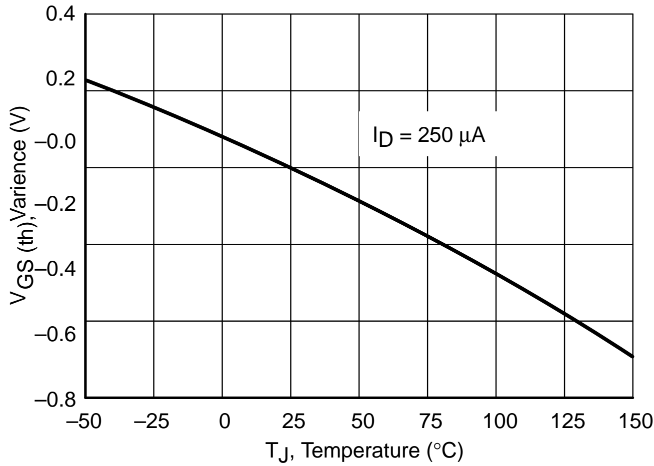


**Figure 9. Threshold Voltage**

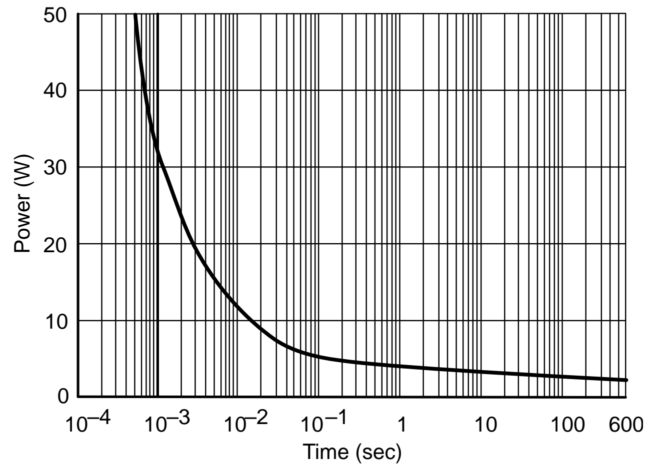


**Figure 10. Single Pulse Power**

## TYPICAL ELECTRICAL CHARACTERISTICS

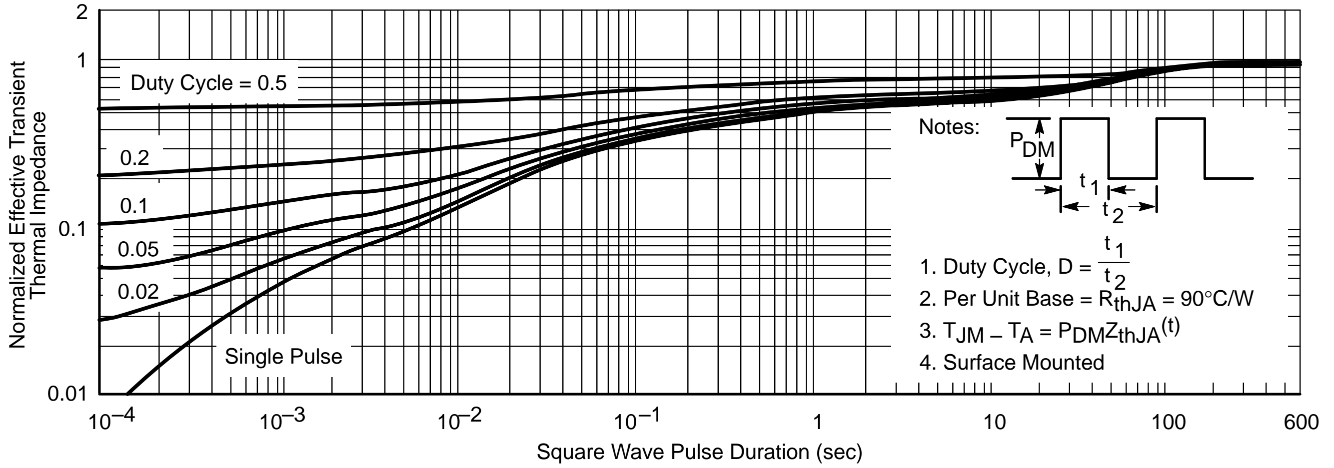


**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

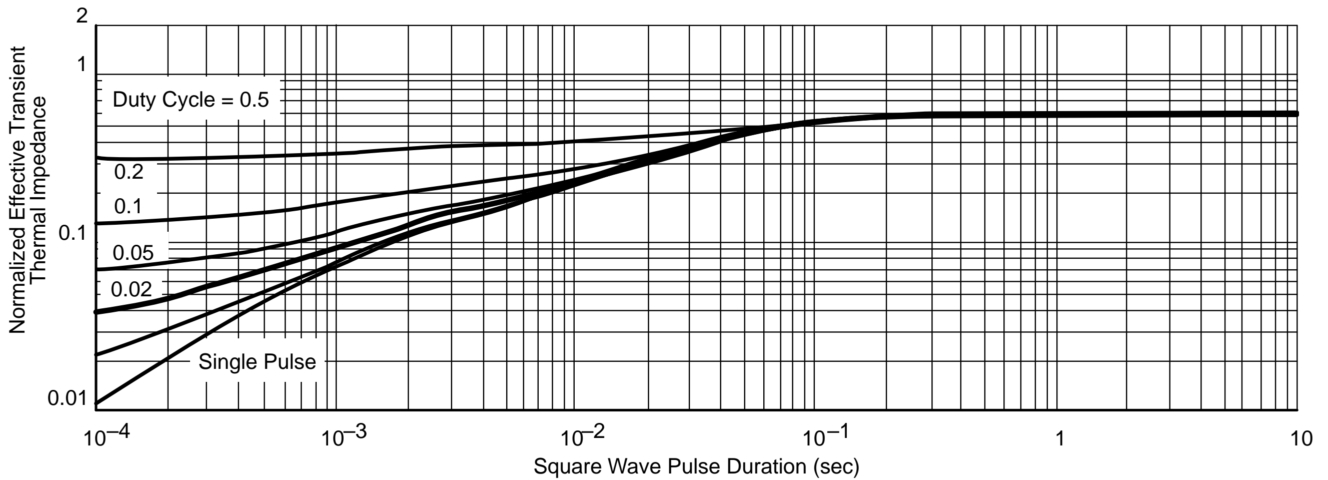


**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

# NTHD5905T1

*Product Preview*

## Dual P-Channel 1.8 V (G-S) MOSFET

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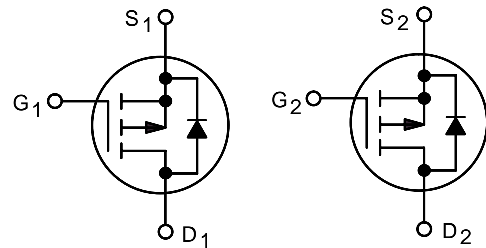
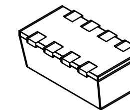
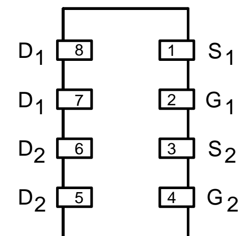



**P–Channel MOSFET** **P–Channel MOSFET**

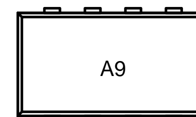


**ChipFET**
**CASE 1206A**
**STYLE 2**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A9 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –8.0 | 0.090 @ $V_{GS}$ = –4.5 V | ±4.1 |
| | 0.130 @ $V_{GS}$ = –2.5 V | ±3.4 |
| | 0.180 @ $V_{GS}$ = –1.8 V | ±2.9 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –8.0 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±8.0 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±4.1<br>±2.9 | <br>±3.0<br>±2.2 | A |
| Pulsed Drain Current | $I_{DM}$ | ±10 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | –1.8 | –0.9 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.1<br>1.1 | <br>1.1<br>0.6 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHD5905T1 | ChipFET | 3000/Tape & Reel |

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.) | $R_{thJA}$ | | | °C/W |
| t ≤ 5 sec | | 50 | 60 | |
| Steady State | | 90 | 110 | |
| Maximum Junction–to–Foot (Drain) Steady State | $R_{thJF}$ | 30 | 40 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = –250 μA | –0.45 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8.0 V | – | – | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –6.4 V, $V_{GS}$ = 0 V | – | – | –1.0 | μA |
| | | $V_{DS}$ = –6.4 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | –5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≤ –5.0 V, $V_{GS}$ = –4.5 V | –10 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = –4.5 V, $I_D$ = –3.0 A | – | 0.075 | 0.090 | Ω |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –2.5 A | – | 0.110 | 0.130 | |
| | | $V_{GS}$ = –1.8 V, $I_D$ = –1.0 A | – | 0.150 | 0.180 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = –5.0 V, $I_D$ = –3.0 A | – | 7.0 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = –0.9 A, $V_{GS}$ = 0 V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –4.0 V, $V_{GS}$ = –4.5 V, $I_D$ = –3.0 A | – | 5.5 | 9.0 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 0.5 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 1.5 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –4.0 V, $R_L$ = 4 Ω, $I_D$ ≅ –1.0 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | – | 10 | 15 | ns |
| Rise Time | $t_r$ | | – | 45 | 70 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 30 | 45 | |
| Fall Time | $t_f$ | | – | 10 | 15 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –0.9 A, di/dt = 100 A/μs | – | 30 | 60 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

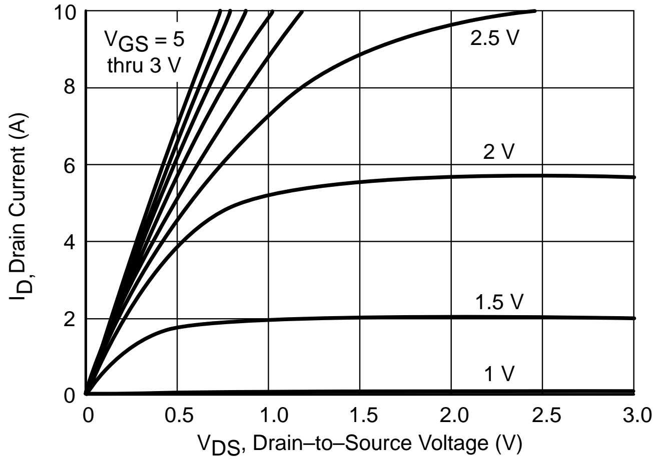



**Figure 1. Output Characteristics**

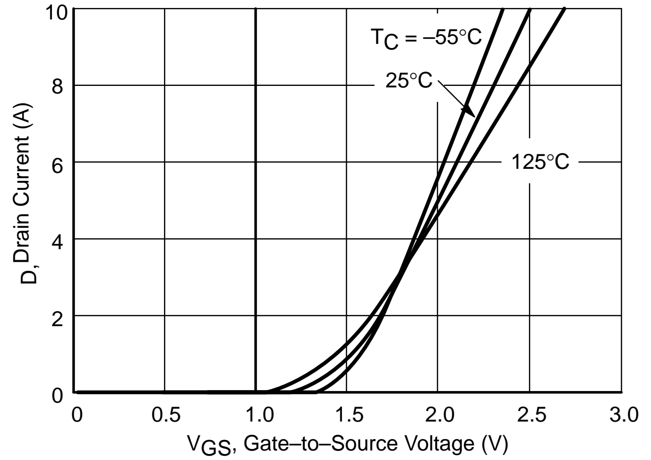



**Figure 2. Transfer Characteristics**

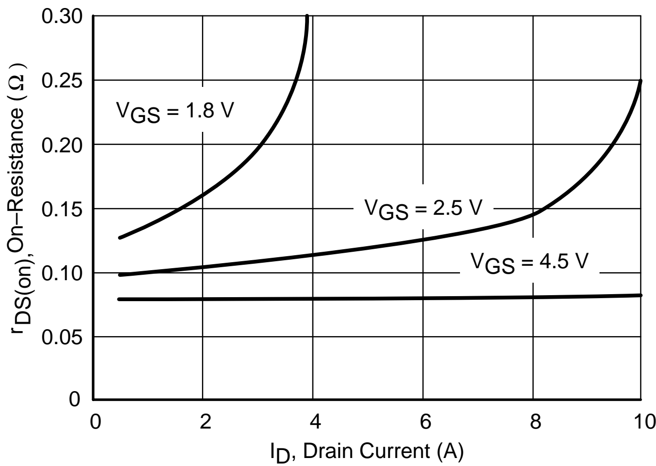



**Figure 3. On–Resistance vs. Drain Current**

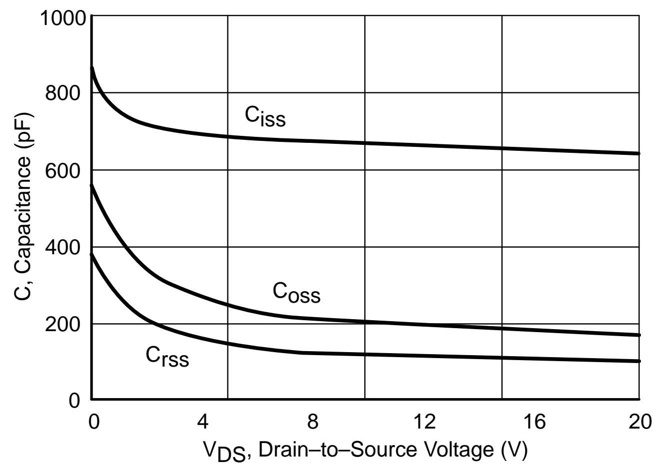



**Figure 4. Capacitance**

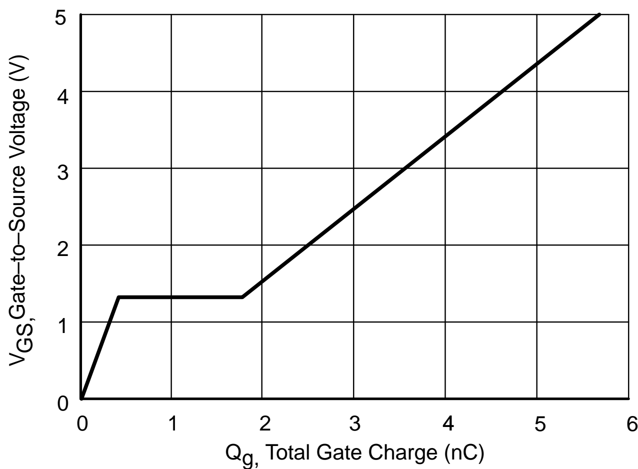



**Figure 5. Gate Charge**

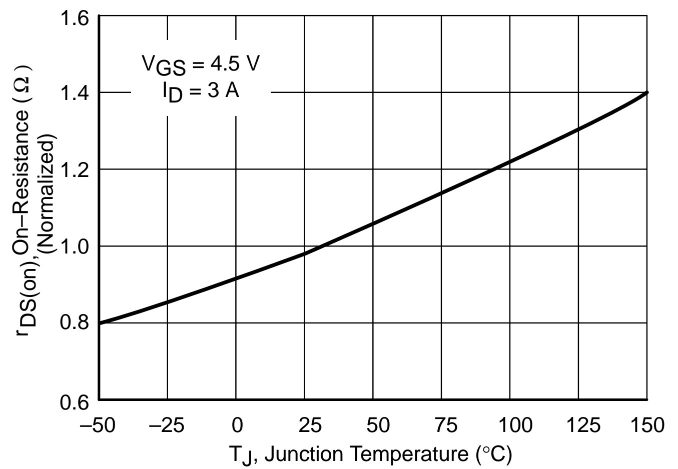



**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

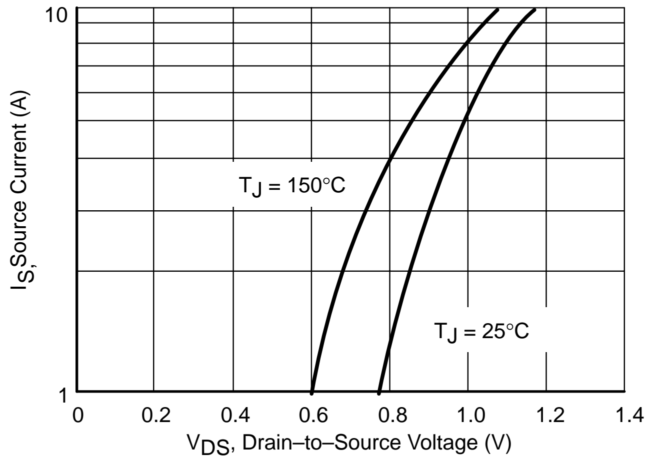



**Figure 7. Source Diode Forward Voltage**

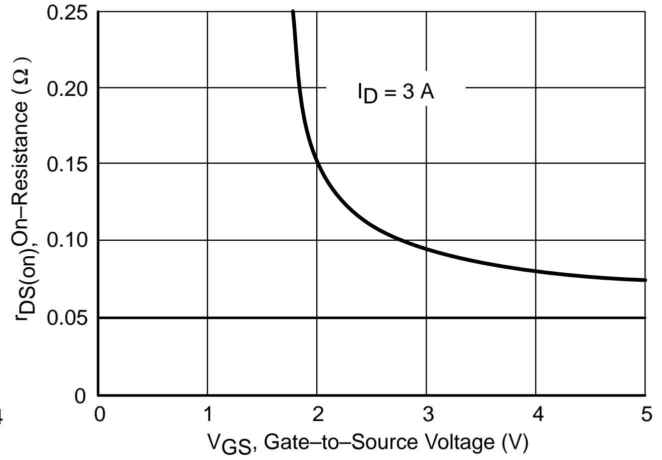



**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

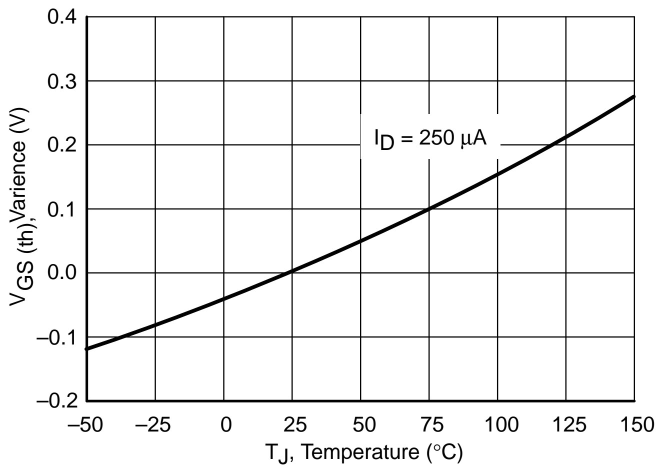



**Figure 9. Threshold Voltage**

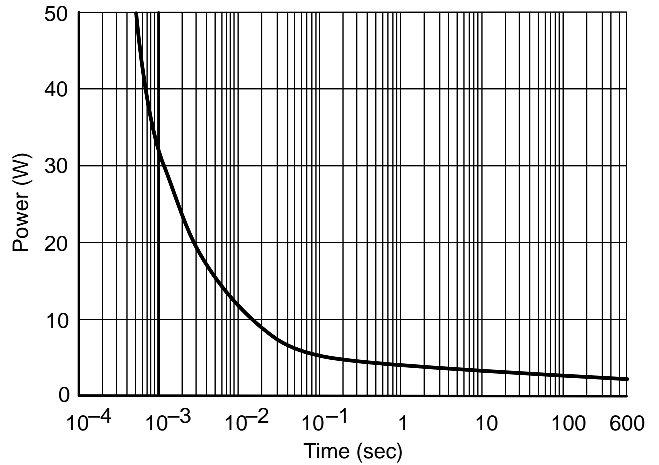



**Figure 10. Single Pulse Power**

## TYPICAL ELECTRICAL CHARACTERISTICS

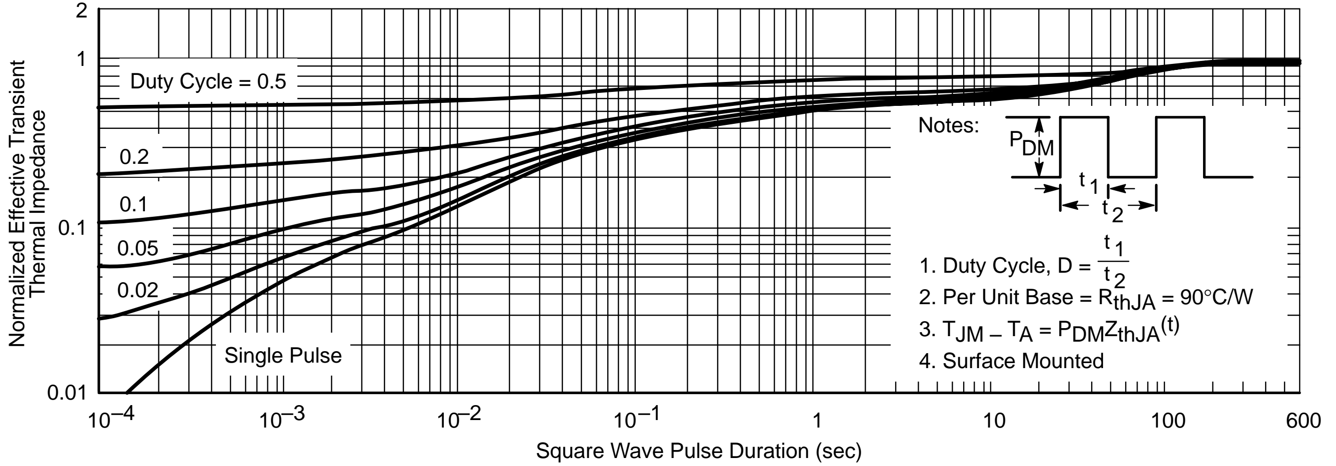



**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

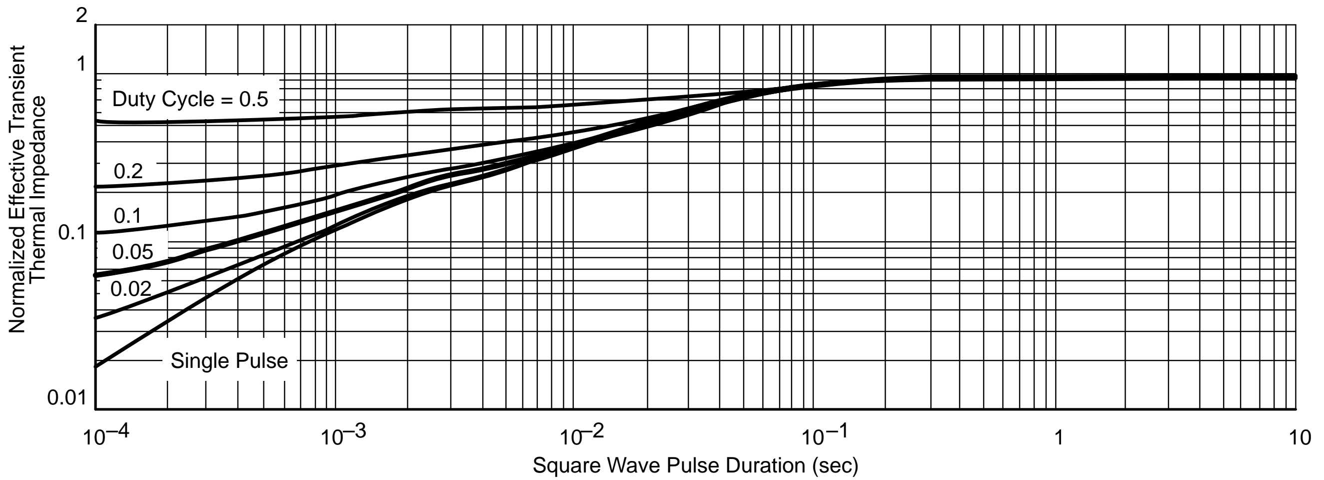



**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

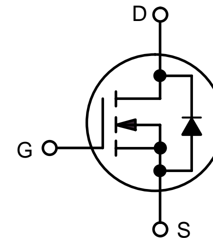
# NTHS5402T1

*Product Preview*

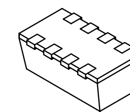
## N-Channel 30 V (D-S) MOSFET

**ON Semiconductor™**

**http://onsemi.com**




**N–Channel MOSFET**

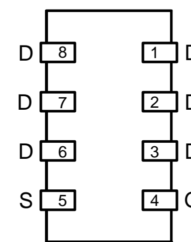


**ChipFET**
**CASE 1206A**
**STYLE 1**

### PRODUCT SUMMARY

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| 30 | 0.035 @ $V_{GS}$ = 10 V | ±6.7 |
| | 0.055 @ $V_{GS}$ = 4.5 V | ±5.3 |

### PIN CONNECTIONS

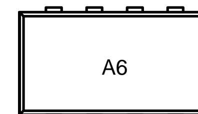



### MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 30 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±20 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±6.7<br>±4.8 | <br>±4.9<br>±3.5 | A |
| Pulsed Drain Current | $I_{DM}$ | ±20 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | 2.1 | 1.1 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.5<br>1.3 | <br>1.3<br>0.7 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

### MARKING DIAGRAM




A6 = Specific Device Code

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| NTHS5402T1 | ChipFET | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.)<br>t ≤ 5 sec<br>Steady State | $R_{thJA}$ | <br>40<br>80 | <br>50<br>95 | °C/W |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 15 | 20 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 μA | 1.0 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±20 V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V | – | – | 1.0 | μA |
| | | $V_{DS}$ = 24 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | 5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≥ 5.0 V, $V_{GS}$ = 10 V | 20 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = 10 V, $I_D$ = 4.9 A | – | 0.030 | 0.035 | Ω |
| | | $V_{GS}$ = 4.5 V, $I_D$ = 3.9 A | – | 0.045 | 0.055 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 4.9 A | – | 15 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = 1.1 A, $V_{GS}$ = 0 V | – | 0.8 | 1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 15 V, $V_{GS}$ = 10 V, $I_D$ = 4.9 A | – | 13 | 20 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 1.3 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 3.1 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 15 V, $R_L$ = 15 Ω, $I_D$ ≅ 1.0 A, $V_{GEN}$ = 10 V, $R_G$ = 6 Ω | – | 10 | 15 | ns |
| Rise Time | $t_r$ | | – | 10 | 15 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 25 | 40 | |
| Fall Time | $t_f$ | | – | 10 | 15 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 1.1 A, di/dt = 100 A/μs | – | 30 | 60 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL CHARACTERISTICS

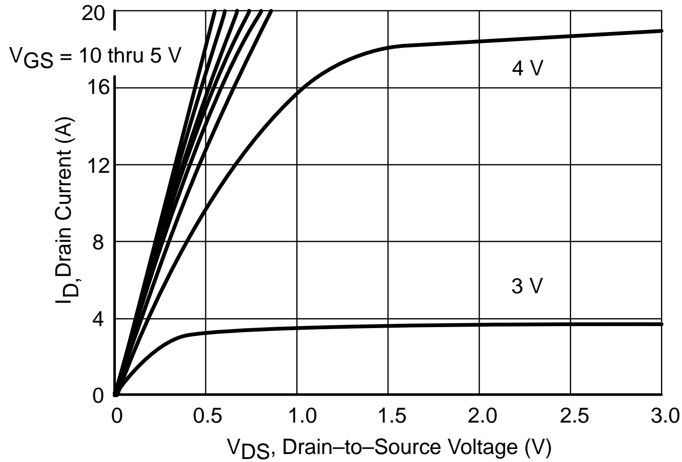



**Figure 1. Output Characteristics**

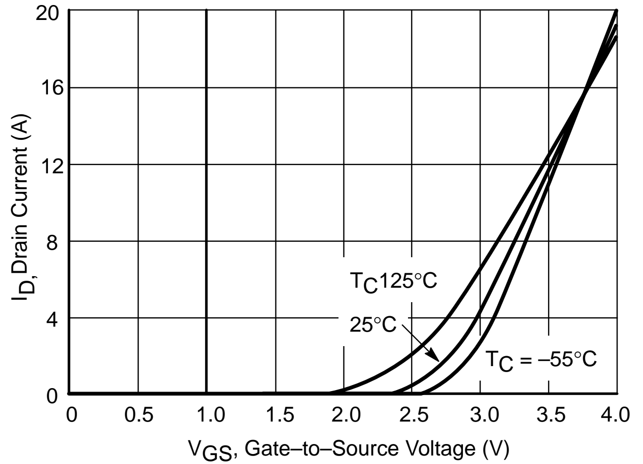



**Figure 2. Transfer Characteristics**

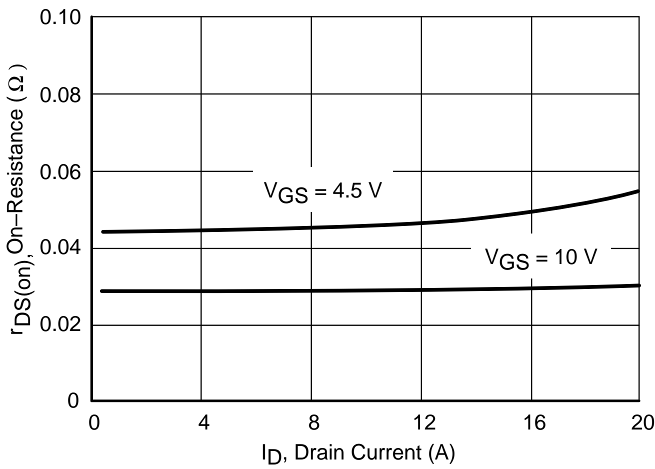



**Figure 3. On–Resistance vs. Drain Current**

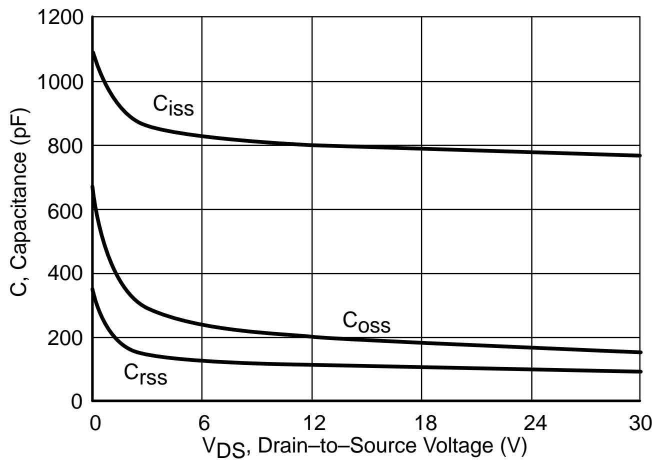



**Figure 4. Capacitance**

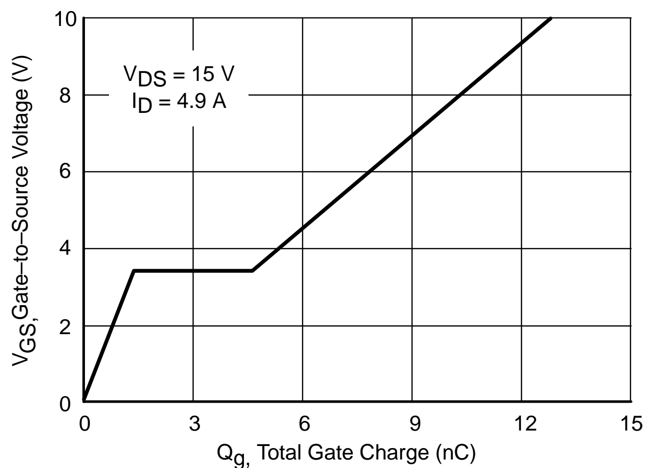



**Figure 5. Gate Charge**

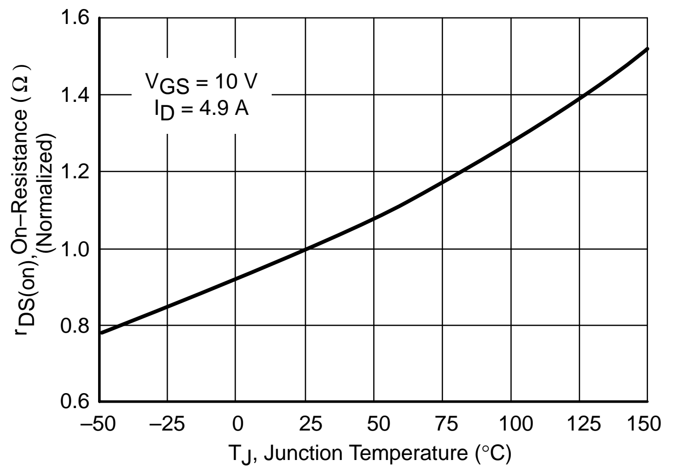



**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL CHARACTERISTICS

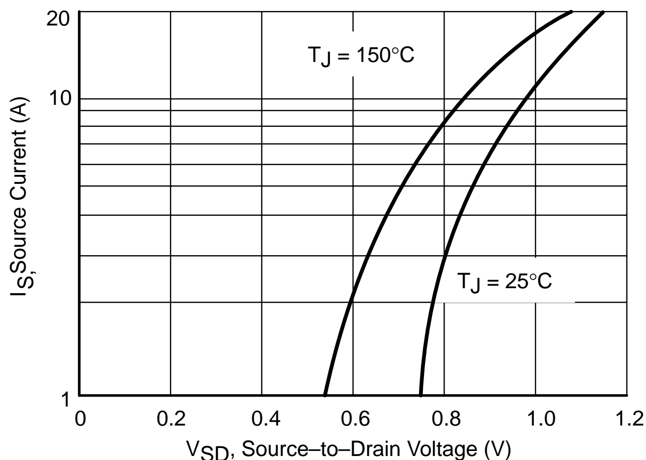



**Figure 7. Source–Drain Diode Forward Voltage**

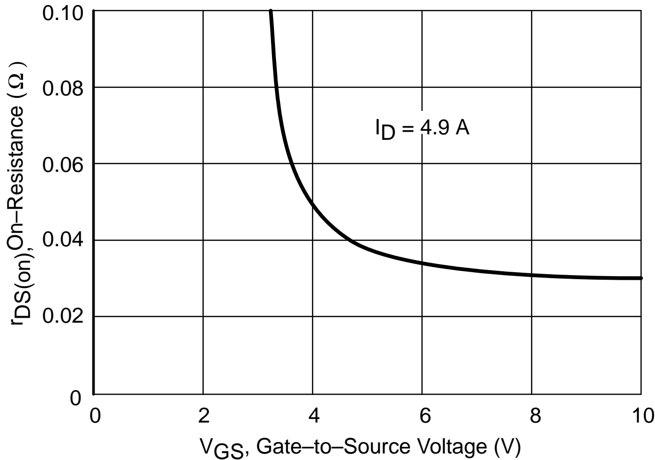



**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

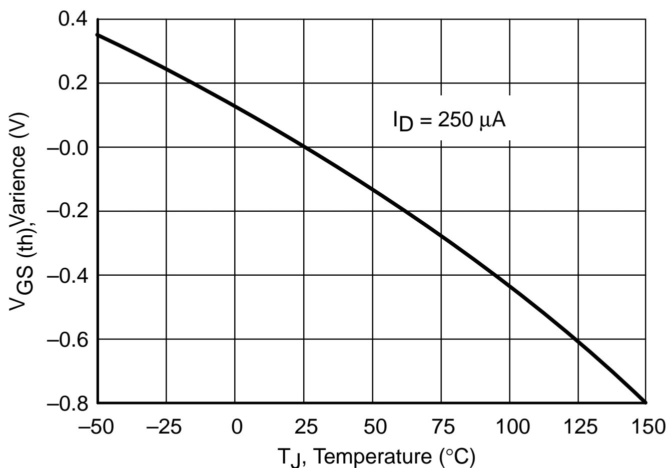



**Figure 9. Threshold Voltage**

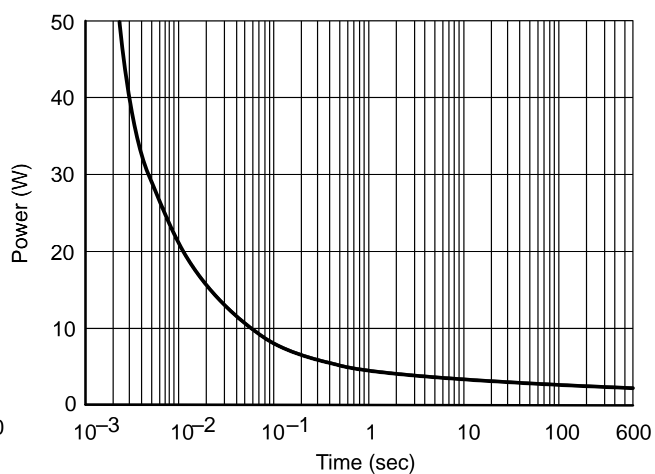



**Figure 10. Single Pulse Power**

## TYPICAL CHARACTERISTICS

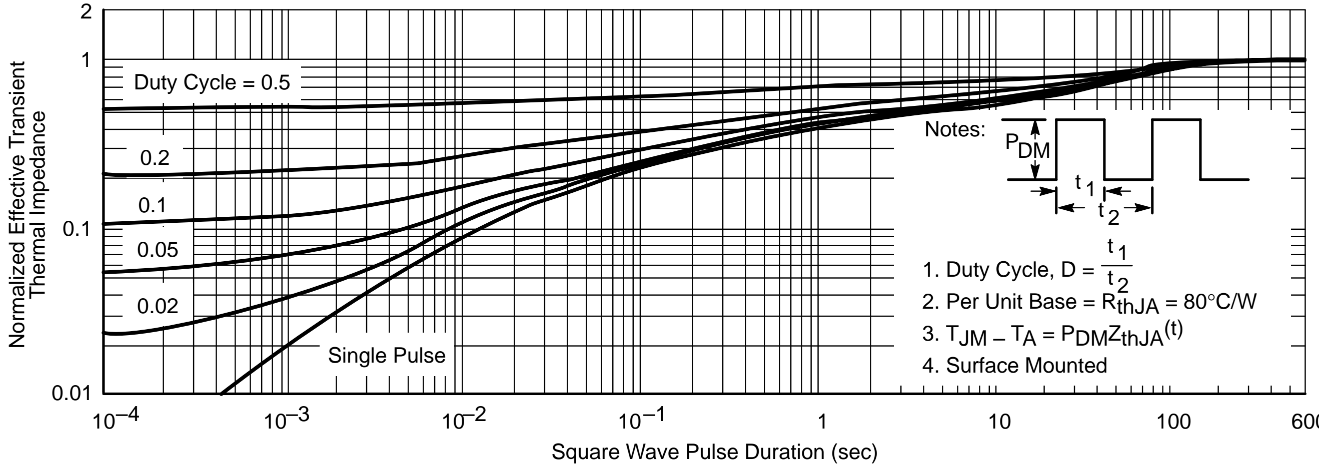



**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

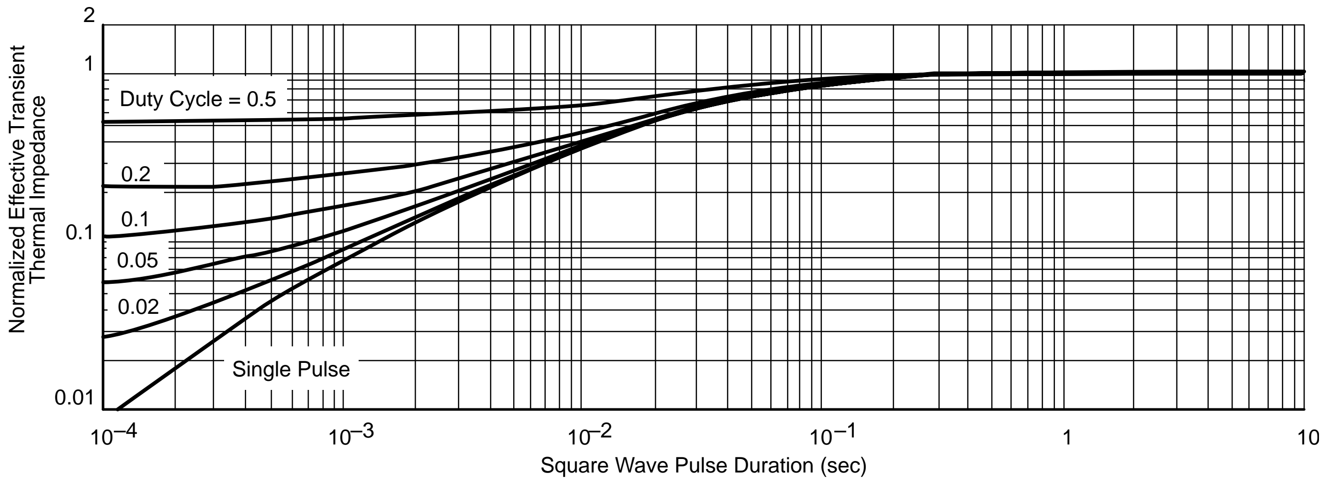



**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

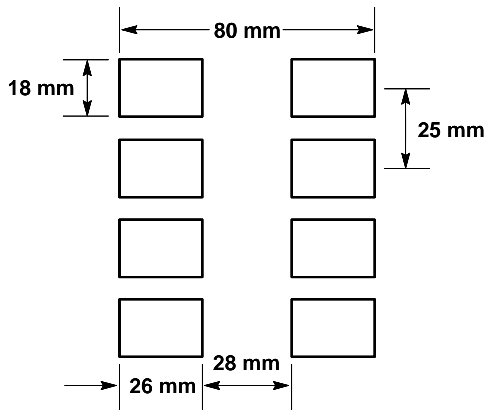



Figure 13.

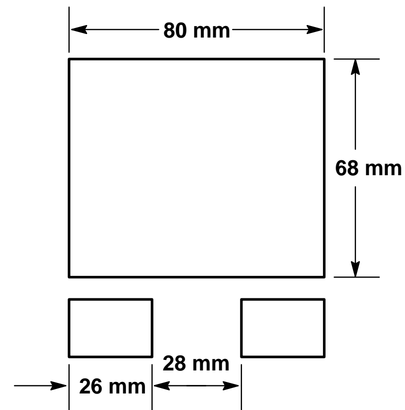



Figure 14.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

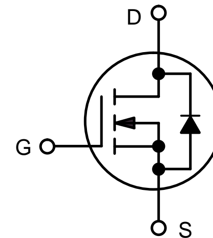
# NTHS5404T1

*Product Preview*

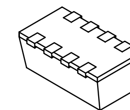
## N-Channel 2.5 V (G-S) MOSFET

**ON Semiconductor**™

**http://onsemi.com**

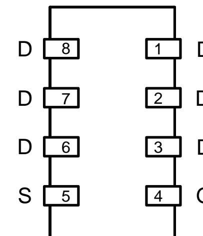



**N–Channel MOSFET**

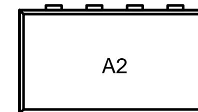


**ChipFET**
**CASE 1206A**
**STYLE 1**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A2 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| 20 | 0.030 @ $V_{GS}$ = 4.5 V | ±7.2 |
| | 0.045 @ $V_{GS}$ = 2.5 V | ±5.9 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±7.2<br>±5.2 | <br>±5.2<br>±3.8 | A |
| Pulsed Drain Current | $I_{DM}$ | ±20 | | A |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | 2.1 | 1.1 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.5<br>1.3 | <br>1.3<br>0.7 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHS5404T1 | ChipFET | 3000/Tape & Reel |

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.)<br>$t \leq 5$ sec<br>Steady State | $R_{thJA}$ | <br>40<br>80 | <br>50<br>95 | °C/W |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 15 | 20 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = 250 μA | 0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V | – | – | 1.0 | μA |
| | | $V_{DS}$ = 16 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | 5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS} \geq$ 5.0 V, $V_{GS}$ = 4.5 V | 20 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = 4.5 V, $I_D$ = 5.2 A | – | 0.025 | 0.030 | Ω |
| | | $V_{GS}$ = 2.5 V, $I_D$ = 4.3 A | – | 0.038 | 0.045 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = 10 V, $I_D$ = 5.2 A | – | 20 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = 1.1 A, $V_{GS}$ = 0 V | – | 0.8 | 1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = 10 V, $V_{GS}$ = 4.5 V, $I_D$ = 5.2 A | – | 12 | 18 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 2.4 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 3.2 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = 10 V, $R_L$ = 10 Ω, $I_D \cong$ 1.0 A, $V_{GEN}$ = 4.5 V, $R_G$ = 6 Ω | – | 20 | 30 | ns |
| Rise Time | $t_r$ | | – | 40 | 60 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 40 | 60 | |
| Fall Time | $t_f$ | | – | 15 | 23 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = 1.1 A, di/dt = 100 A/μs | – | 30 | 60 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

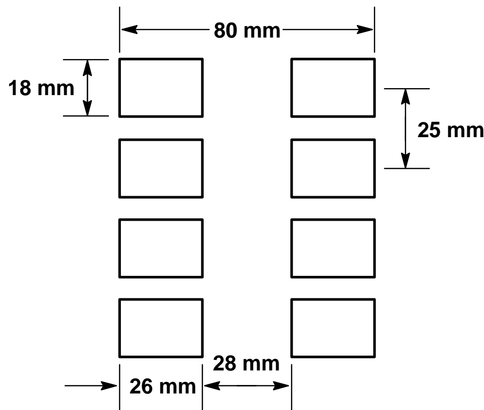


Figure 1.

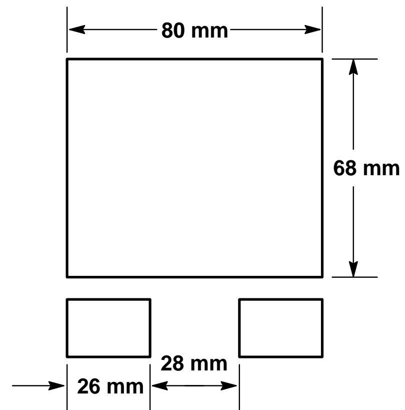


Figure 2.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 1. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 2 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

# NTHS5441T1

*Product Preview*

## P-Channel 2.5 V (G-S) MOSFET

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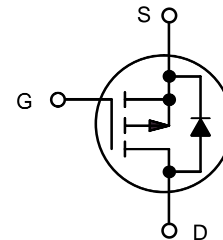
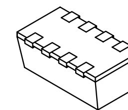
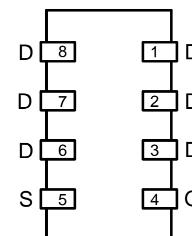



**P–Channel MOSFET**

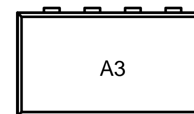


**ChipFET**
**CASE 1206A**
**STYLE 1**

### PIN CONNECTIONS




### MARKING DIAGRAM




A3 = Specific Device Code

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| NTHS5441T1 | ChipFET | 3000/Tape & Reel |

### PRODUCT SUMMARY

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –20 | 0.055 @ $V_{GS}$ = –4.5 V | ±5.3 |
| | 0.06 @ $V_{GS}$ = –3.6 V | ±5.1 |
| | 0.083 @ $V_{GS}$ = –2.5 V | ±4.3 |

### MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±5.3<br>±3.8 | <br>±3.9<br>±2.8 | A |
| Pulsed Drain Current | $I_{DM}$ | ±20 | | A |
| Continuous Source Current (Note 1.) | $I_S$ | –2.1 | –1.1 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.5<br>1.3 | <br>1.3<br>0.7 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

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**THERMAL CHARACTERISTICS**

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.) | $R_{thJA}$ | | | °C/W |
| t ≤ 5 sec | | 40 | 50 | |
| Steady State | | 80 | 95 | |
| Maximum Junction–to–Foot (Drain) Steady State | $R_{thJF}$ | 15 | 20 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = –250 μA | –0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 12 V | – | – | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | – | – | –1.0 | μA |
| | | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | –5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≤ –5.0 V, $V_{GS}$ = –4.5 V | –20 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = –3.6 V, $I_D$ = –3.7 A | – | 0.050 | 0.06 | Ω |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –3.1 A | – | 0.070 | 0.083 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = –10 V, $I_D$ = –3.9 A | – | 12 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = –1.1 A, $V_{GS}$ = 0 V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –3.9 A | – | 11 | 22 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 3.0 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 2.5 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –10 V, $R_L$ = 10 Ω, $I_D$ ≅ –1.0 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | – | 20 | 30 | ns |
| Rise Time | $t_r$ | | – | 35 | 55 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 65 | 100 | |
| Fall Time | $t_f$ | | – | 45 | 70 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –1.1 A, di/dt = 100 A/μs | – | 30 | 60 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

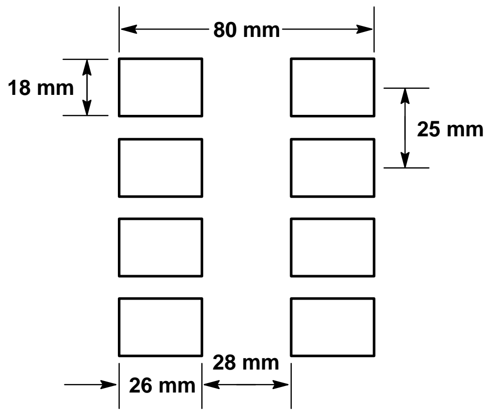


Figure 1.

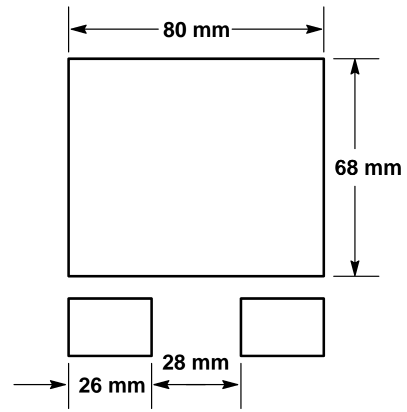


Figure 2.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 1. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 2 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

# NTHS5443T1

*Product Preview*

# P-Channel 2.5 V (G-S) MOSFET

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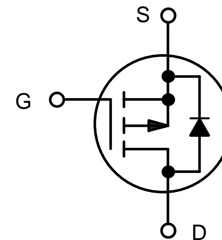
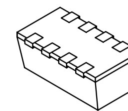
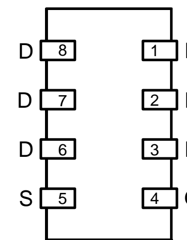



**P–Channel MOSFET**

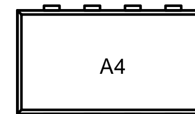


**ChipFET**
**CASE 1206A**
**STYLE 1**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A4 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $R_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –20 | 0.065 @ $V_{GS}$ = –4.5 V | ± 4.9 |
| | 0.074 @ $V_{GS}$ = –3.6 V | ± 4.6 |
| | 0.110 @ $V_{GS}$ = –2.5 V | ± 3.8 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –20 | | V |
| Gate–Source Voltage | $V_{GS}$ | ± 12 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>± 4.9<br>± 3.5 | <br>± 3.6<br>± 2.6 | A |
| Pulsed Drain Current | $I_{DM}$ | ± 15 | | A |
| Continuous Source Current (Note 1.) | $I_{AS}$ | –2.1 | –1.1 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.5<br>1.3 | <br>1.3<br>0.7 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHS5443T1 | ChipFET | 3000/Tape & Reel |

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.)<br>t ≤ 5 sec<br>Steady State | $R_{thJA}$ | <br>40<br>80 | <br>50<br>95 | °C/W |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 15 | 20 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = –250 μA | –0.6 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ±12 V | – | – | ±100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V | – | – | –1.0 | μA |
| | | $V_{DS}$ = –16 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | –5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≤ –5.0 V, $V_{GS}$ = –4.5 V | –15 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = –4.5 V, $I_D$ = –3.6 A | – | 0.056 | 0.065 | Ω |
| | | $V_{GS}$ = –3.6 V, $I_D$ = –3.3 A | – | 0.065 | 0.074 | |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –2.7 A | – | 0.095 | 0.110 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = –10 V, $I_D$ = –3.6 A | – | 10 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = –1.1 A, $V_{GS}$ = 0 V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –10 V, $V_{GS}$ = –4.5 V, $I_D$ = –3.6 A | – | 9.0 | 14 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 2.2 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 2.2 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –10 V, $R_L$ = 10 Ω, $I_D$ ≅ –1.0 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | – | 15 | 25 | μs |
| Rise Time | $t_r$ | | – | 30 | 45 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 50 | 75 | |
| Fall Time | $t_f$ | | – | 35 | 50 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –1.1 A, di/dt = 100 A/μs | – | 30 | 60 | ns |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

# NTHS5445T1

*Product Preview*

## P-Channel 1.8 V (G-S) MOSFET

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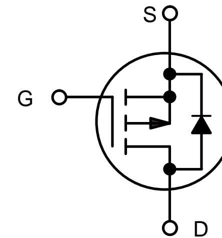
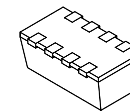
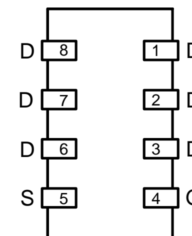



**P–Channel MOSFET**

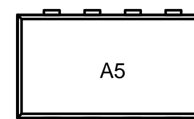


**ChipFET**
**CASE 1206A**
**STYLE 1**

**PIN CONNECTIONS**




**MARKING DIAGRAM**




A5 = Specific Device Code

**PRODUCT SUMMARY**

| $V_{DS}$ (V) | $r_{DS(on)}$ (Ω) | $I_D$ (A) |
|---|---|---|
| –8.0 | 0.035 @ $V_{GS}$ = –4.5 V | ±7.1 |
| | 0.047 @ $V_{GS}$ = –2.5 V | ±6.2 |
| | 0.062 @ $V_{GS}$ = –1.8 V | ±5.7 |

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

| Rating | Symbol | 5 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | –8.0 | | V |
| Gate–Source Voltage | $V_{GS}$ | ±8.0 | | V |
| Continuous Drain Current ($T_J$ = 150°C) (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $I_D$ | <br>±7.1<br>±5.2 | <br>±5.2<br>±3.7 | A |
| Pulsed Drain Current | $I_{DM}$ | ±20 | | A |
| Continuous Source Current (Note 1.) | $I_S$ | –2.1 | –1.1 | A |
| Maximum Power Dissipation (Note 1.)<br>$T_A$ = 25°C<br>$T_A$ = 85°C | $P_D$ | <br>2.5<br>1.3 | <br>1.3<br>0.7 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |

1. Surface Mounted on 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTHS5445T1 | ChipFET | 3000/Tape & Reel |

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## THERMAL CHARACTERISTICS

| Characteristic | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.) | $R_{thJA}$ | | | °C/W |
| t ≤ 5 sec | | 40 | 50 | |
| Steady State | | 80 | 95 | |
| Maximum Junction–to–Foot (Drain)<br>Steady State | $R_{thJF}$ | 15 | 20 | °C/W |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Static** | | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}$, $I_D$ = –250 μA | –0.45 | – | – | V |
| Gate–Body Leakage | $I_{GSS}$ | $V_{DS}$ = 0 V, $V_{GS}$ = ± 8.0 V | – | – | ± 100 | nA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = –6.4 V, $V_{GS}$ = 0 V | – | – | –1.0 | μA |
| | | $V_{DS}$ = –6.4 V, $V_{GS}$ = 0 V, $T_J$ = 85°C | – | – | –5.0 | |
| On–State Drain Current (Note 3.) | $I_{D(on)}$ | $V_{DS}$ ≤ –5.0 V, $V_{GS}$ = –4.5 V | –20 | – | – | A |
| Drain–Source On–State Resistance (Note 3.) | $r_{DS(on)}$ | $V_{GS}$ = –4.5 V, $I_D$ = –5.2 A | – | 0.030 | 0.035 | Ω |
| | | $V_{GS}$ = –2.5 V, $I_D$ = –4.5 A | – | 0.040 | 0.047 | |
| | | $V_{GS}$ = –1.8 V, $I_D$ = –2.0 A | – | 0.052 | 0.062 | |
| Forward Transconductance (Note 3.) | $g_{fs}$ | $V_{DS}$ = –5.0 V, $I_D$ = –5.2 A | – | 18 | – | S |
| Diode Forward Voltage (Note 3.) | $V_{SD}$ | $I_S$ = –1.1 A, $V_{GS}$ = 0 V | – | –0.8 | –1.2 | V |
| **Dynamic** (Note 4.) | | | | | | |
| Total Gate Charge | $Q_g$ | $V_{DS}$ = –4.0 V, $V_{GS}$ = –4.5 V, $I_D$ = –5.2 A | – | 17 | 26 | nC |
| Gate–Source Charge | $Q_{gs}$ | | – | 2.8 | – | |
| Gate–Drain Charge | $Q_{gd}$ | | – | 2.6 | – | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{DD}$ = –4.0 V, $R_L$ = 4 Ω, $I_D$ ≅ –1.0 A, $V_{GEN}$ = –4.5 V, $R_G$ = 6 Ω | – | 15 | 25 | ns |
| Rise Time | $t_r$ | | – | 45 | 70 | |
| Turn–Off Delay Time | $t_{d(off)}$ | | – | 110 | 165 | |
| Fall Time | $t_f$ | | – | 65 | 100 | |
| Source–Drain Reverse Recovery Time | $t_{rr}$ | $I_F$ = –1.1 A, di/dt = 100 A/μs | – | 30 | 60 | |

2. Surface Mounted on 1″ x 1″ FR4 Board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

## TYPICAL ELECTRICAL CHARACTERISTICS

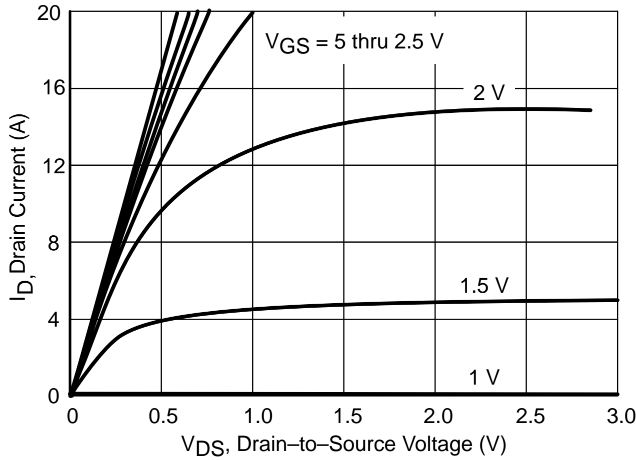


**Figure 1. Output Characteristics**

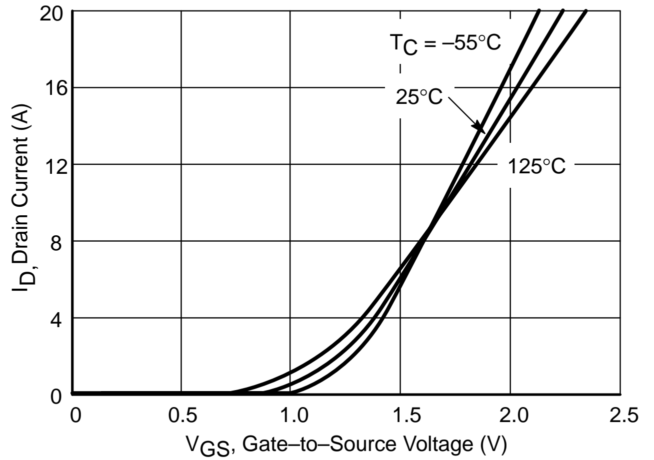


**Figure 2. Transfer Characteristics**

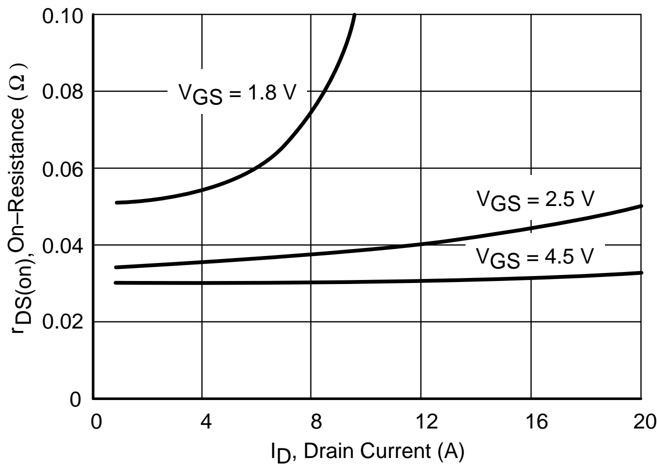


**Figure 3. On–Resistance vs. Drain Current**

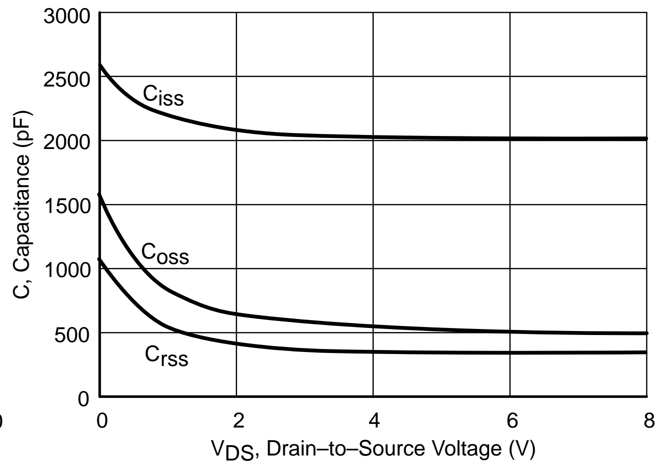


**Figure 4. Capacitance**

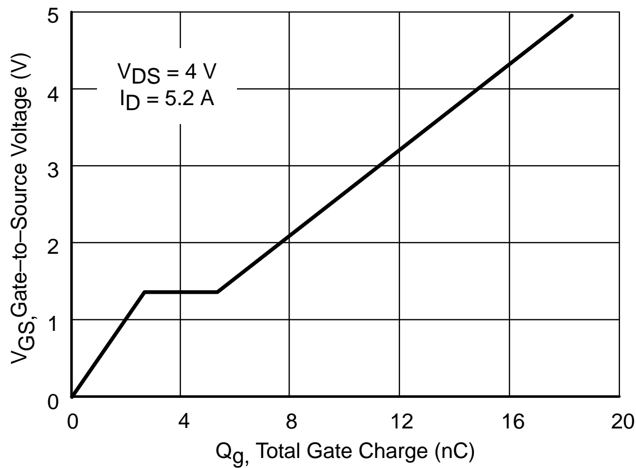


**Figure 5. Gate Charge**

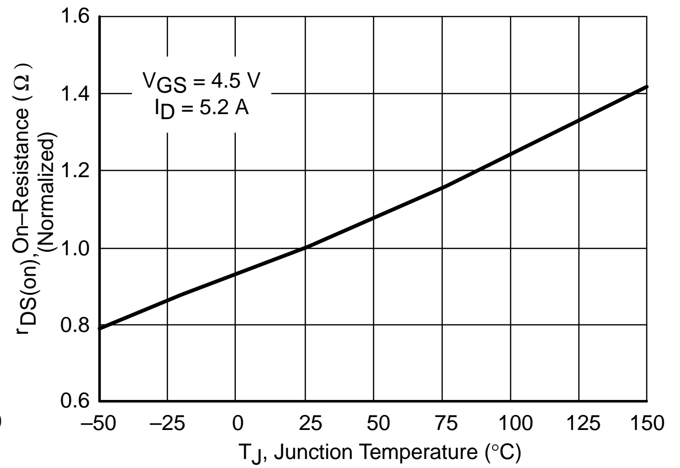


**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

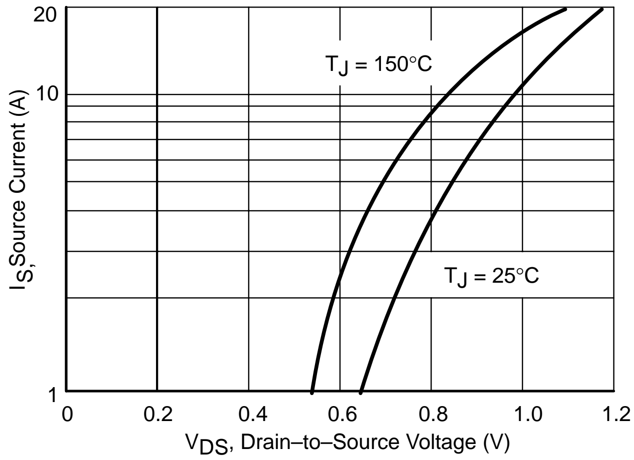


**Figure 7. Source–Drain Diode Forward Voltage**

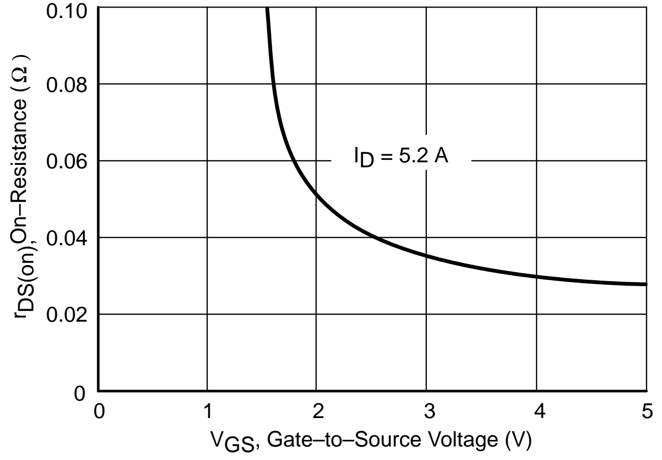


**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

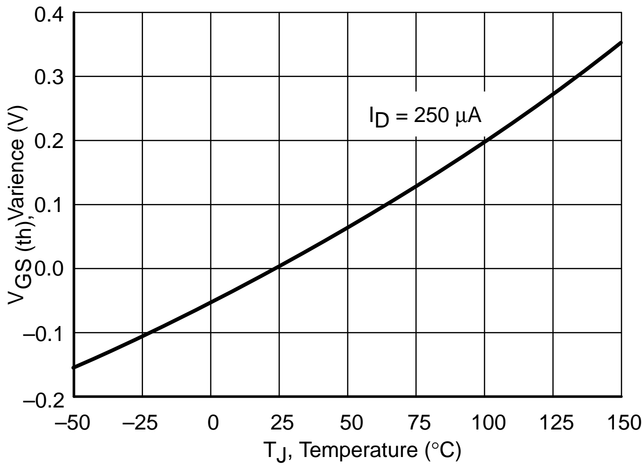


**Figure 9. Threshold Voltage**

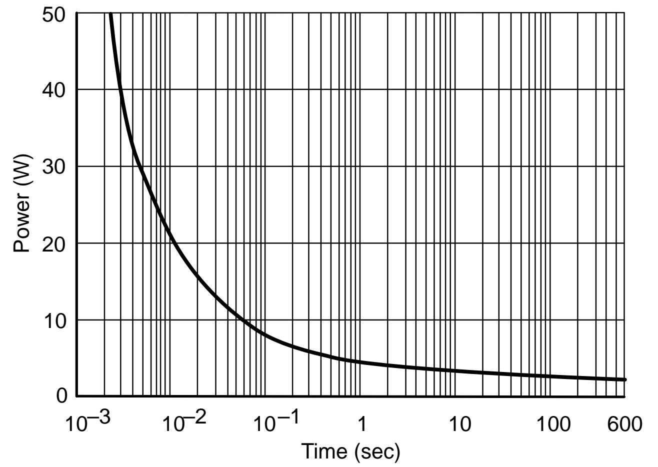


**Figure 10. Single Pulse Power**

## TYPICAL ELECTRICAL CHARACTERISTICS

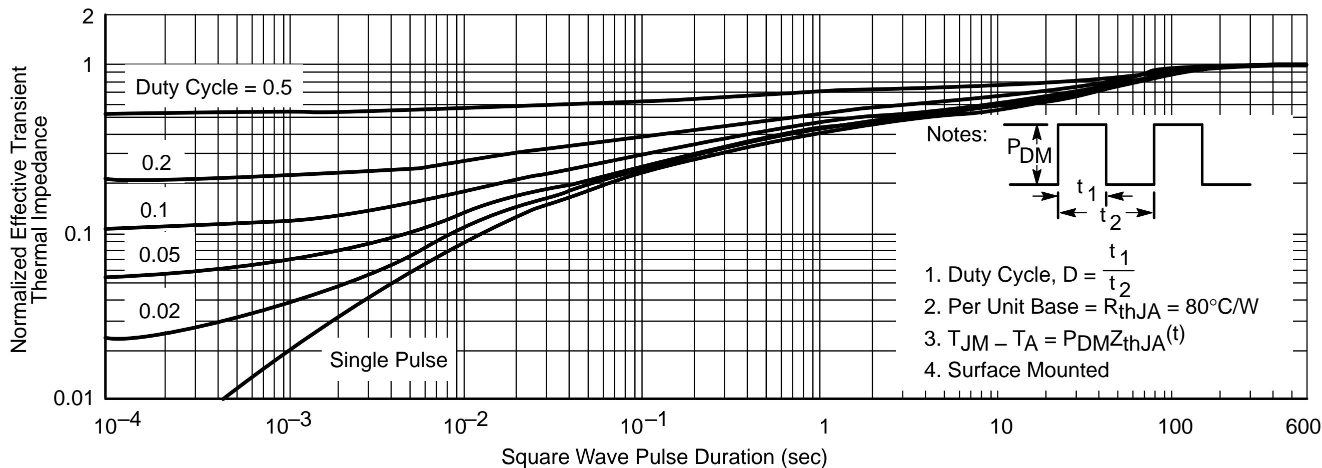


**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

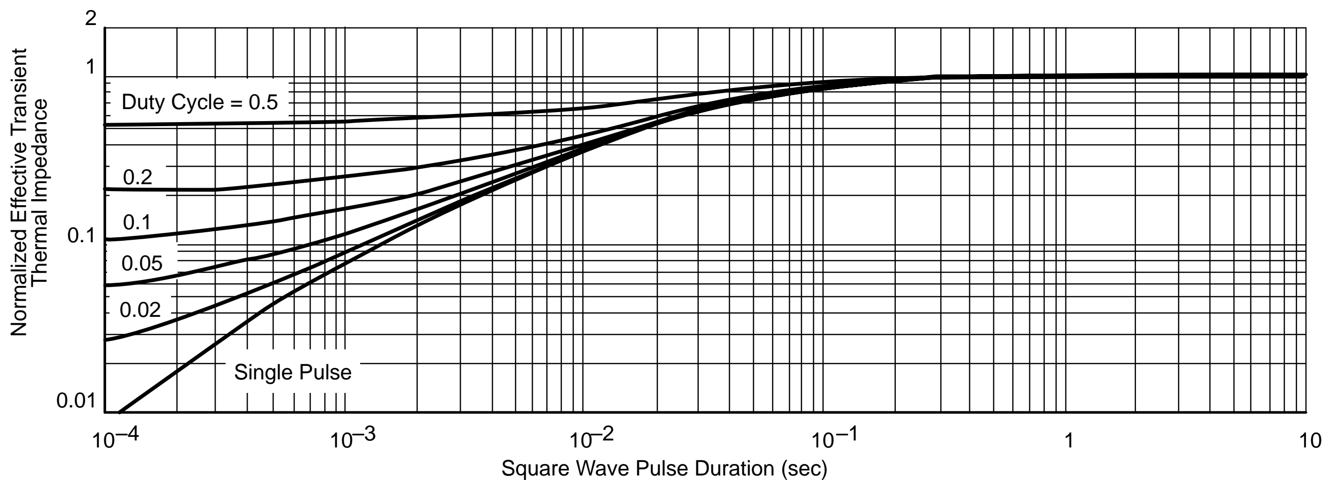


**Figure 12. Normalized Thermal Transient Impedance, Junction–to–Foot**

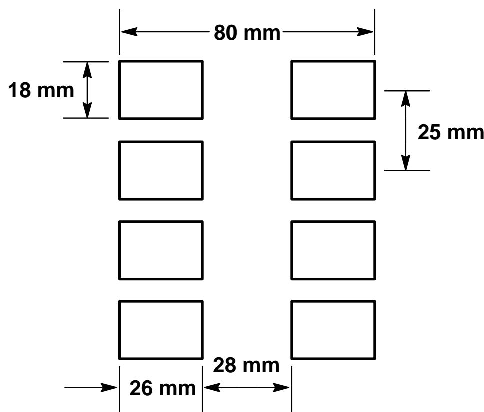


Figure 13.

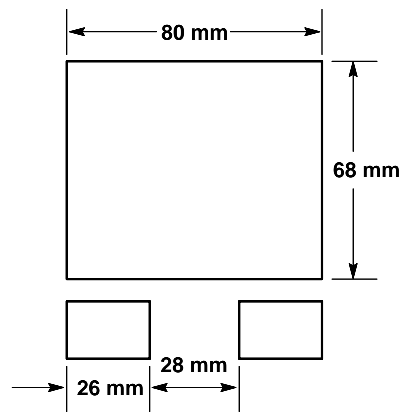


Figure 14.

## BASIC PAD PATTERNS

The basic pad layout with dimensions is shown in Figure 13. This is sufficient for low power dissipation MOSFET applications, but power semiconductor performance requires a greater copper pad area, particularly for the drain leads.

The minimum recommended pad pattern shown in Figure 14 improves the thermal area of the drain connections (pins 1, 2, 3, 6, 7, 8) while remaining within the confines of the basic footprint. The drain copper area is 0.0054 sq. in. (or 3.51 sq. mm). This will assist the power dissipation path away from the device (through the copper leadframe) and into the board and exterior chassis (if applicable) for the single device. The addition of a further copper area and/or the addition of vias to other board layers will enhance the performance still further.

# NTMD3P03R2

**ON Semiconductor™**

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*Product Preview*

## Power MOSFET -3.05 Amps, -30 Volts

### Dual P–Channel SO–8

**Features**

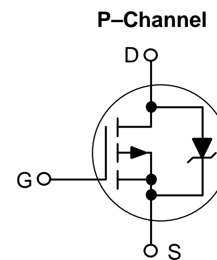
- High Efficiency Components in a Dual SO–8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for the SO–8 Package is Provided

**Applications**

- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

**–3.05 AMPERES**
**–30 VOLTS**
**0.085 Ω @ $V_{GS}$ = –10 V**

**P–Channel**

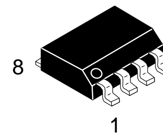



**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

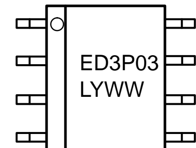
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –30 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | V |
| Thermal Resistance – Junction–to–Ambient (Note 1.) | $R_{θJA}$ | 171 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.73 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –2.34 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –1.87 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –8.0 | A |
| Thermal Resistance – Junction–to–Ambient (Note 2.) | $R_{θJA}$ | 100 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.25 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –3.05 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –2.44 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –12 | A |
| Thermal Resistance – Junction–to–Ambient (Note 3.) | $R_{θJA}$ | 62.5 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –3.86 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –3.1 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –15 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –30 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –7.5 Apk, L = 5 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 140 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, t = Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

**MARKING DIAGRAM**

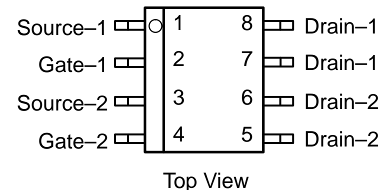



**SO–8**
**CASE 751**
**STYLE 11**




ED3P03 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMD3P03R2 | SO–8 | 2500/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | –30<br>– | –<br>–30 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C)<br>($V_{DS}$ = –30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | –<br>–<br>– | –<br>–<br>– | –1.0<br>–20<br>–2.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | –1.0<br>– | –1.7<br>3.6 | –2.5<br>– | Vdc |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc)<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.5 Adc) | | $R_{DS(on)}$ | –<br>– | 0.063<br>0.090 | 0.085<br>0.125 | Ω |
| Forward Transconductance ($V_{DS}$ = –15 Vdc, $I_D$ = –3.05 Adc) | | $g_{FS}$ | – | 5.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 520 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 170 | 325 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 70 | 135 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. and 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –3.05 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 22 | ns |
| Rise Time | | $t_r$ | – | 16 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 80 | |
| Fall Time | | $t_f$ | – | 45 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –1.5 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 42 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc) | $Q_{tot}$ | – | 16 | 25 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.5 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 V)<br>($I_S$ = –3.05 Adc, $V_{GS}$ = 0 V, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.96<br>–0.78 | –1.25<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 34 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

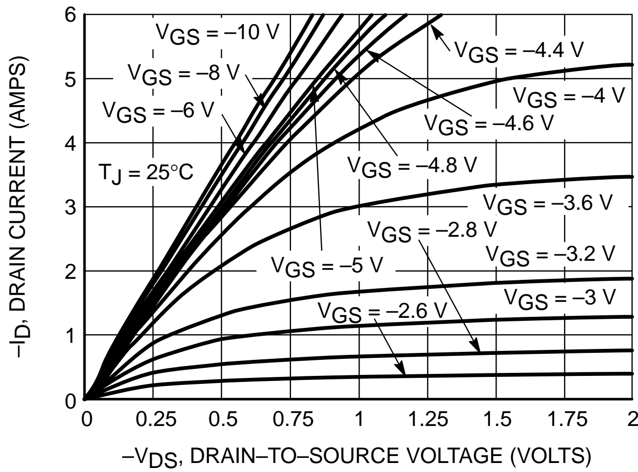



**Figure 1. On−Region Characteristics**

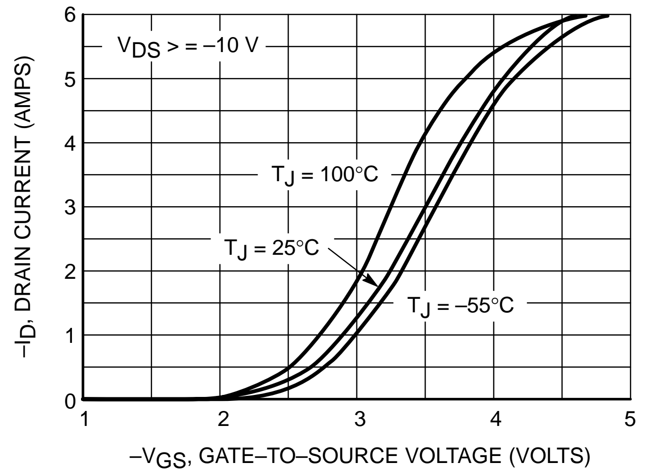



**Figure 2. Transfer Characteristics**

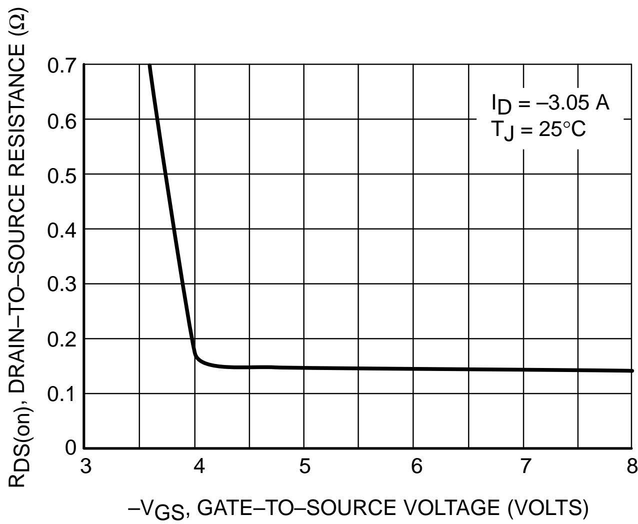



**Figure 3. On−Resistance vs. Gate−to−Source Voltage**

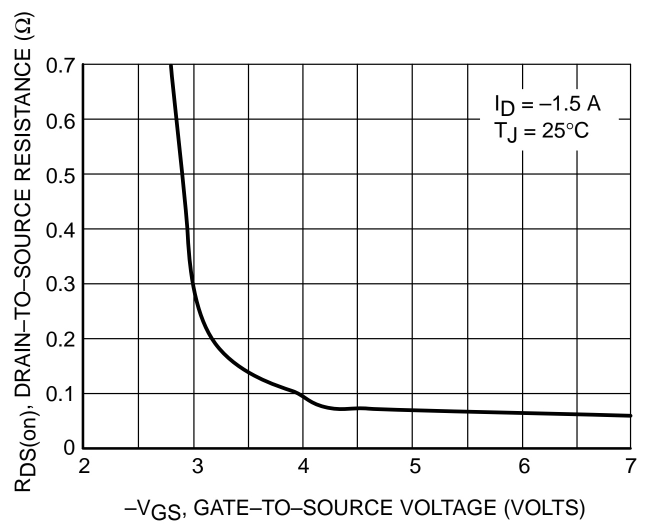



**Figure 4. On−Resistance vs. Gate−to−Source Voltage**

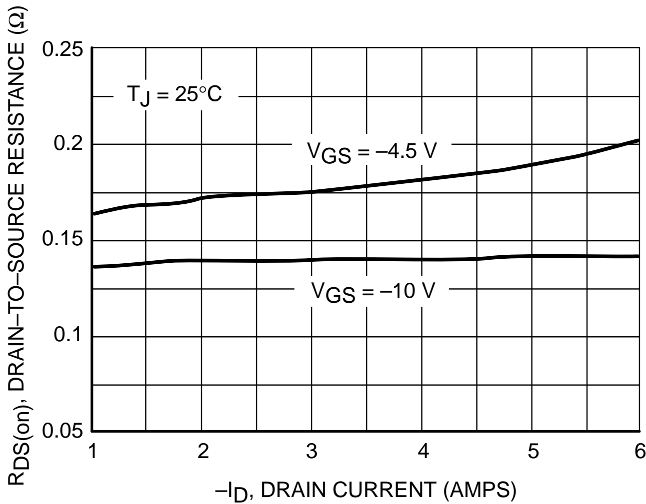



**Figure 5. On−Resistance vs. Drain Current and Gate Voltage**

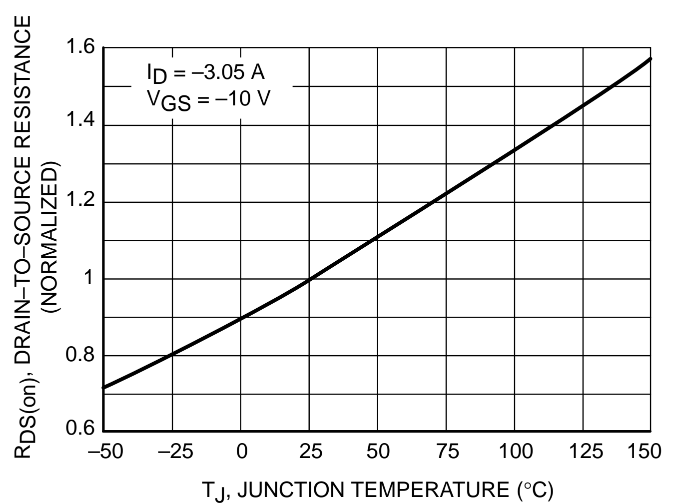



**Figure 6. On Resistance Variation with Temperature**

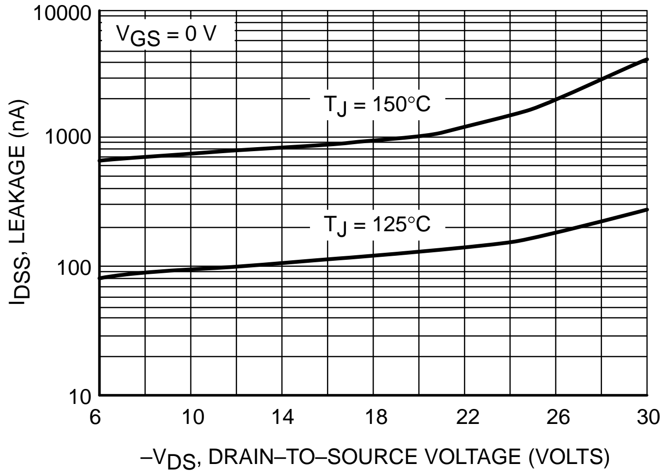



**Figure 7. Drain–to–Source Leakage Current vs. Voltage**

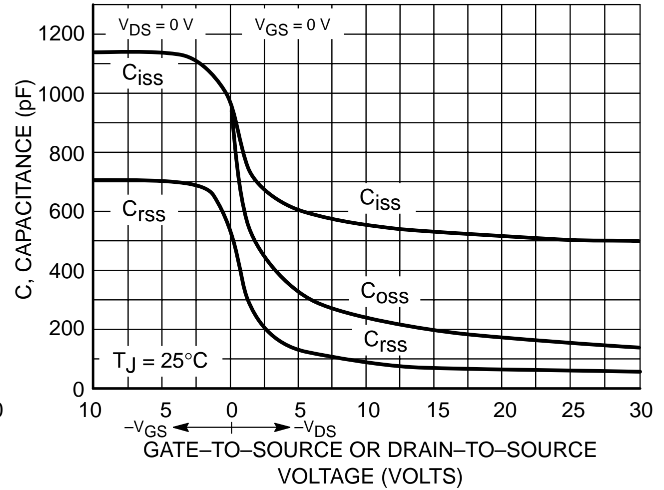



**Figure 8. Capacitance Variation**

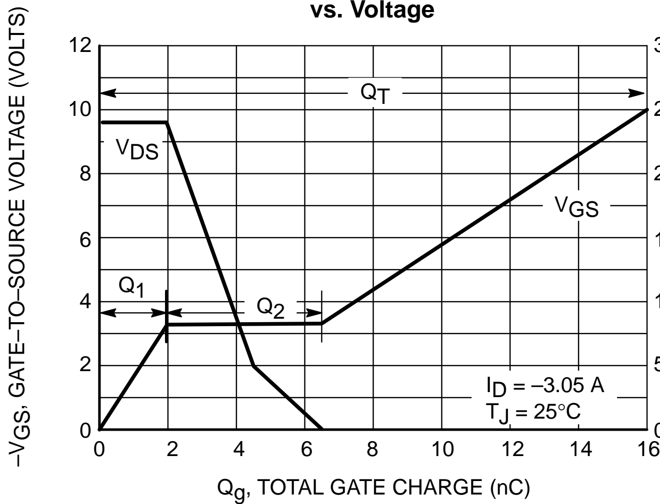



**Figure 9. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

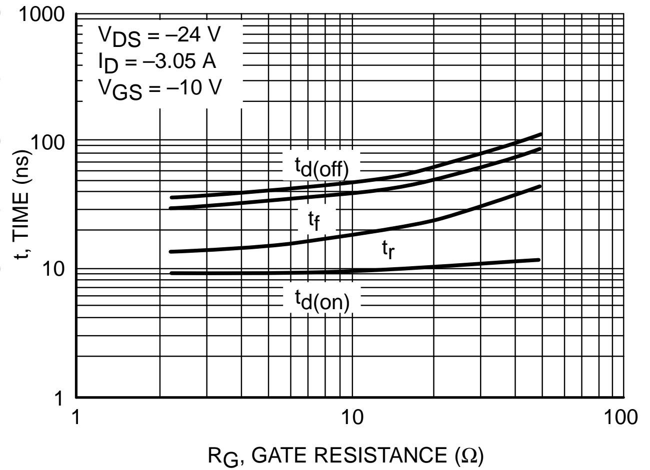



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

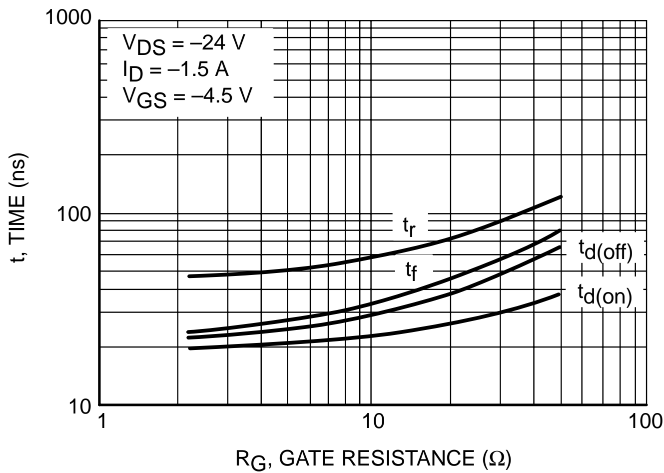



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

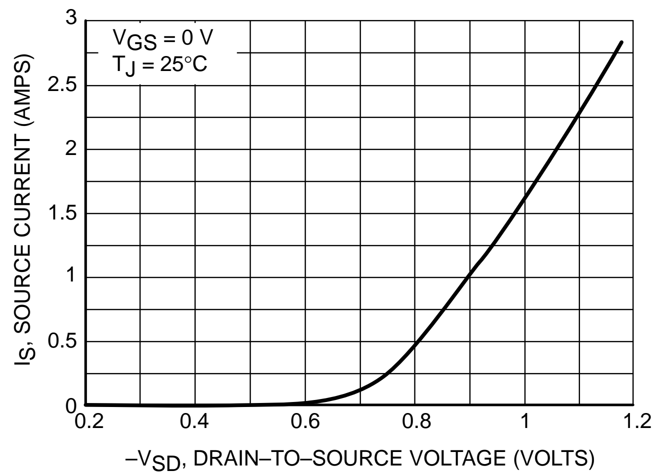



**Figure 12. Diode Forward Voltage vs. Current**

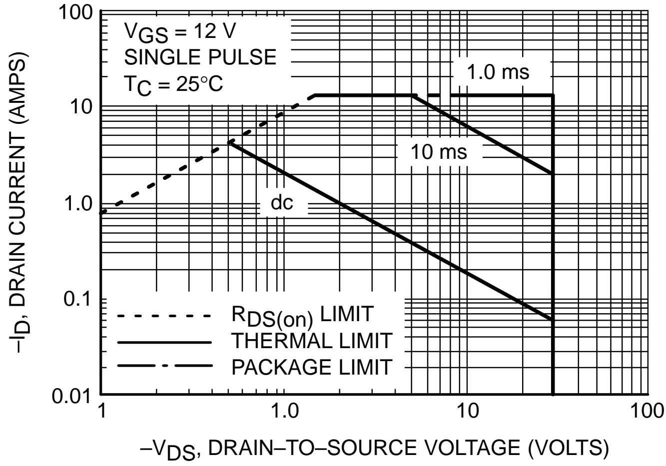



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

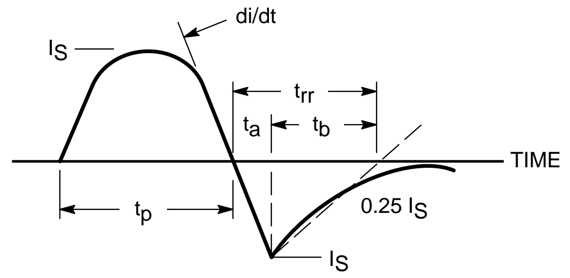



**Figure 14. Diode Reverse Recovery Waveform**

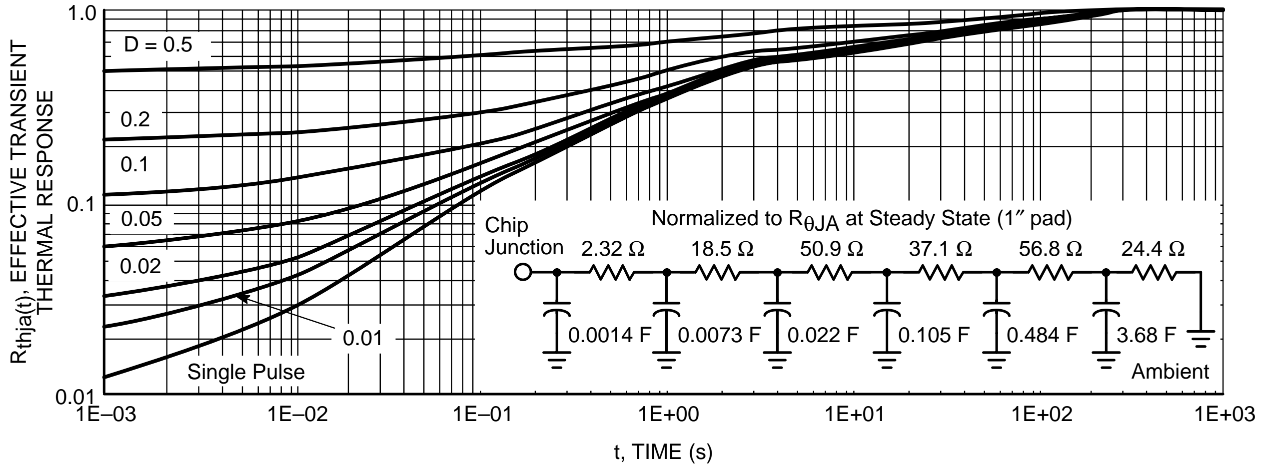
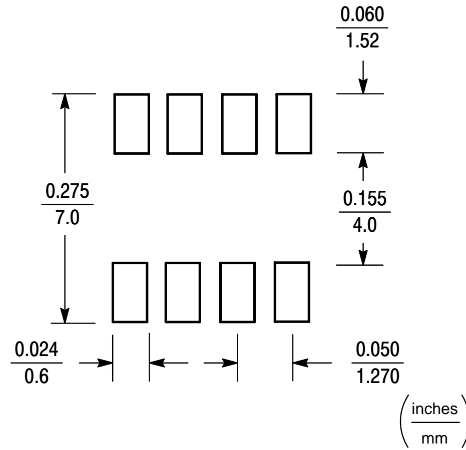



**Figure 15. FET Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

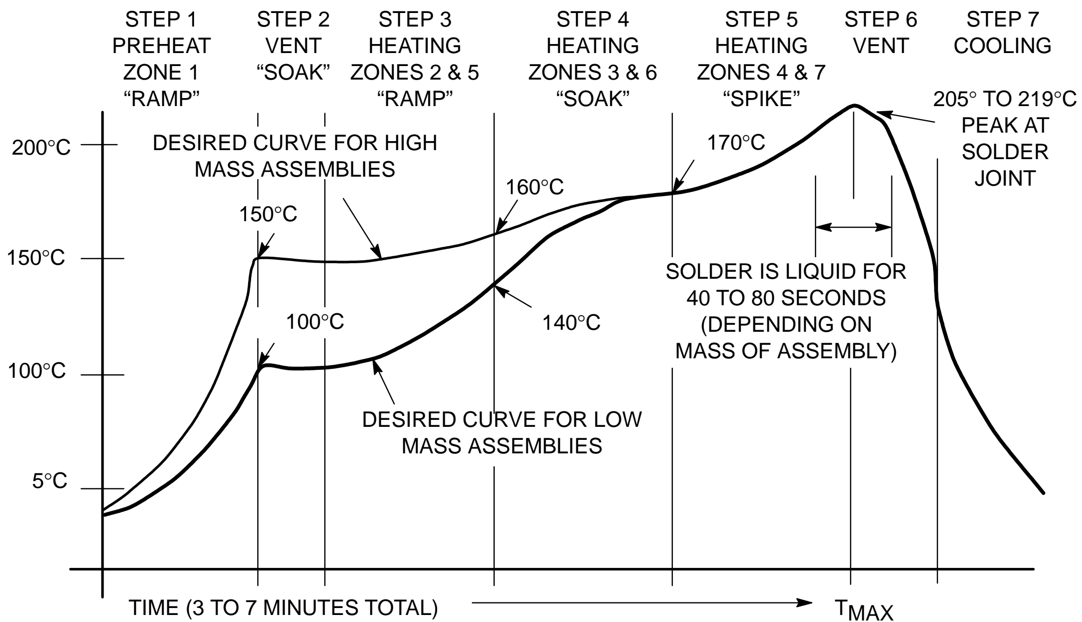



**Figure 16. Typical Solder Heating Profile**

# NTMD6N02R2

**ON Semiconductor™**

**http://onsemi.com**

*Product Preview*

## Power MOSFET 6.0 Amps, 20 Volts

### N–Channel Enhancement Mode Dual SO–8 Package

**Features**

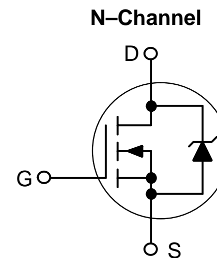
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SO–8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO–8 Mounting Information Provided

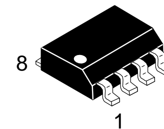
**Applications**

- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, Cellular and Cordless Telephones and PCMCIA Cards

**6.0 AMPERES**
**20 VOLTS**
**35 mΩ @ $V_{GS}$ = 4.5 V**

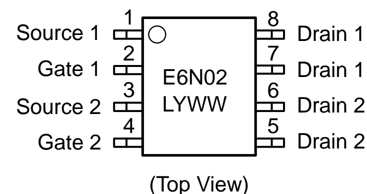
**N–Channel**




**SO–8**
**CASE 751**
**STYLE 11**

**MARKING DIAGRAM & PIN ASSIGNMENT**




(Top View)

E6N02 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | 6.5 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | 5.5 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 20 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 102 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.22 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | 5.07 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | 4.07 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 16 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 172 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.73 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | 3.92 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | 3.14 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 12 | A |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), t < 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR–4 or G–10 PCB, t = steady state.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMD6N02R2 | SO–8 | 2500/Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (continued)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 6.0 Apk, L = 20 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 360 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 19.2 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = +12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | 0.6 | 0.9 | 1.2 | Vdc |
| Temperature Coefficient (Negative) | | | – | –3.0 | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.028 | 0.035 | Ω |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.0 Adc) | | | – | 0.028 | 0.043 | |
| ($V_{GS}$ = 2.7 Vdc, $I_D$ = 2.0 Adc) | | | – | 0.033 | 0.048 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 3.0 Adc) | | | – | 0.035 | 0.049 | |
| Forward Transconductance ($V_{DS}$ = 12 Vdc, $I_D$ = 3.0 Adc) | | $g_{FS}$ | – | 10 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 785 | 1100 | pF |
| Output Capacitance | | $C_{oss}$ | – | 260 | 450 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 75 | 180 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. and 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 16 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 20 | ns |
| Rise Time | | $t_r$ | – | 50 | 90 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 75 | |
| Fall Time | | $t_f$ | – | 80 | 130 | |
| Turn–On Delay Time | ($V_{DD}$ = 16 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 11 | 18 | ns |
| Rise Time | | $t_r$ | – | 35 | 65 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 75 | |
| Fall Time | | $t_f$ | – | 60 | 110 | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 4.5 Vdc, $I_D$ = 6.0 Adc) | $Q_{tot}$ | – | 12 | 20 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.0 | – | |

5. Handling precautions to protect against electrostatic discharge is mandatory
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (continued) (Note 8.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BODY–DRAIN DIODE RATINGS** (Note 9.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>–<br>– | 0.83<br>0.88<br>0.75 | 1.1<br>1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 30 | – | ns |
| | | $t_a$ | – | 15 | – | |
| | | $t_b$ | – | 15 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.02 | – | µC |

8. Handling precautions to protect against electrostatic discharge is mandatory.
9. Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.

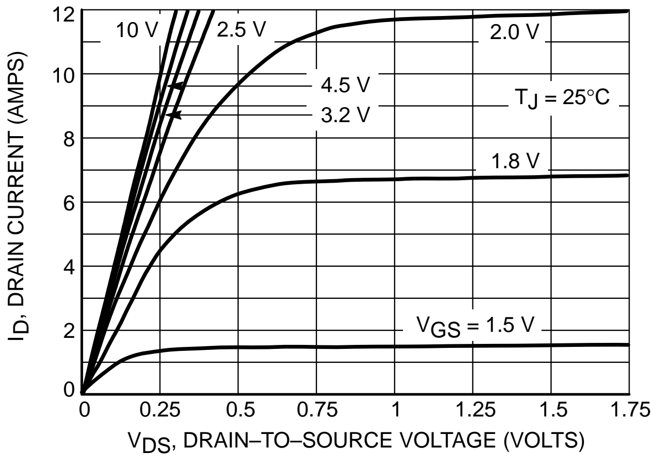



**Figure 1. On–Region Characteristics**

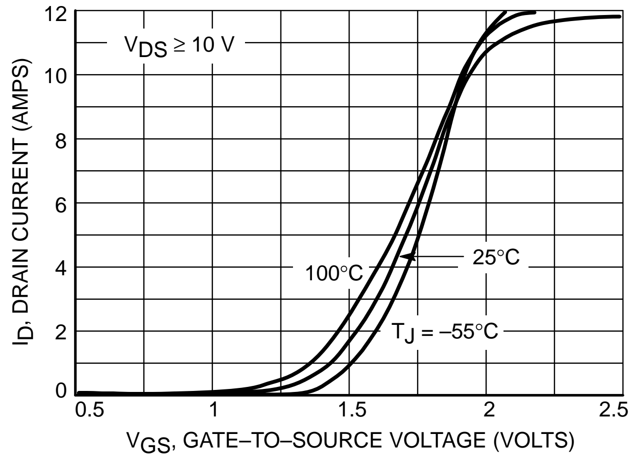



**Figure 2. Transfer Characteristics**

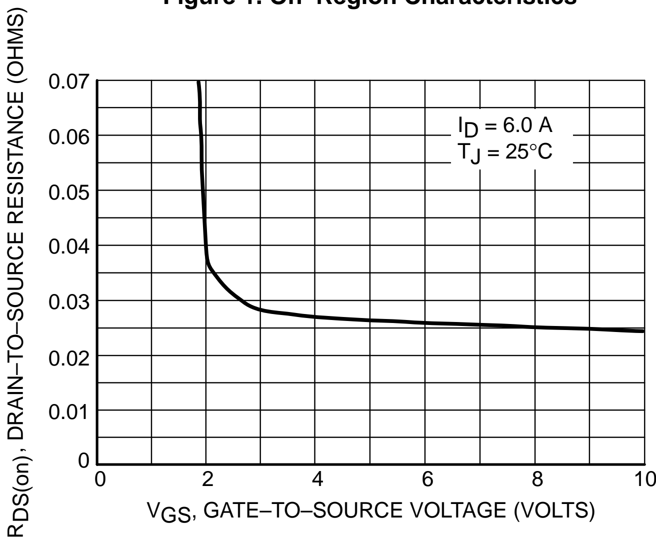



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

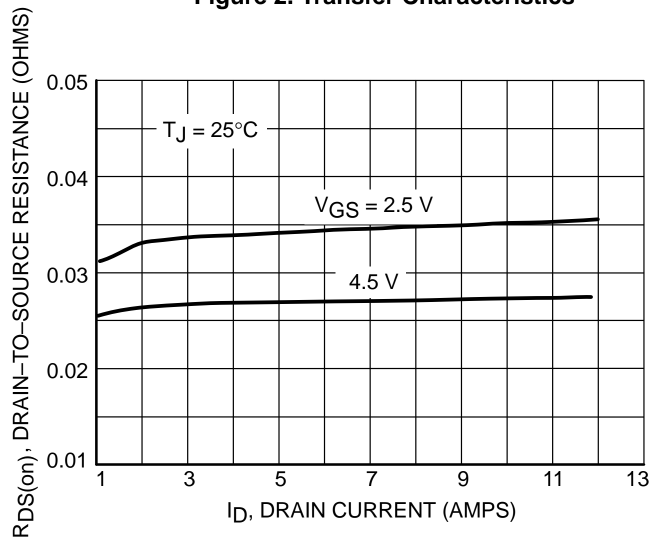



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

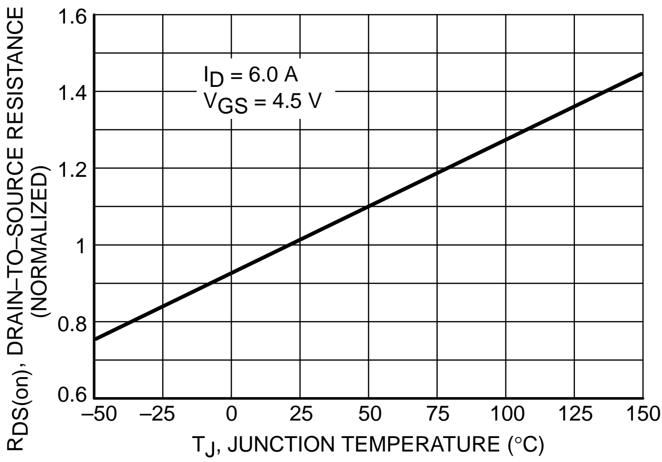



**Figure 5. On–Resistance Variation with Temperature**

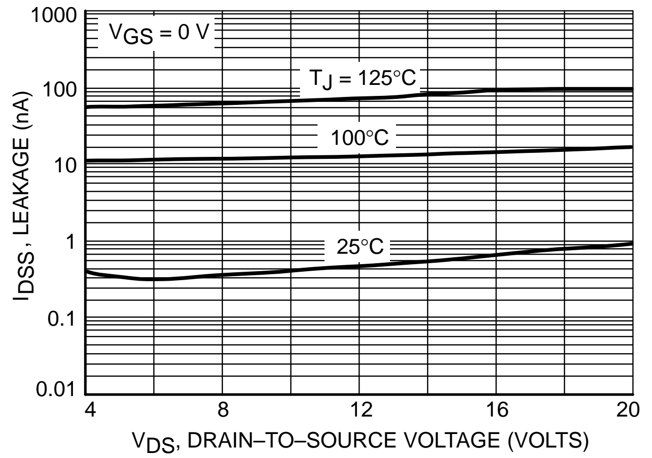



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

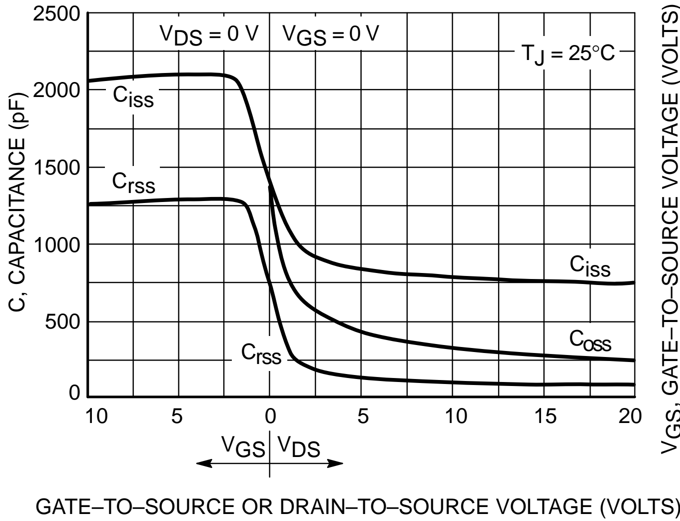



**Figure 7. Capacitance Variation**

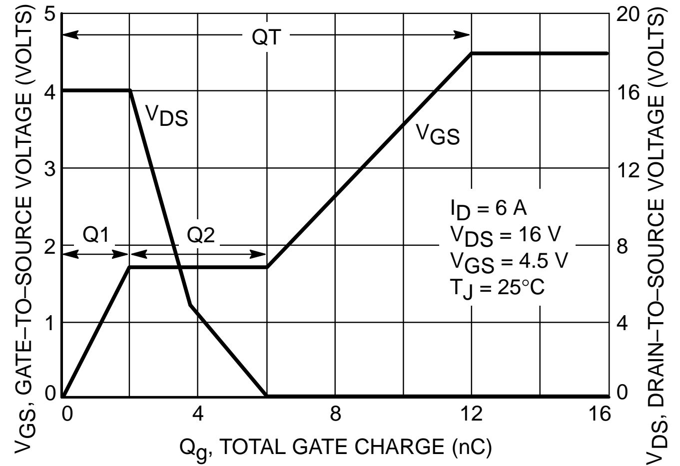



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

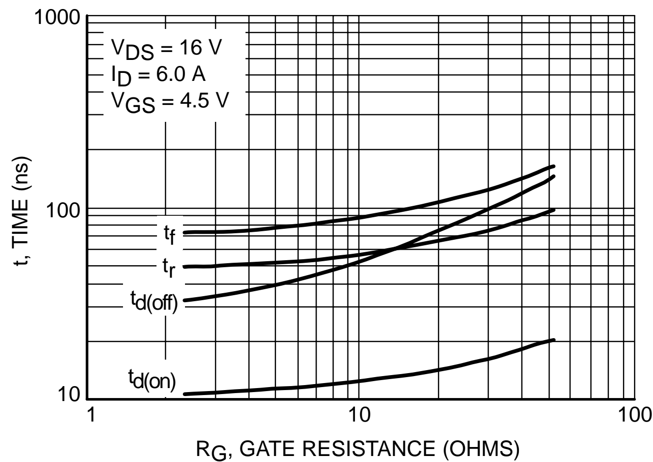



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

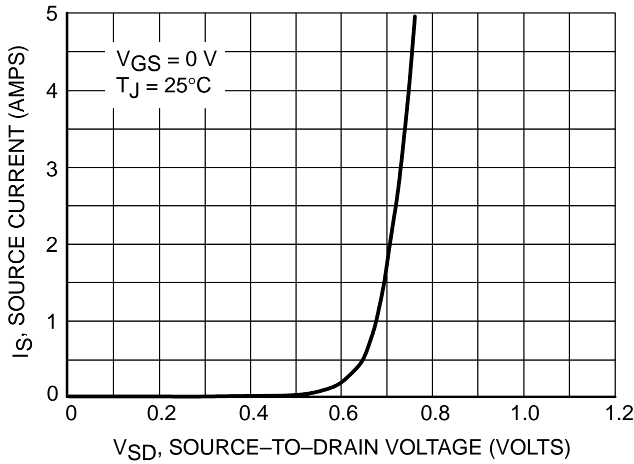



**Figure 10. Diode Forward Voltage versus Current**

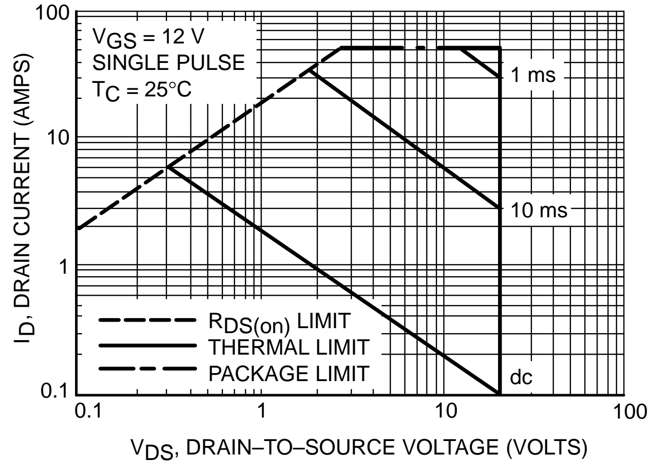



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

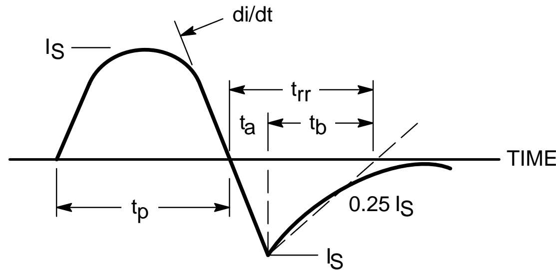



**Figure 12. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

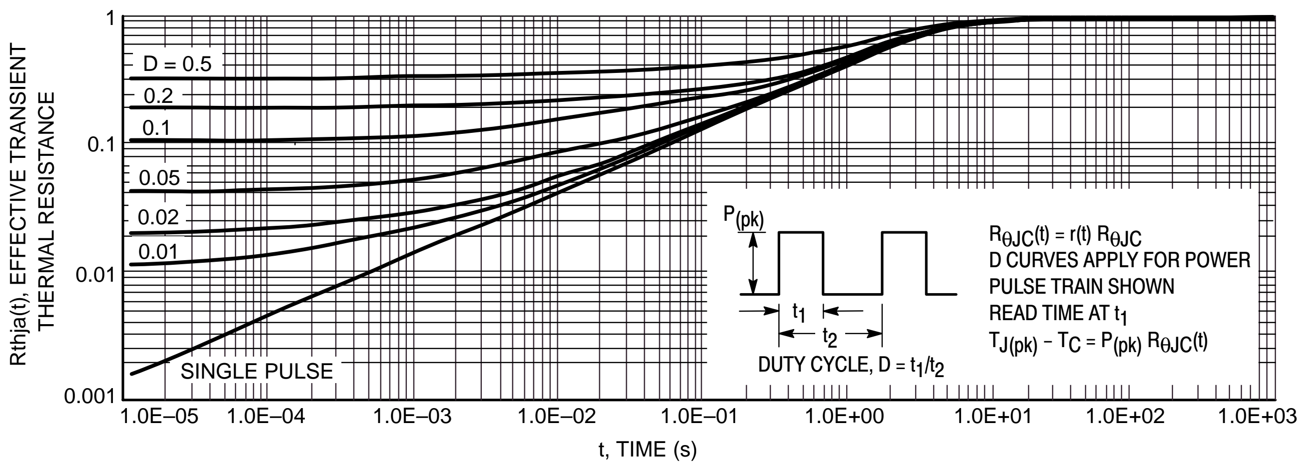
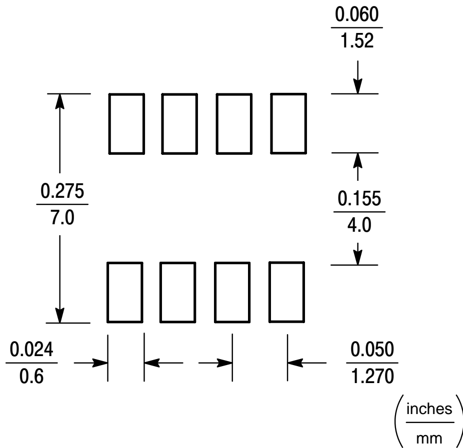



**Figure 13. Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

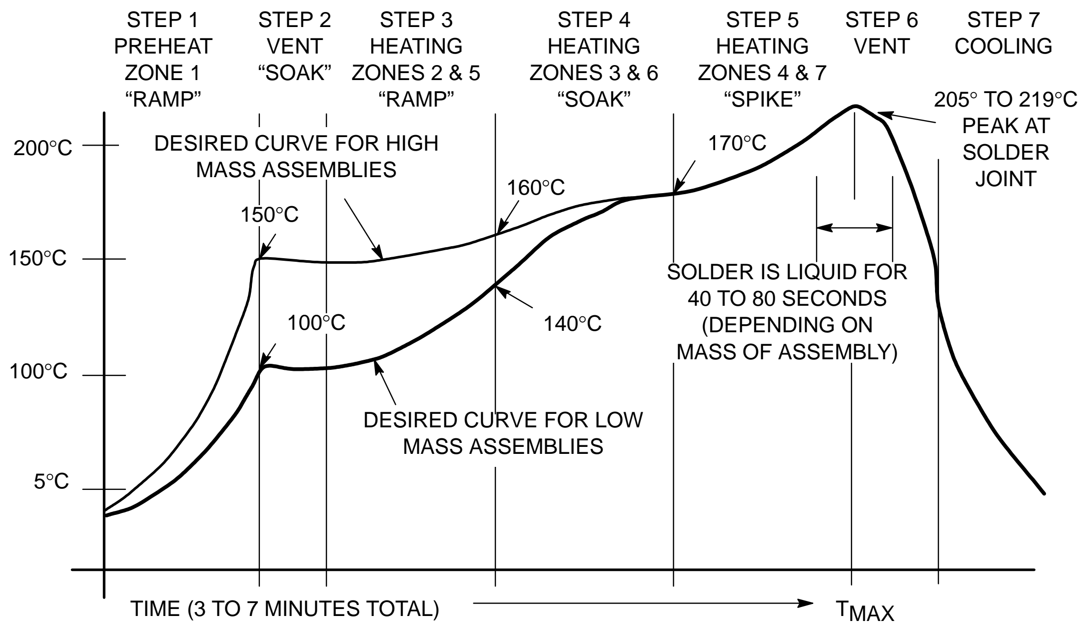



**Figure 14. Typical Solder Heating Profile**

# NTMD6P02R2

**Preferred Device**

# Power MOSFET 6 Amps, 20 Volts

## P–Channel SO–8, Dual

**ON Semiconductor™**

**http://onsemi.com**

### Features

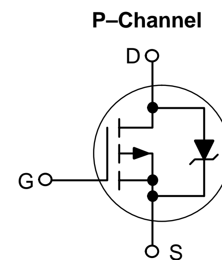
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual SO–8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO–8 Mounting Information Provided

### Applications

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

**6 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 33 mΩ**

**P–Channel**

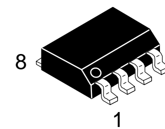



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

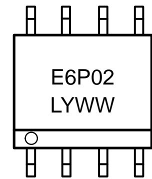
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –7.8 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –5.7 | A |
| Maximum Operating Power Dissipation | $P_D$ | 0.5 | W |
| Maximum Operating Drain Current | $I_D$ | –3.89 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –40 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 98 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.28 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –6.2 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –4.6 | A |
| Maximum Operating Power Dissipation | $P_D$ | 0.3 | W |
| Maximum Operating Drain Current | $I_D$ | –3.01 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –35 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 166 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.75 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –4.8 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –3.5 | A |
| Maximum Operating Power Dissipation | $P_D$ | 0.2 | W |
| Maximum Operating Drain Current | $I_D$ | –2.48 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –30 | A |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), t = 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR–4 or G–10 PCB, t = steady state.
4. Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

**MARKING DIAGRAM**

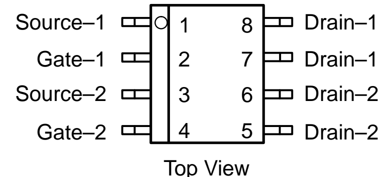



**SO–8, Dual**
**CASE 751**
**STYLE 11**




E6P02 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMD6P02R2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (continued)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –5.0 Vdc, Peak $I_L$ = –5.0 Apk, L = 40 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc) | $V_{(BR)DSS}$ | –20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | – | –11.6 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | $I_{DSS}$ | – | – | –1.0 | μAdc |
| ($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | | – | – | –5.0 | |
| Gate–Body Leakage Current ($V_{GS}$ = –12 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +12 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | $V_{GS(th)}$ | –0.6 | –0.88 | –1.20 | Vdc |
| Temperature Coefficient (Negative) | | – | 2.6 | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –6.2 Adc) | $R_{DS(on)}$ | – | 0.027 | 0.033 | Ω |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –5.0 Adc) | | – | 0.038 | 0.050 | |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –3.1 Adc) | | – | 0.038 | – | |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –6.2 Adc) | $g_{FS}$ | – | 15 | – | Mhos |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1380 | 1700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 515 | 775 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 250 | 450 | |

**SWITCHING CHARACTERISTICS** (Notes 6. and 7.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | 25 | ns |
| Rise Time | | $t_r$ | – | 20 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 85 | 125 | |
| Fall Time | | $t_f$ | – | 50 | 110 | |
| Turn–On Delay Time | ($V_{DD}$ = –16 Vdc, $I_D$ = –6.2 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 17 | – | ns |
| Rise Time | | $t_r$ | – | 65 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | – | |
| Fall Time | | $t_f$ | – | 80 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –6.2 Adc) | $Q_{tot}$ | – | 20 | 35 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 4.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 8.0 | – | |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (continued) (Note 8.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **BODY–DRAIN DIODE RATINGS** (Note 9..) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.80<br>–0.65 | –1.2<br>– | Vdc |
| Diode Forward On–Voltage | ($I_S$ = –6.2 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –6.2 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.95<br>–0.80 | –<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 50 | 80 | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_r$ | – | 30 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.04 | – | µC |

8. Handling precautions to protect against electrostatic discharge is mandatory.
9. Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.

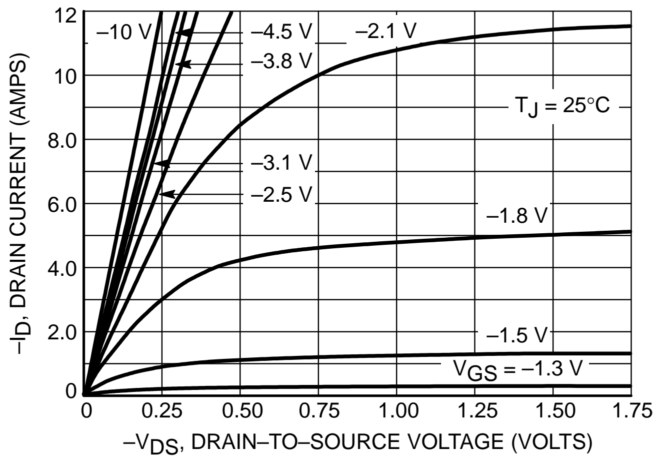



**Figure 1. On–Region Characteristics**

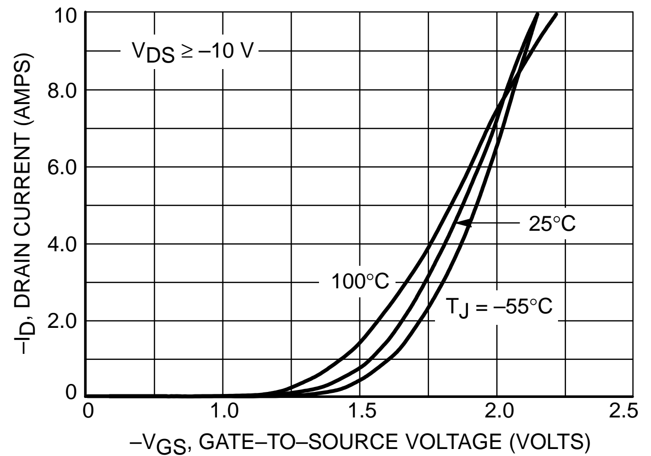



**Figure 2. Transfer Characteristics**

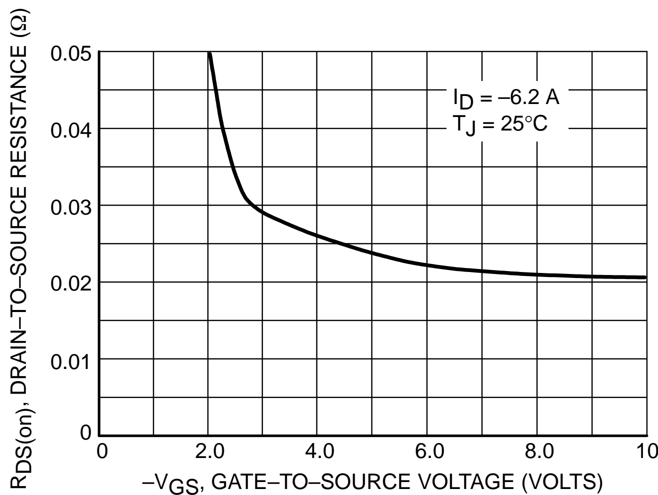



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

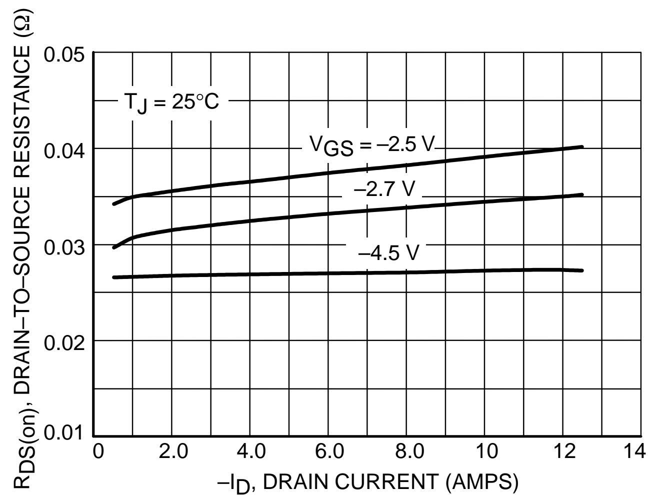



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

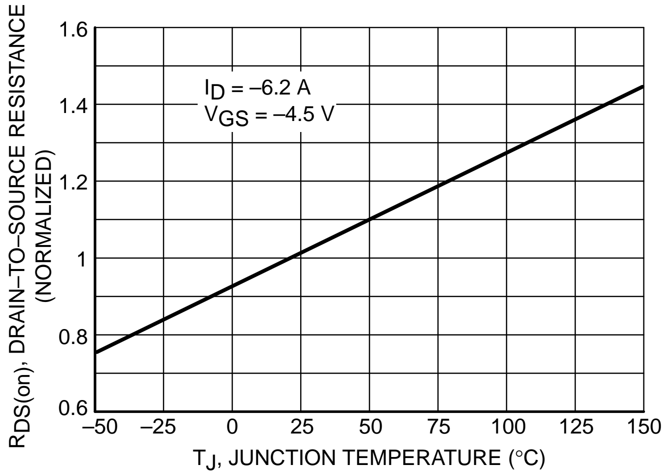



**Figure 5. On–Resistance Variation with Temperature**

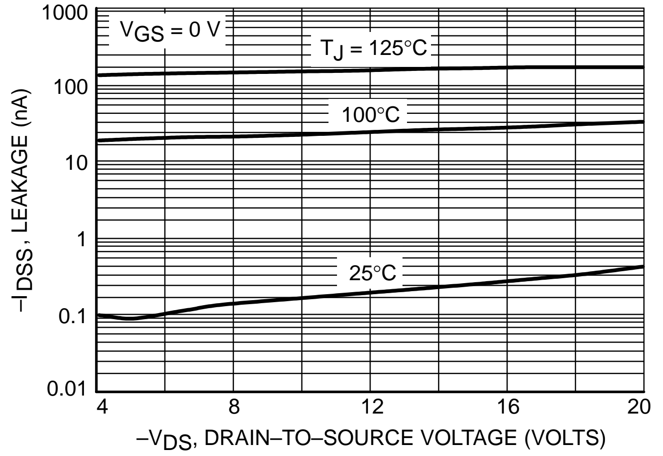



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

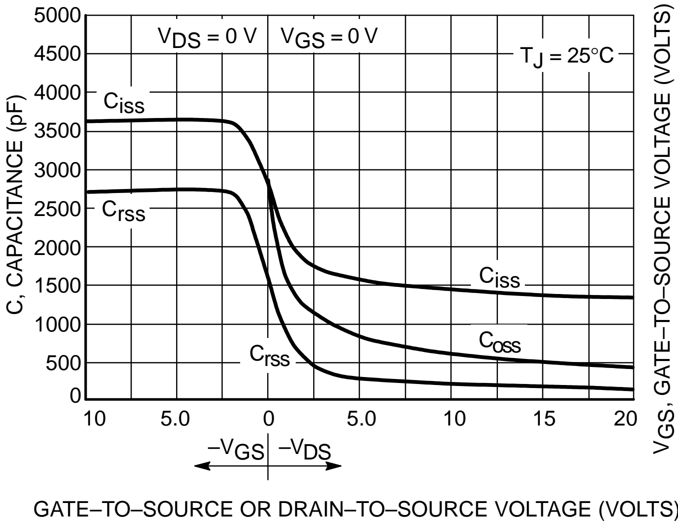



**Figure 7. Capacitance Variation**

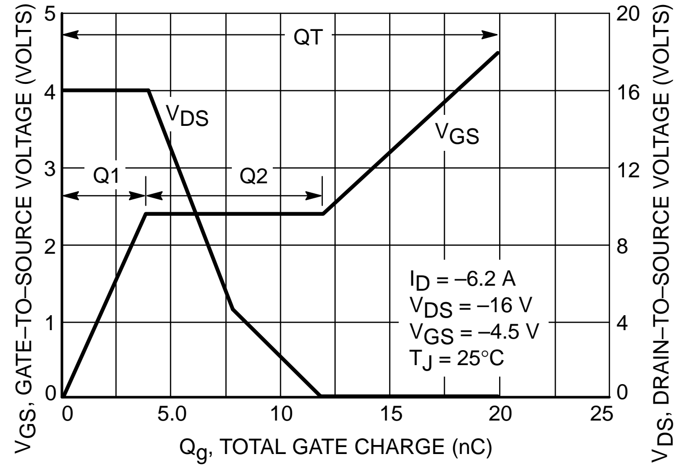



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

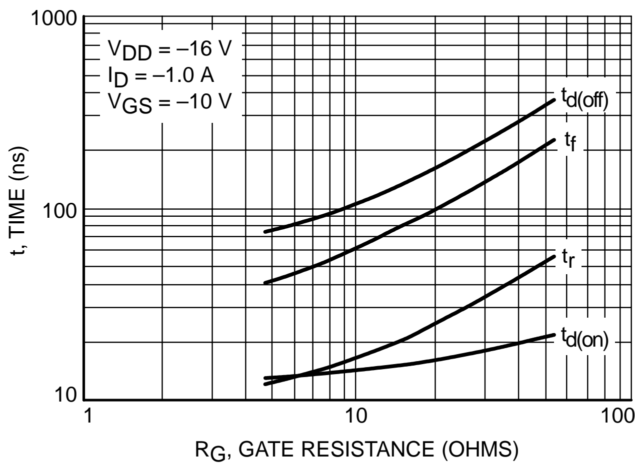



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

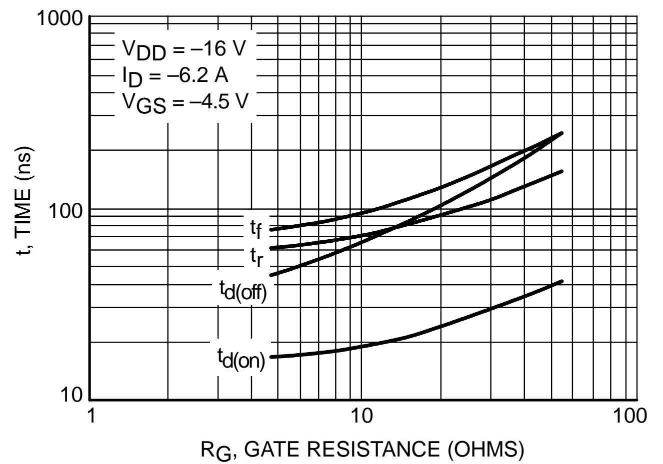



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

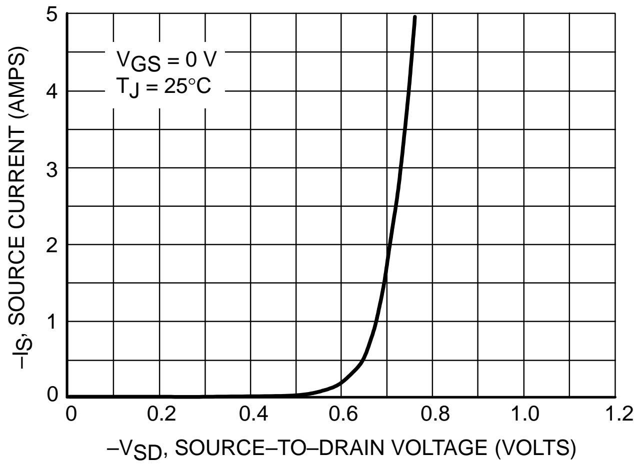



**Figure 11. Diode Forward Voltage versus Current**

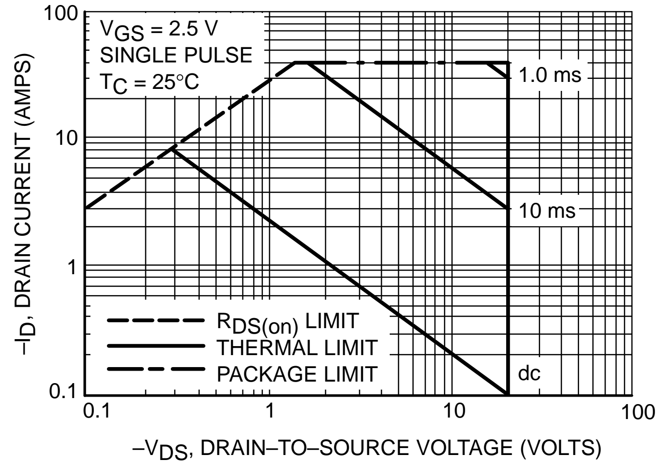



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

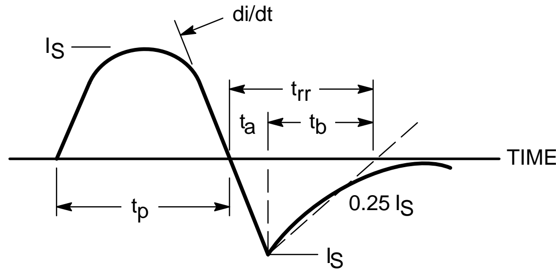



**Figure 13. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

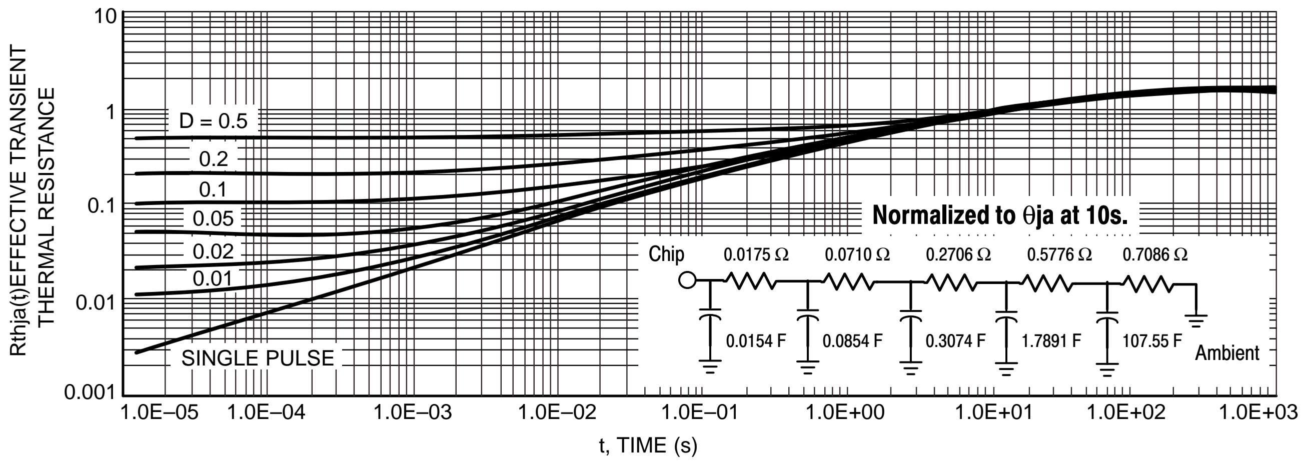
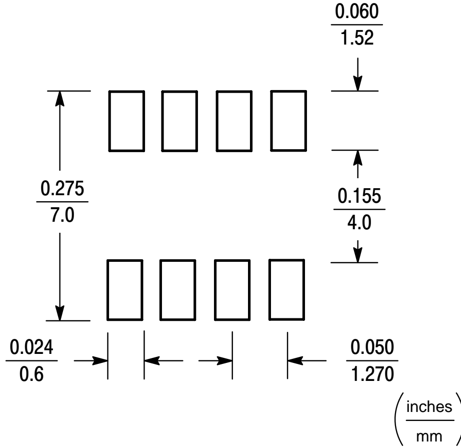



**Figure 14. Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

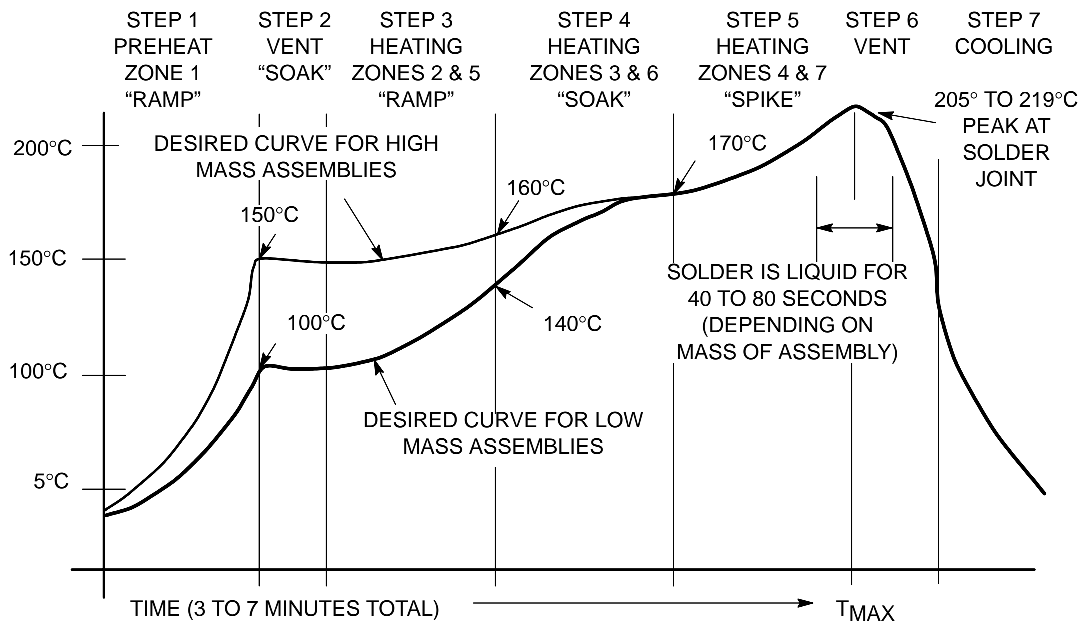



**Figure 15. Typical Solder Heating Profile**

# NTMD7C02

# Power MOSFET 9.5 Amps, 20 Volts (N-Ch) 4 Amps, 20 Volts (P-Ch)

## Complementary SO–8

**ON Semiconductor™**

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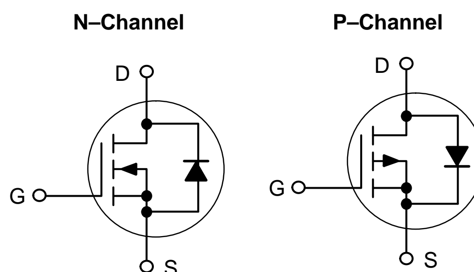
**9.5 AMPERES, 20 VOLTS**
**$R_{DS(on)}$ = 24 mΩ (N–Channel)**
**4 AMPERES, 20 VOLTS**
**$R_{DS(on)}$ = 108 mΩ (P–Channel)**

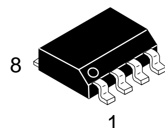



**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

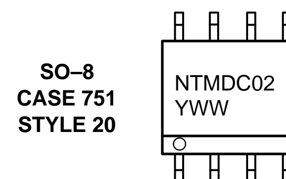
| Rating | Symbol | N | P | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | –20 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ±20 | ±12 | Vdc |
| Drain Current – Continuous (Note 1.) | $I_D$ | 7.0 | 4.5 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |
| Thermal Resistance (Note 2.) – Junction–to–Ambient | $R_{\theta JA}$ | 50 | 50 | °C/W |

1. Mounted on 1″ square FR–4 board.
2. Mounted on 1″ square FR–4 board, t ≤ 10 seconds.

**MARKING DIAGRAM**

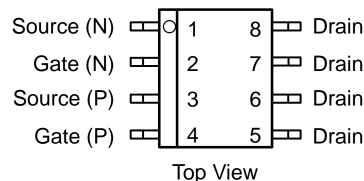



**SO–8**
**CASE 751**
**STYLE 20**




NTMDC02 = Device Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMD7C02R2 | SO–8 | 2500 Units/Rail |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Test Conditions | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | | (N) | – | – | 1.0 | |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | | (P) | – | – | 1.0 | |
| Gate–Body Leakage Current | | $I_{GSS}$ | | | | | nAdc |
| ($V_{GS}$ = 20 Vdc, $V_{DS}$ = 0 Vdc) | | | (N) | – | – | 100 | |
| ($V_{GS}$ = 12 Vdc, $V_{DS}$ = 0 Vdc) | | | (P) | – | – | 100 | |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | | |
| Gate Threshold Voltage | | $V_{GS(th)}$ | | | | | Vdc |
| ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | | (N) | 1.0 | – | – | |
| ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | | (P) | 0.6 | – | – | |
| Static Drain–to–Source On–State Resistance | | $R_{DS(on)}$ | | | | | mOhms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 7.0 Adc) | | | (N) | – | 19 | 24 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.5 Adc) | | | (P) | – | 63 | 74 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 3.5 Adc) | | | (P) | – | 94 | 108 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 1470<br>500 | 1750<br>570 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 660<br>190 | 770<br>220 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 189<br>58 | 260<br>80 | |
| **SWITCHING CHARACTERISTICS** | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 22<br>12 | 30<br>20 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 38<br>22 | 50<br>30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 38<br>36 | 50<br>50 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 31<br>24 | 45<br>35 | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 4.5 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 16<br>7.0 | 20<br>9.0 | nC |
| | | $Q_{gs}$ | (N)<br>(P) | –<br>– | 4.5<br>0.6 | 6.0<br>1.0 | |
| | | $Q_{gd}$ | (N)<br>(P) | –<br>– | 7.0<br>1.7 | 9.0<br>2.5 | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | | |
| Forward On–Voltage (Note 3.) | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | $V_{SD}$ | (N)<br>(P) | –<br>– | 730<br>840 | 760<br>870 | Vdc |
| Reverse Recovery Time | ($I_F$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, di/dt = 100 Aμs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 104<br>24 | 160<br>36 | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 18<br>13.5 | 28<br>22 | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 85<br>11 | 140<br>20 | |
| Reverse Recovery Stored Charge | | $Q_{rr}$ | (N)<br>(P) | –<br>– | 0.082<br>0.018 | 0.12<br>0.028 | μC |

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle= 2%.

# NTMS10P02R2

**ON Semiconductor™**

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*Product Preview*

## Power MOSFET -10 Amps, -20 Volts

### P–Channel Enhancement–Mode Single SO–8 Package

**Features**

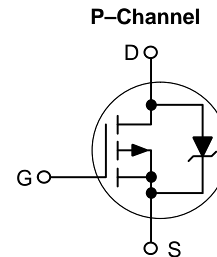
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature SO–8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- SO–8 Mounting Information Provided

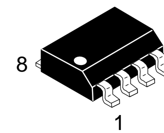
**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

**–10 AMPERES**
**–20 VOLTS**
**14 mΩ @ $V_{GS}$ = –4.5 V**

**P–Channel**




**SO–8**
**CASE 751**
**STYLE 12**

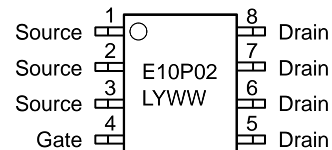
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Vdc |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.5 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –10 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –8.0 | A |
| Maximum Operating Power Dissipation | $P_D$ | 0.6 | W |
| Maximum Operating Drain Current | $I_D$ | –5.5 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –50 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 80 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.6 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –8.8 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –6.4 | A |
| Maximum Operating Power Dissipation | $P_D$ | 0.4 | W |
| Maximum Operating Drain Current | $I_D$ | –4.5 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –44 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = 5.0 Apk, L = 40 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. Cu 0.06″ thick single sided), t = 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. Cu 0.06″ thick single sided), t = steady state.
3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**MARKING DIAGRAM & PIN ASSIGNMENT**




Top View

E10P02 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMS10P02R2 | SO–8 | 2500/Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | –20<br>– | –<br>–12.1 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–5.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | –0.6<br>– | –0.88<br>2.8 | –1.20<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –10 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –8.8 Adc) | | $R_{DS(on)}$ | –<br>– | 0.012<br>0.017 | 0.014<br>0.020 | Ω |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –10 Adc) | | $g_{FS}$ | – | 30 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3100 | 3640 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1100 | 1670 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 475 | 1010 | |
| **SWITCHING CHARACTERISTICS** (Notes 5. & 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 25 | 35 | ns |
| Rise Time | | $t_r$ | – | 40 | 65 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 110 | 190 | |
| Fall Time | | $t_f$ | – | 110 | 190 | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –10 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 25 | – | ns |
| Rise Time | | $t_r$ | – | 100 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 100 | – | |
| Fall Time | | $t_f$ | – | 125 | – | |
| Total Gate Charge | ($V_{DS}$ = –10 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –10 Adc) | $Q_{tot}$ | – | 48 | 70 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 6.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 17 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 5.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –2.1 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –2.1 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.72<br>–0.60 | –1.2<br>– | Vdc |
| Diode Forward On–Voltage | ($I_S$ = –10 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.90<br>–0.75 | –<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –2.1 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 65 | 100 | ns |
| | | $t_a$ | – | 25 | – | |
| | | $t_b$ | – | 40 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.075 | – | μC |

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

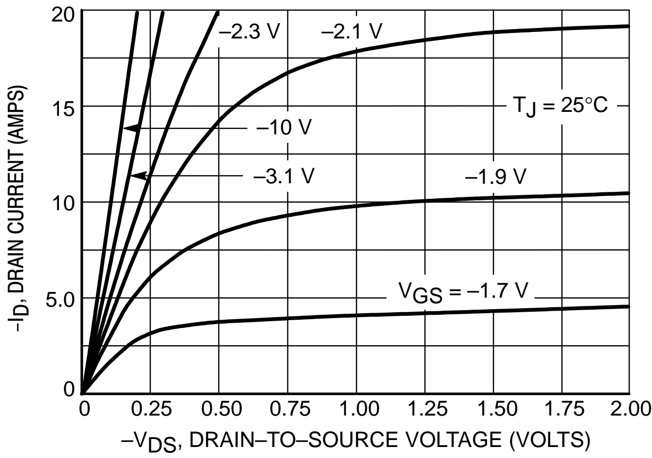



**Figure 1. On–Region Characteristics**

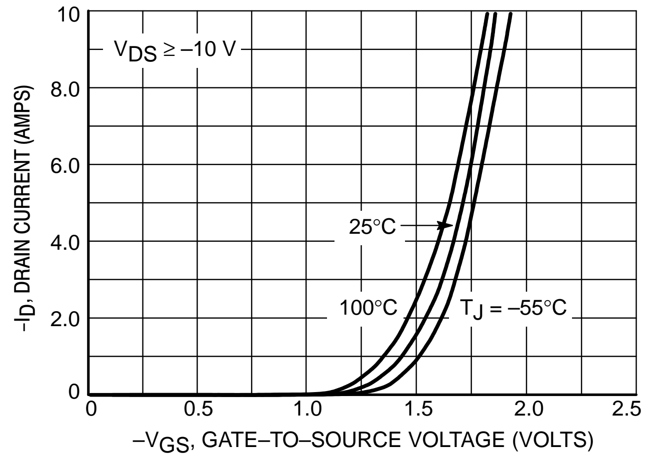



**Figure 2. Transfer Characteristics**

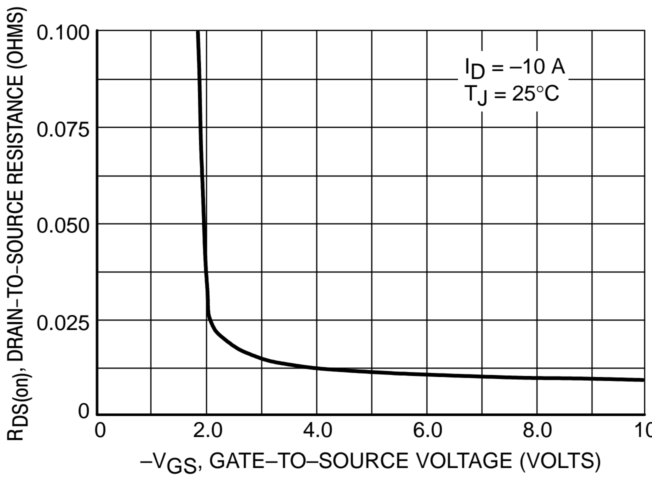



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

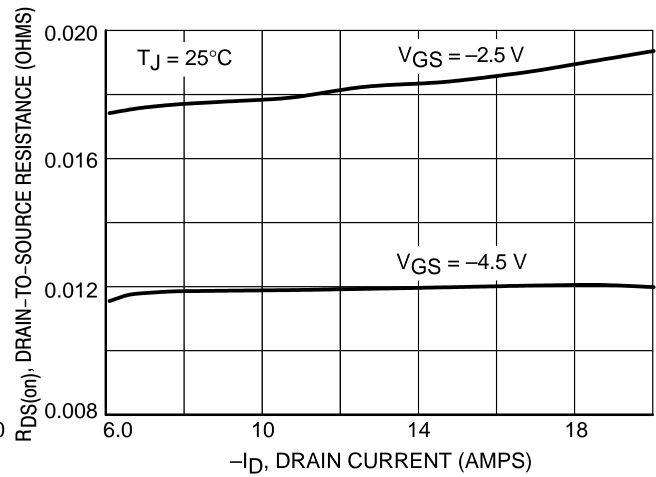



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

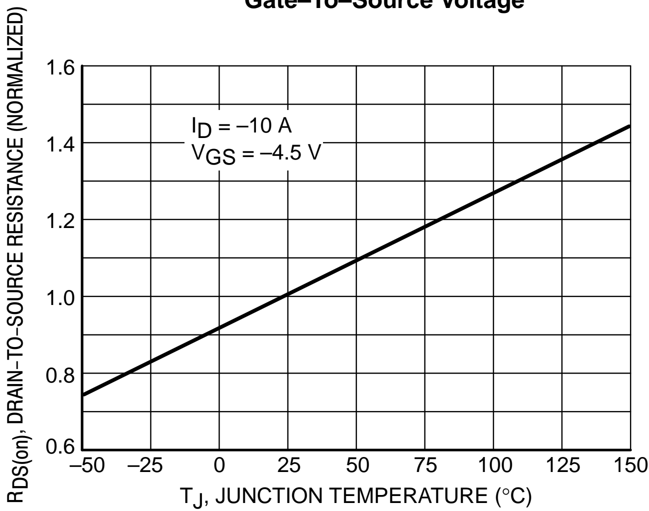



**Figure 5. On–Resistance Variation with Temperature**

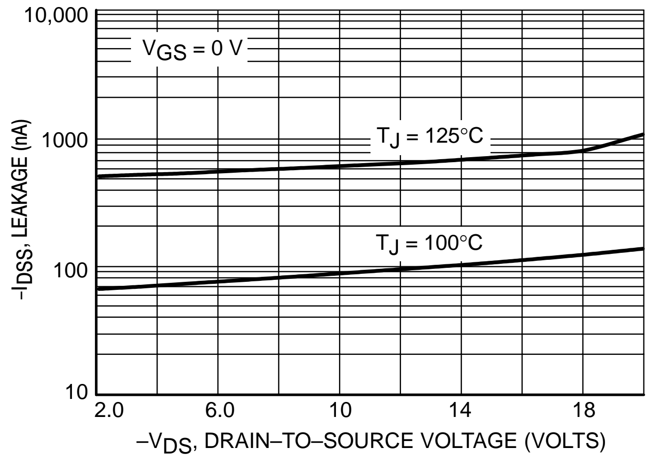



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

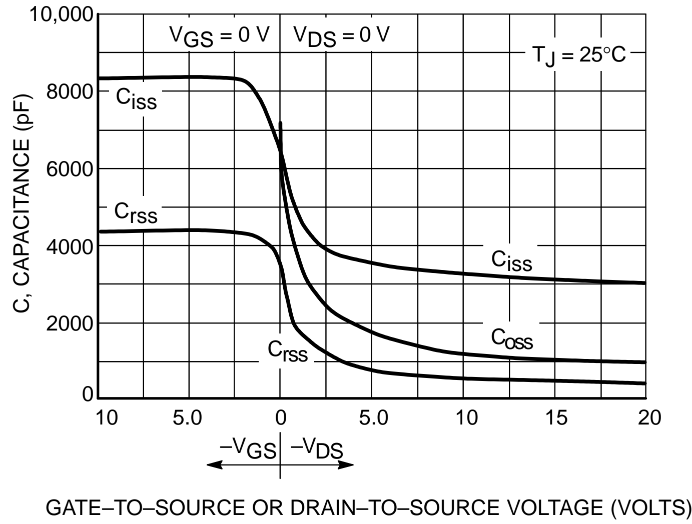



**Figure 7. Capacitance Variation**

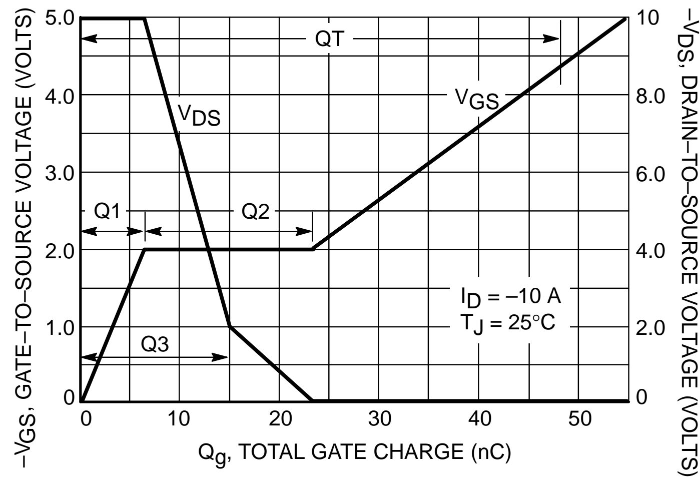



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

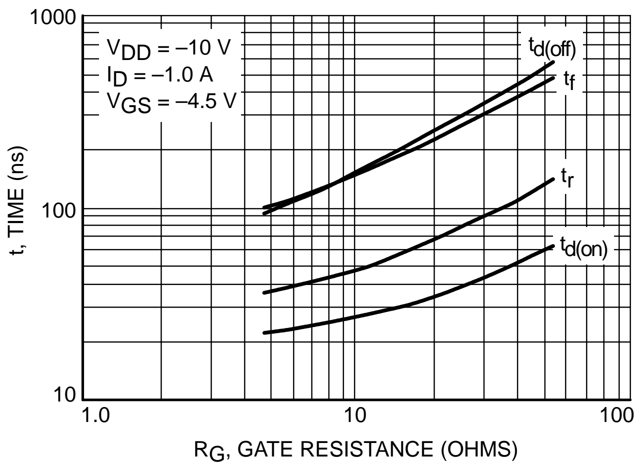



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

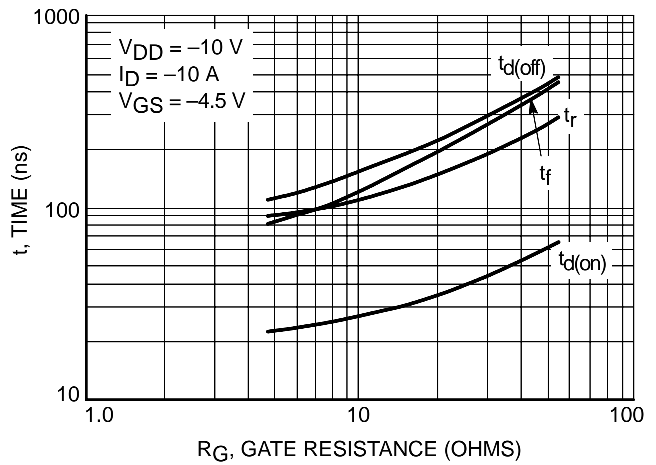



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

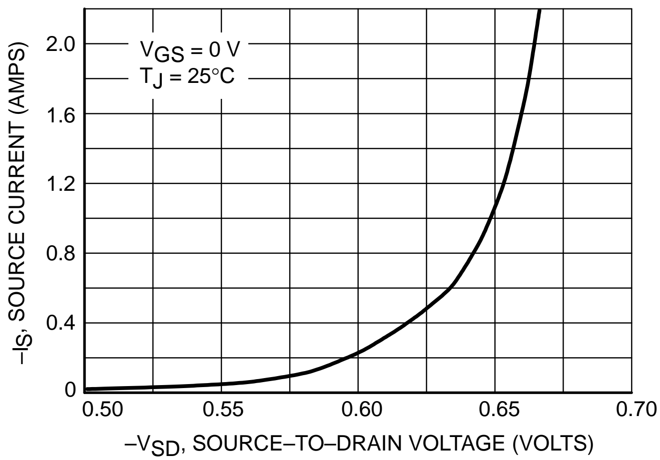



**Figure 11. Diode Forward Voltage versus Current**

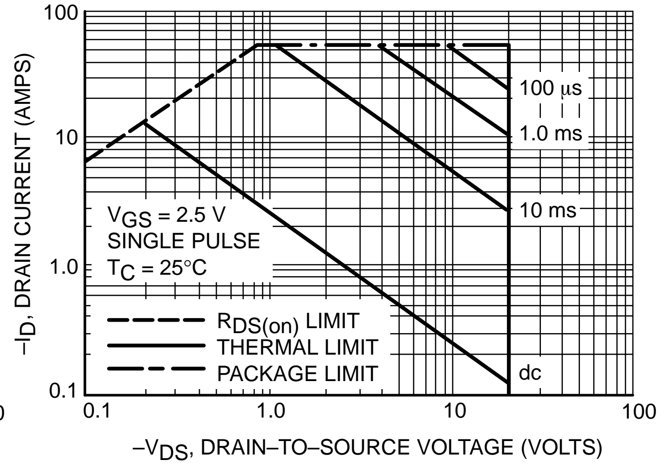



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

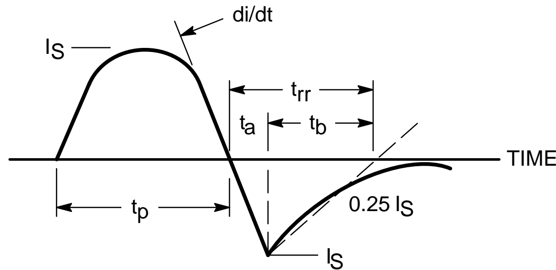



**Figure 13. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

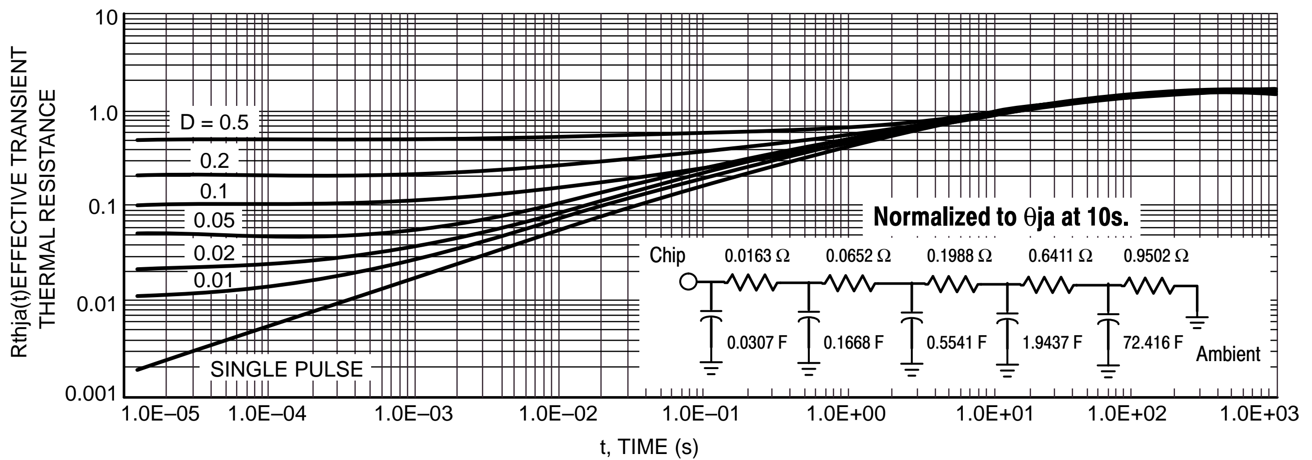
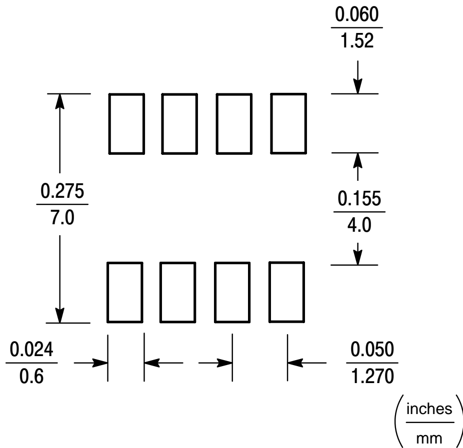



**Figure 14. Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

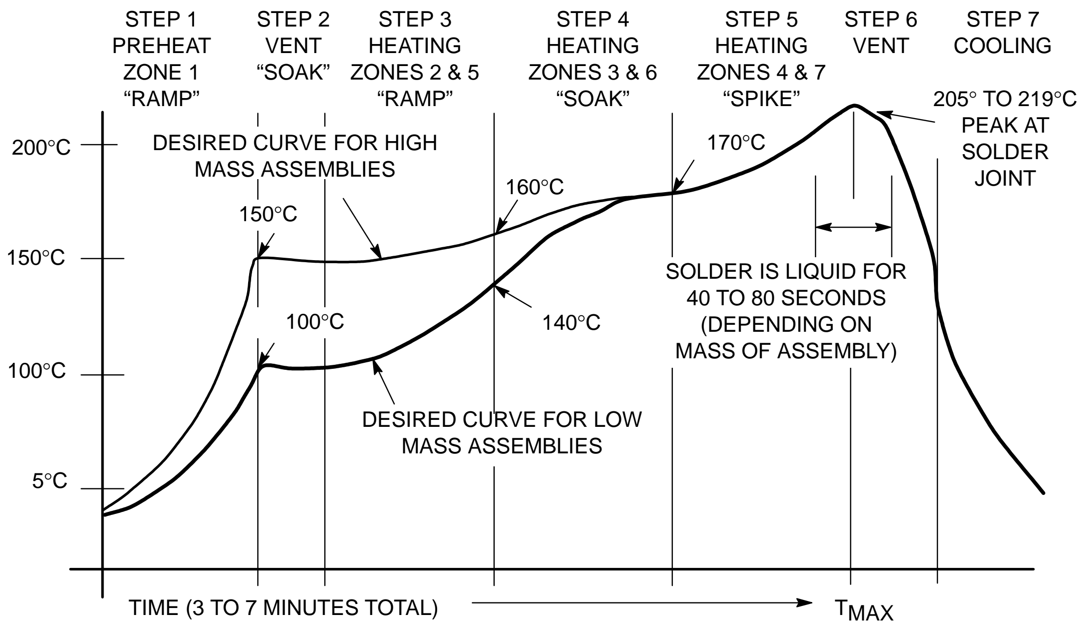



**Figure 15. Typical Solder Heating Profile**

# NTMS3P03R2

*Product Preview*

# Power MOSFET -3.05 Amps, -30 Volts

## P–Channel SO–8

**ON Semiconductor™**

**http://onsemi.com**

**–3.05 AMPERES**
**–30 VOLTS**
**0.085 Ω @ $V_{GS}$ = –10 V**

### Features

- High Efficiency Components in a Single SO–8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for the SO–8 Package is Provided

### Applications

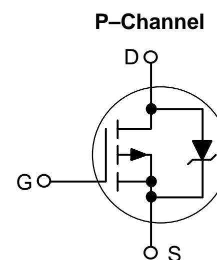
- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

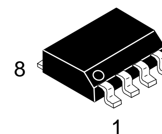
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –30 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 171 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.73 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –2.34 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –1.87 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –8.0 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 100 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.25 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –3.05 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –2.44 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –12 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current @ 25°C | $I_D$ | –3.86 | A |
| Continuous Drain Current @ 70°C | $I_D$ | –3.1 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –15 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –30 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –7.5 Apk, L = 5 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 140 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, t = Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

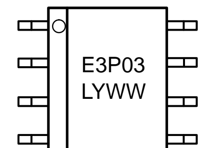
P–Channel




**MARKING DIAGRAM**

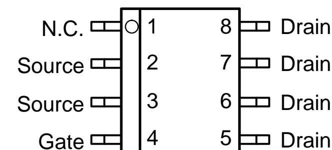



**SO–8**
**CASE 751**
**STYLE 13**




E3P03 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMS3P03R2 | SO–8 | 2500/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc) | | $V_{(BR)DSS}$ | –30 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | –30 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = –30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –1.0 | μAdc |
| ($V_{DS}$ = –30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | –10 | |
| Gate–Body Leakage Current ($V_{GS}$ = –20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –1.0 | –1.7 | –2.5 | Vdc |
| Temperature Coefficient (Negative) | | | – | 3.6 | – | |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc) | | $R_{DS(on)}$ | – | 0.063 | 0.085 | Ω |
| ($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.5 Adc) | | | – | 0.090 | 0.115 | |
| Forward Transconductance ($V_{DS}$ = –15 Vdc, $I_D$ = –3.05 Adc) | | $g_{FS}$ | – | 5.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 520 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 170 | 325 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 70 | 135 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. & 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –3.05 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 22 | ns |
| Rise Time | | $t_r$ | – | 16 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 80 | |
| Fall Time | | $t_f$ | – | 45 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –1.5 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 42 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc) | $Q_{tot}$ | – | 16 | 25 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.5 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 V) | $V_{SD}$ | – | –0.96 | –1.25 | Vdc |
| | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 V, $T_J$ = 125°C) | | – | –0.78 | – | |
| Reverse Recovery Time | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 34 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

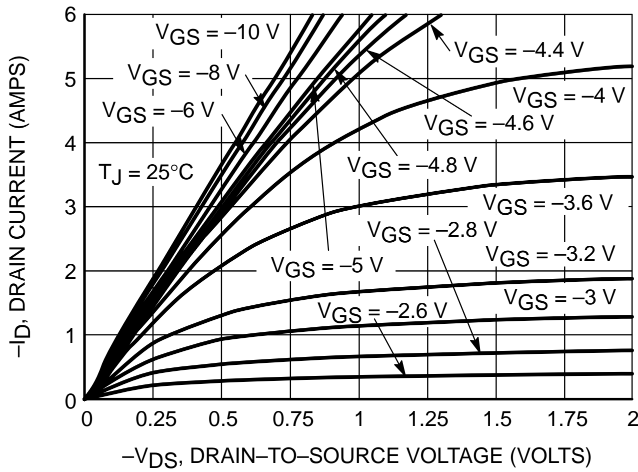



**Figure 1. On–Region Characteristics**

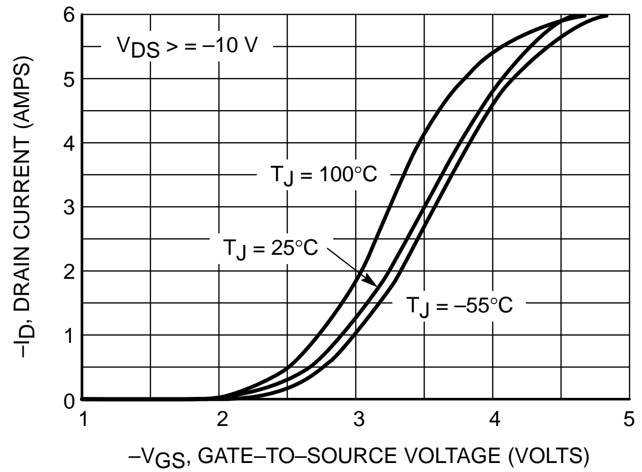



**Figure 2. Transfer Characteristics**

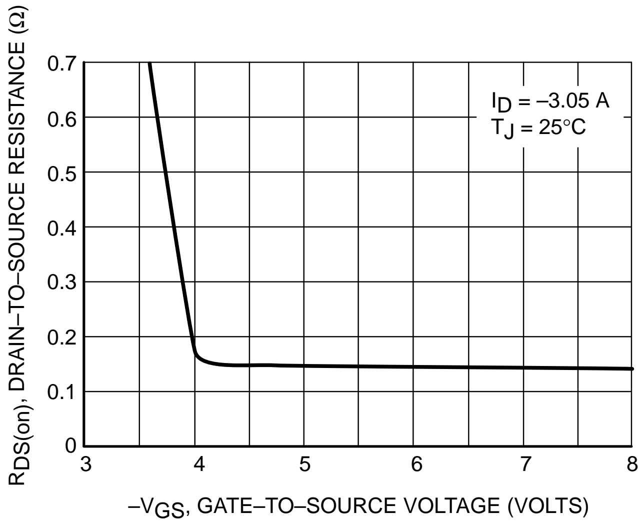



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

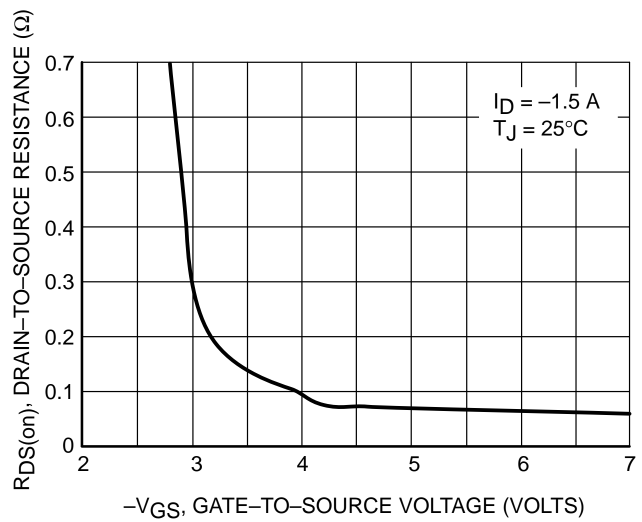



**Figure 4. On–Resistance vs. Gate–to–Source Voltage**

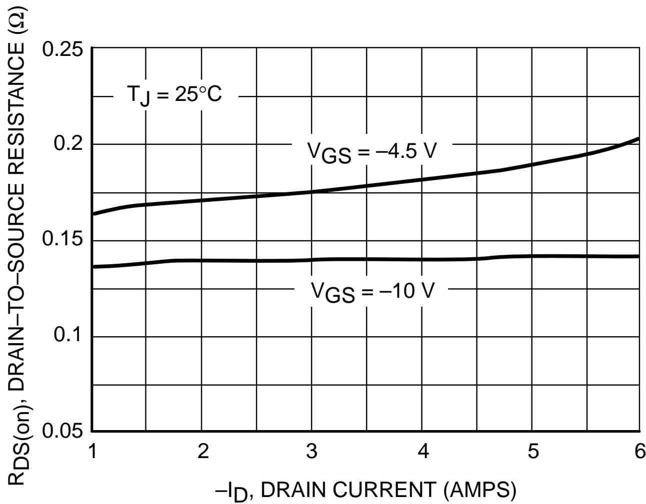



**Figure 5. On–Resistance vs. Drain Current and Gate Voltage**

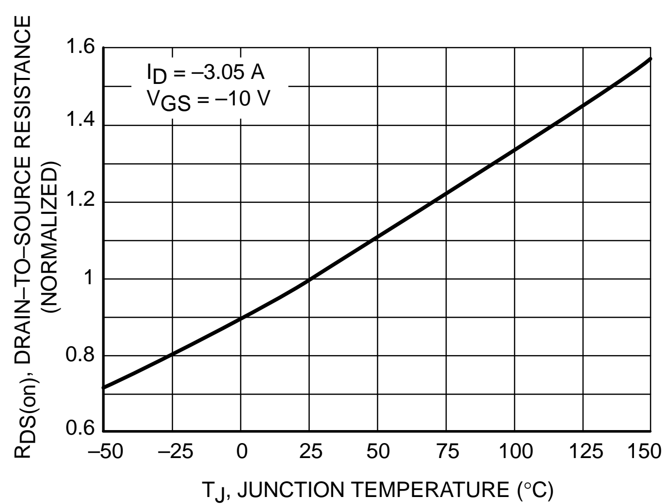



**Figure 6. On Resistance Variation with Temperature**

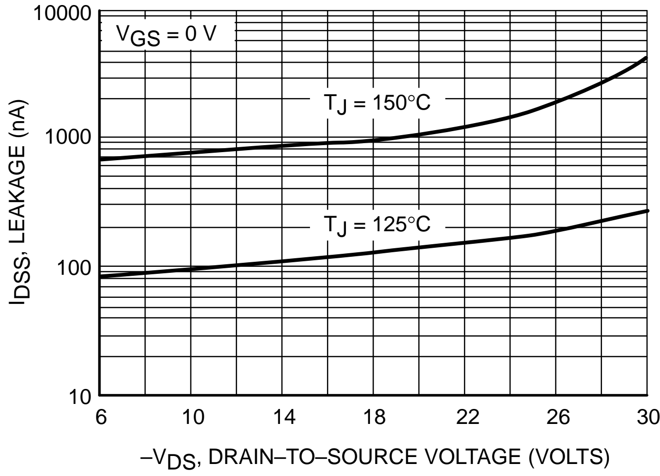



**Figure 7. Drain–to–Source Leakage Current vs. Voltage**

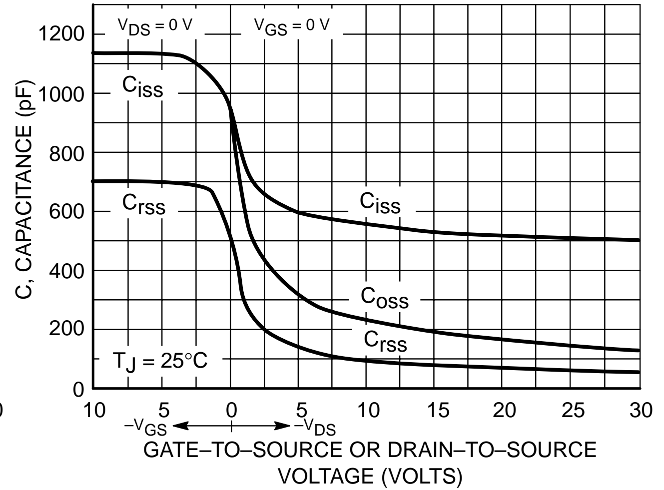



**Figure 8. Capacitance Variation**

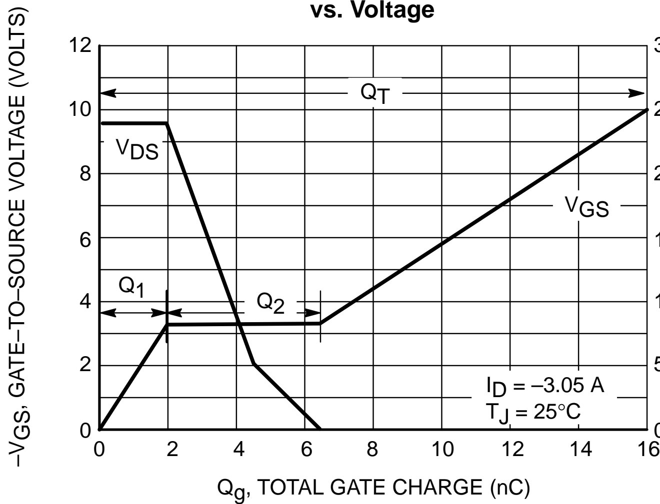



**Figure 9. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

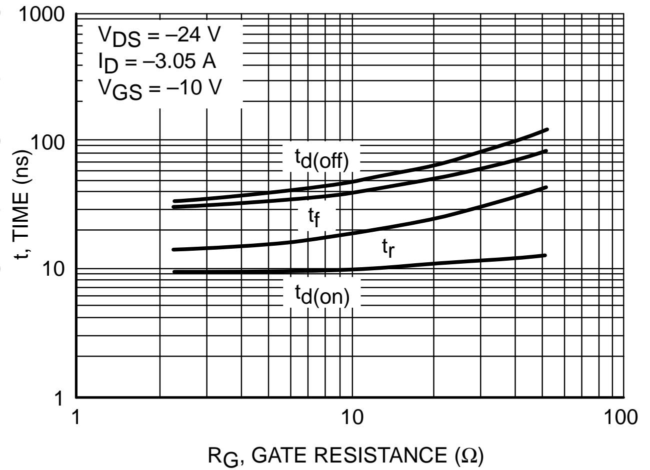



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

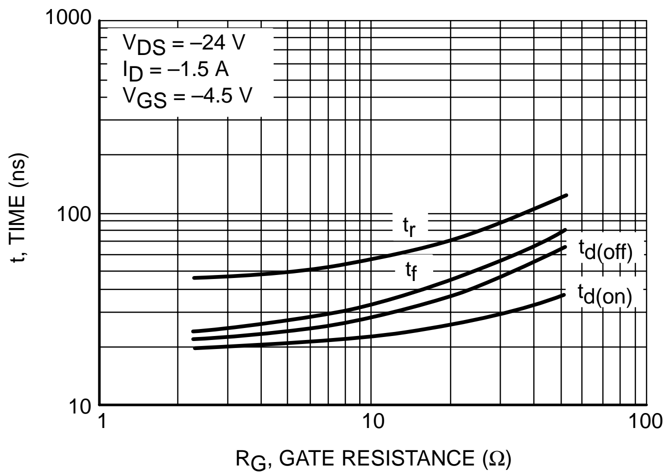



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

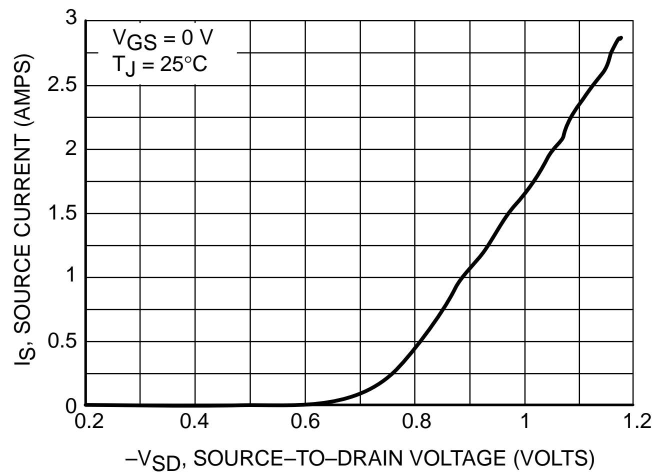



**Figure 12. Diode Forward Voltage vs. Current**

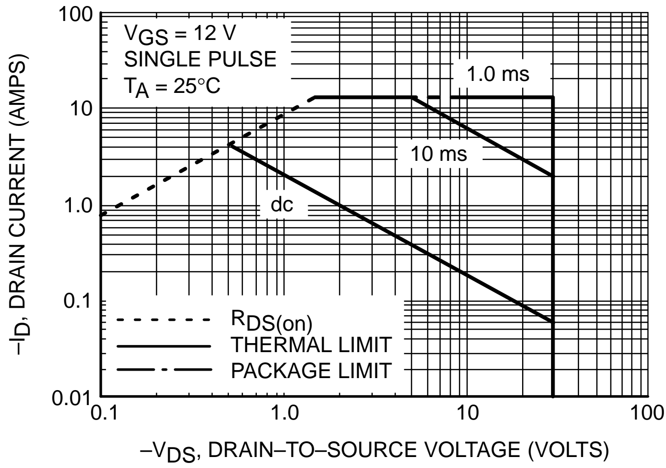



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

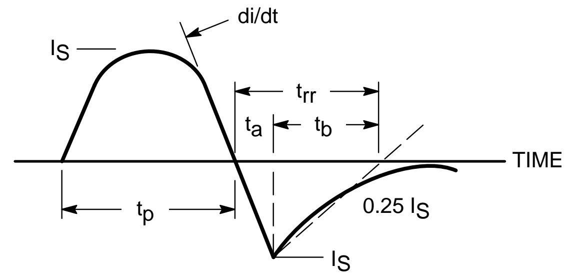



**Figure 14. Diode Reverse Recovery Waveform**

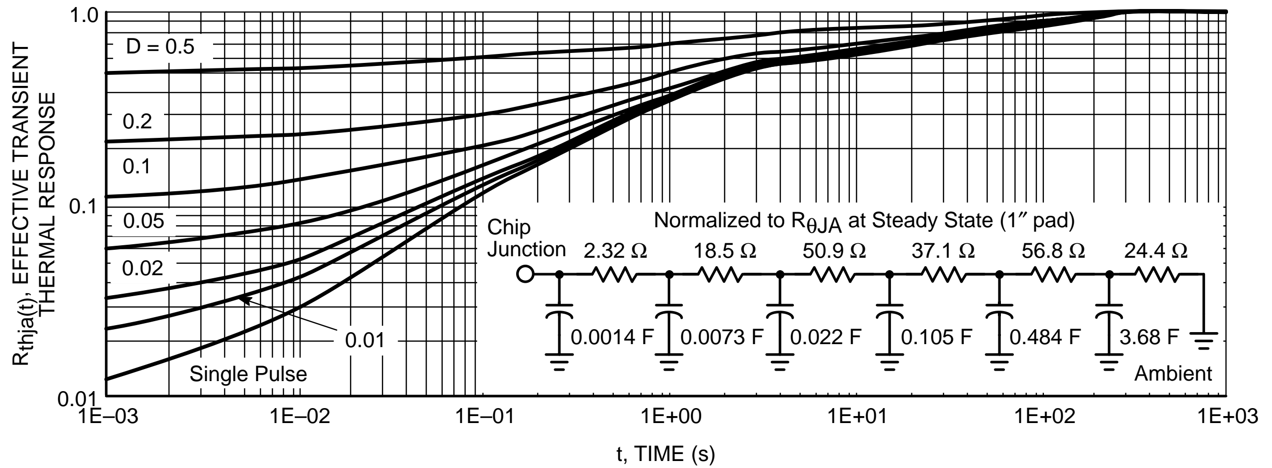
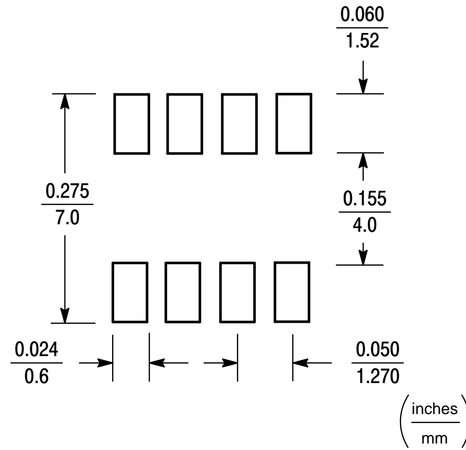



**Figure 15. FET Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

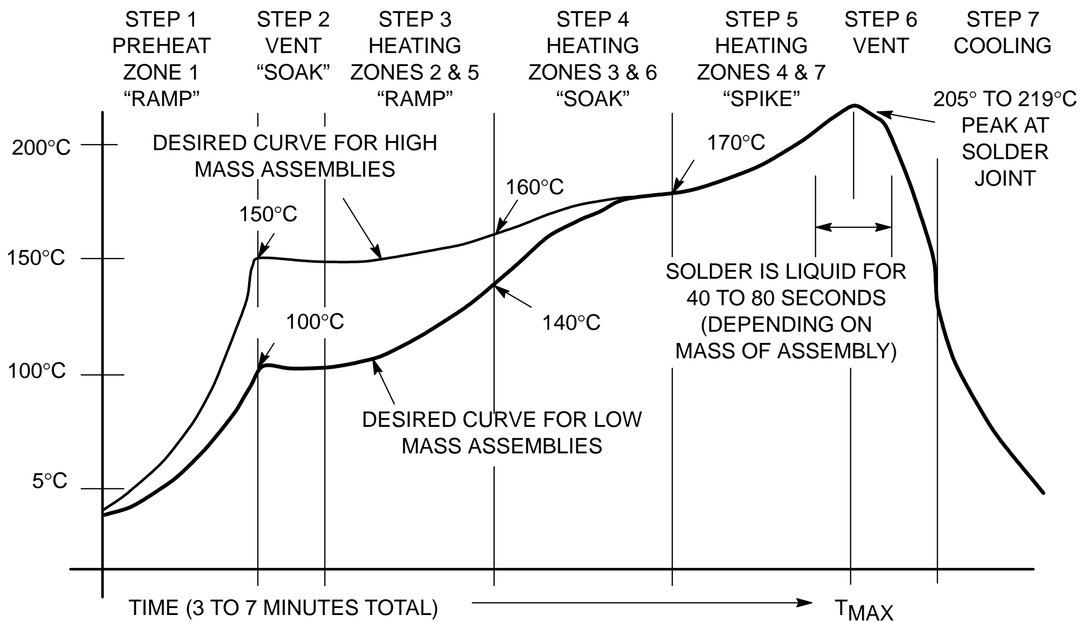



**Figure 16. Typical Solder Heating Profile**

# NTMS4N01R2

**ON Semiconductor™**

**http://onsemi.com**

## Power MOSFET 4.2 Amps, 20 Volts

### N–Channel Enhancement–Mode Single SO–8 Package

**Features**

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO–8 Surface Mount Package Saving Board Space; Mounting Information for the SO–8 Package is Provided
- $I_{DSS}$ Specified at Elevated Temperature
- Drain–to–Source Avalanche Energy Specified
- Diode Exhibits High Speed, Soft Recovery

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

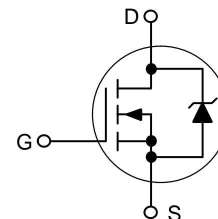
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

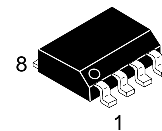
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | 20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.5 | W |
| Continuous Drain Current @ 25°C | $I_D$ | 5.9 | A |
| Continuous Drain Current @ 70°C | $I_D$ | 4.7 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 25 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 100 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.25 | W |
| Continuous Drain Current @ 25°C | $I_D$ | 4.2 | A |
| Continuous Drain Current @ 70°C | $I_D$ | 3.3 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 20 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 162 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.77 | W |
| Continuous Drain Current @ 25°C | $I_D$ | 3.3 | A |
| Continuous Drain Current @ 70°C | $I_D$ | 2.6 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | 15 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 7.5 Apk, L = 6 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 169 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR–4 or G–10 PCB, t = Steady State.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**4.2 AMPERES**
**20 VOLTS**
**0.045 Ω @ $V_{GS}$ = 4.5 V**

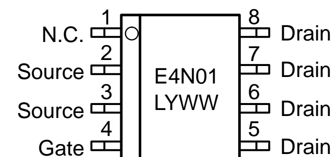
**Single N–Channel**




**SO–8**
**CASE 751**
**STYLE 13**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Top View

E4N01 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMS4N01R2 | SO–8 | 2500/Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 20 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | | – | 0.2 | – | |
| Gate–Body Leakage Current ($V_{GS}$ = +10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.6 | 0.95 | 1.2 | Vdc |
| Temperature Coefficient (Negative) | | | – | –3.0 | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.2 Adc) | | $R_{DS(on)}$ | – | 0.030 | 0.04 | Ω |
| ($V_{GS}$ = 2.7 Vdc, $I_D$ = 2.1 Adc) | | | – | 0.035 | 0.05 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 2.0 Adc) | | | – | 0.037 | – | |
| Forward Transconductance ($V_{DS}$ = 2.5 Vdc, $I_D$ = 2.0 Adc) | | $g_{FS}$ | – | 10 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 870 | 1200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 260 | 400 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 60 | 100 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. & 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 12 Vdc, $I_D$ = 4.2 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 13 | 25 | ns |
| Rise Time | | $t_r$ | – | 35 | 65 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 75 | |
| Fall Time | | $t_f$ | – | 50 | 90 | |
| Total Gate Charge | ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 4.5 Vdc, $I_D$ = 4.2 Adc) | $Q_{tot}$ | – | 11 | 16 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 3.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.85 | 1.1 | Vdc |
| | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.70 | – | |
| Reverse Recovery Time | ($I_S$ = 4.2 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 20 | – | ns |
| | | $t_a$ | – | 12 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.01 | – | μC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

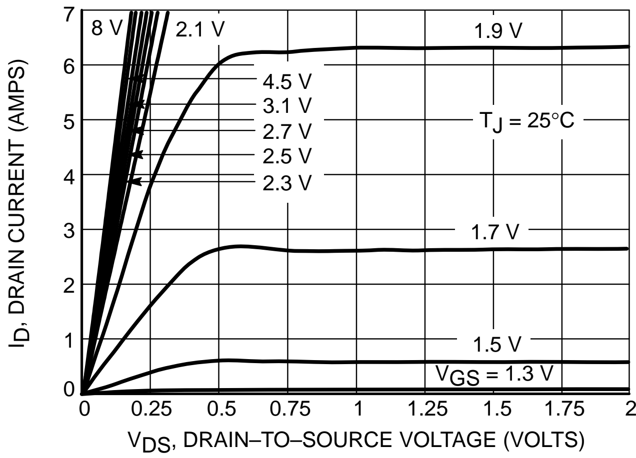



**Figure 1. On–Region Characteristics**

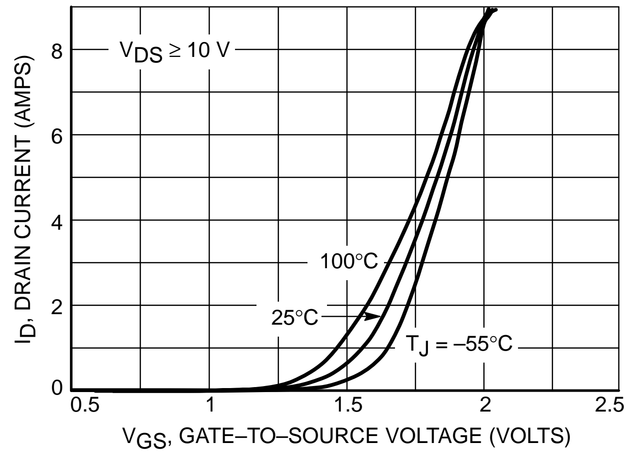



**Figure 2. Transfer Characteristics**

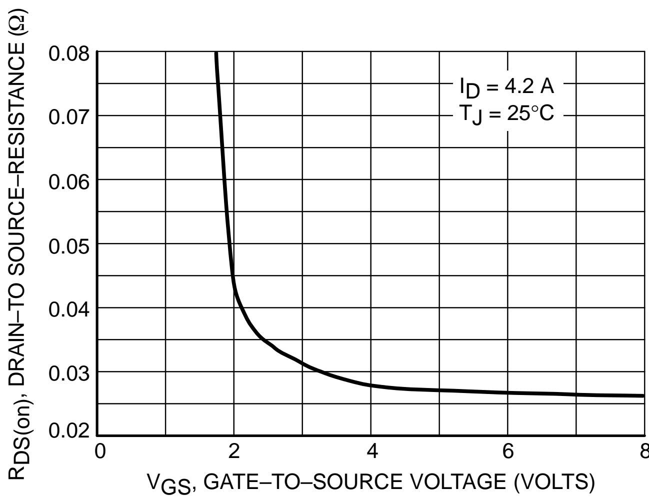



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

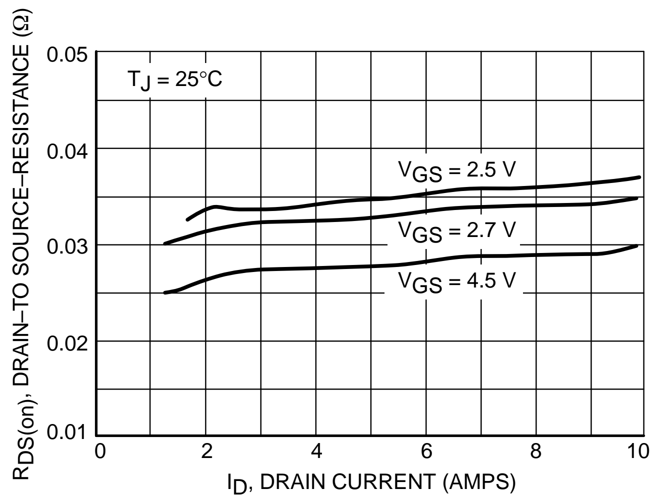



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

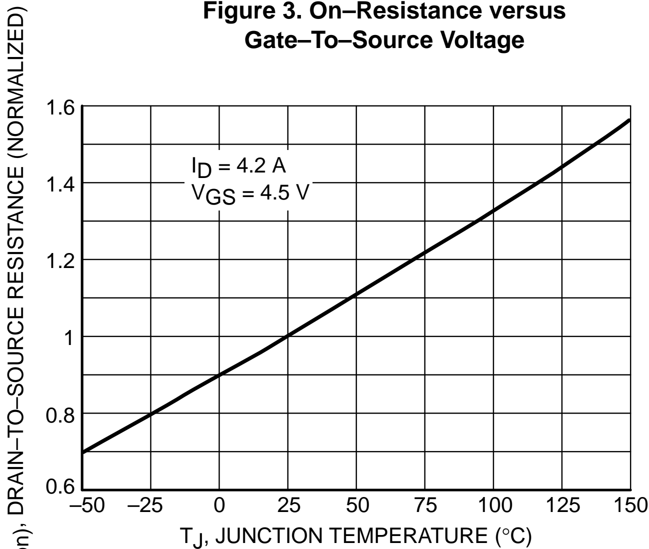



**Figure 5. On–Resistance Variation with Temperature**

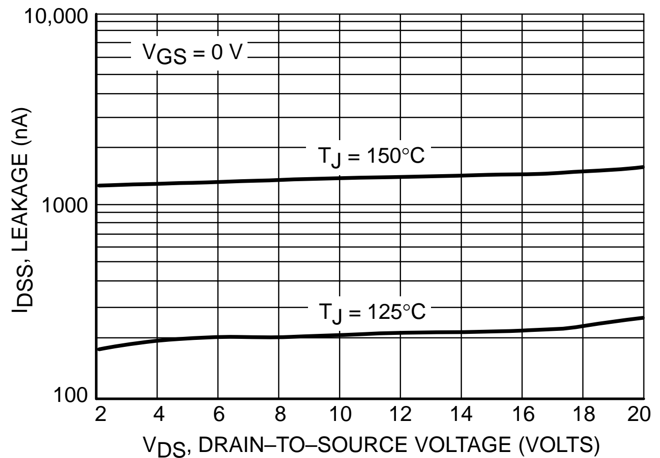



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

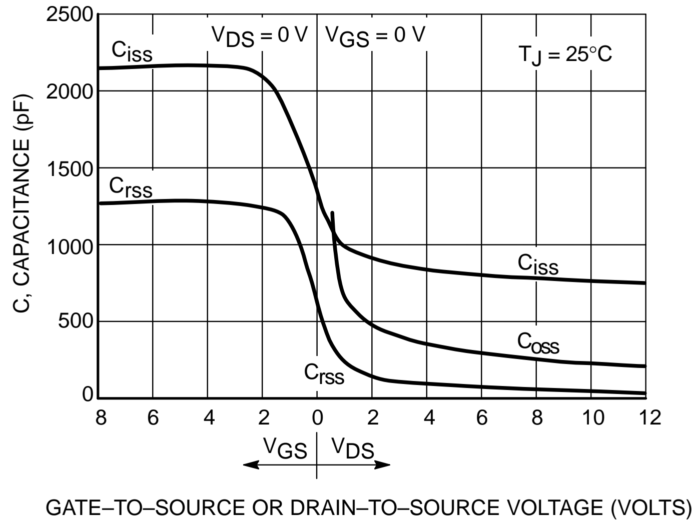



**Figure 7. Capacitance Variation**

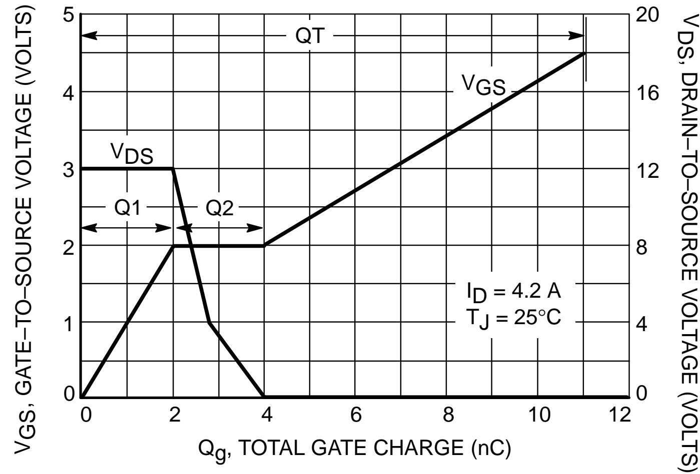



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

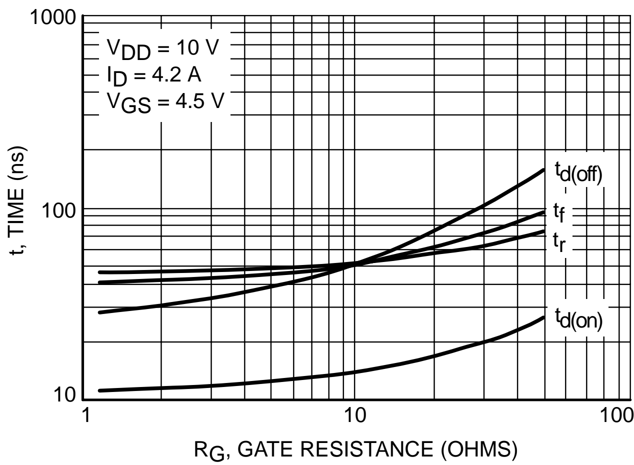



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

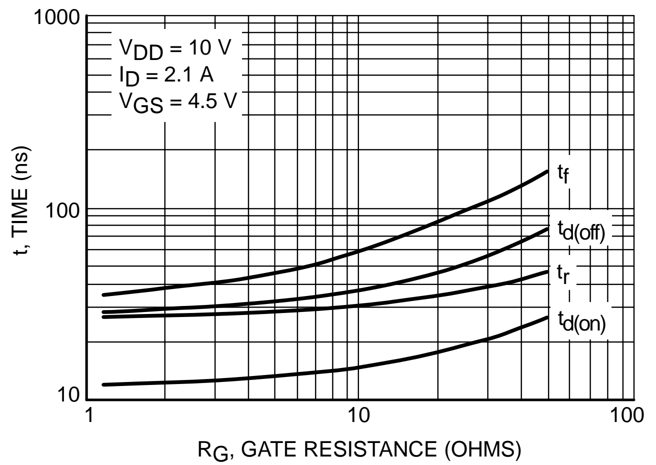



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

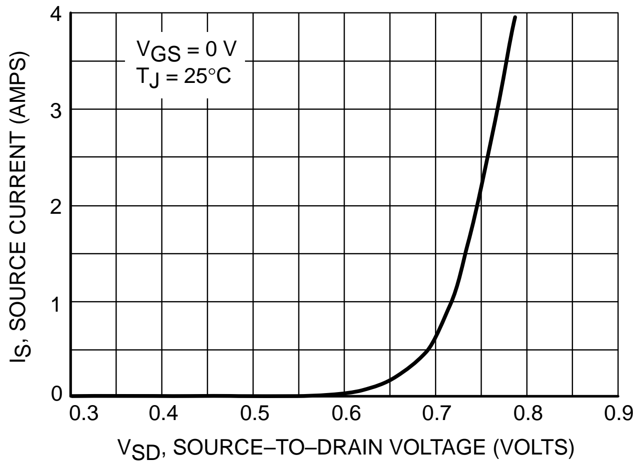



**Figure 11. Diode Forward Voltage versus Current**

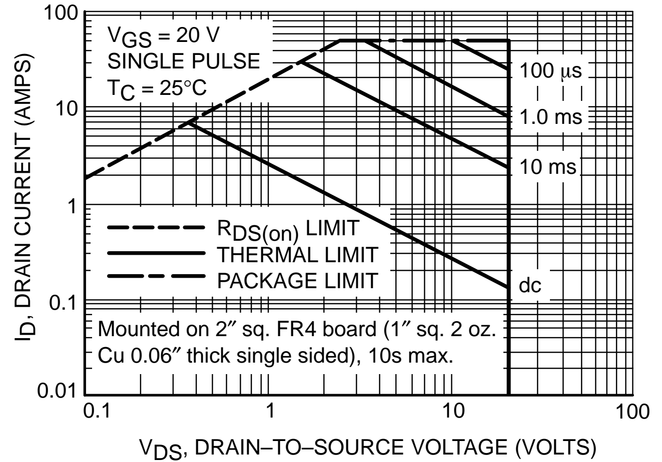



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

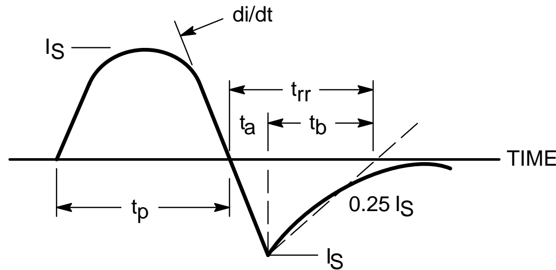



**Figure 13. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

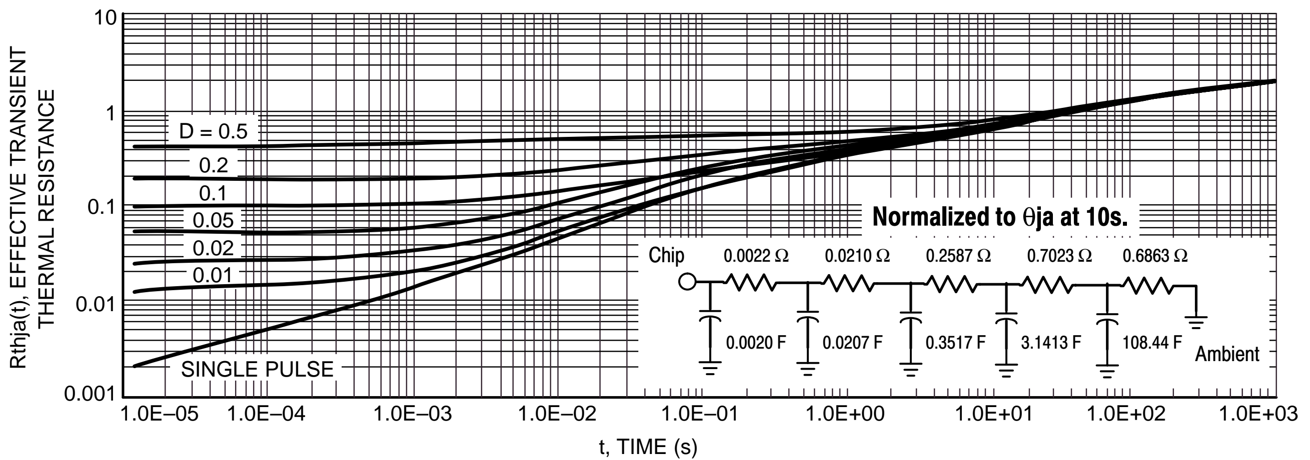
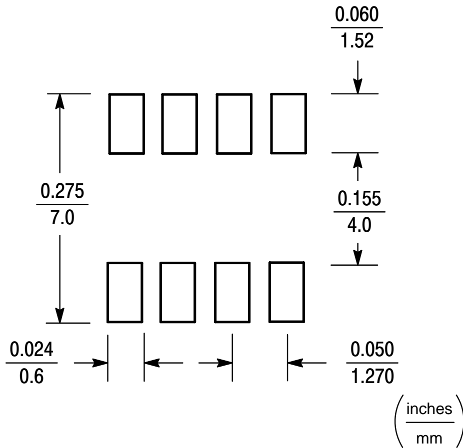



**Figure 14. Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.

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- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

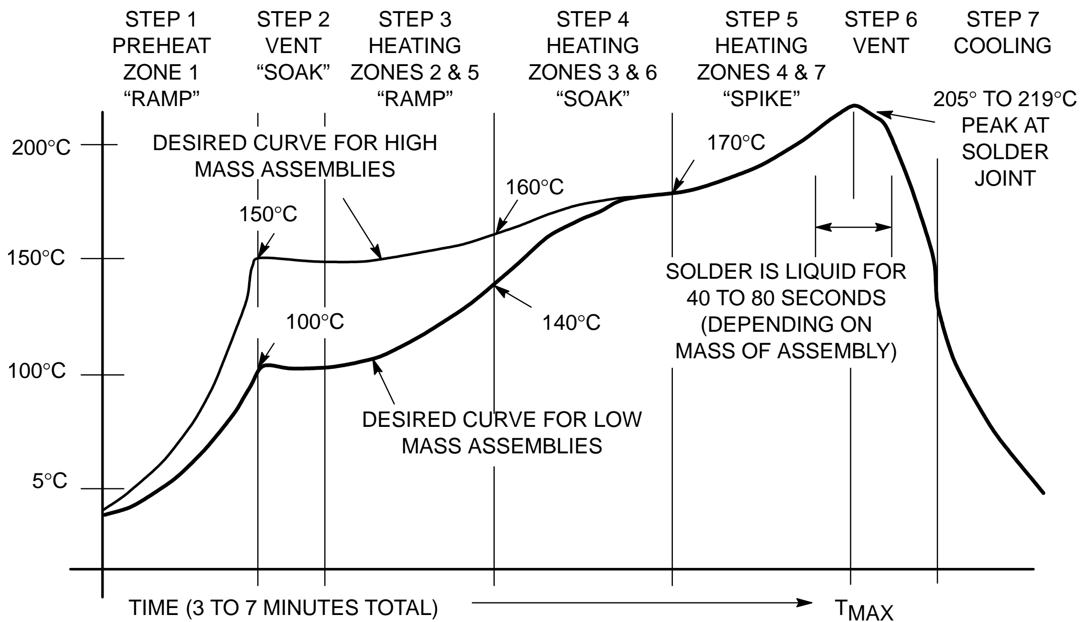



**Figure 15. Typical Solder Heating Profile**

# NTMS4P01R2

*Product Preview*

## Power MOSFET -4.5 Amps, -12 Volts

### P–Channel Enhancement–Mode Single SO–8 Package

ON Semiconductor™

http://onsemi.com

**–4.5 AMPERES**
**–12 VOLTS**
**0.045 Ω @ $V_{GS}$ = –4.5 V**

**Features**

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Drain–to–Source Avalanche Energy Specified
- Mounting Information for the SO–8 Package is Provided

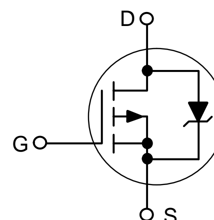
**Applications**

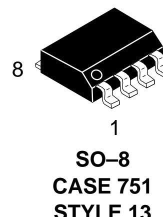
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

**MAXIMUM RATINGS**

Please See the Table on the Following Page

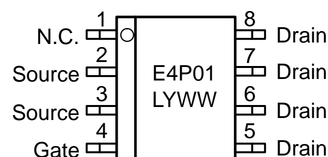
**Single P–Channel**




**SO–8**
**CASE 751**
**STYLE 13**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Top View

E4P01 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMS4P01R2 | SO–8 | 2500/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –12 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | –12 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | V |
| Thermal Resistance –<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>50<br>2.5<br>–6.04<br>–4.82<br>1.2<br>–4.18<br>–20 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>85<br>1.47<br>–4.50<br>–3.65<br>0.7<br>–3.20<br>–15 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>159<br>0.79<br>–3.40<br>–2.72<br>0.38<br>–2.32<br>–12 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = –12 Vdc, $V_{GS}$ = –5.0 Vdc, Peak $I_L$ = –8.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 320 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR–4 or G–10 PCB, t = Steady State.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 µAdc) | | $V_{(BR)DSS}$ | –12 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | –15 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = –12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –1.0 | µAdc |
| ($V_{DS}$ = –12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | –10 | |
| Gate–Body Leakage Current ($V_{GS}$ = –10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 µAdc) | | $V_{GS(th)}$ | –0.65 | –0.9 | –1.15 | Vdc |
| Temperature Coefficient (Negative) | | | – | 2.9 | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –4.5 Adc) | | $R_{DS(on)}$ | – | 0.030 | 0.045 | Ω |
| ($V_{GS}$ = –2.7 Vdc, $I_D$ = –2.25 Adc) | | | – | 0.040 | 0.055 | |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –2.25 Adc) | | | – | 0.045 | – | |
| Forward Transconductance ($V_{DS}$ = –2.5 Vdc, $I_D$ = –2.25 Adc) | | $g_{FS}$ | – | 10 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –9.6 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1435 | 1850 | pF |
| Output Capacitance | | $C_{oss}$ | – | 635 | 1000 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 210 | 400 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. & 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –12 Vdc, $I_D$ = –4.5 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | 35 | ns |
| Rise Time | | $t_r$ | – | 60 | 100 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 65 | 100 | |
| Fall Time | | $t_f$ | – | 75 | 125 | |
| Total Gate Charge | ($V_{DS}$ = –9.6 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –4.5 Adc) | $Q_{tot}$ | – | 20 | 35 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 4.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 7.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –4.5 Adc, $V_{GS}$ = 0 V) | $V_{SD}$ | – | –0.9 | –1.25 | Vdc |
| | ($I_S$ = –4.5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | –0.7 | – | |
| Reverse Recovery Time | ($I_S$ = –4.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 18 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | µC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

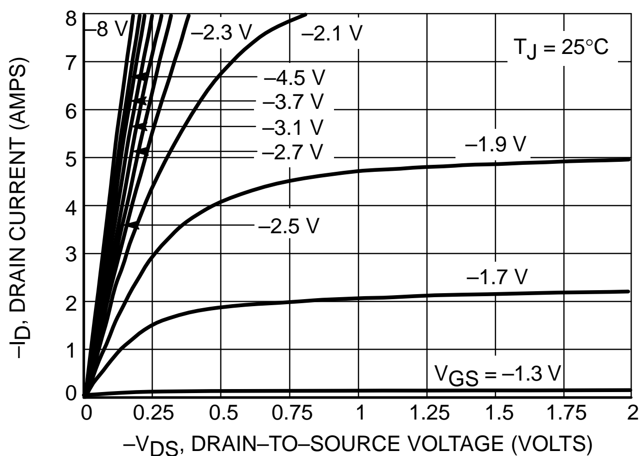



**Figure 1. On−Region Characteristics**

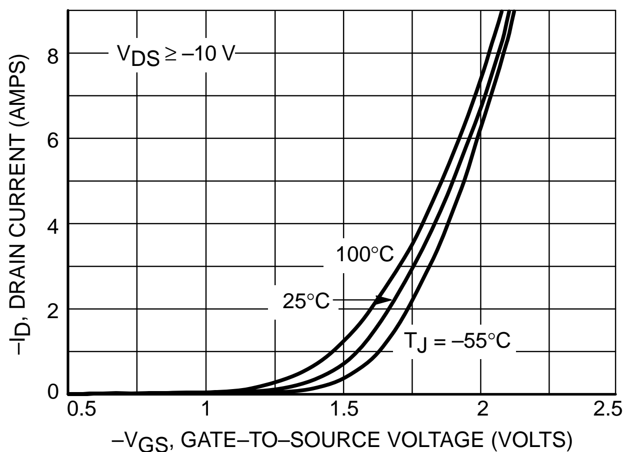



**Figure 2. Transfer Characteristics**

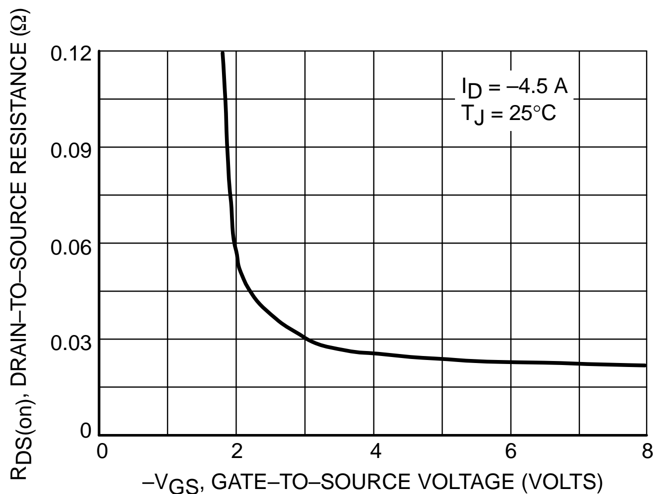



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

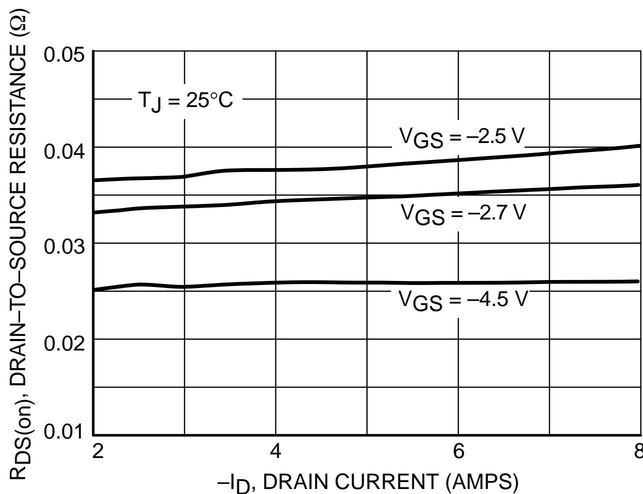



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

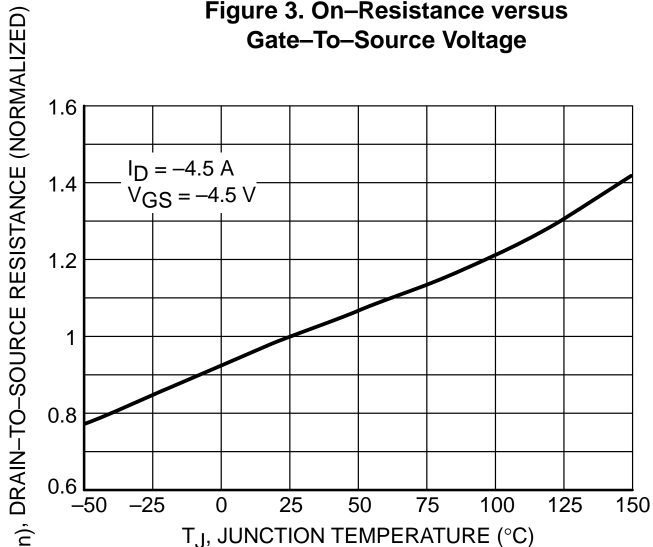



**Figure 5. On−Resistance Variation with Temperature**

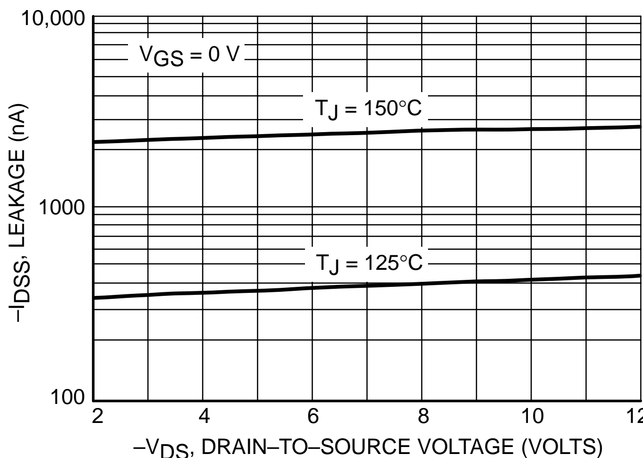



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

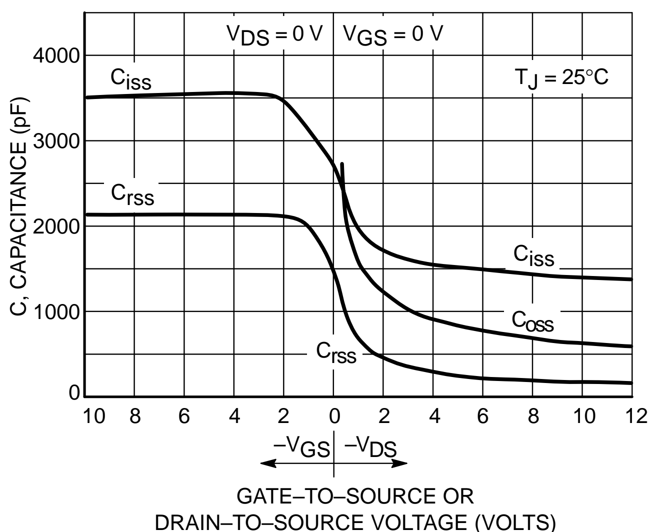



**Figure 7. Capacitance Variation**

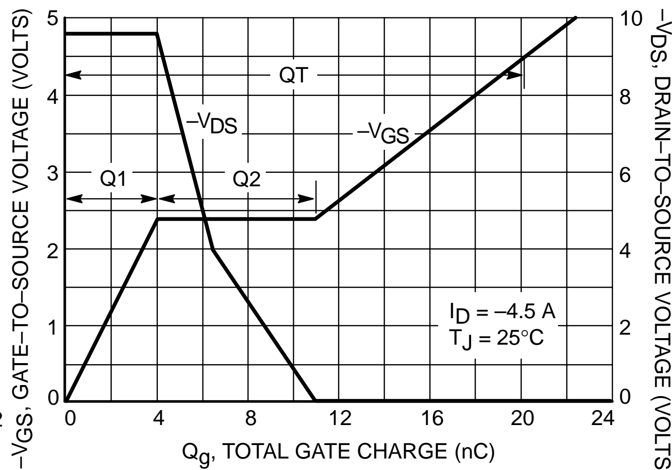



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

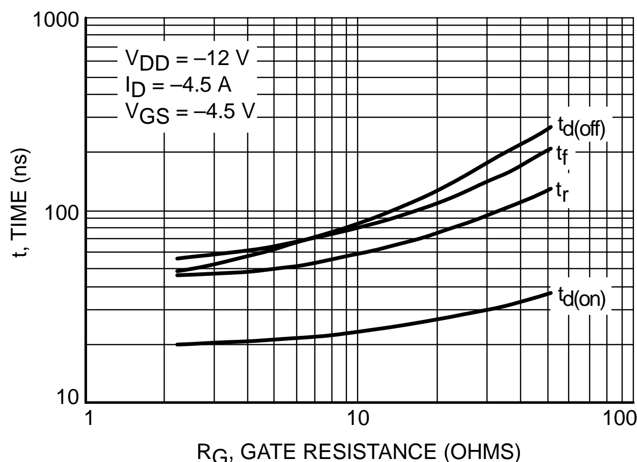



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

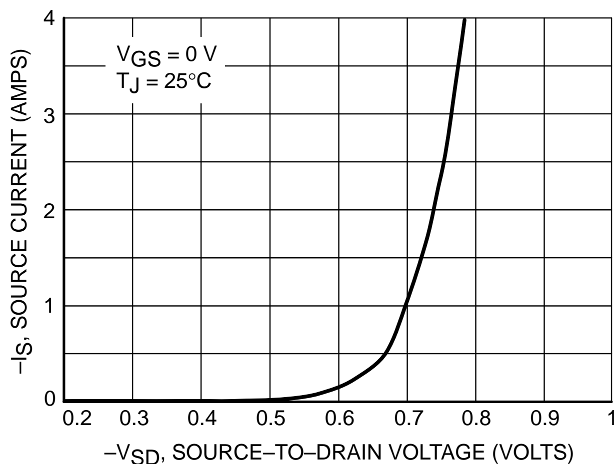



**Figure 10. Diode Forward Voltage versus Current**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

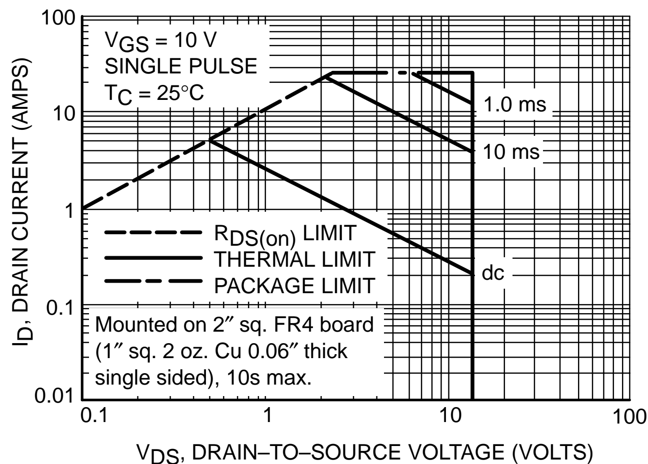



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

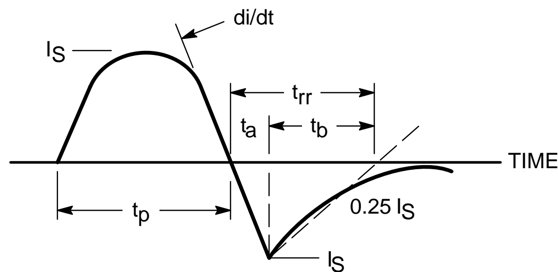



**Figure 12. Diode Reverse Recovery Waveform**

### TYPICAL ELECTRICAL CHARACTERISTICS

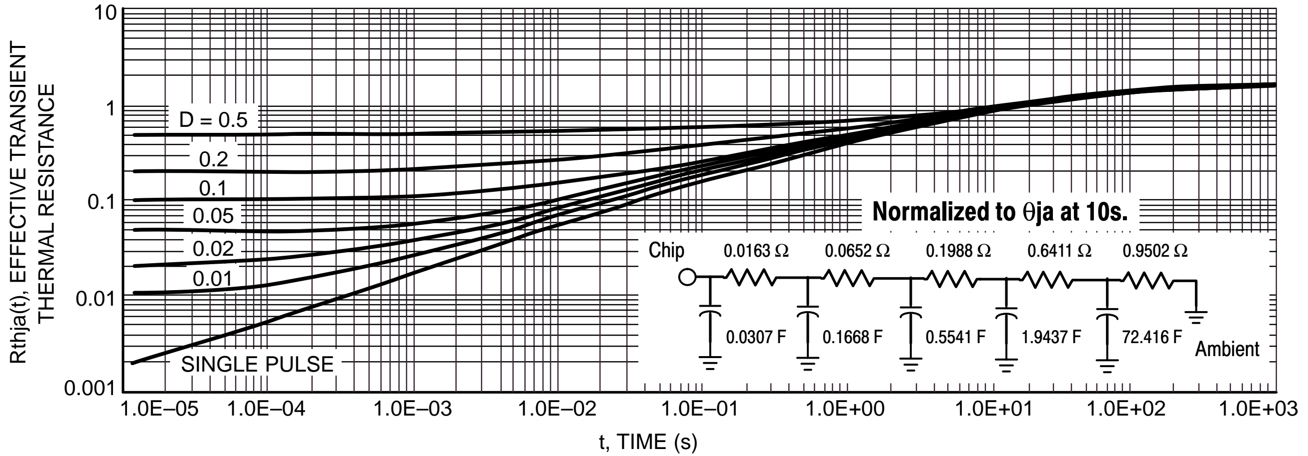
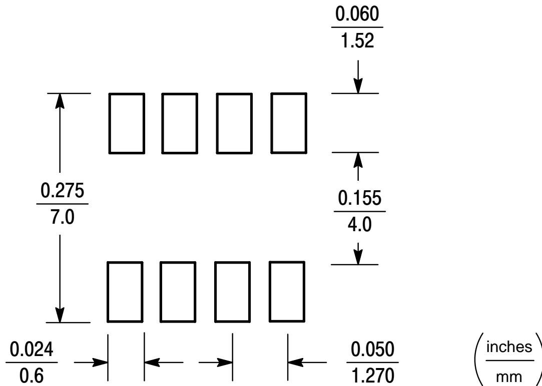



**Figure 13. Thermal Response**

## INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

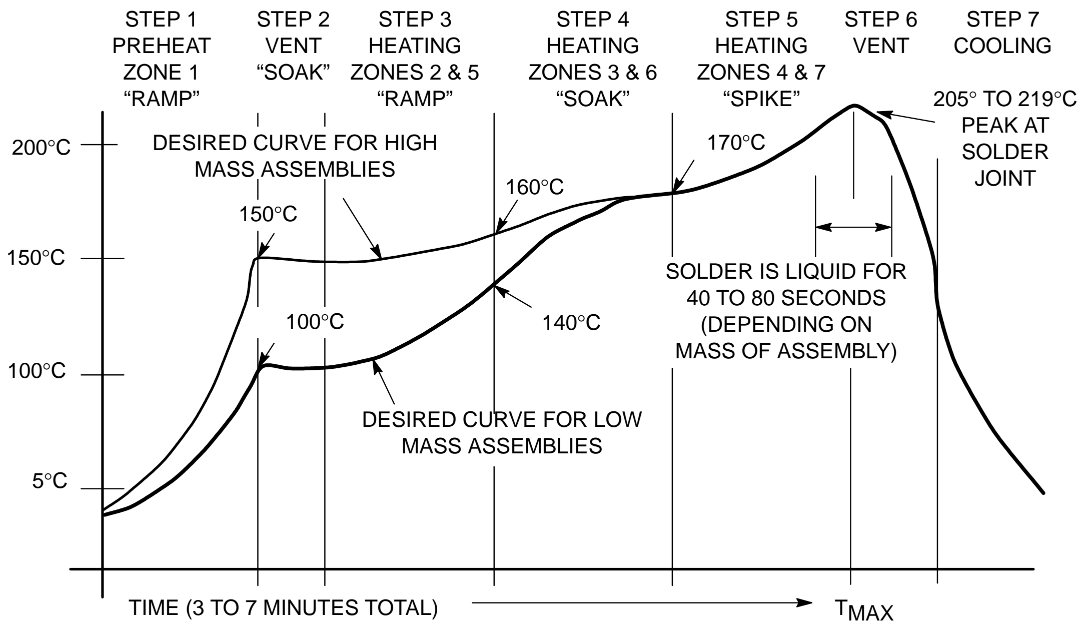



**Figure 14. Typical Solder Heating Profile**

# NTMS5P02R2

*Product Preview*

## Power MOSFET
## -5.4 Amps, -20 Volts

### P–Channel Enhancement–Mode
### Single SO–8 Package

**Features**

- High Density Power MOSFET with Ultra Low $R_{DS(on)}$ Providing Higher Efficiency
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Drain–to–Source Avalanche Energy Specified
- Mounting Information for the SO–8 Package is Provided

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular & Cordless Telephones

**MAXIMUM RATINGS**

| Please See the Table on the Following Page |
|---|

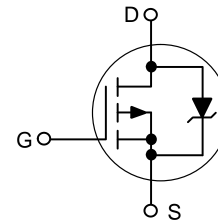
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

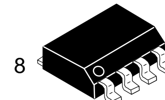
**ON Semiconductor™**

**http://onsemi.com**

**–5.4 AMPERES**
**–20 VOLTS**
**0.033 Ω @ $V_{GS}$ = –4.5 V**

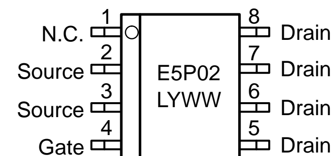
**Single P–Channel**




**SO–8**
**CASE 751**
**STYLE 13**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Top View

| | |
|---|---|
| E5P02 | = Device Code |
| L | = Assembly Location |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMS5P02R2 | SO–8 | 2500/Tape & Reel |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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | V |
| Thermal Resistance –<br>Junction–to–Ambient (Note 1)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>50<br>2.5<br>–7.05<br>–5.62<br>1.2<br>–4.85<br>–28 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>85<br>1.47<br>–5.40<br>–4.30<br>0.7<br>–3.72<br>–20 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ 25°C<br>Continuous Drain Current @ 70°C<br>Maximum Operating Power Dissipation<br>Maximum Operating Drain Current<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$P_D$<br>$I_D$<br>$I_{DM}$ | <br>159<br>0.79<br>–3.95<br>–3.15<br>0.38<br>–2.75<br>–12 | <br>°C/W<br>W<br>A<br>A<br>W<br>A<br>A |
| Operating and Storage<br>Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = –20 Vdc, $V_{GS}$ = –5.0 Vdc, Peak $I_L$ = –8.5 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 360 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t = steady state.
3. Minimum FR–4 or G–10 PCB, t = Steady State.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 5.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc) | | $V_{(BR)DSS}$ | –20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | –15 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –1.0 | μAdc |
| ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | –10 | |
| ($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C) | | | – | –0.2 | – | |
| Gate–Body Leakage Current ($V_{GS}$ = –10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +10 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc) | | $V_{GS(th)}$ | –0.65 | –0.9 | –1.25 | Vdc |
| Temperature Coefficient (Negative) | | | – | 2.9 | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = –4.5 Vdc, $I_D$ = –5.4 Adc) | | $R_{DS(on)}$ | – | 0.026 | 0.033 | Ω |
| ($V_{GS}$ = –2.5 Vdc, $I_D$ = –2.7 Adc) | | | – | 0.037 | 0.048 | |
| Forward Transconductance ($V_{DS}$ = –9.0 Vdc, $I_D$ = –5.4 Adc) | | $g_{FS}$ | – | 15 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1375 | 1900 | pF |
| Output Capacitance | | $C_{oss}$ | – | 510 | 900 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 200 | 380 | |
| **SWITCHING CHARACTERISTICS** (Notes 6. & 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –16 Vdc, $I_D$ = –1.0 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 18 | 35 | ns |
| Rise Time | | $t_r$ | – | 25 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 70 | 125 | |
| Fall Time | | $t_f$ | – | 55 | 100 | |
| Turn–On Delay Time | ($V_{DD}$ = –16 Vdc, $I_D$ = –5.4 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 22 | – | ns |
| Rise Time | | $t_r$ | – | 70 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 65 | – | |
| Fall Time | | $t_f$ | – | 90 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –5.4 Adc) | $Q_{tot}$ | – | 20 | 35 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 4.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 7.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 6.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –5.4 Adc, $V_{GS}$ = 0 V) | $V_{SD}$ | – | –0.95 | –1.25 | Vdc |
| | ($I_S$ = –5.4 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | –0.72 | – | |
| Reverse Recovery Time | ($I_S$ = –5.4 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 40 | 75 | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

5. Handling precautions to protect against electrostatic discharge is mandatory.
6. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
7. Switching characteristics are independent of operating junction temperature.

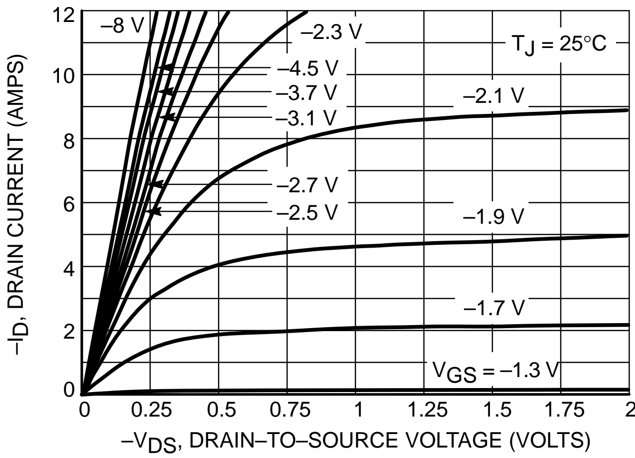



**Figure 1. On−Region Characteristics**

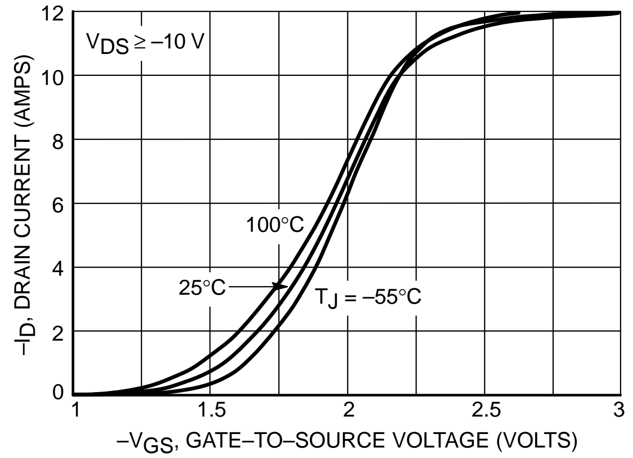



**Figure 2. Transfer Characteristics**

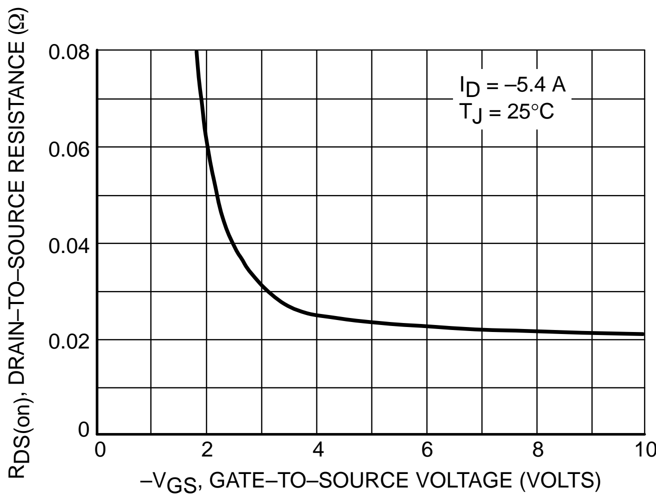



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

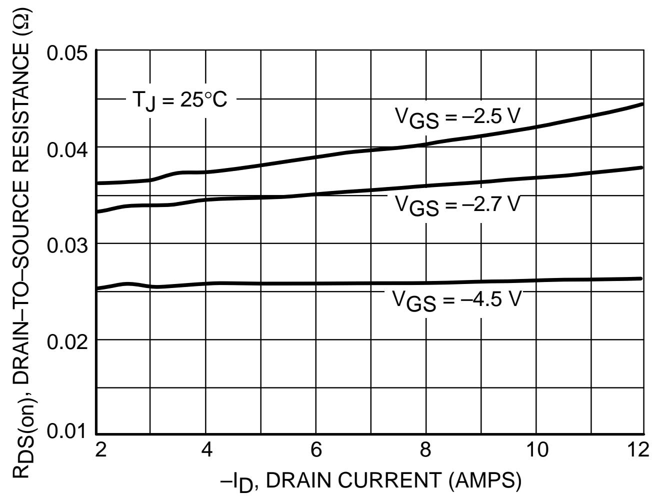



**Figure 4. On-Resistance versus Drain Current and Gate Voltage**

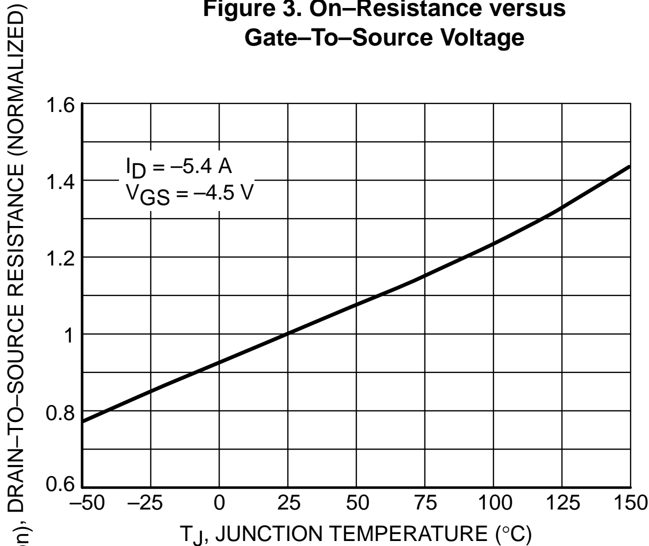



**Figure 5. On−Resistance Variation with Temperature**

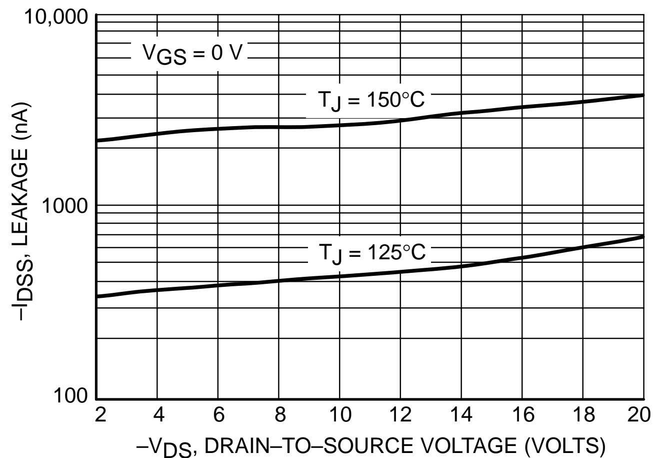



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

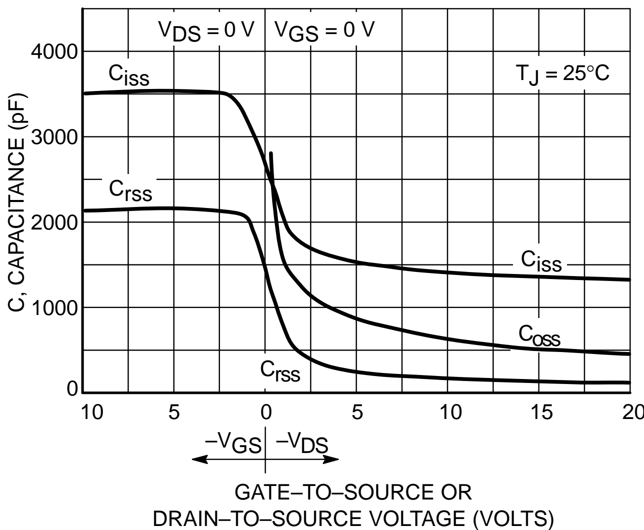



**Figure 7. Capacitance Variation**

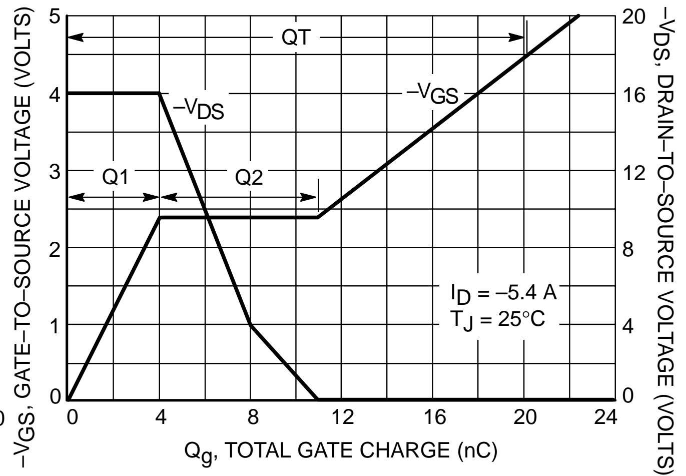



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

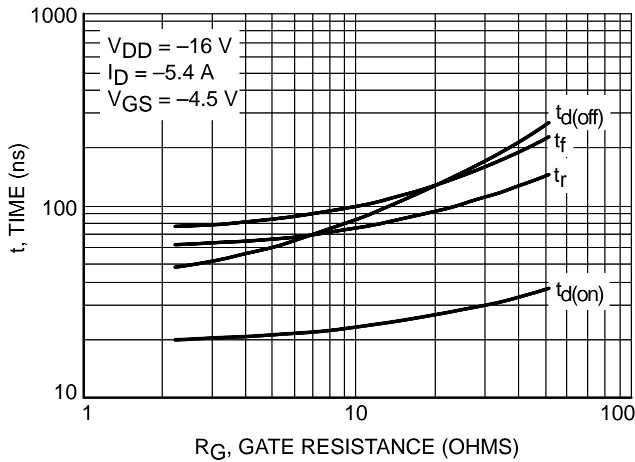



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

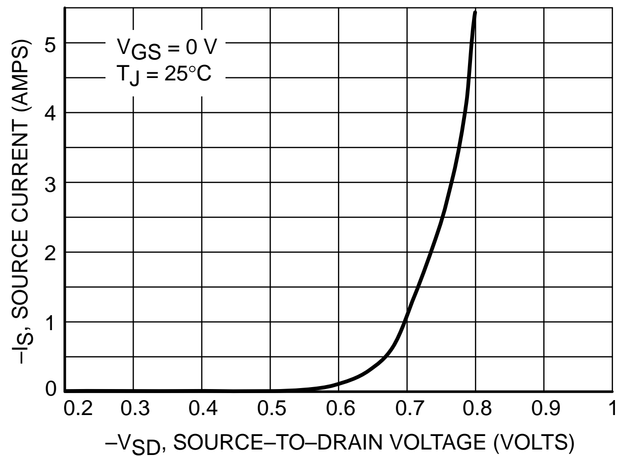



**Figure 10. Diode Forward Voltage versus Current**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

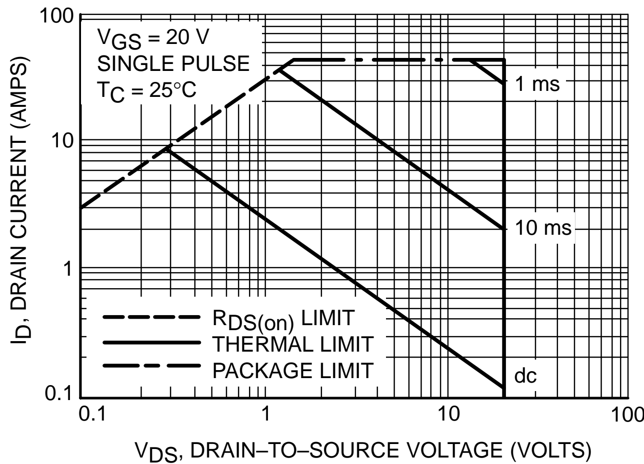



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

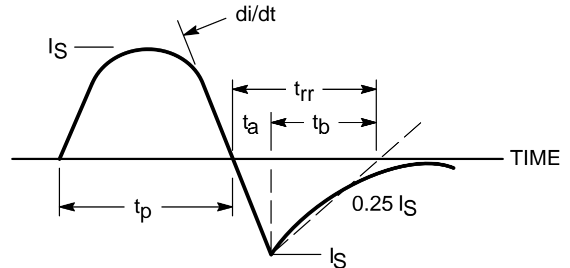



**Figure 12. Diode Reverse Recovery Waveform**

### TYPICAL ELECTRICAL CHARACTERISTICS

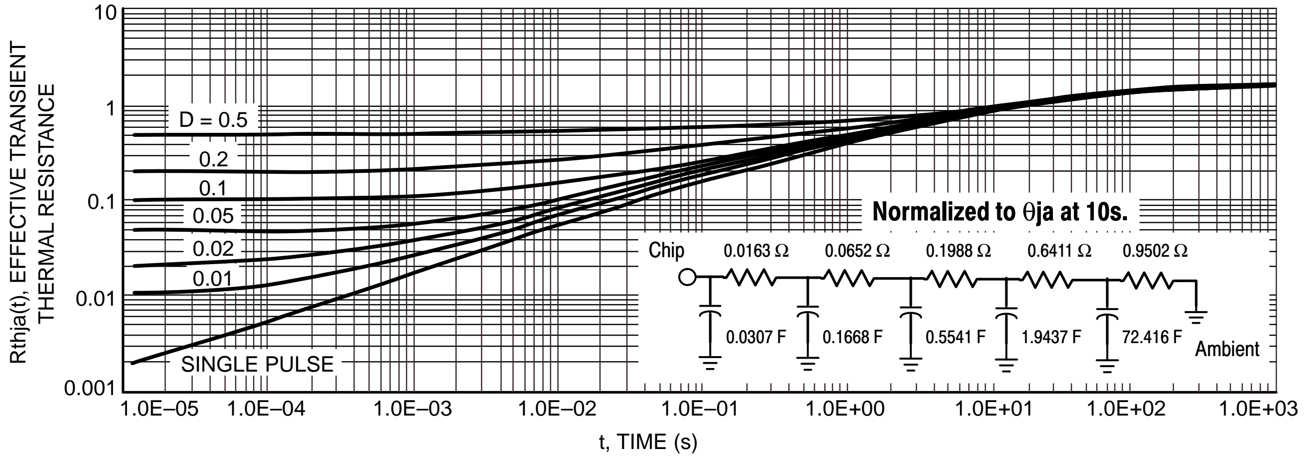
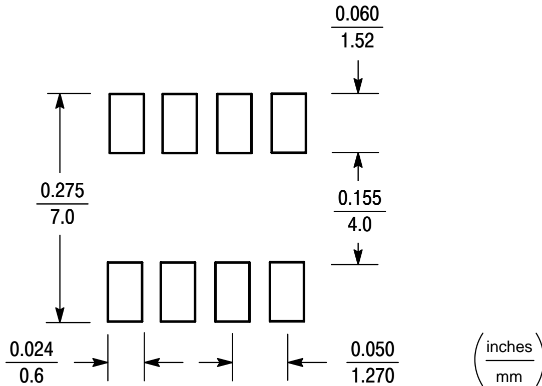



**Figure 13. Thermal Response**

## INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

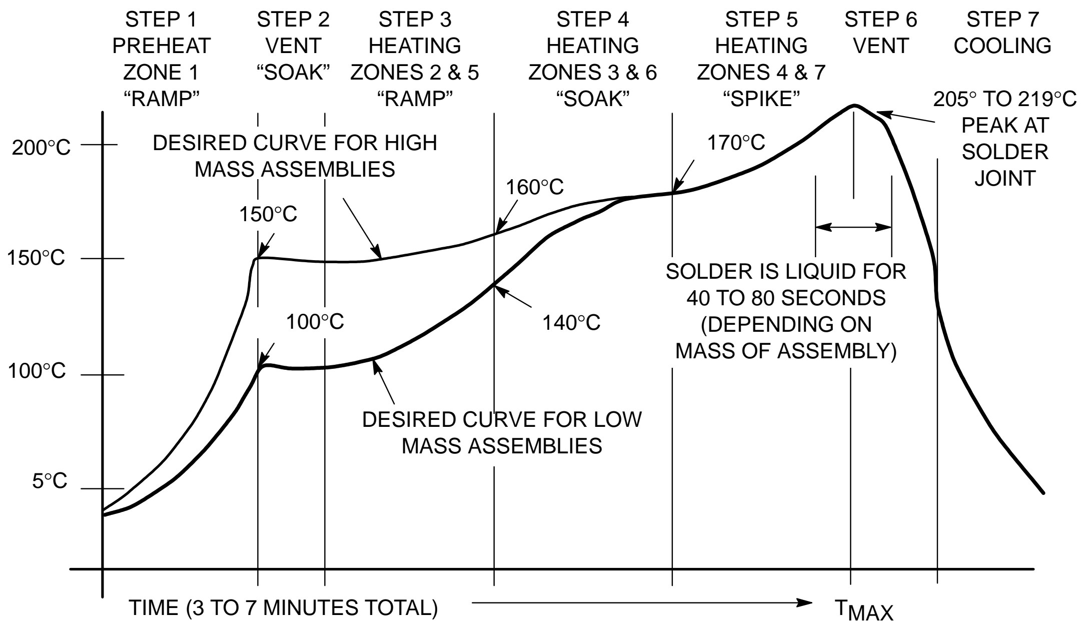



**Figure 14. Typical Solder Heating Profile**

# NTMSD2P102LR2

*Product Preview*

## FETKY™

## Power MOSFET and Schottky Diode Dual SO–8 Package

**ON Semiconductor™**

**http://onsemi.com**

**MOSFET**
**–2.3 AMPERES**
**–20 VOLTS**
**90 mΩ @ $V_{GS}$ = –4.5 V**

**SCHOTTKY DIODE**
**2.0 AMPERES**
**20 VOLTS**
**580 mV @ $I_F$ = 2.0 A**

**Features**

- High Efficiency Components in a Single SO–8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$, Schottky Diode with Low $V_F$
- Logic Level Gate Drive
- Independent Pin–Outs for MOSFET and Schottky Die Allowing for Flexibility in Application Use
- Less Component Placement for Board Space Savings
- SO–8 Surface Mount Package, Mounting Information for SO–8 Package Provided

**Applications**

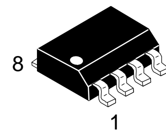
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

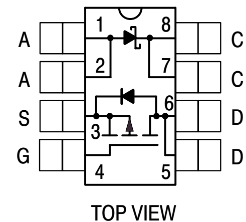
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 10 | V |
| Thermal Resistance – Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 4.) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 175<br>0.71<br>–2.3<br>–1.45<br>–9.0 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance – Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 4.) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 105<br>1.19<br>–2.97<br>–1.88<br>–12 | °C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance – Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 100°C<br>Pulsed Drain Current (Note 4.) | $R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | 62.5<br>2.0<br>–3.85<br>–2.43<br>–15 | °C/W<br>W<br>A<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –5.0 Apk, L = 28 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 350 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

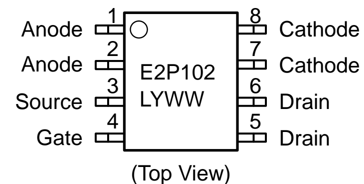



**SO–8**
**CASE 751**
**STYLE 18**




TOP VIEW

**MARKING DIAGRAM & PIN ASSIGNMENTS**




(Top View)

E2P102 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMSD2P102LR2 | SO–8 | 2500/Tape & Reel |

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**SCHOTTKY MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 20 | V |
| Average Forward Current (Note 5.)<br>(Rated $V_R$, $T_A$ = 100°C) | $I_O$ | 1.0 | A |
| Peak Repetitive Forward Current<br>(Note 5.) (Rated $V_R$, Square Wave, 20 kHz, $T_A$ = 105°C) | $I_{FRM}$ | 2.0 | A |
| Non–Repetitive Peak Surge Current (Note 5.)<br>(Surge Applied at Rated Load Conditions, Half–Wave, Single Phase, 60 Hz) | $I_{FSM}$ | 20 | A |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>–20<br>– | <br>–<br>–12.7 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>–1.0<br>–25 | μAdc |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C) | $I_{DSS}$ | <br>– | <br>– | <br>–2.0 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = –10 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | <br>– | <br>– | <br>–100 | nAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = +10 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>–0.5<br>– | <br>–0.90<br>2.5 | <br>–1.5<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc)<br>($V_{GS}$ = –2.7 Vdc, $I_D$ = –1.2 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –1.2 Adc) | $R_{DS(on)}$ | <br>–<br>–<br>– | <br>0.070<br>0.100<br>0.110 | <br>0.090<br>0.130<br>0.150 | Ω |
| Forward Transconductance<br>($V_{DS}$ = –10 Vdc, $I_D$ = –1.2 Adc) | $g_{FS}$ | <br>– | <br>4.2 | <br>– | Mhos |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | 300 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 100 | 175 | |

5. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
6. Handling precautions to protect against electrostatic discharge is mandatory.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (continued) (Note 7.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Notes 8. & 9.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –2.4 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 35 | 65 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 33 | 60 | |
| Fall Time | | $t_f$ | – | 29 | 55 | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.2 Adc, $V_{GS}$ = –2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | – | ns |
| Rise Time | | $t_r$ | – | 40 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc) | $Q_{tot}$ | – | 10 | 18 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 5.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 8.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.88<br>–0.75 | –1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 37 | – | ns |
| | | $t_a$ | – | 16 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.025 | – | µC |

**SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 8.)

| Characteristic | Condition | Symbol | $T_J$ = 25°C | $T_J$ = 125°C | Unit |
|---|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage | $I_F$ = 1.0 Adc<br>$I_F$ = 2.0 Adc | $V_F$ | 0.47<br>0.58 | 0.39<br>0.53 | Volts |
| Maximum Instantaneous Reverse Current | $V_R$ = 20 Vdc | $I_R$ | 0.05 | 10 | mA |
| Maximum Voltage Rate of Change | $V_R$ = 20 Vdc | dV/dt | 10,000 | | V/µs |

7. Handling precautions to protect against electrostatic discharge is mandatory.
8. Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.
9. Switching characteristics are independent of operating junction temperature.

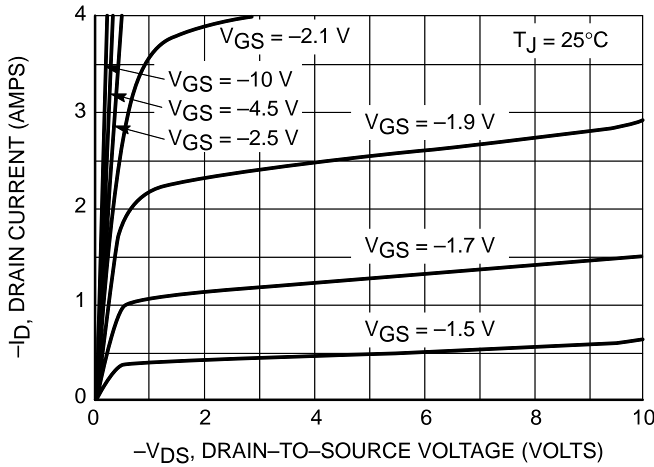



**Figure 1. On–Region Characteristics.**

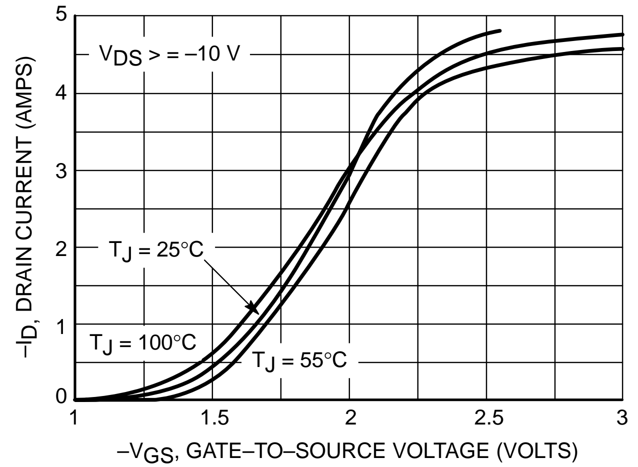



**Figure 2. Transfer Characteristics.**

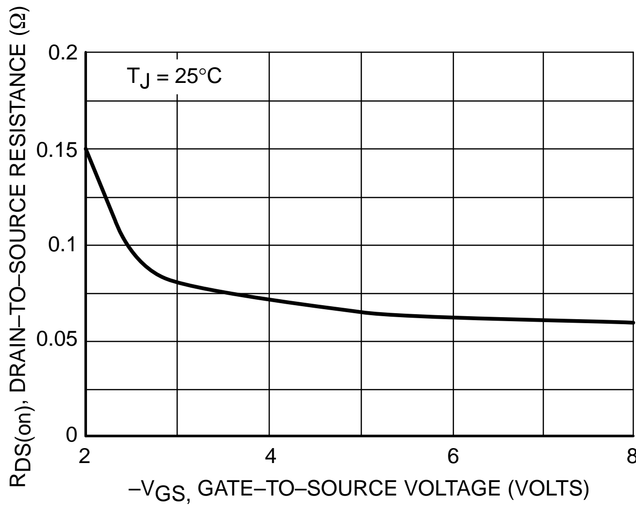



**Figure 3. On–Resistance vs. Gate–to–Source Voltage.**

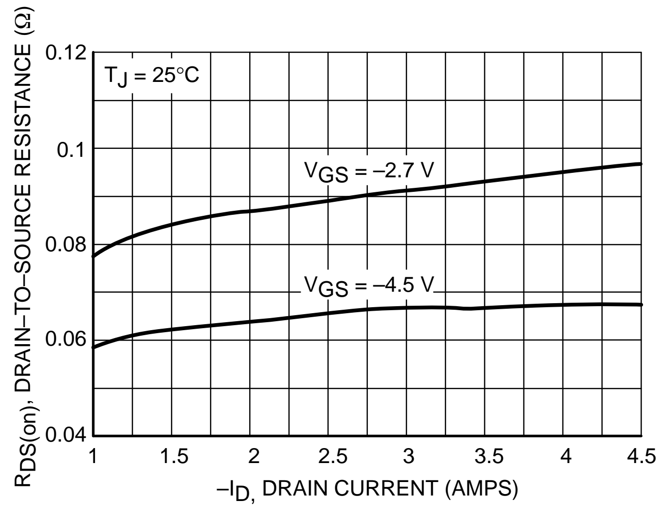



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage.**

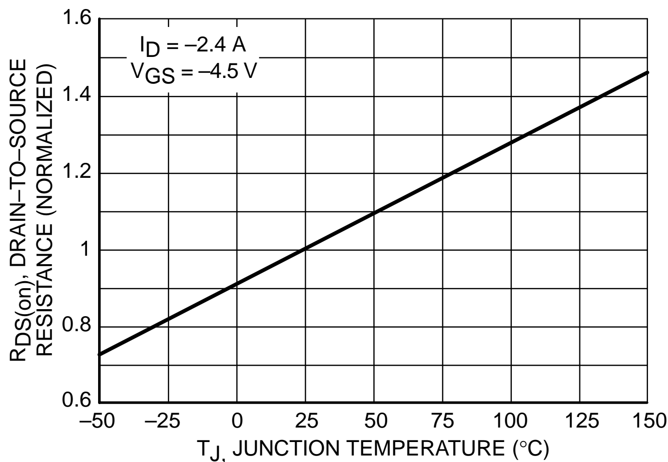



**Figure 5. On–Resistance Variation with Temperature.**

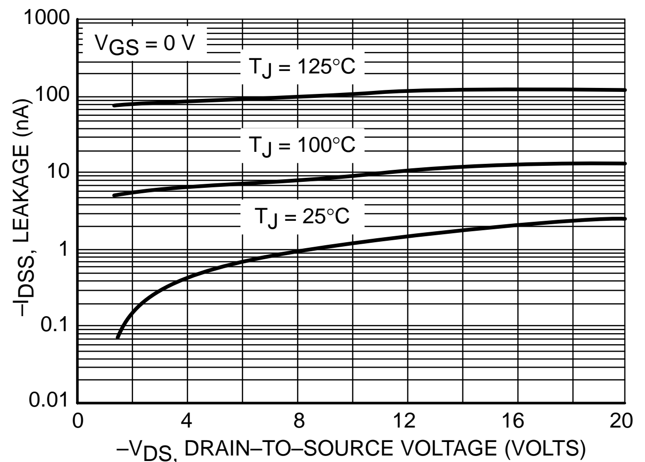



**Figure 6. Drain–to–Source Leakage Current vs. Voltage.**

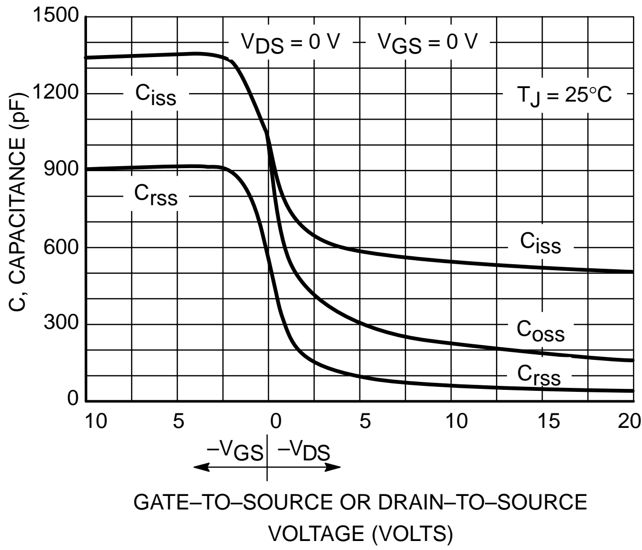



**Figure 7. Capacitance Variation**

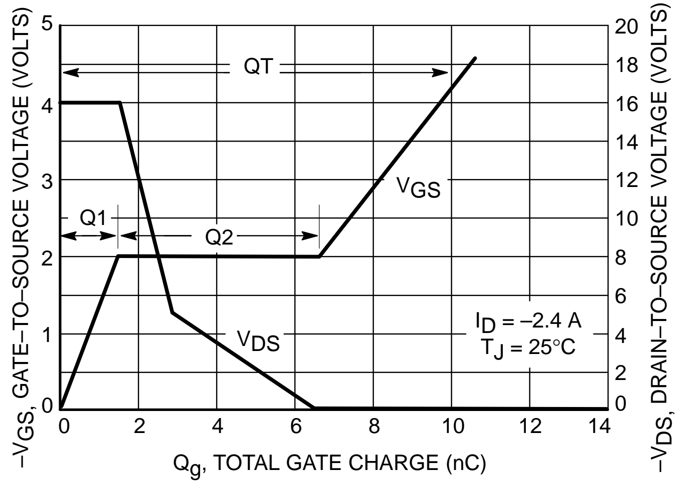



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

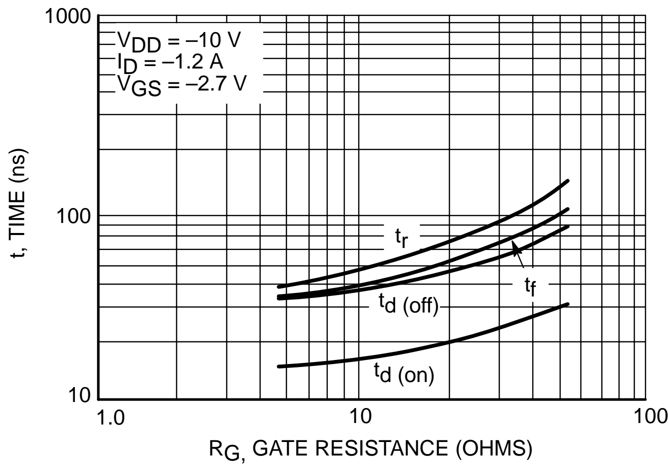



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

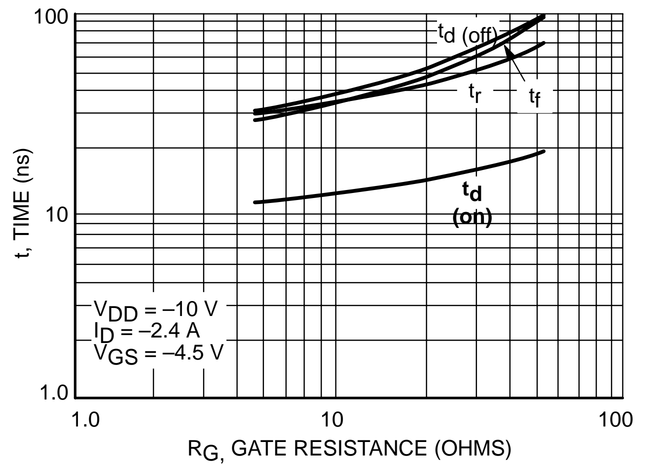



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

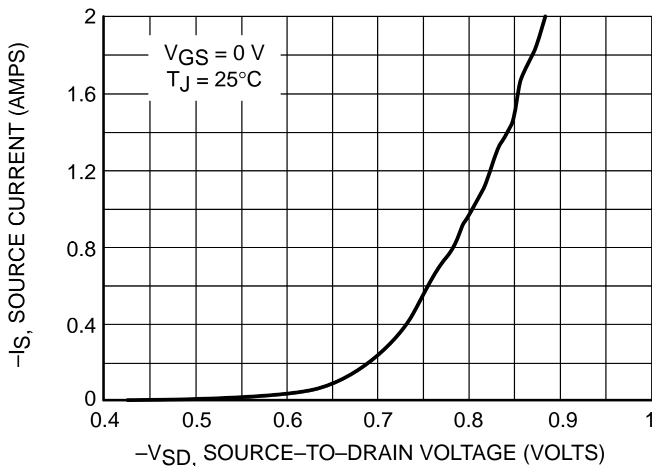



**Figure 11. Diode Forward Voltage versus Current**

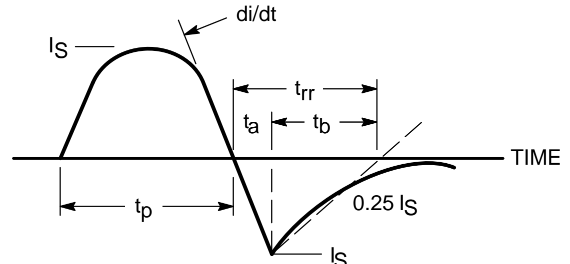



**Figure 12. Diode Reverse Recovery Waveform**

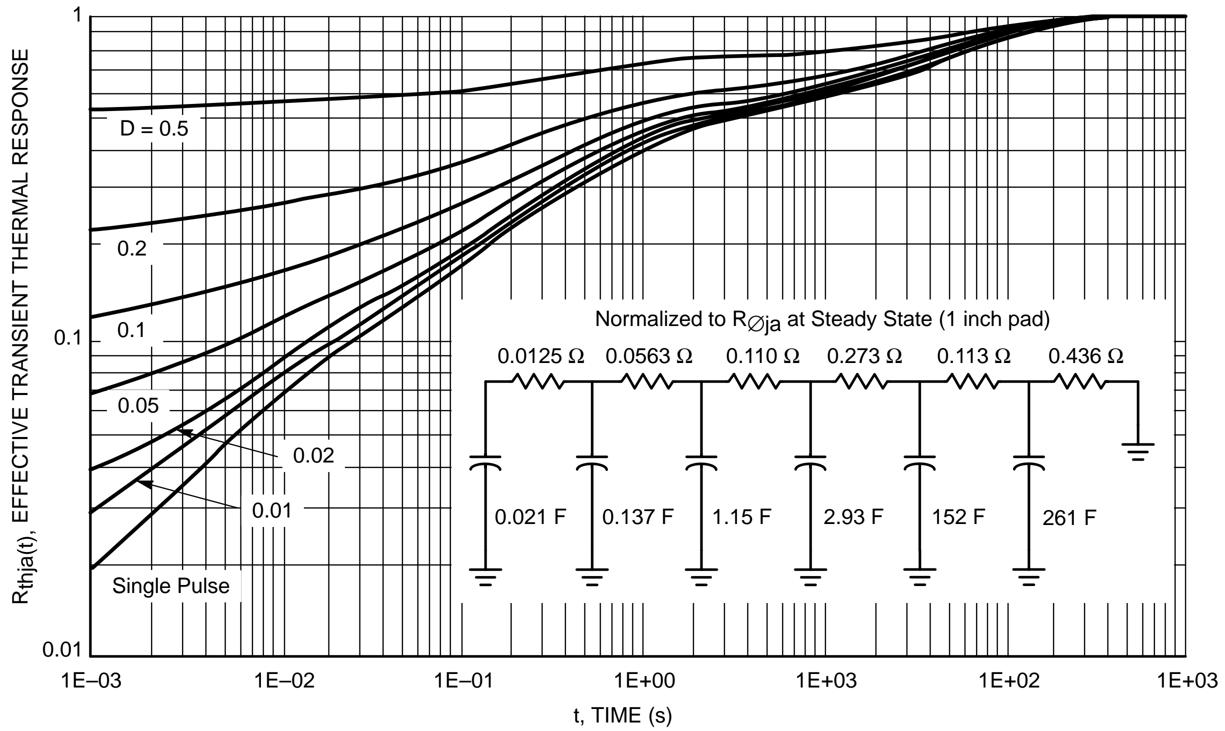



**Figure 13. FET Thermal Response**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

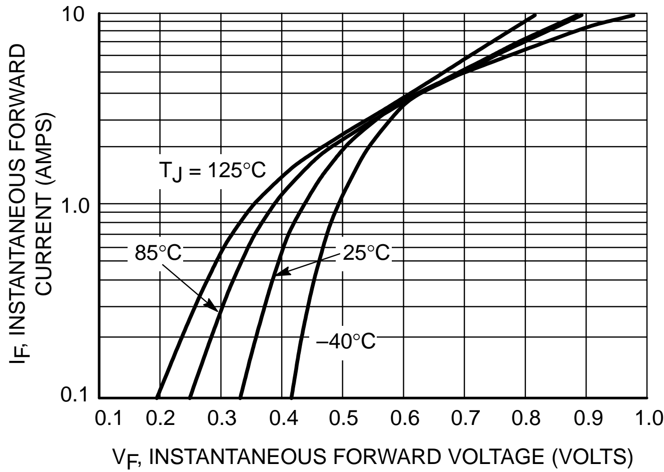



**Figure 14. Typical Forward Voltage**

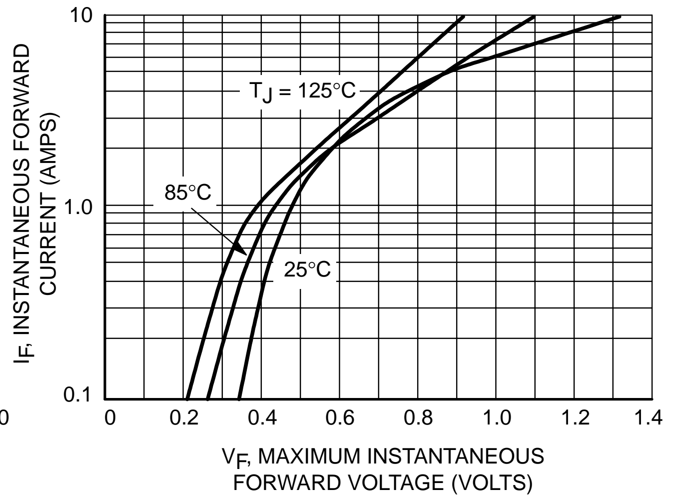



**Figure 15. Maximum Forward Voltage**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

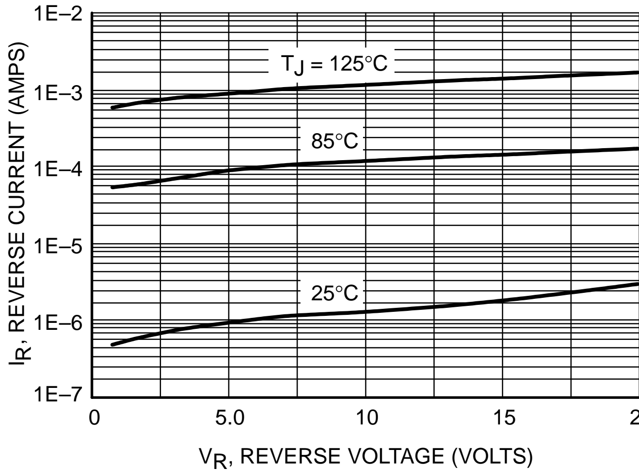



**Figure 16. Typical Reverse Current**

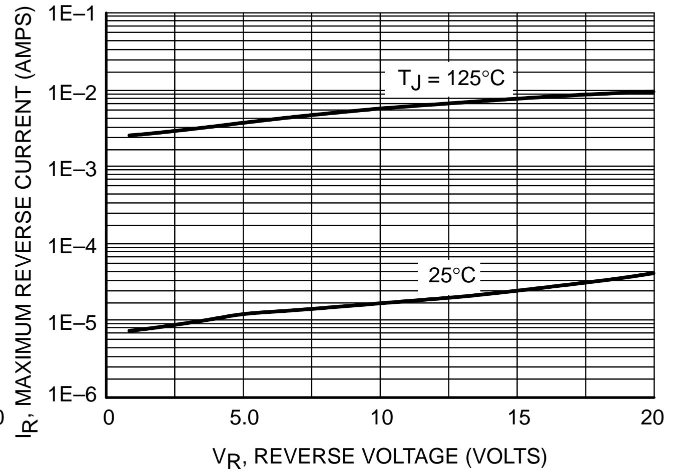



**Figure 17. Maximum Reverse Current**

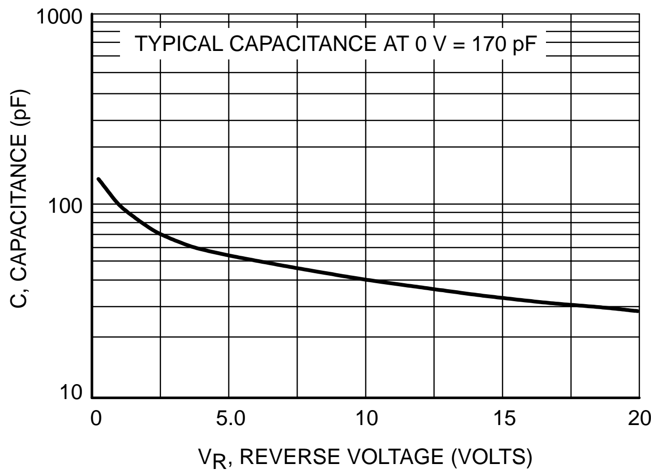



**Figure 18. Typical Capacitance**

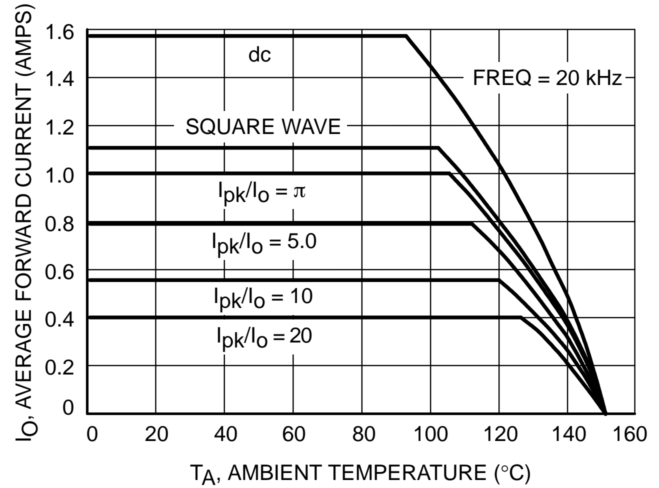



**Figure 19. Current Derating**

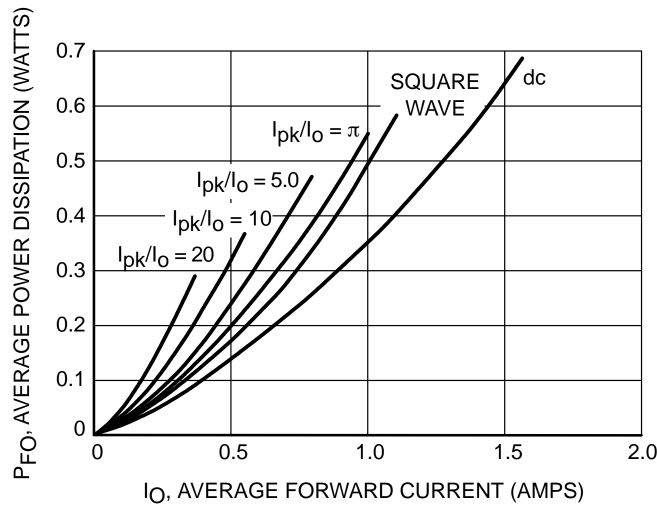



**Figure 20. Forward Power Dissipation**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

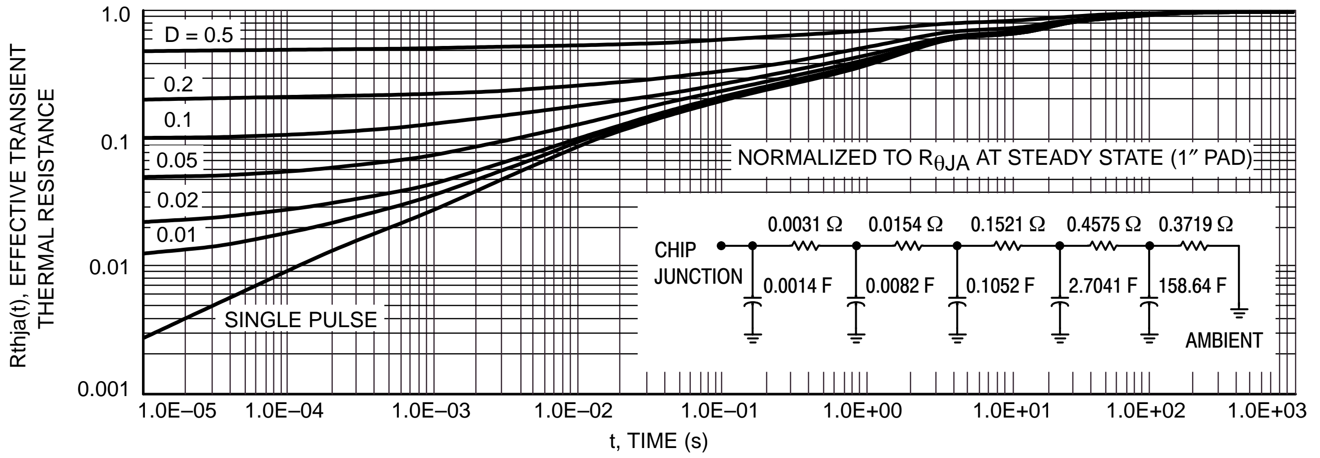
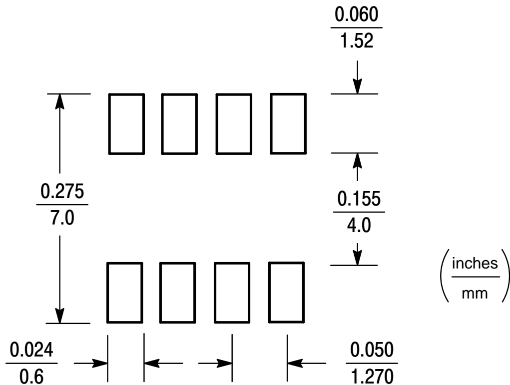



**Figure 21. Schottky Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 22 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

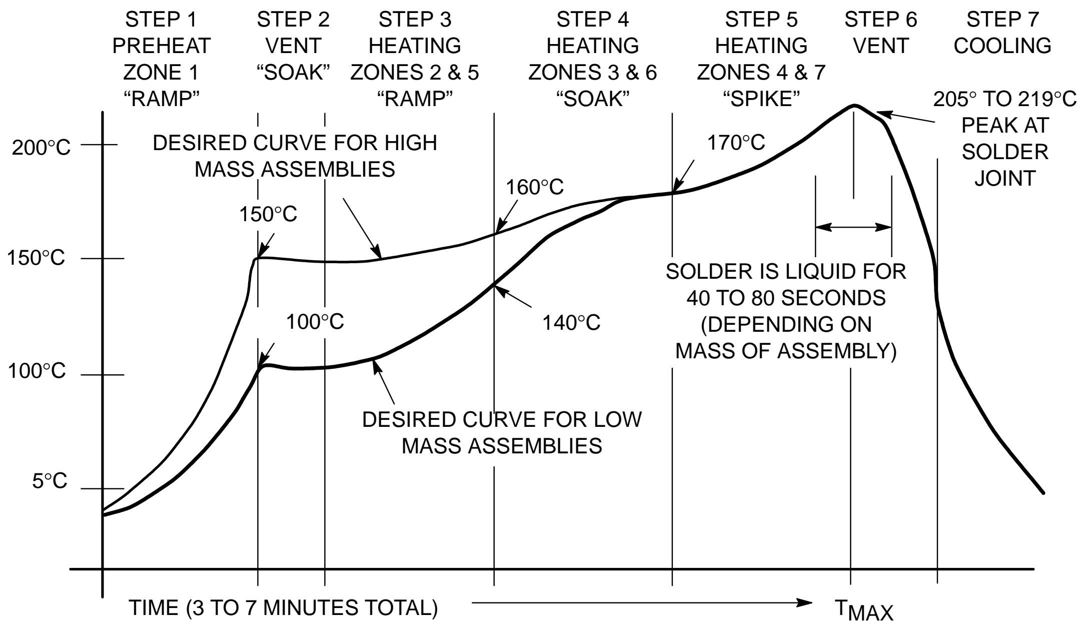



**Figure 22. Typical Solder Heating Profile**

# NTMSD3P102R2

*Product Preview*

**FETKY™**

## P–Channel Enhancement–Mode Power MOSFET and Schottky Diode Dual SO–8 Package

**ON Semiconductor™**

**http://onsemi.com**

**MOSFET**
**–3.05 AMPERES**
**–20 VOLTS**
**0.085 Ω @ $V_{GS}$ = –10 V**

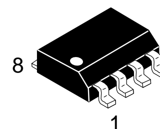
**SCHOTTKY DIODE**
**1.0 AMPERES**
**20 VOLTS**
**470 mV @ $I_F$ = 1.0 A**

### Features

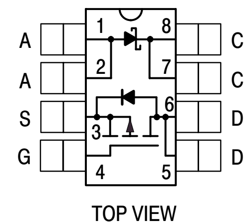
- High Efficiency Components in a Single SO–8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$, Schottky Diode with Low $V_F$
- Independent Pin–Outs for MOSFET and Schottky Die Allowing for Flexibility in Application Use
- Less Component Placement for Board Space Savings
- SO–8 Surface Mount Package, Mounting Information for SO–8 Package Provided

### Applications

- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

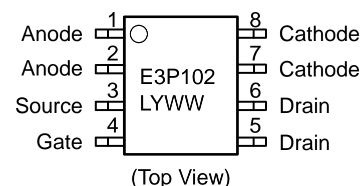



**SO–8**
**CASE 751**
**STYLE 18**




TOP VIEW

**MARKING DIAGRAM & PIN ASSIGNMENTS**




(Top View)

E3P102 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | V |
| Thermal Resistance –<br>Junction–to–Ambient (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>171<br>0.73<br>–2.34<br>–1.87<br>–8.0 | <br>°C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 2.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>100<br>1.25<br>–3.05<br>–2.44<br>–12 | <br>°C/W<br>W<br>A<br>A<br>A |
| Thermal Resistance –<br>Junction–to–Ambient (Note 3.)<br>Total Power Dissipation @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 25°C<br>Continuous Drain Current @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 4.) | <br>$R_{\theta JA}$<br>$P_D$<br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>62.5<br>2.0<br>–3.86<br>–3.10<br>–15 | <br>°C/W<br>W<br>A<br>A<br>A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –7.5 Apk, L = 5 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 140 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMSD3P102R2 | SO–8 | 2500/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**SCHOTTKY MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 20 | V |
| Thermal Resistance – Junction–to–Ambient (Note 5.) | $R_{\theta JA}$ | 204 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 6.) | $R_{\theta JA}$ | 122 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 7.) | $R_{\theta JA}$ | 83 | °C/W |
| Average Forward Current (Note 7.)<br>(Rated $V_R$, $T_A$ = 100°C) | $I_O$ | 1.0 | A |
| Peak Repetitive Forward Current<br>(Note 7.) (Rated $V_R$, Square Wave, 20 kHz, $T_A$ = 105°C) | $I_{FRM}$ | 2.0 | A |
| Non–Repetitive Peak Surge Current (Note 7.)<br>(Surge Applied at Rated Load Conditions, Half–Wave, Single Phase, 60 Hz) | $I_{FSM}$ | 20 | A |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 8.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>–20<br>– | <br>–<br>–30 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = –20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>–1.0<br>–25 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = –20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>–1.0<br>– | <br>–1.7<br>3.6 | <br>–2.5<br>– | Vdc |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc)<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.5 Adc) | $R_{DS(on)}$ | <br>–<br>– | <br>0.063<br>0.090 | <br>0.085<br>0.125 | Ω |
| Forward Transconductance<br>($V_{DS}$ = –15 Vdc, $I_D$ = –3.05 Adc) | $g_{FS}$ | – | 5.0 | – | Mhos |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 518 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 190 | 350 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 70 | 135 | |

5. Minimum FR–4 or G–10 PCB, Steady State.
6. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
7. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
8. Handling precautions to protect against electrostatic discharge is mandatory.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 9.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Notes 10. & 11.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –20 Vdc, $I_D$ = –3.05 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 22 | ns |
| Rise Time | | $t_r$ | – | 16 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 80 | |
| Fall Time | | $t_f$ | – | 45 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = –20 Vdc, $I_D$ = –1.5 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 42 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –20 Vdc, $V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc) | $Q_{tot}$ | – | 16 | 25 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.5 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 10.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.96<br>–0.78 | –1.25<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 34 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

**SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 10.)

| Characteristic | | Symbol | $T_J$ = 25°C | $T_J$ = 125°C | Unit |
|---|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage | $I_F$ = 1.0 Adc<br>$I_F$ = 2.0 Adc | $V_F$ | 0.47<br>0.58 | 0.39<br>0.53 | Volts |
| Maximum Instantaneous Reverse Current | $V_R$ = 20 Vdc | $I_R$ | 0.05 | 10 | mA |
| Maximum Voltage Rate of Change | $V_R$ = 20 Vdc | dV/dt | 10,000 | | V/μs |

9. Handling precautions to protect against electrostatic discharge is mandatory.
10. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
11. Switching characteristics are independent of operating junction temperature.

## TYPICAL MOSFET ELECTRICAL CHARACTERISTICS

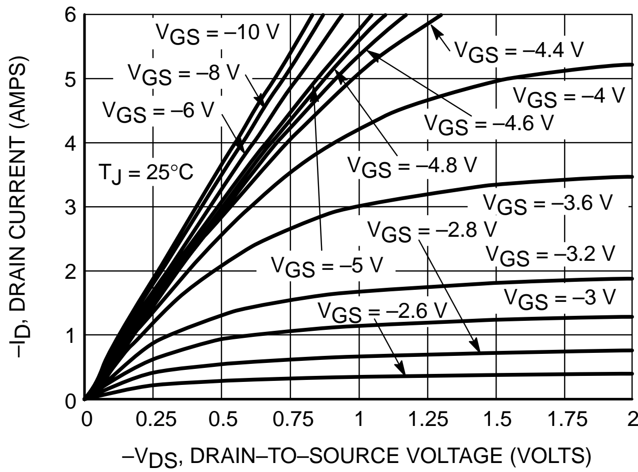



**Figure 1. On–Region Characteristics**

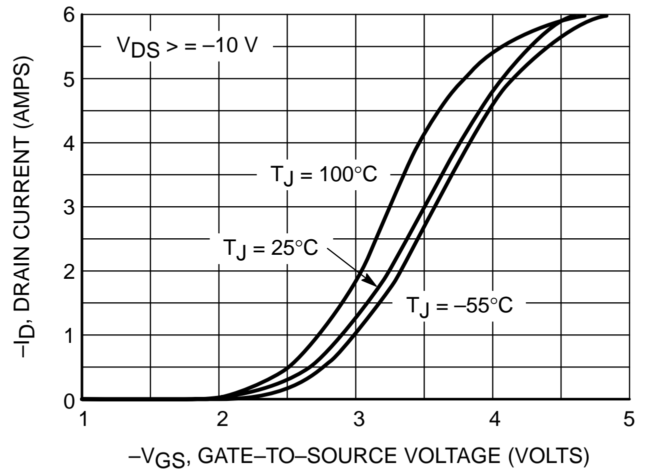



**Figure 2. Transfer Characteristics**

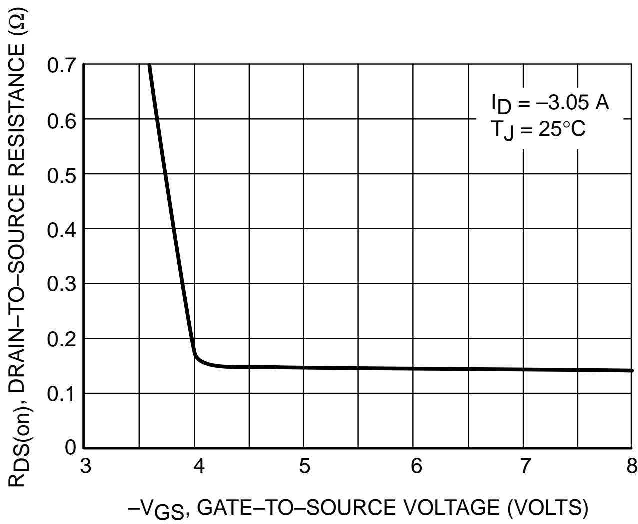



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

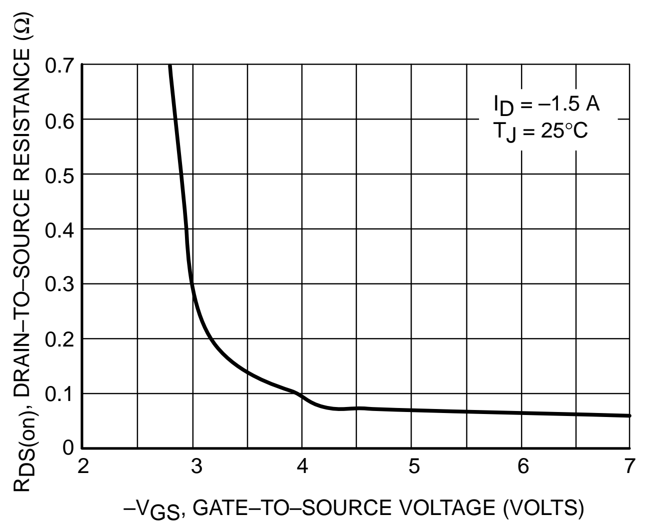



**Figure 4. On–Resistance vs. Gate–to–Source Voltage**

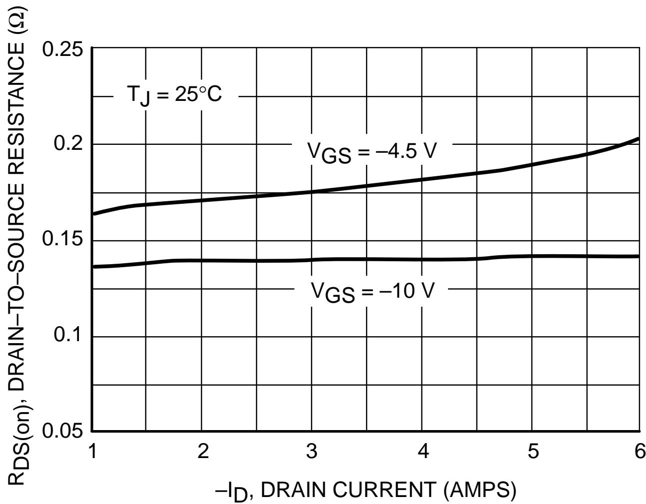



**Figure 5. On–Resistance vs. Drain Current and Gate Voltage**

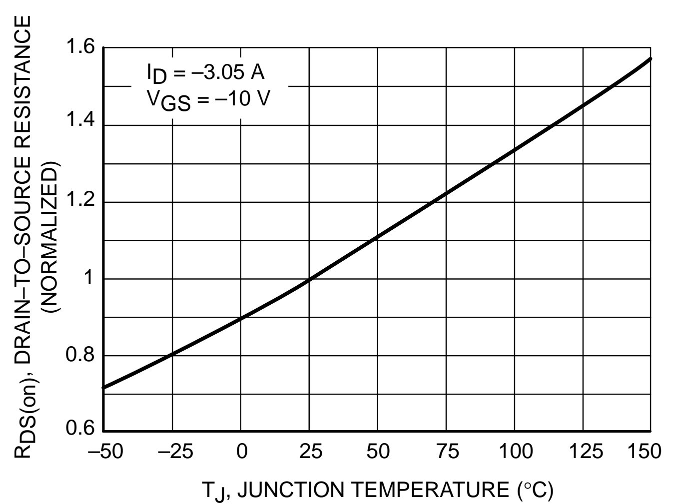



**Figure 6. On Resistance Variation with Temperature**

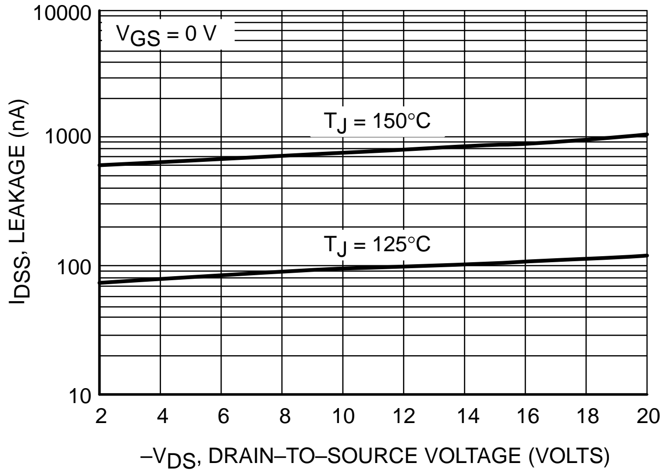



**Figure 7. Drain–to–Source Leakage Current vs. Voltage**

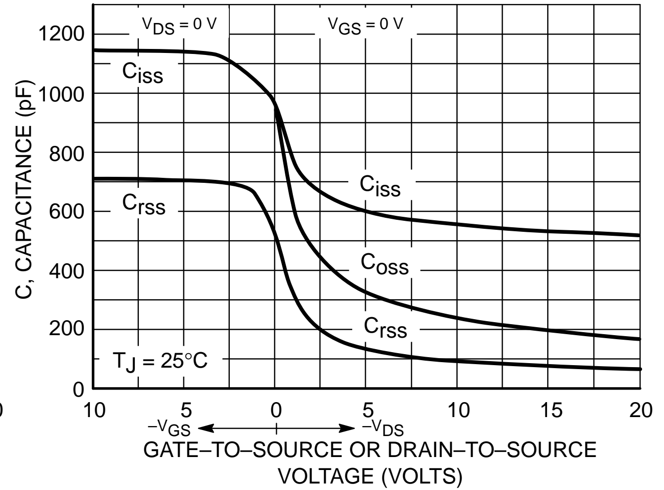



**Figure 8. Capacitance Variation**

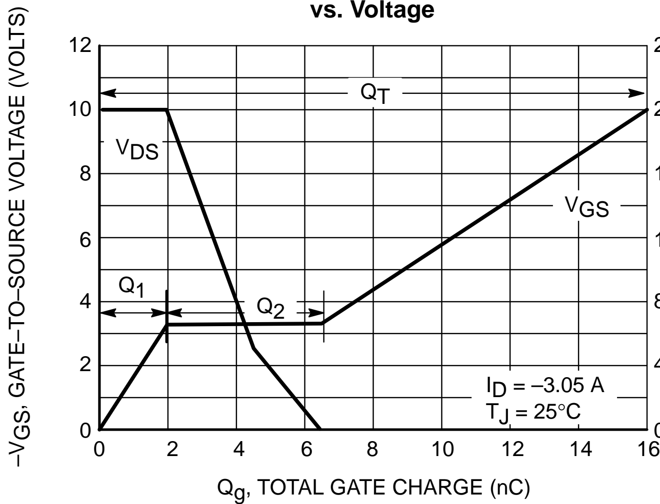



**Figure 9. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

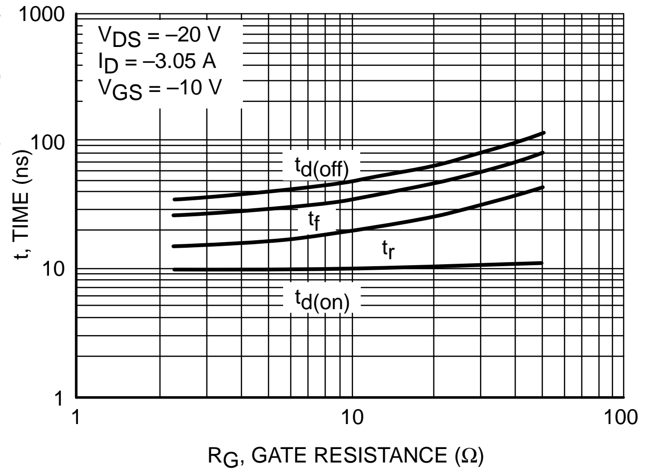



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

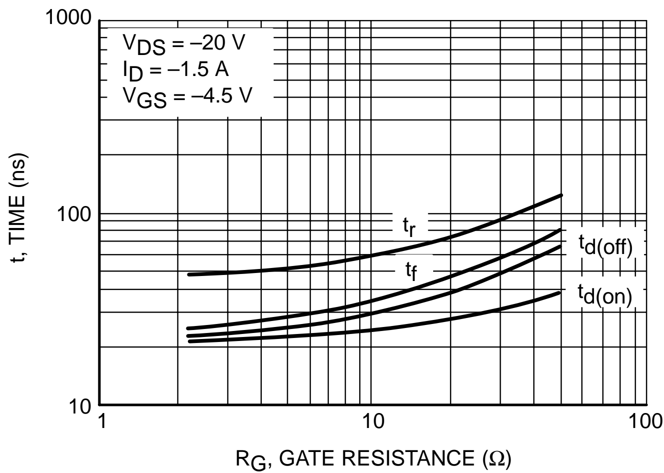



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

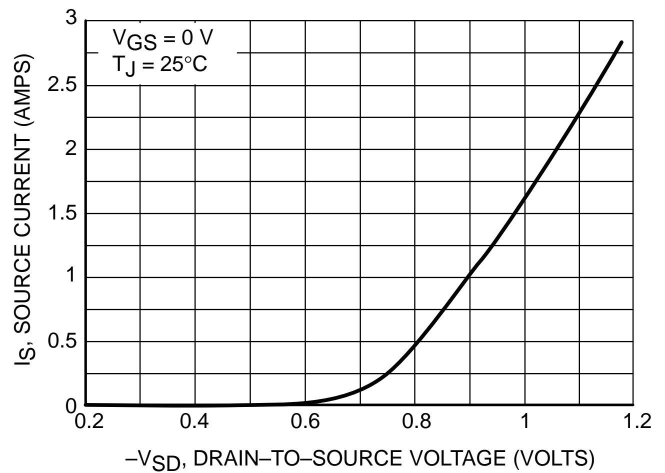



**Figure 12. Diode Forward Voltage vs. Current**

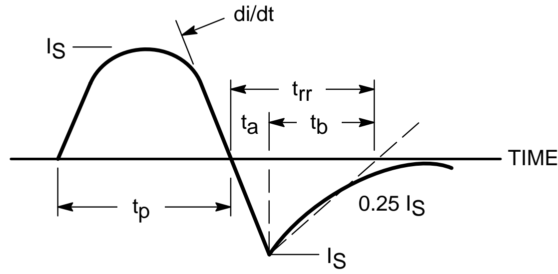



**Figure 13. Diode Reverse Recovery Waveform**

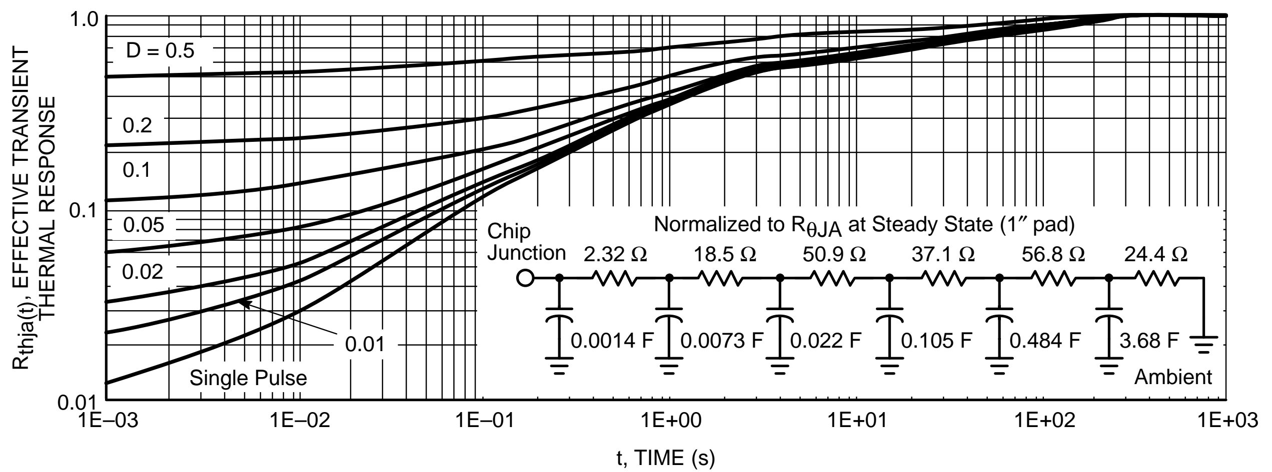



**Figure 14. FET Thermal Response**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

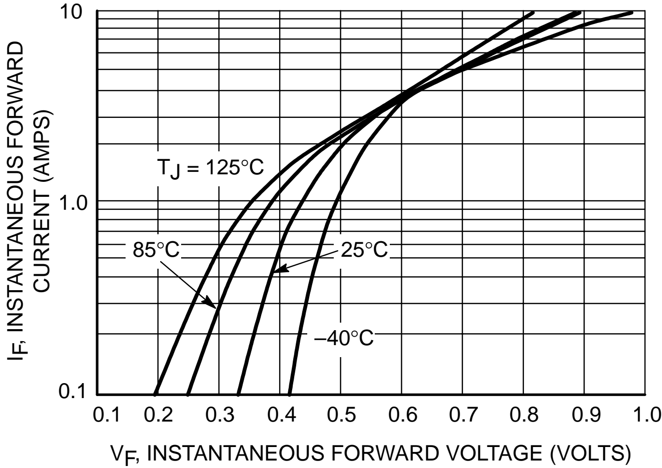



**Figure 15. Typical Forward Voltage**

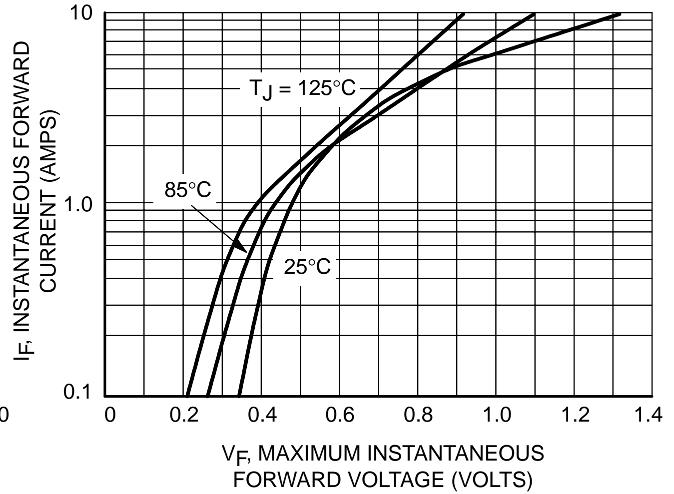



**Figure 16. Maximum Forward Voltage**

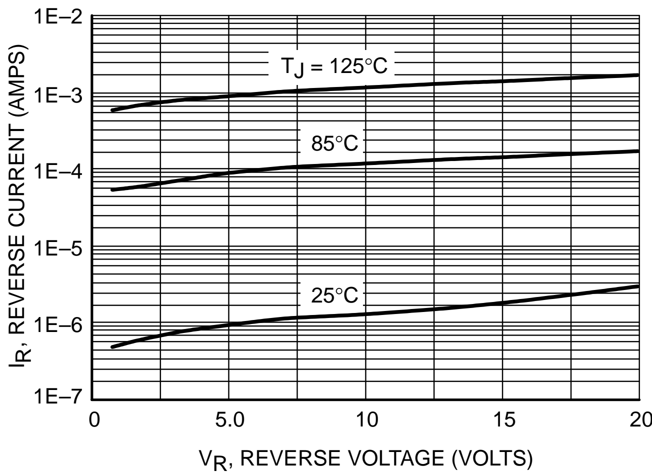



**Figure 17. Typical Reverse Current**

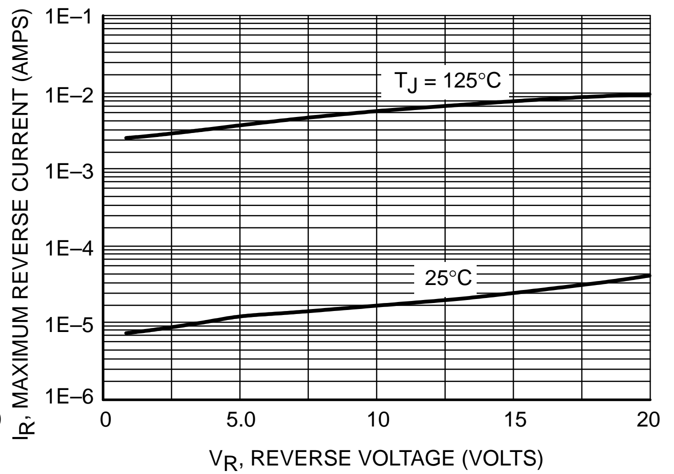



**Figure 18. Maximum Reverse Current**

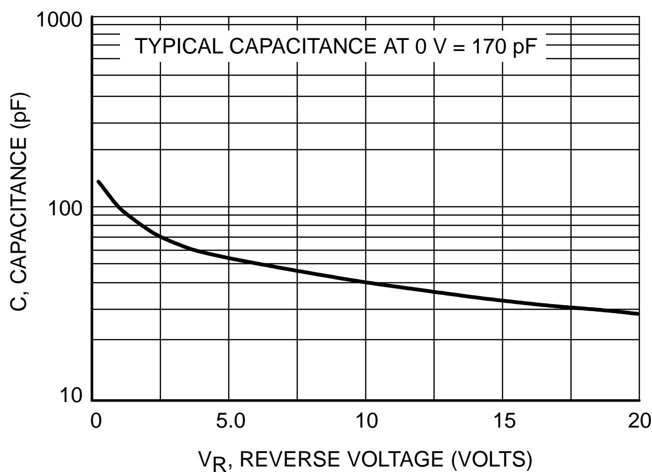



**Figure 19. Typical Capacitance**

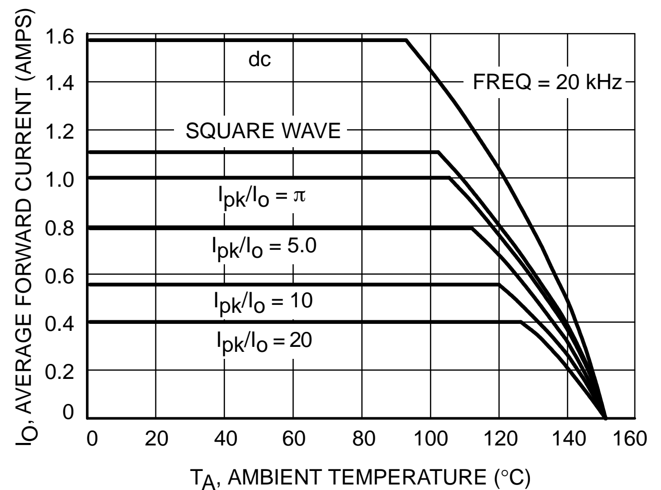



**Figure 20. Current Derating**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

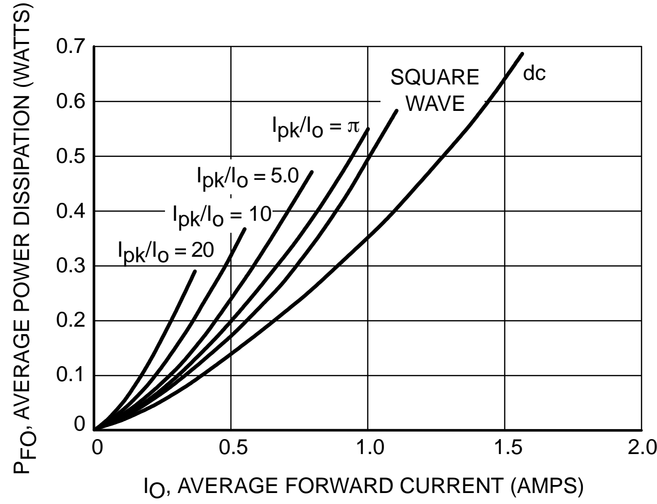



**Figure 21. Forward Power Dissipation**

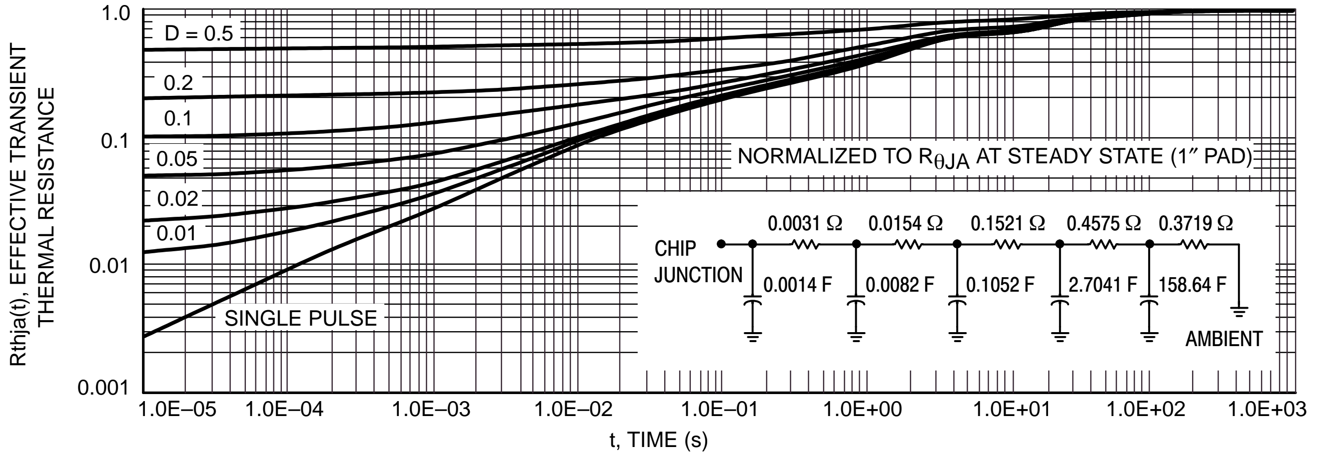
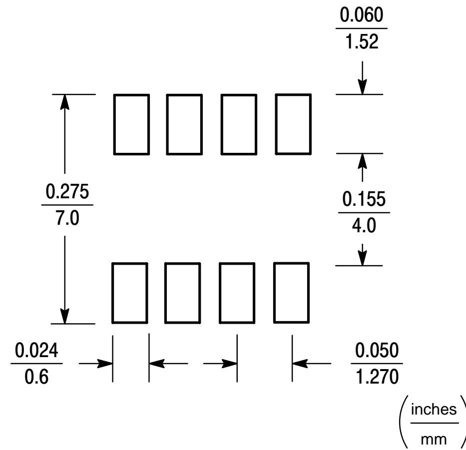



**Figure 22. Schottky Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 23 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

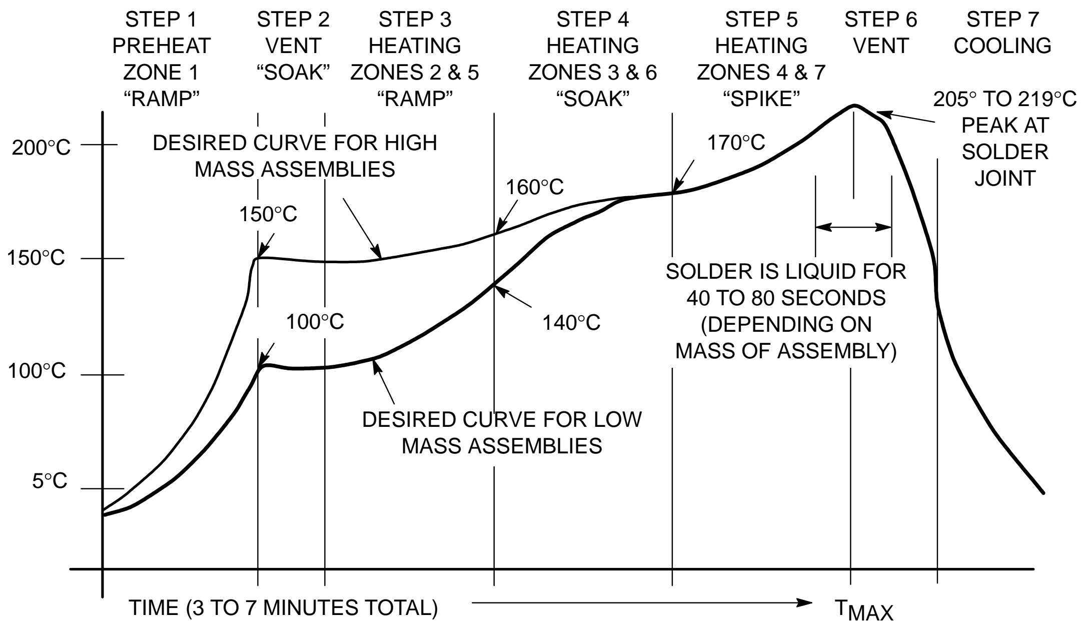



**Figure 23. Typical Solder Heating Profile**

# NTMSD3P303R2

**ON Semiconductor™**

http://onsemi.com

*Product Preview*

## FETKY™

## P–Channel Enhancement–Mode Power MOSFET and Schottky Diode Dual SO–8 Package

**Features**

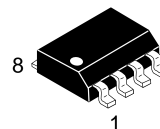
- High Efficiency Components in a Single SO–8 Package
- High Density Power MOSFET with Low $R_{DS(on)}$, Schottky Diode with Low $V_F$
- Independent Pin–Outs for MOSFET and Schottky Die Allowing for Flexibility in Application Use
- Less Component Placement for Board Space Savings
- SO–8 Surface Mount Package, Mounting Information for SO–8 Package Provided

**Applications**

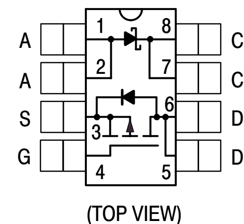
- DC–DC Converters
- Low Voltage Motor Control
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

**MOSFET**
**–3.05 AMPERES**
**–30 VOLTS**
**0.085 Ω @ $V_{GS}$ = –10 V**

**SCHOTTKY DIODE**
**3.0 AMPERES**
**30 VOLTS**
**420 mV @ $I_F$ = 3.0 A**

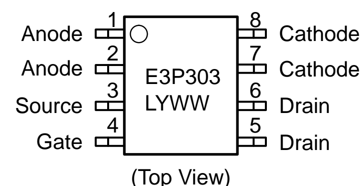



**SO–8**
**CASE 751**
**STYLE 18**




(TOP VIEW)

**MARKING DIAGRAM & PIN ASSIGNMENTS**




(Top View)

E3P303 = Device Code
L = Assembly Location
Y = Year
WW = Work Week

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –30 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 171 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.73 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.34 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.87 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –8.0 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 100 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.25 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.05 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –2.44 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –12 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.86 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –3.10 | A |
| Pulsed Drain Current (Note 4.) | $I_{DM}$ | –15 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –30 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –7.5 Apk, L = 5 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 140 | mJ |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
4. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTMSD3P303R2 | SO–8 | 2500/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**SCHOTTKY MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 30 | V |
| Thermal Resistance – Junction–to–Ambient (Note 5.) | $R_{\theta JA}$ | 197 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 6.) | $R_{\theta JA}$ | 97 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 7.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Average Forward Current (Note 7.)<br>(Rated $V_R$, $T_A$ = 100°C) | $I_O$ | 3.0 | A |
| Peak Repetitive Forward Current (Note 7.)<br>(Rated $V_R$, Square Wave, 20 kHz, $T_A$ = 105°C) | $I_{FRM}$ | 6.0 | A |
| Non–Repetitive Peak Surge Current (Note 7.)<br>(Surge Applied at Rated Load Conditions, Half–Wave, Single Phase, 60 Hz) | $I_{FSM}$ | 30 | A |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 8.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>–30<br>– | <br>–<br>–30 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = –30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 25°C)<br>($V_{DS}$ = –30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>–1.0<br>–25 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = –20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | <br>– | <br>– | <br>–100 | nAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>–1.0<br>– | <br>–1.7<br>3.6 | <br>–2.5<br>– | Vdc |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc)<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.5 Adc) | $R_{DS(on)}$ | <br>–<br>– | <br>0.063<br>0.090 | <br>0.085<br>0.125 | Ω |
| Forward Transconductance<br>($V_{DS}$ = –15 Vdc, $I_D$ = –3.05 Adc) | $g_{FS}$ | <br>– | <br>5.0 | <br>– | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 520 | 750 | pF |
| Output Capacitance | $C_{oss}$ | – | 170 | 325 | |
| Reverse Transfer Capacitance | $C_{rss}$ | – | 70 | 135 | |

5. Minimum FR–4 or G–10 PCB, Steady State.
6. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
7. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), t ≤ 10 seconds.
8. Handling precautions to protect against electrostatic discharge is mandatory.

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 9.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Notes 10. & 11.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –3.05 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 22 | ns |
| Rise Time | | $t_r$ | – | 16 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 80 | |
| Fall Time | | $t_f$ | – | 45 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –1.5 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 42 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = –10 Vdc, $I_D$ = –3.05 Adc) | $Q_{tot}$ | – | 16 | 25 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.5 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 10.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.96<br>–0.78 | –1.25<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –3.05 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 34 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | µC |

**SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 10.)

| Characteristic | Condition | Symbol | $T_J$ = 25°C | $T_J$ = 125°C | Unit |
|---|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage | $I_F$ = 100 mAdc<br>$I_F$ = 3.0 Adc<br>$I_F$ = 6.0 Adc | $V_F$ | 0.28<br>0.42<br>0.50 | 0.13<br>0.33<br>0.45 | Volts |
| Maximum Instantaneous Reverse Current | $V_R$ = 30 Vdc | $I_R$ | 250 | 25 | µA<br>mA |
| Maximum Voltage Rate of Change | $V_R$ = 30 Vdc | dV/dt | 10,000 | | V/µs |

9. Handling precautions to protect against electrostatic discharge is mandatory.
10. Indicates Pulse Test: Pulse Width = 300 µs max, Duty Cycle = 2%.
11. Switching characteristics are independent of operating junction temperature.

## TYPICAL MOSFET ELECTRICAL CHARACTERISTICS

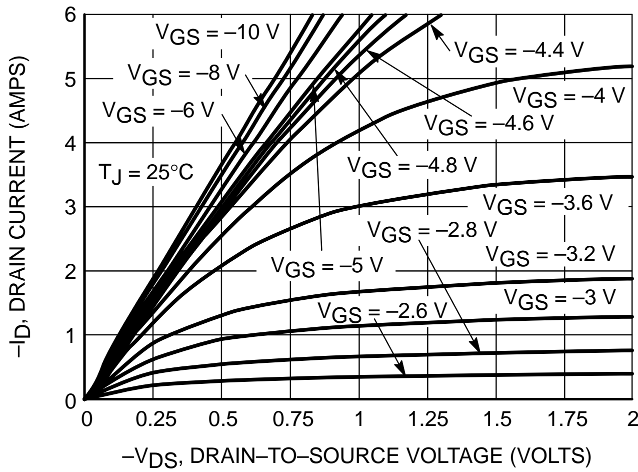



**Figure 1. On–Region Characteristics**

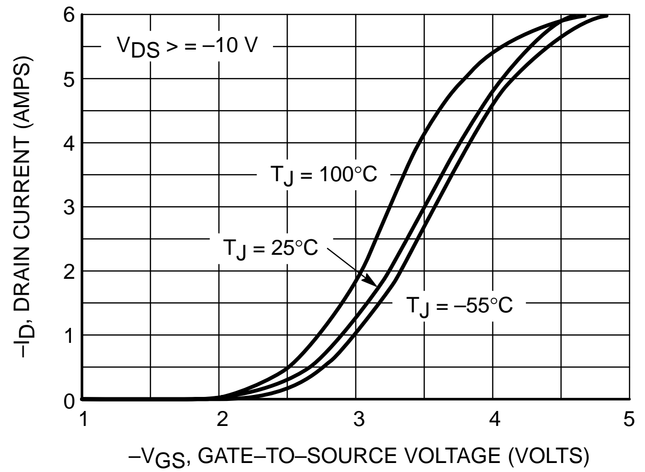



**Figure 2. Transfer Characteristics**

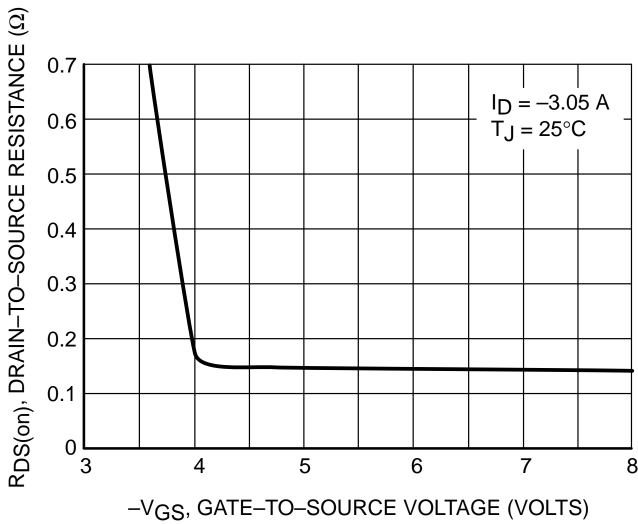



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

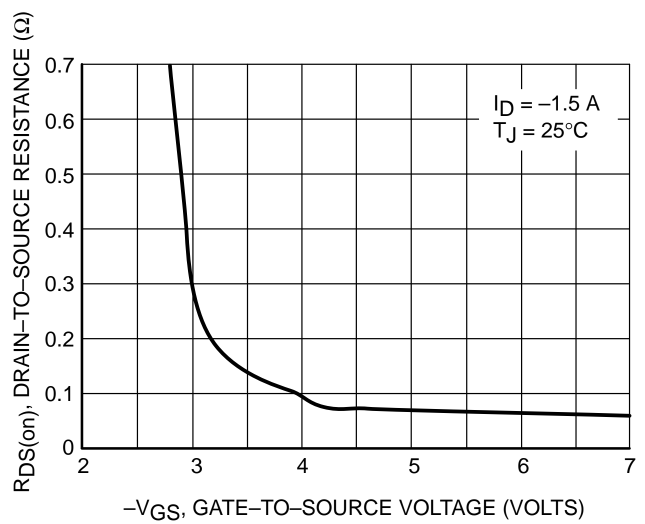



**Figure 4. On–Resistance vs. Gate–to–Source Voltage**

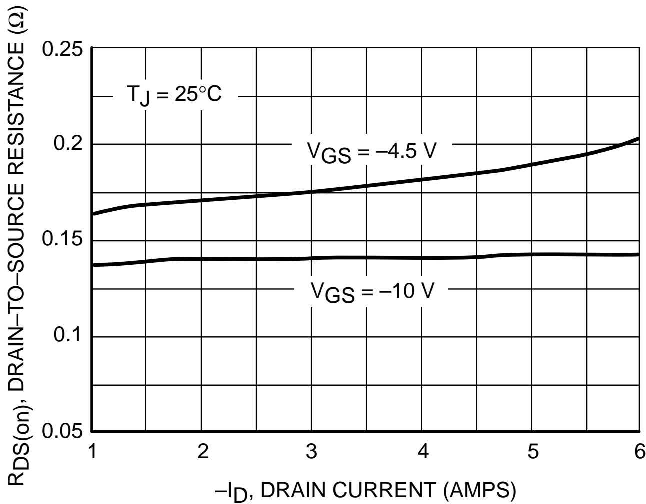



**Figure 5. On–Resistance vs. Drain Current and Gate Voltage**

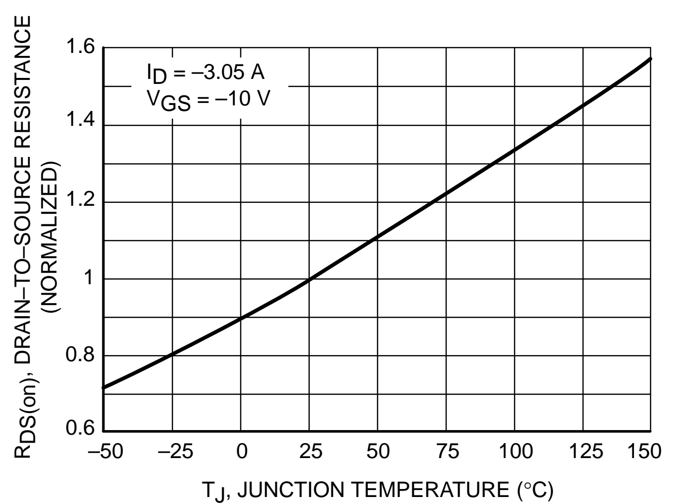



**Figure 6. On Resistance Variation with Temperature**

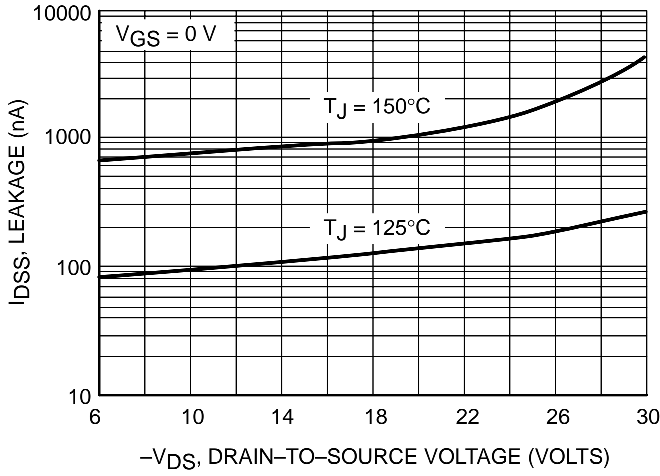



**Figure 7. Drain–to–Source Leakage Current vs. Voltage**

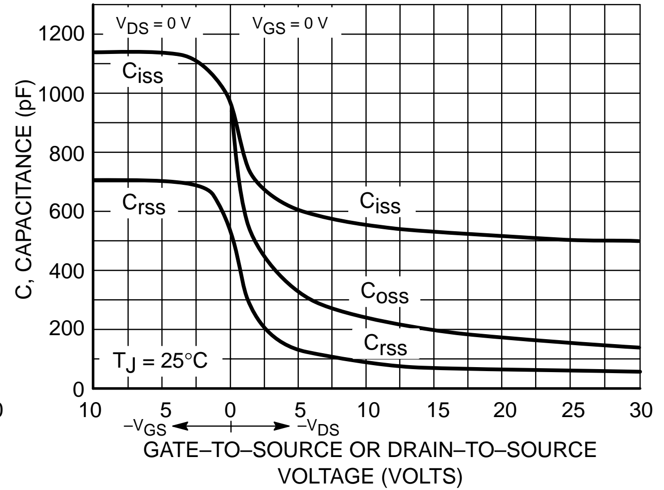



**Figure 8. Capacitance Variation**

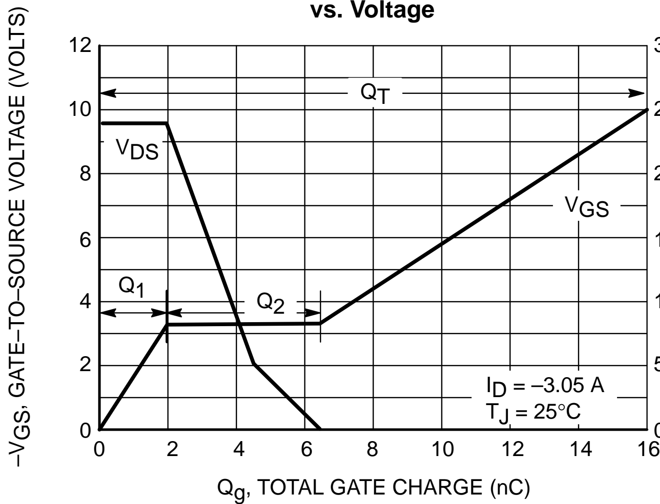



**Figure 9. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

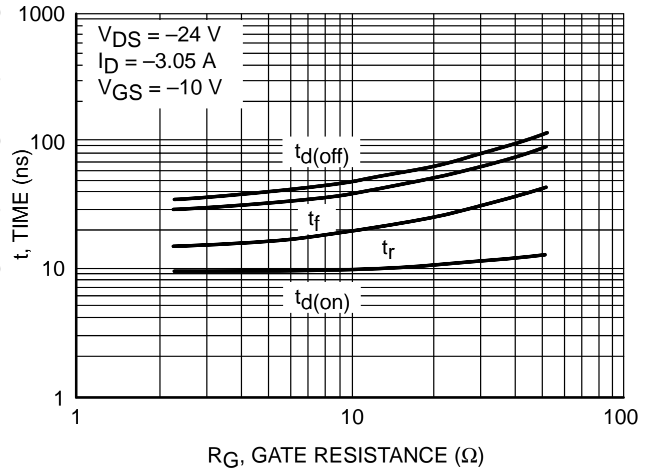



**Figure 10. Resistive Switching Time Variation vs. Gate Resistance**

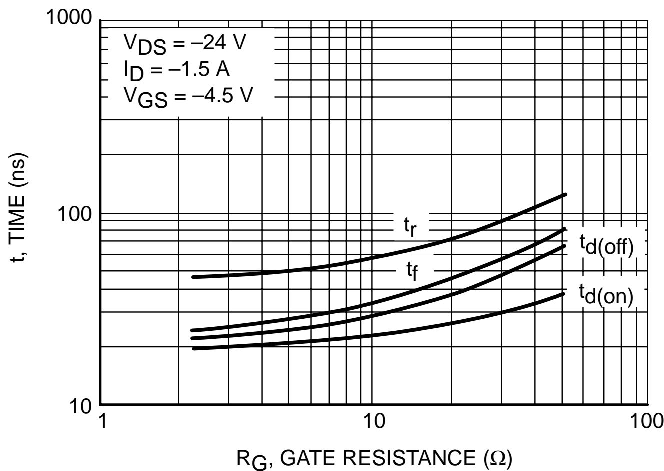



**Figure 11. Resistive Switching Time Variation vs. Gate Resistance**

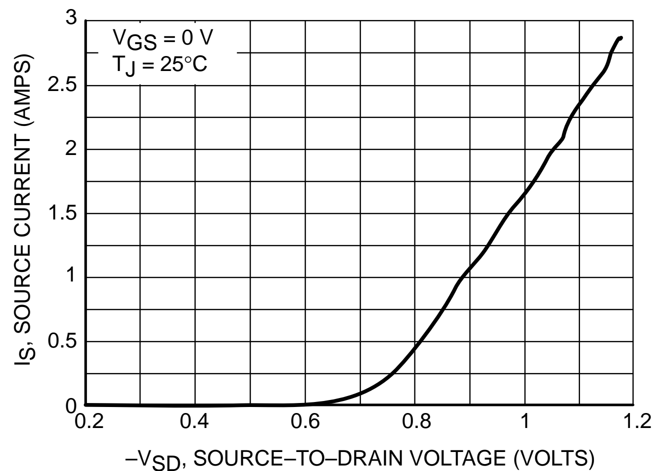



**Figure 12. Diode Forward Voltage vs. Current**

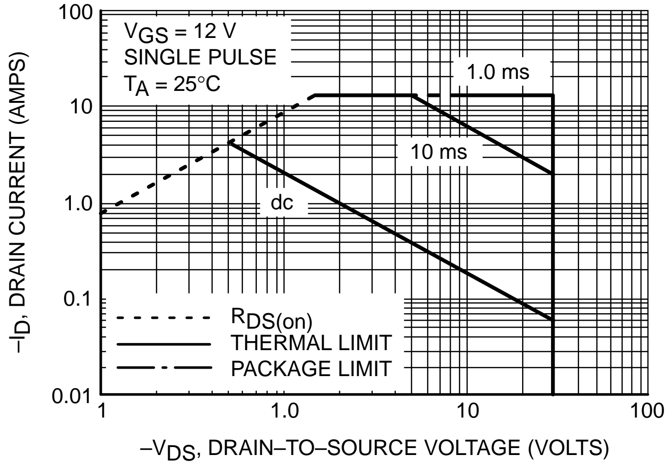



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

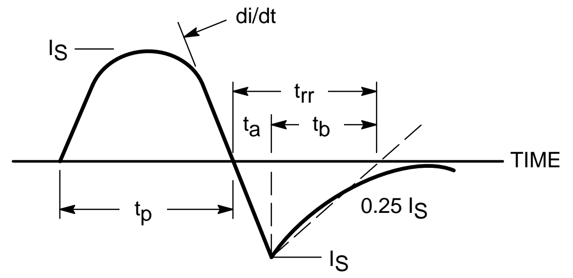



**Figure 14. Diode Reverse Recovery Waveform**

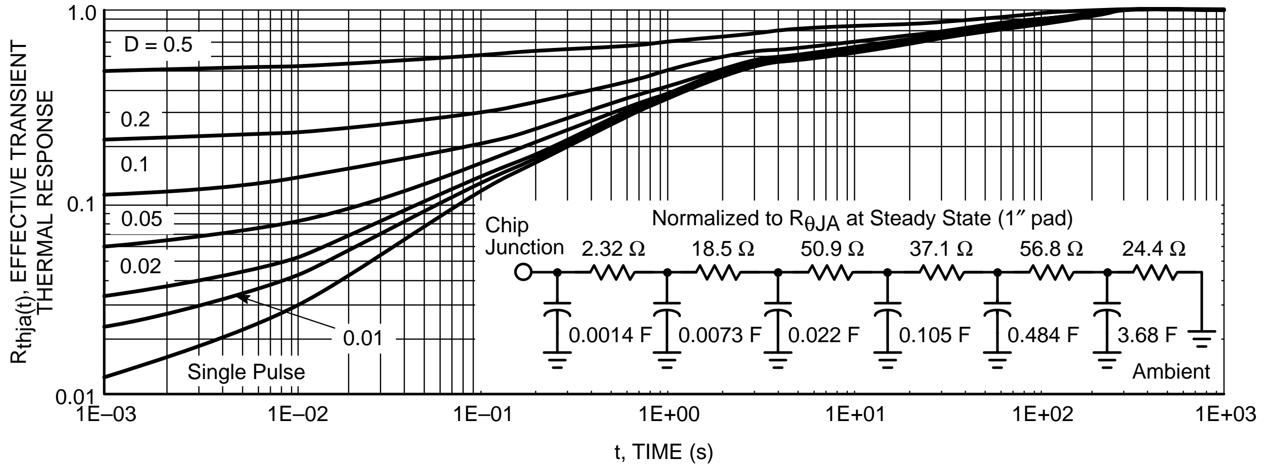



**Figure 15. FET Thermal Response**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

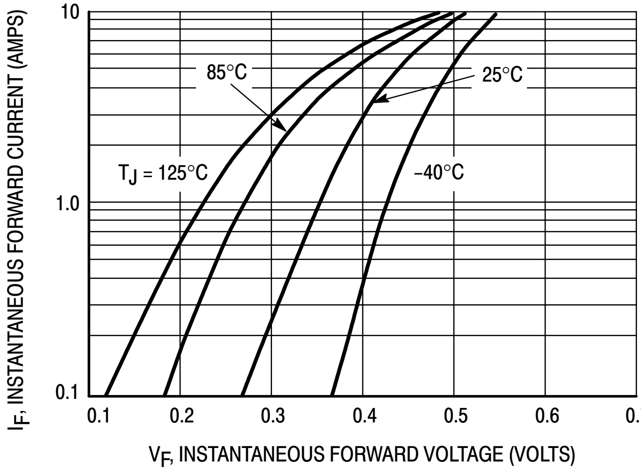



**Figure 16. Typical Forward Voltage**

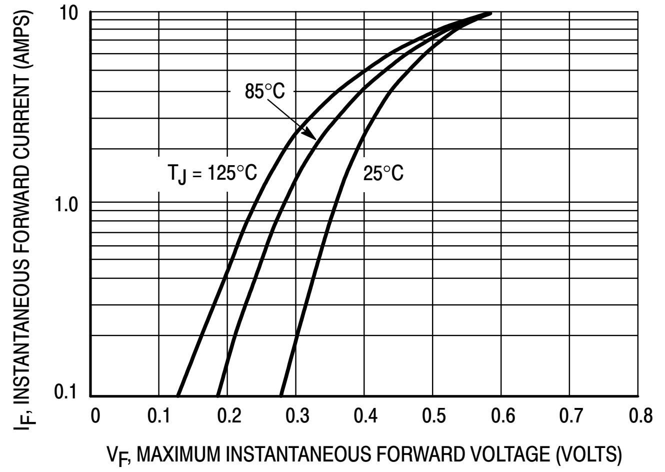



**Figure 17. Maximum Forward Voltage**

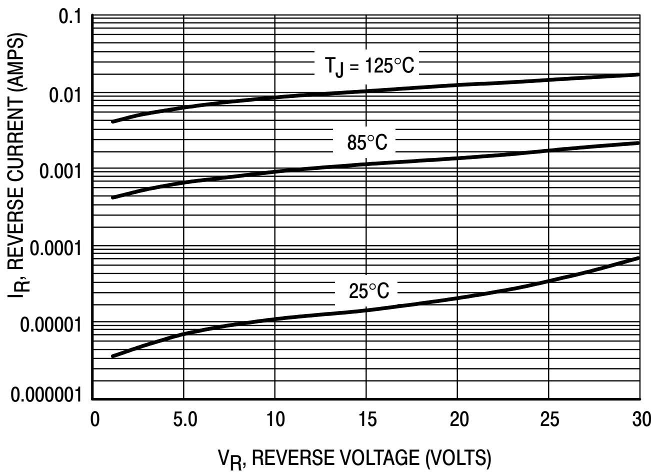



**Figure 18. Typical Reverse Current**

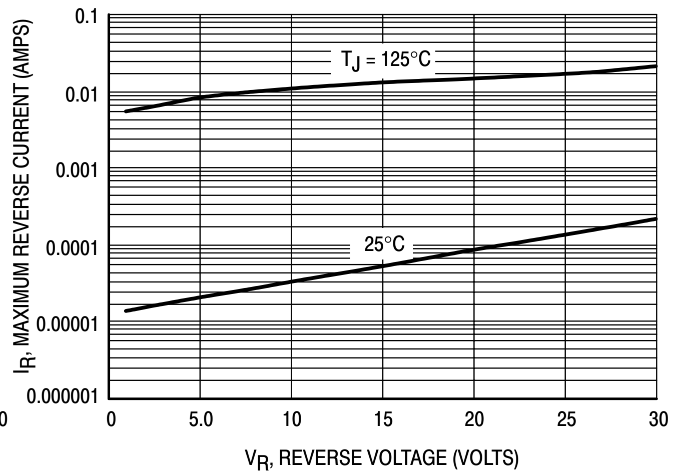



**Figure 19. Maximum Reverse Current**

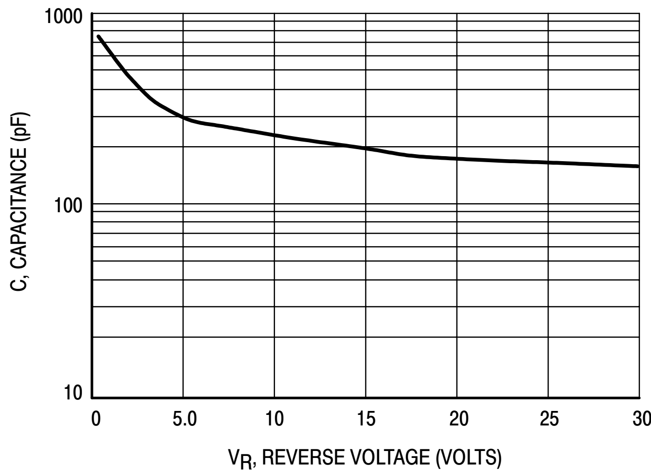



**Figure 20. Typical Capacitance**

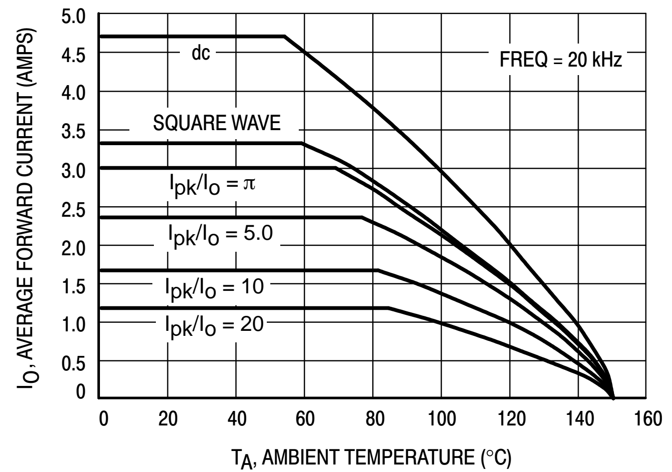



**Figure 21. Current Derating**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

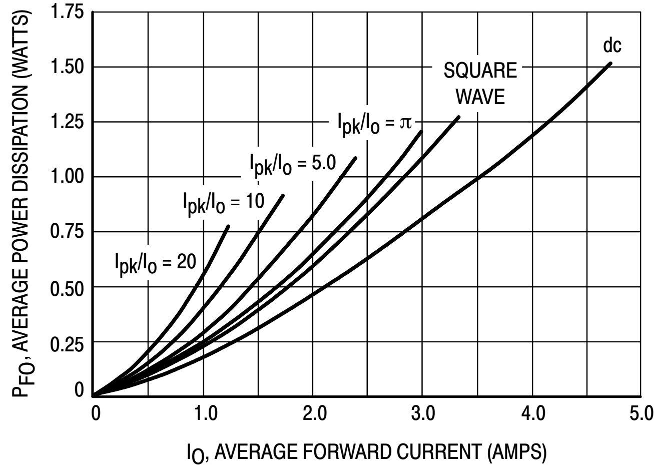



**Figure 22. Forward Power Dissipation**

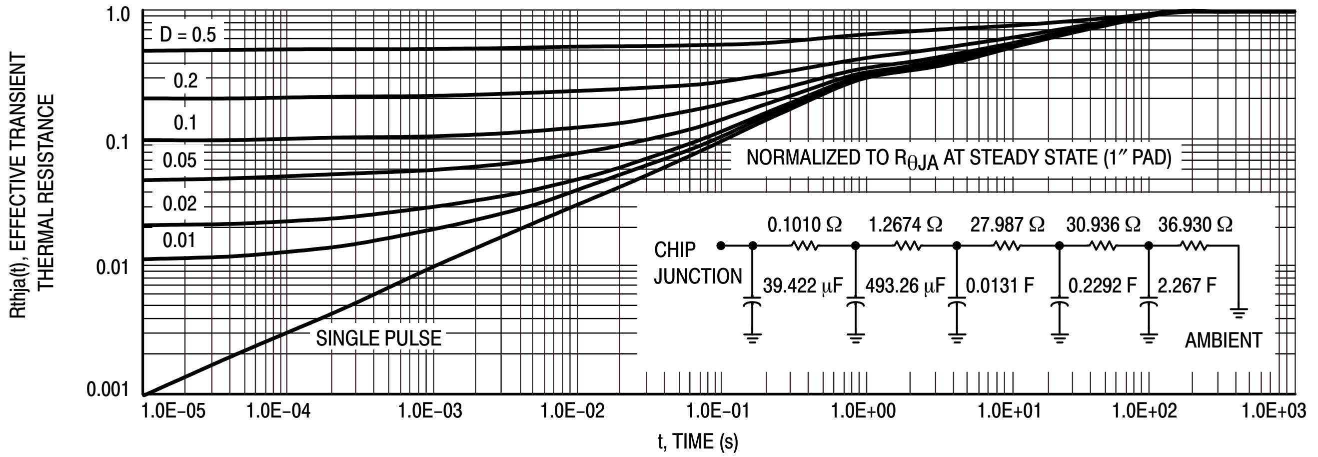
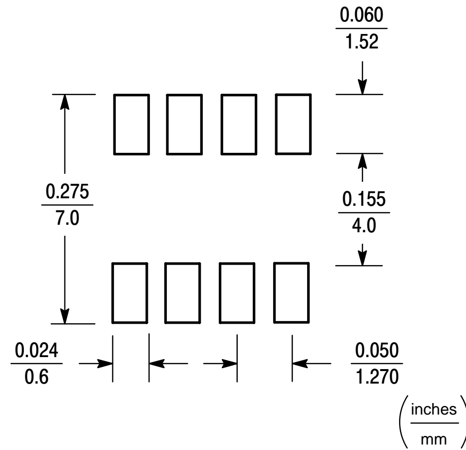



**Figure 23. Schottky Thermal Response**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 24 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

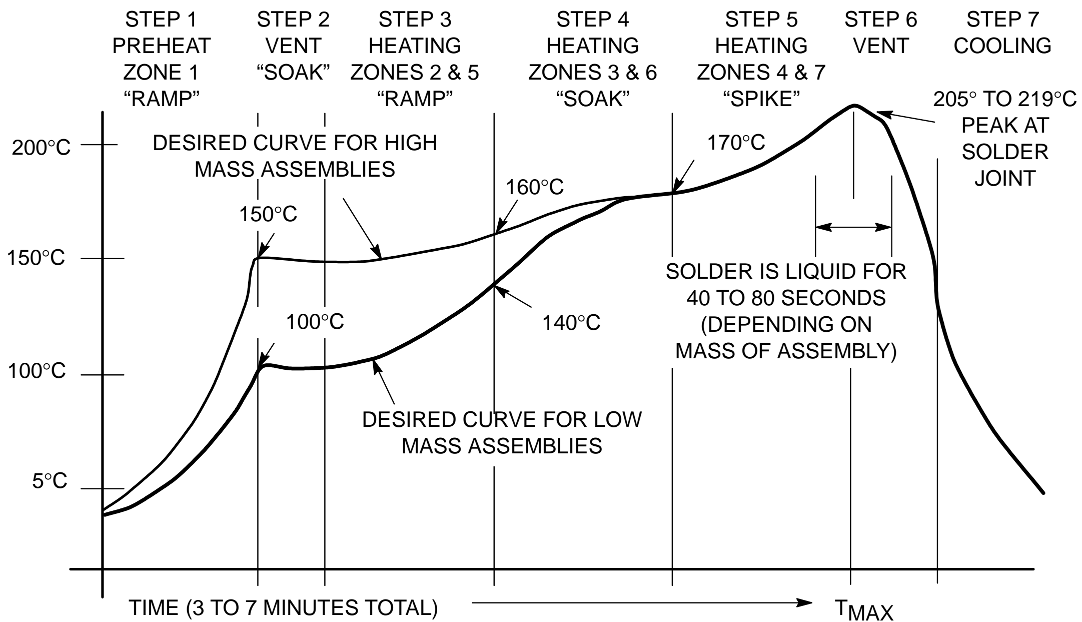



**Figure 24. Typical Solder Heating Profile**

# NTP27N06

ON Semiconductor™

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*Advance Information*

# Power MOSFET 27 Amps, 60 Volts

## N–Channel TO–220

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

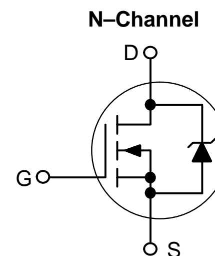
- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter $V_{SD}$ Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**27 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 46 mΩ**

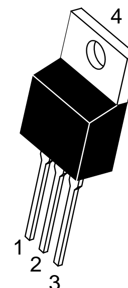
N–Channel



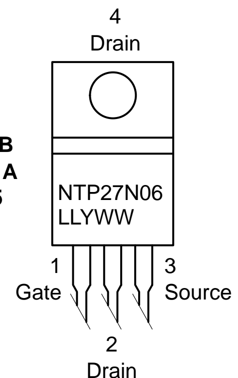

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±20<br>±30 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>27<br>15<br>80 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 88.2<br>0.59 | W<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, L = 0.3 mH, $I_L$(pk) = 27 A, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 109 | mJ |
| Thermal Resistance – Junction–to–Case | $R_{\theta JC}$ | 1.7 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




NTP27N06 = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTP27N06 | TO–220AB | 50 Units/Rail |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 1.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>70<br>79.4 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Note 1.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.8<br>6.9 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 1.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 13.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>37.5 | <br>46 | mΩ |
| Static Drain–to–Source On–Resistance (Note 1.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 27 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 13.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>1.05<br>2.12 | <br>1.5<br>– | Vdc |
| Forward Transconductance (Note 1.) ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | – | 13.2 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 725 | 1015 | pF |
| Output Capacitance | | $C_{oss}$ | – | 213 | 300 | |
| Transfer Capacitance | | $C_{rss}$ | – | 58 | 120 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 27 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 1.) | $t_{d(on)}$ | – | 13.6 | 30 | ns |
| Rise Time | | $t_r$ | – | 62.7 | 125 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 26.6 | 60 | |
| Fall Time | | $t_f$ | – | 70.4 | 140 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 27 Adc, $V_{GS}$ = 10 Vdc) (Note 1.) | $Q_T$ | – | 21.2 | 30 | nC |
| | | $Q_1$ | – | 5.6 | – | |
| | | $Q_2$ | – | 7.3 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc) (Note 1.)<br>($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.05<br>0.93 | 1.25<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 1.) | $t_{rr}$ | – | 42 | – | ns |
| | | $t_a$ | – | 26 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.07 | – | μc |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

# NTP45N06, NTB45N06

ON Semiconductor™

http://onsemi.com

## Power MOSFET 45 Amps, 60 Volts

### N–Channel TO–220 and D2PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

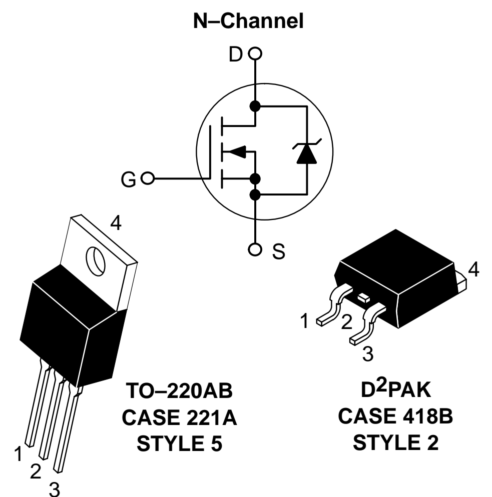
**Features**

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter $V_{SD}$ Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

**45 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 26 mΩ**




**TO–220AB**
**CASE 221A**
**STYLE 5**

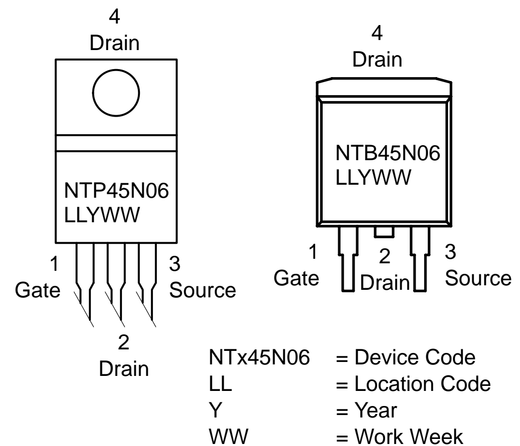
**D2PAK**
**CASE 418B**
**STYLE 2**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>±20<br>±30 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>45<br>30<br>150 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 125<br>0.83<br>3.2<br>2.4 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vdc, RG = 25 Ω, $I_{L(pk)}$ = 40 A, L = 0.3 mH, $V_{DS}$ = 60 Vdc) | $E_{AS}$ | 240 | mJ |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 in$^2$).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 in$^2$).

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




NTx45N06 = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTP45N06 | TO–220AB | 50 Units/Rail |
| NTB45N06 | D2PAK | 50 Units/Rail |
| NTB45N06T4 | D2PAK | 800/Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Case<br>– Junction–to–Ambient (Note 3.)<br>– Junction–to–Ambient (Note 4.) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 1.2<br>46.8<br>63.2 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 5.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>70<br>57 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 5.) | | | | | | |
| Gate Threshold Voltage (Note 5.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.8<br>7.2 | <br>4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 5.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 22.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>21 | <br>26 | mOhm |
| Static Drain–to–Source On–Voltage (Note 5.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 45 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 22.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.93<br>0.93 | <br>1.4<br>– | Vdc |
| Forward Transconductance (Note 5.) ($V_{DS}$ = 8.0 Vdc, $I_D$ = 12 Adc) | | $g_{FS}$ | – | 16.6 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1224 | 1725 | pF |
| Output Capacitance | | $C_{oss}$ | – | 345 | 485 | |
| Transfer Capacitance | | $C_{rss}$ | – | 76 | 160 | |
| **SWITCHING CHARACTERISTICS** (Note 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) (Note 5.) | $t_{d(on)}$ | – | 10 | 25 | ns |
| Rise Time | | $t_r$ | – | 101 | 200 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 33 | 70 | |
| Fall Time | | $t_f$ | – | 106 | 220 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 10 Vdc) (Note 5.) | $Q_T$ | – | 33 | 46 | nC |
| | | $Q_1$ | – | 6.4 | – | |
| | | $Q_2$ | – | 15 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc) (Note 5.)<br>($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.08<br>0.93 | 1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 5.) | $t_{rr}$ | – | 53.1 | – | ns |
| | | $t_a$ | – | 36 | – | |
| | | $t_b$ | – | 16.9 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.087 | – | μC |

3. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
4. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 $in^2$).
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

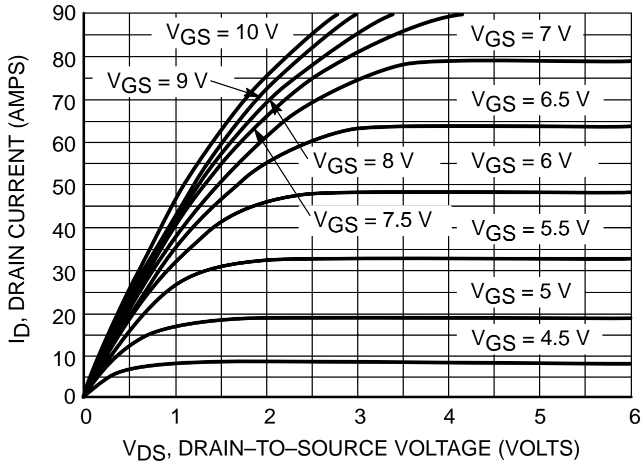



**Figure 1. On–Region Characteristics**

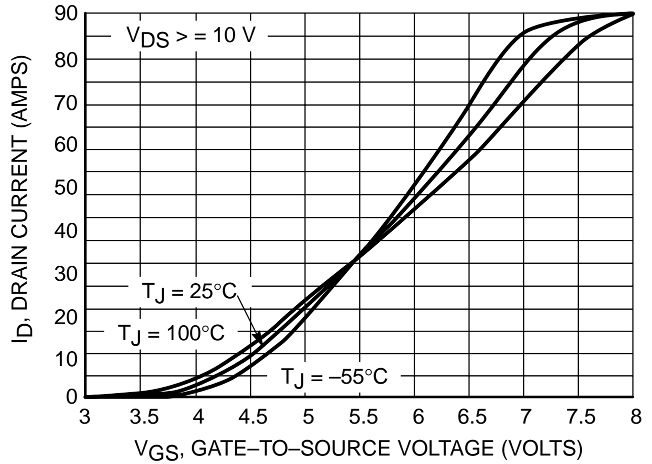



**Figure 2. Transfer Characteristics**

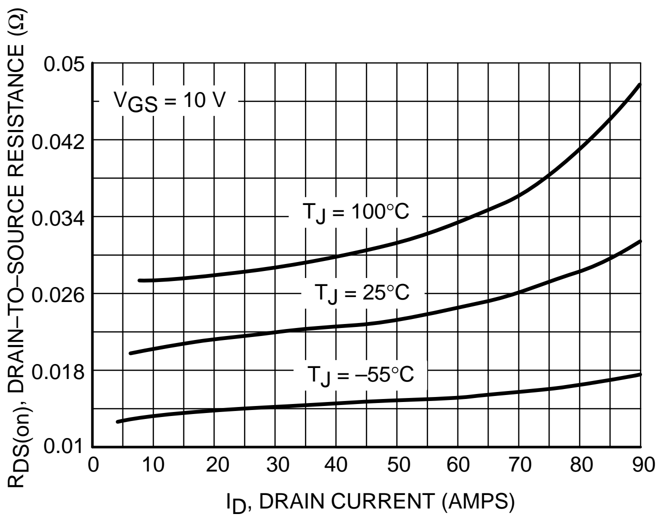



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

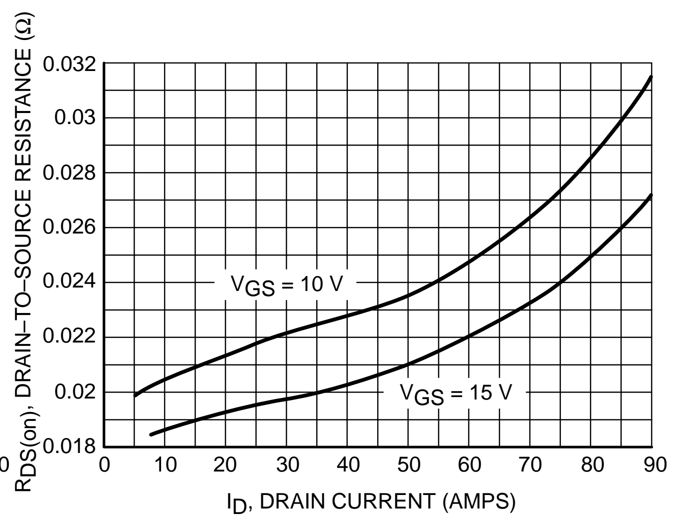



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

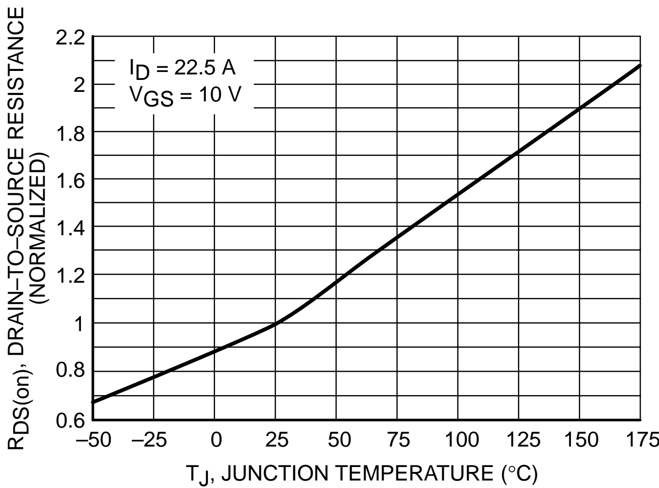



**Figure 5. On–Resistance Variation with Temperature**

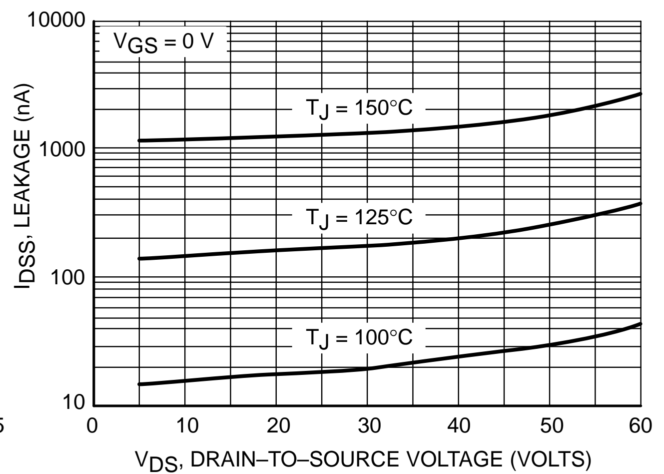



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

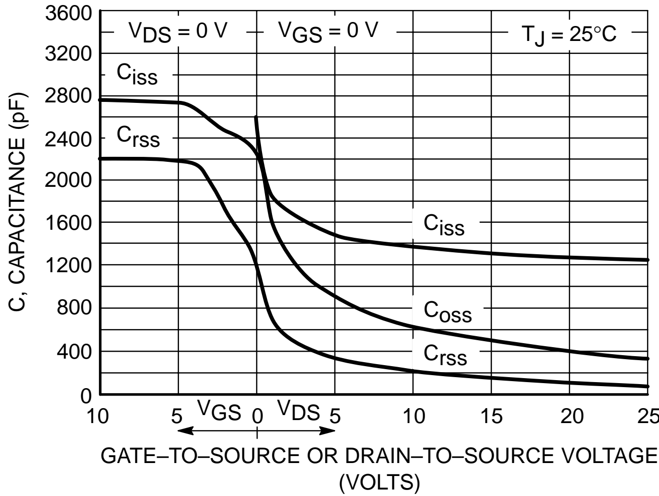



**Figure 7. Capacitance Variation**

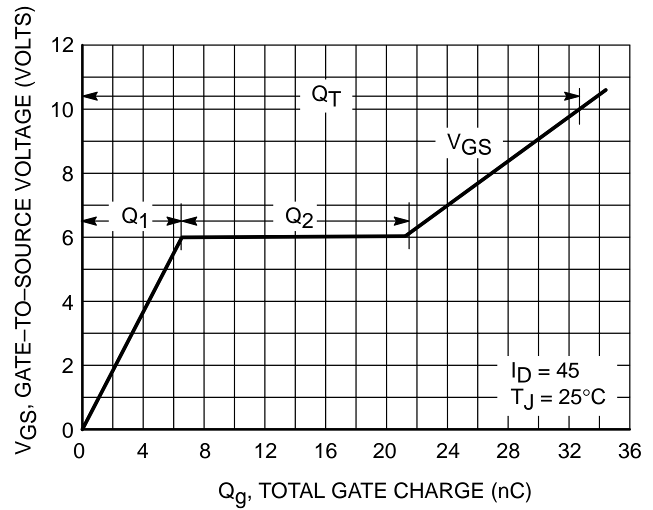



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

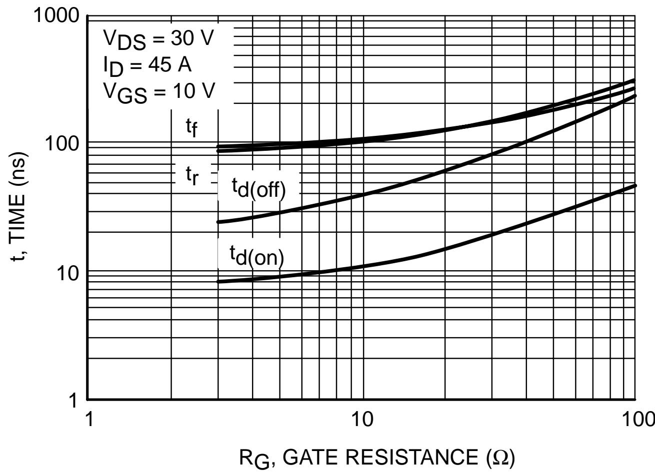



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

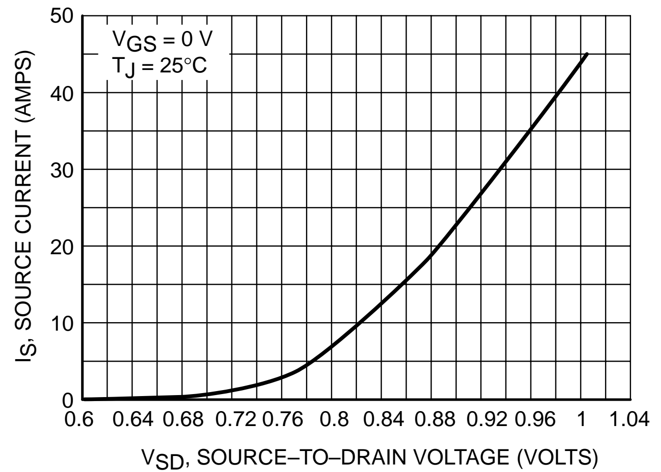



**Figure 10. Diode Forward Voltage vs. Current**

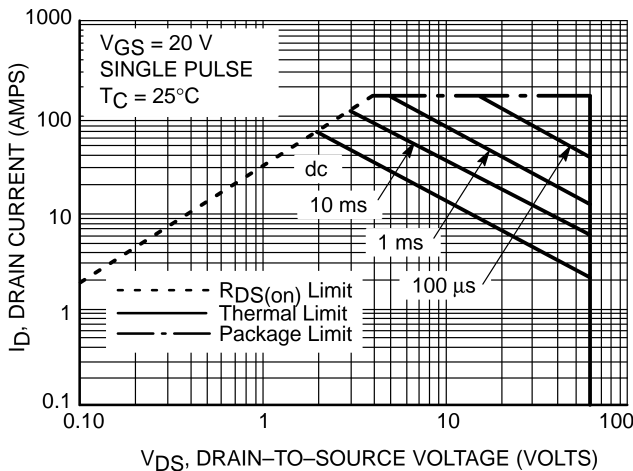



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

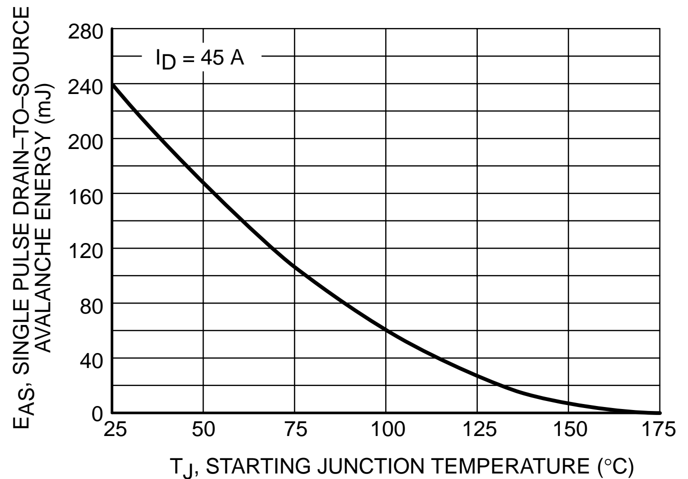



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

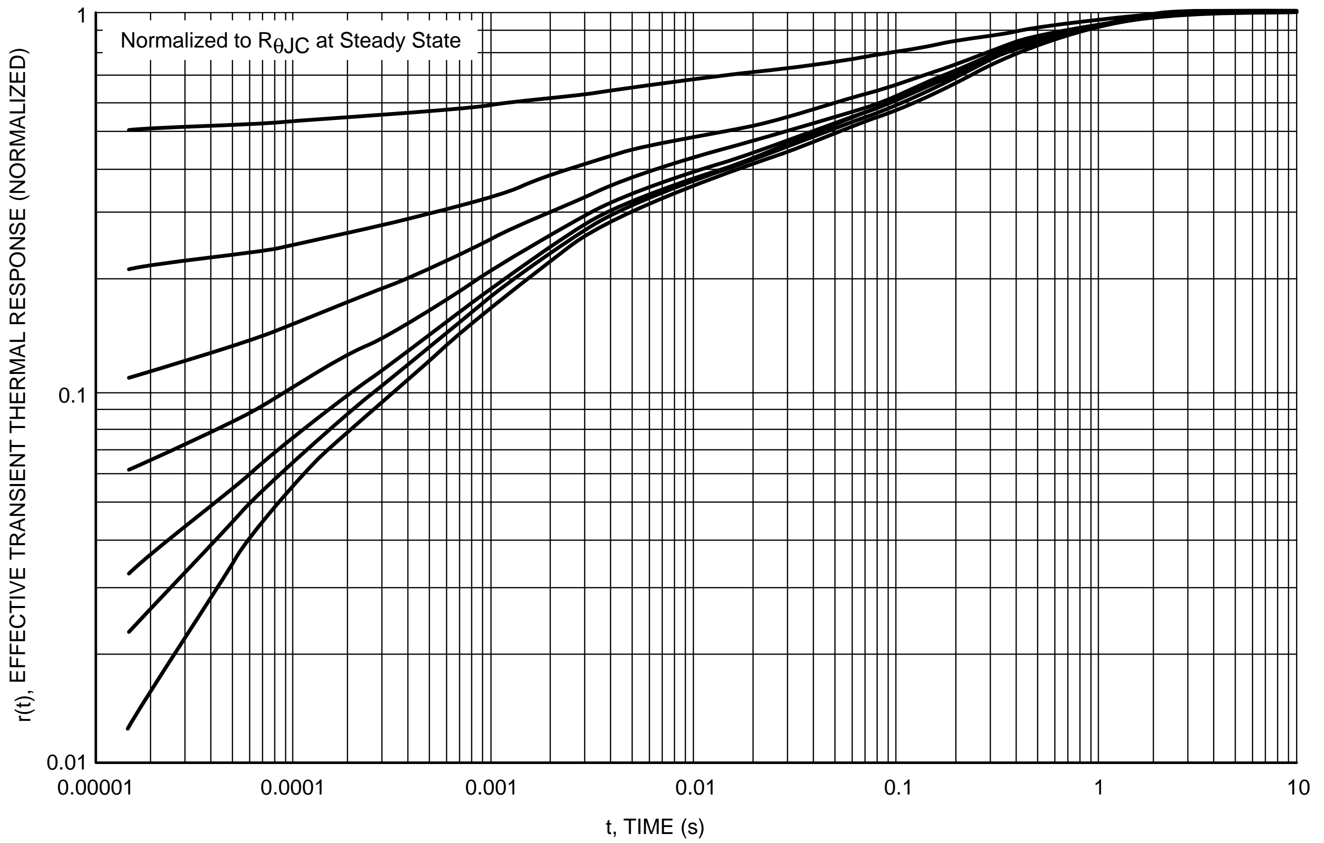



**Figure 13. Thermal Response**

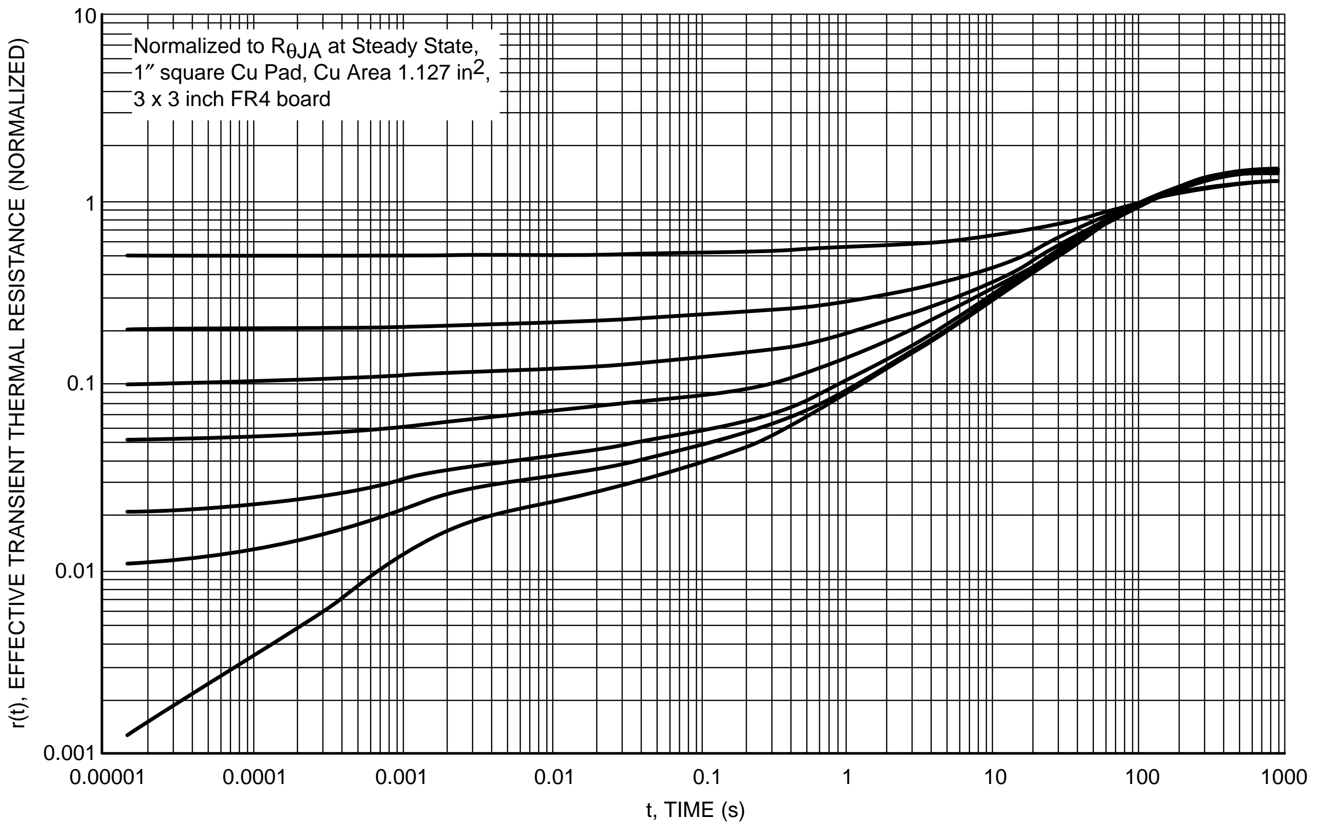



**Figure 14. Thermal Response**

# NTP45N06L, NTB45N06L

**ON Semiconductor™**

http://onsemi.com

## Power MOSFET
## 45 Amps, 60 Volts, Logic Level
### N–Channel TO–220 and $D^2PAK$

**45 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

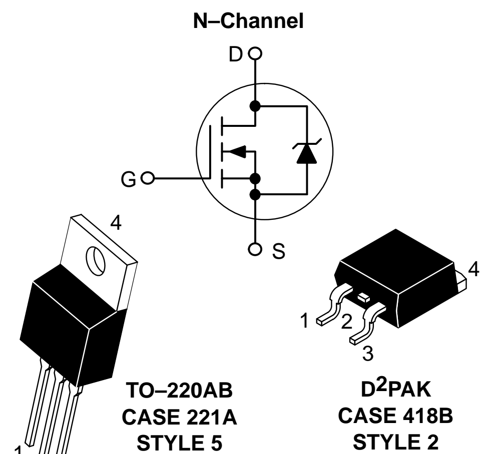
Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

**Features**

- Higher Current Rating
- Lower $R_{DS(on)}$
- Lower $V_{DS(on)}$
- Lower Capacitances
- Lower Total Gate Charge
- Tighter $V_{SD}$ Specification
- Lower Diode Reverse Recovery Time
- Lower Reverse Recovery Stored Charge

**Typical Applications**

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

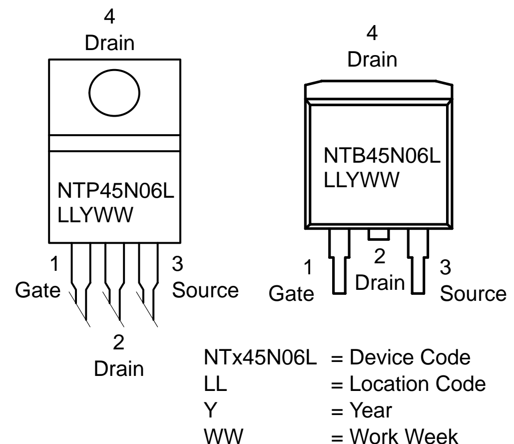



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 10 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GS}$ | <br>± 15<br>± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>45<br>30<br>150 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 125<br>0.83<br>3.2<br>2.4 | W<br>W/°C<br>W<br>W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 5.0 Vdc, L = 0.3 mH $I_{L(pk)}$ = 40 A, $V_{DS}$ = 60 Vdc, $R_G$ = 25 Ω) | $E_{AS}$ | 240 | mJ |

1. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
2. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 $in^2$).

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




NTx45N06L = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTP45N06L | TO–220AB | 50 Units/Rail |
| NTB45N06L | $D^2PAK$ | 50 Units/Rail |
| NTB45N06LT4 | $D^2PAK$ | 800/Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Case<br>– Junction–to–Ambient (Note 3.)<br>– Junction–to–Ambient (Note 4.) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 1.2<br>46.8<br>63.2 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>67<br>67.2 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 5.) | | | | | | |
| Gate Threshold Voltage (Note 5.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.8<br>4.7 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 5.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 22.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>23 | <br>28 | mOhm |
| Static Drain–to–Source On–Voltage (Note 5.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 45 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 22.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>1.03<br>0.93 | <br>1.51<br>– | Vdc |
| Forward Transconductance (Note 5.) ($V_{DS}$ = 8.0 Vdc, $I_D$ = 12 Adc) | | $g_{FS}$ | – | 22.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1212 | 1700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 352 | 480 | |
| Transfer Capacitance | | $C_{rss}$ | – | 90 | 180 | |
| **SWITCHING CHARACTERISTICS** (Note 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) (Note 5.) | $t_{d(on)}$ | – | 13 | 30 | ns |
| Rise Time | | $t_r$ | – | 341 | 680 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 36 | 75 | |
| Fall Time | | $t_f$ | – | 158 | 320 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 5.0 Vdc) (Note 5.) | $Q_T$ | – | 23 | 32 | nC |
| | | $Q_1$ | – | 4.6 | – | |
| | | $Q_2$ | – | 14.1 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc) (Note 5.)<br>($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.01<br>0.92 | 1.15<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 5.) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 30 | – | |
| | | $t_b$ | – | 26 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.09 | – | μC |

3. When surface mounted to an FR4 board using 1″ pad size, (Cu Area 1.127 $in^2$).
4. When surface mounted to an FR4 board using the minimum recommended pad size, (Cu Area 0.412 $in^2$).
5. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
6. Switching characteristics are independent of operating junction temperatures.

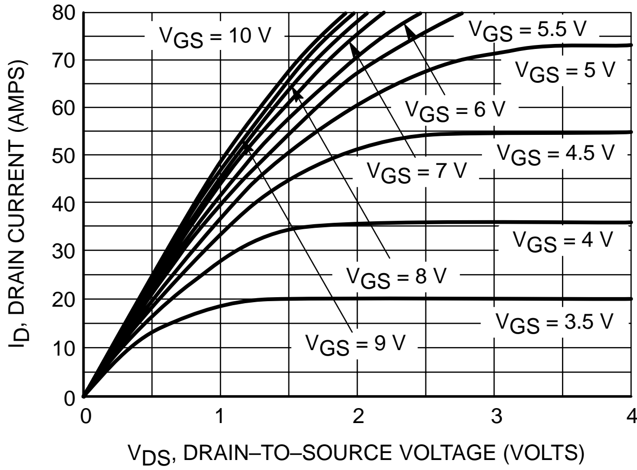



**Figure 1. On–Region Characteristics**

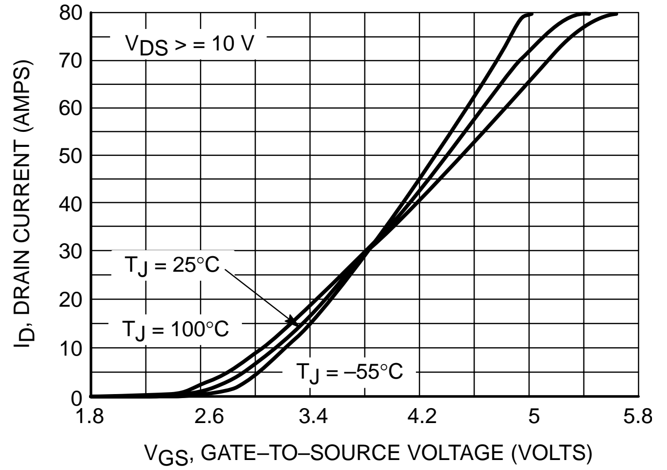



**Figure 2. Transfer Characteristics**

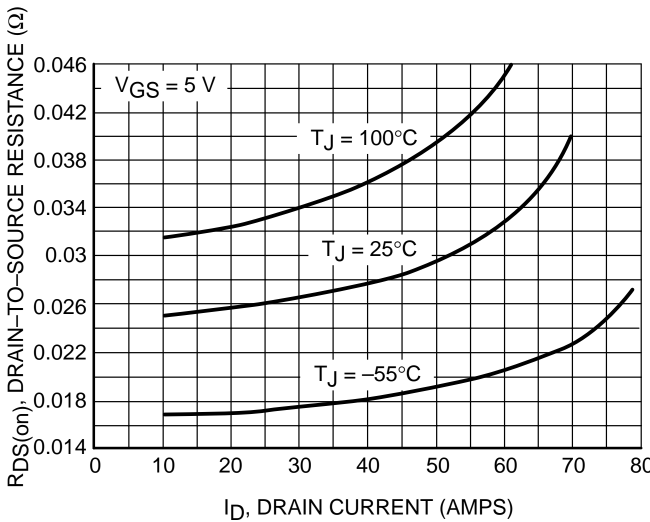



**Figure 3. On–Resistance vs. Gate–to–Source Voltage**

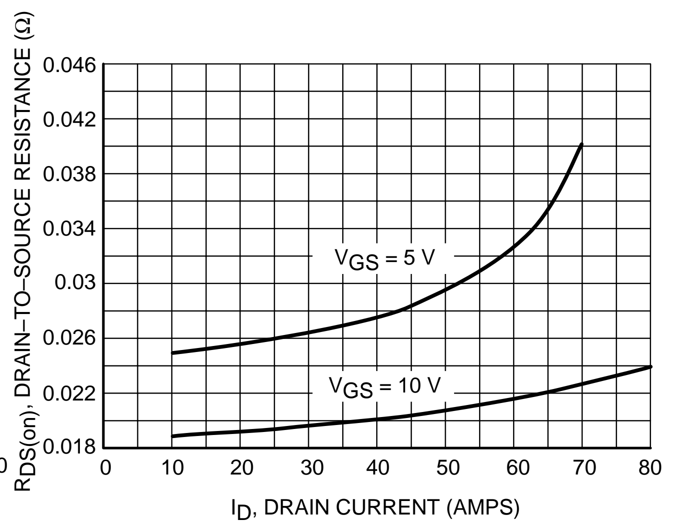



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

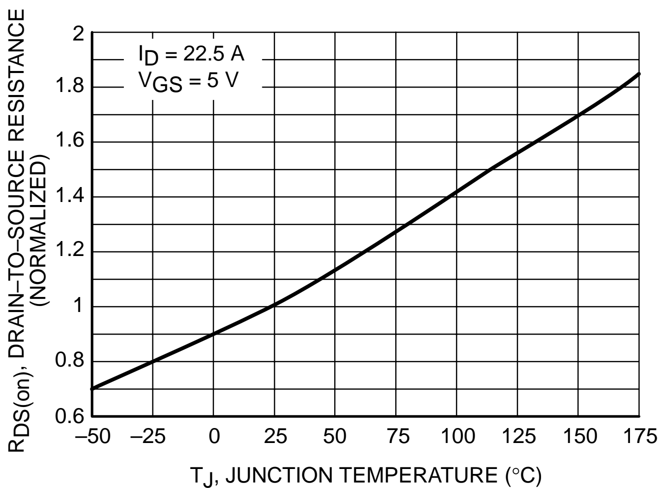



**Figure 5. On–Resistance Variation with Temperature**

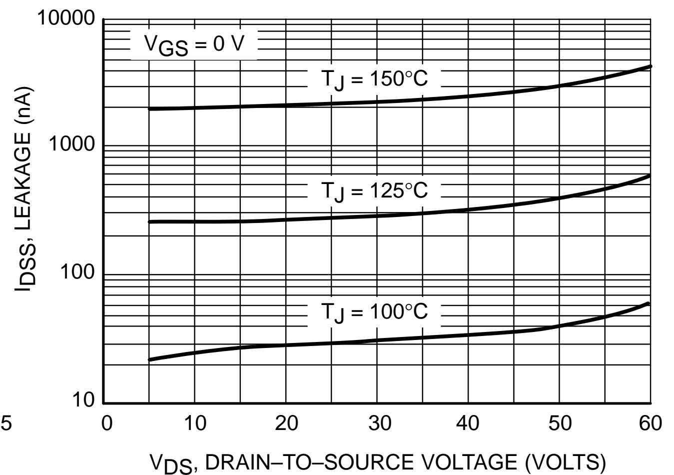



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

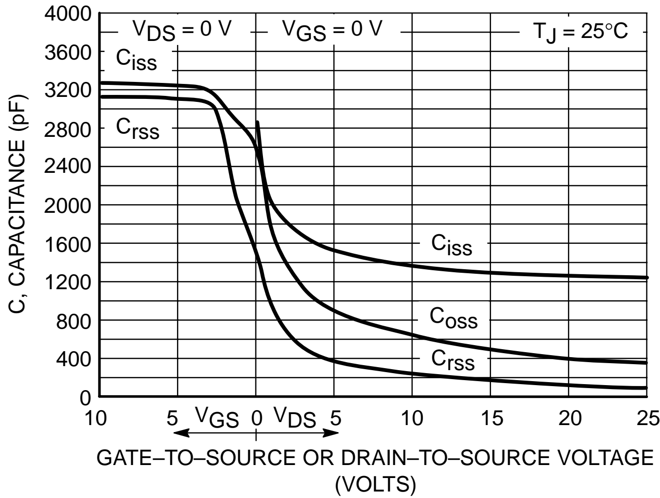



**Figure 7. Capacitance Variation**

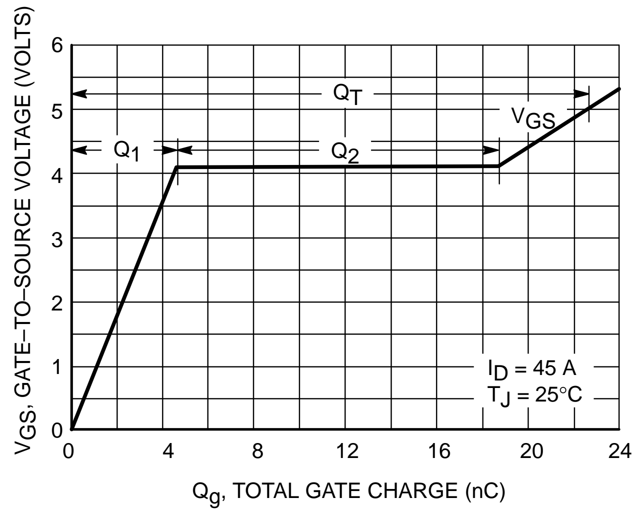



**Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge**

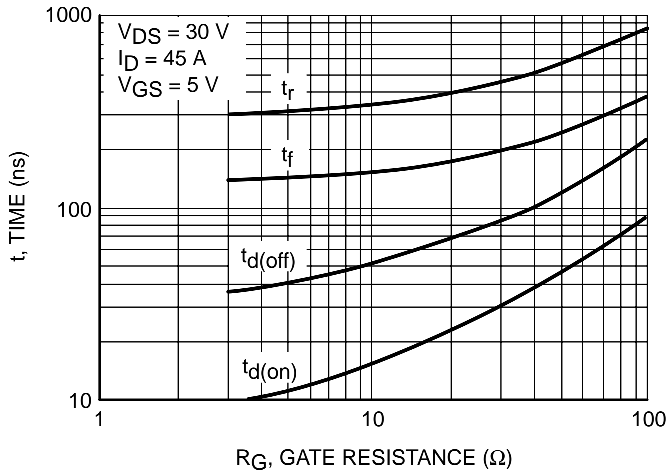



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

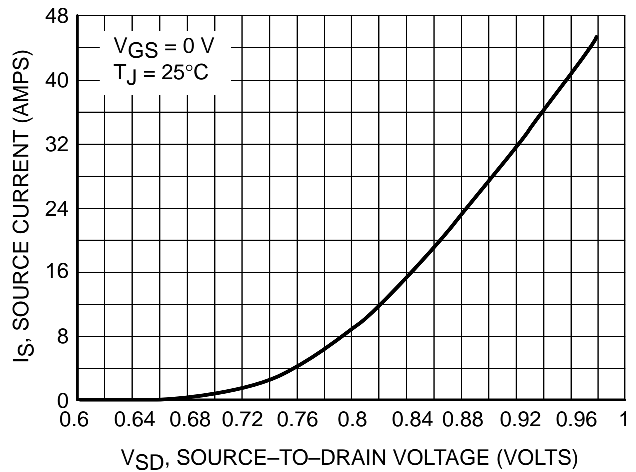



**Figure 10. Diode Forward Voltage vs. Current**

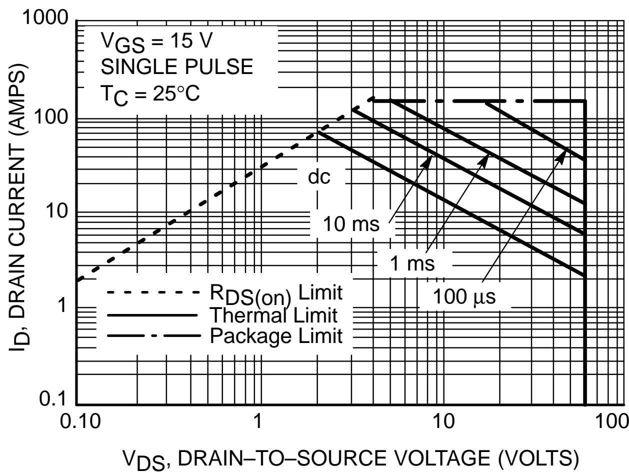



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

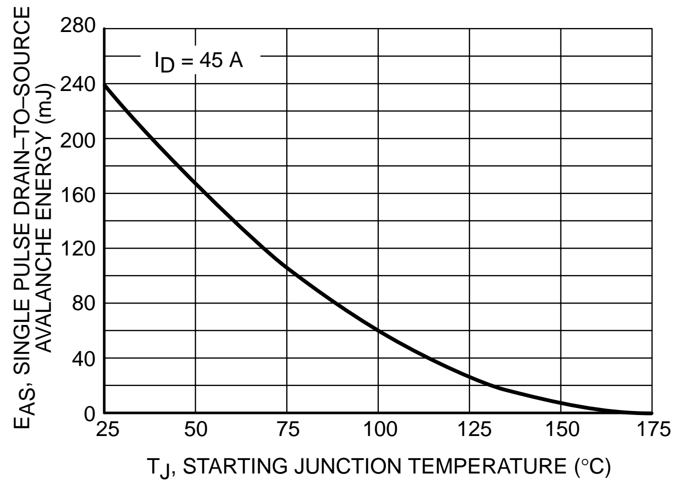



**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**

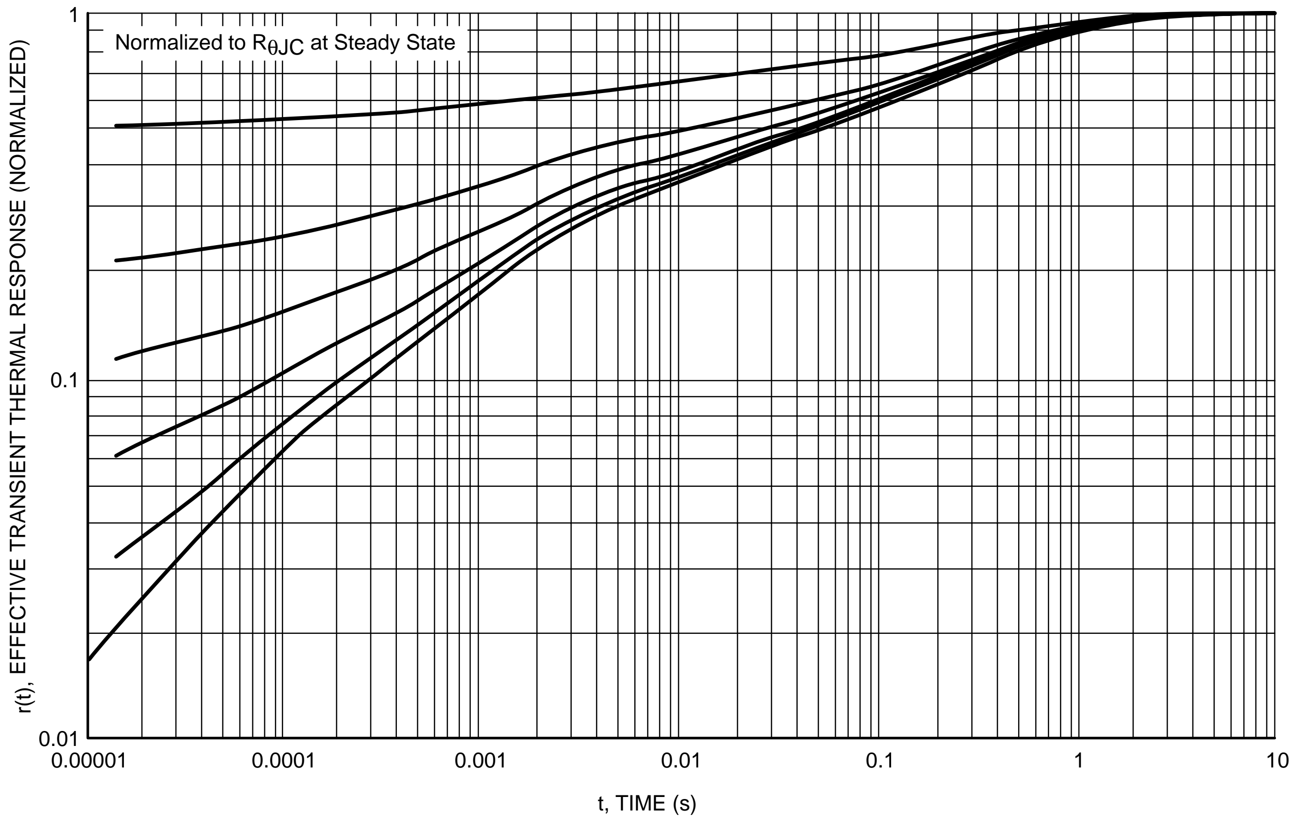



**Figure 13. Thermal Response**

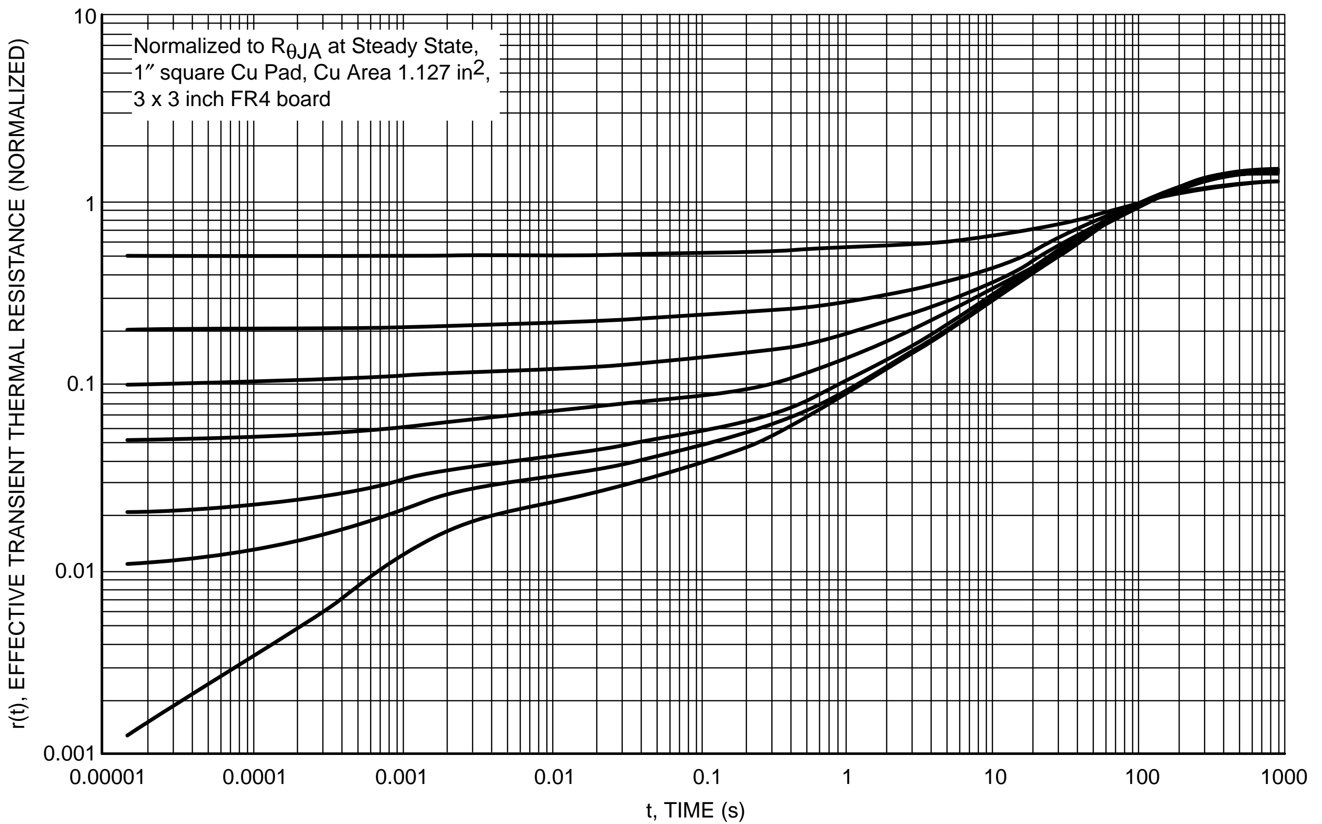



**Figure 14. Thermal Response**

# NTP75N03-06, NTB75N03-06

# Power MOSFET 75 Amps, 30 Volts

## N–Channel TO–220 and $D^2$PAK

This 10 $V_{GS}$ gate drive vertical Power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain–to–source diode has a ideal fast but soft recovery.

**Features**

- Ultra–Low $R_{DS(on)}$, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC Rated HBM Class 1, MM Class B, CDM Class 0

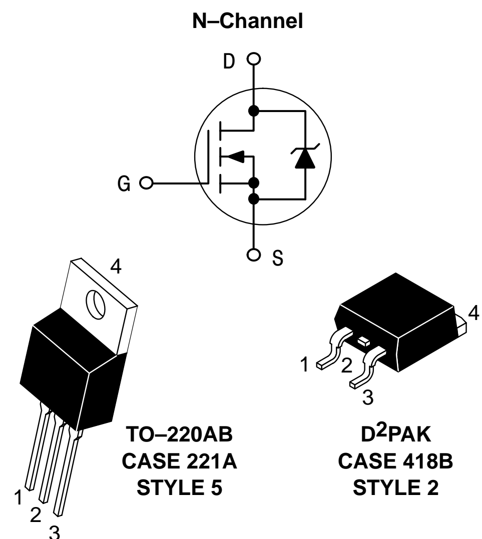
**Typical Applications**

- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTP1306 and MTB1306 in Many Applications

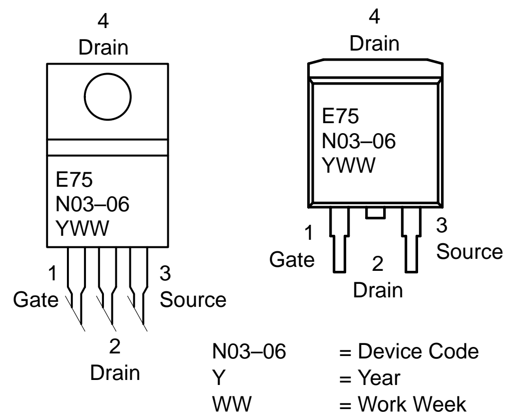
**ON Semiconductor™**

**http://onsemi.com**

**75 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 6.5 mΩ**




**MARKING DIAGRAMS & PIN ASSIGNMENTS**




N03–06 = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTP75N03–06 | TO–220 | 50 Units/Rail |
| NTB75N03–06 | D2PAK | 50 Units/Rail |
| NTB75N03–06T4 | D2PAK | 800 Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage<br>(RGS = 10 MΩ) | $V_{DGB}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Non–repetitive (tp ≤ 10 ms) | $V_{GS}$ | ±24 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>75<br>59<br>225 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 150<br>1.0<br>2.5 | W<br>W/°C<br>W |
| Operating and Storage Temperature Range | $T_J$ and $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 38 Vdc, $V_{GS}$ = 10 Vdc, L = 1 mH, $I_L$(pk) = 55 A, $V_{DS}$ = 40 Vdc) | $E_{AS}$ | 1500 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | <br>°C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage (Note 2.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{(BR)DSS}$ | <br>30 | <br>–<br>–57 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current | ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Note 2.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.6<br>–6 | <br>2.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 2.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>5.3 | <br>6.5 | mΩ |
| Static Drain–to–Source On Resistance (Note 2.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 75 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.53<br>0.35 | <br>0.68<br>0.50 | Vdc |
| Forward Transconductance (Notes 2. & 4.) | ($V_{DS}$ = 3 Vdc, $I_D$ = 20 Adc) | $g_{FS}$ | – | 58 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** (Note 4.) | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 4398 | 5635 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1160 | 1894 | |
| Transfer Capacitance | | $C_{rss}$ | – | 317 | 430 | |
| **SWITCHING CHARACTERISTICS** (Notes 3. & 4.) | | | | | | |
| Turn–On Delay Time | ($V_{GS}$ = 5.0 Vdc, $V_{DD}$ = 20 Vdc, $I_D$ = 75 Adc, $R_G$ = 4.7 Ω) (Note 2.) | $t_{d(on)}$ | – | 31 | 48 | ns |
| Rise Time | | $t_r$ | – | 510 | 986 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 99 | 120 | |
| Fall Time | | $t_f$ | – | 203 | 300 | |
| Gate Charge | ($V_{GS}$ = 5.0 Vdc, $I_D$ = 75 Adc, $V_{DS}$ = 24 Vdc) (Note 2.) | $Q_T$ | – | 52 | 122 | nC |
| | | $Q_1$ | – | 6.6 | 28 | |
| | | $Q_2$ | – | 28 | 66 | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C)<br>(Note 2.) | $V_{SD}$ | –<br>– | 1.19<br>1.09 | 1.25<br>– | Vdc |
| Reverse Recovery Time (Note 4.) | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 37 | – | ns |
| | | $t_a$ | – | 20 | – | |
| Reverse Recovery Stored Charge (Note 4.) | | $t_b$ | – | 17 | – | μC |
| | | $Q_{RR}$ | – | 0.023 | – | |

2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.
4. From characterization test data.

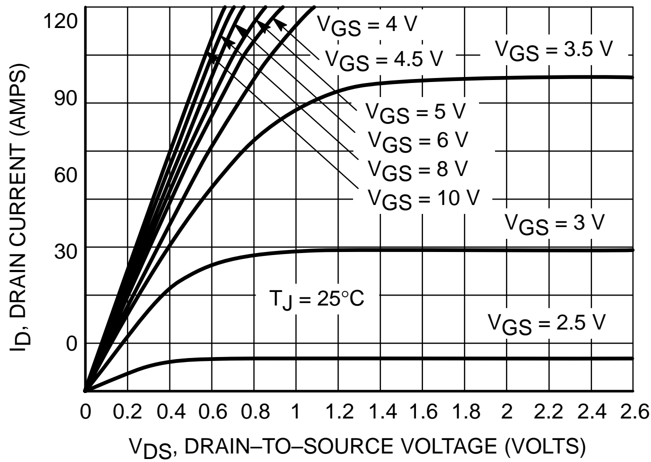



**Figure 1. On–Region Characteristics**

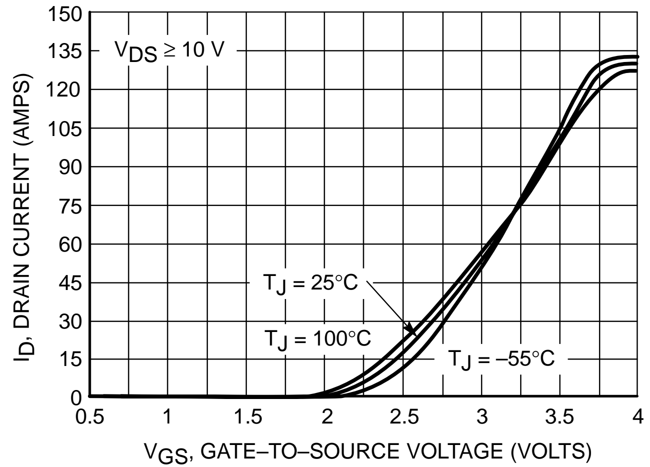



**Figure 2. Transfer Characteristics**

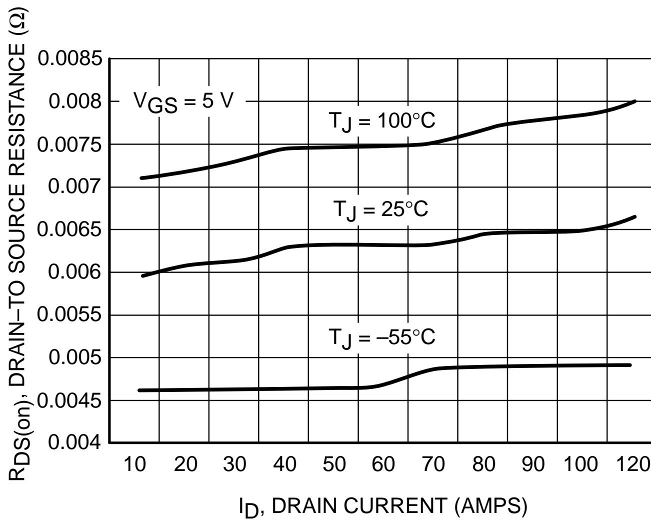



**Figure 3. On–Resistance vs. Drain Current and Temperature**

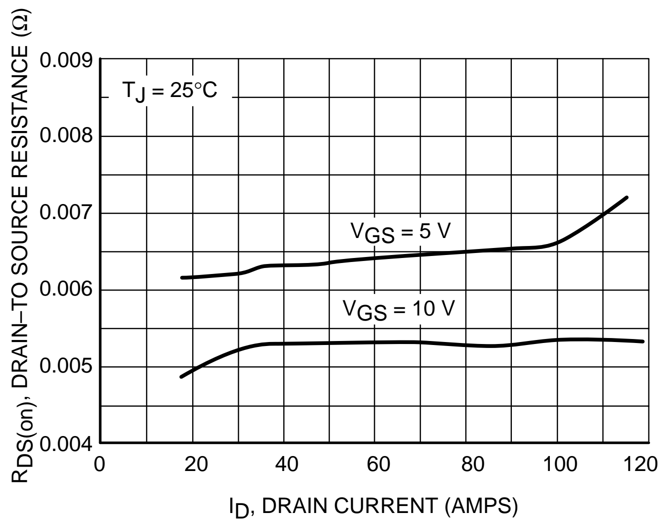



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

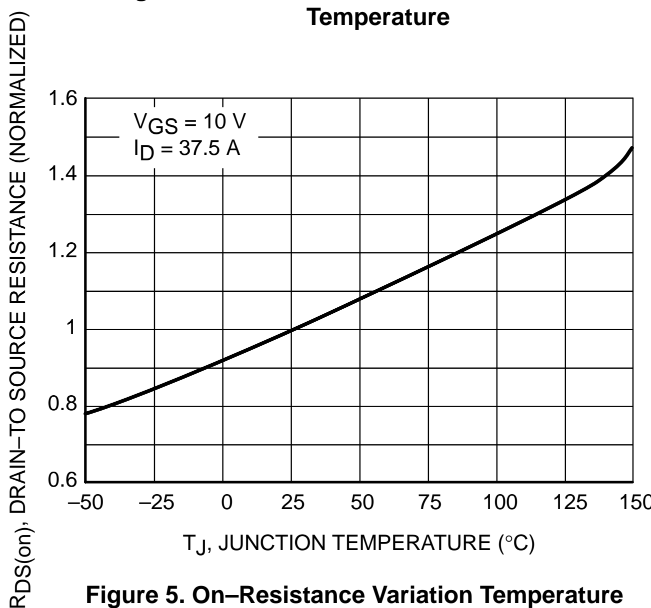



**Figure 5. On–Resistance Variation Temperature**

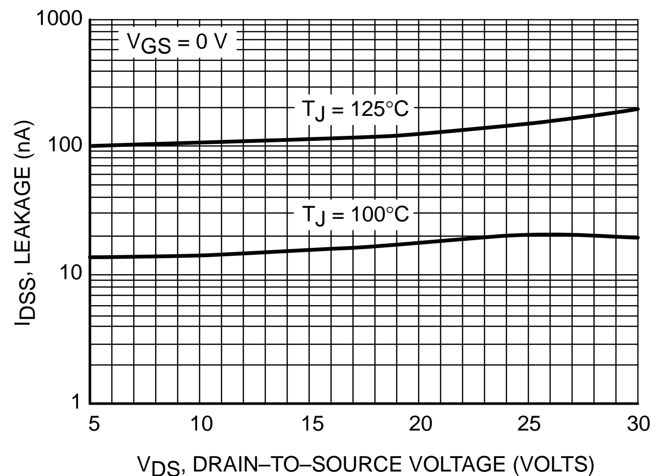



**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

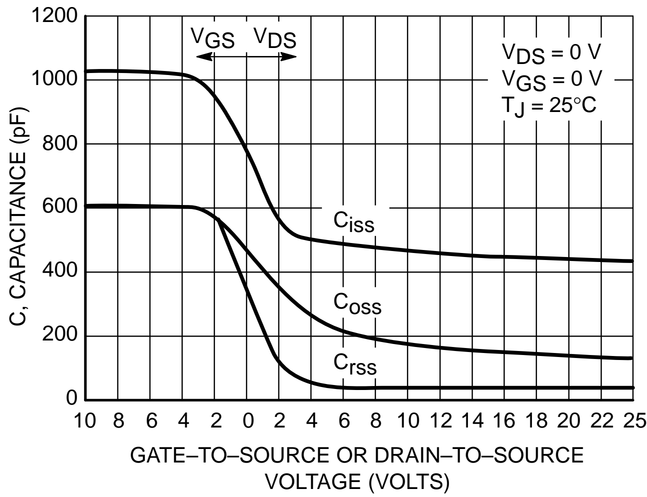



**Figure 7. Capacitance Variation**

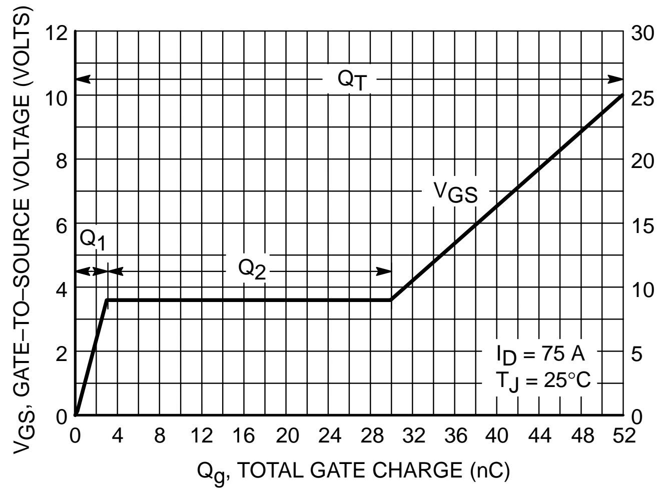



**Figure 8. Gate–to–Source Voltage vs. Total Charge**

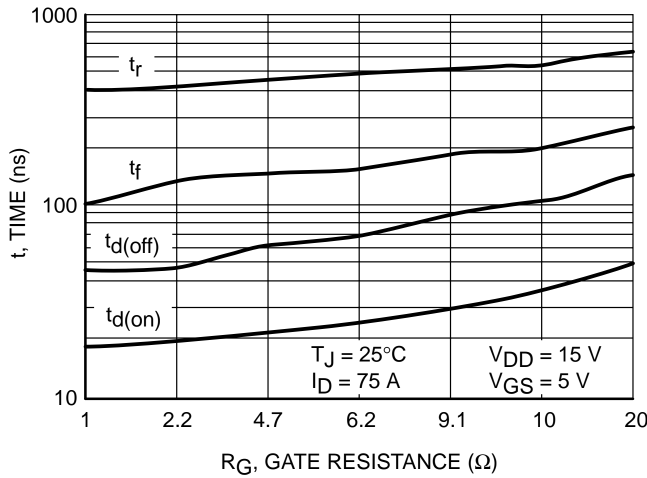



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

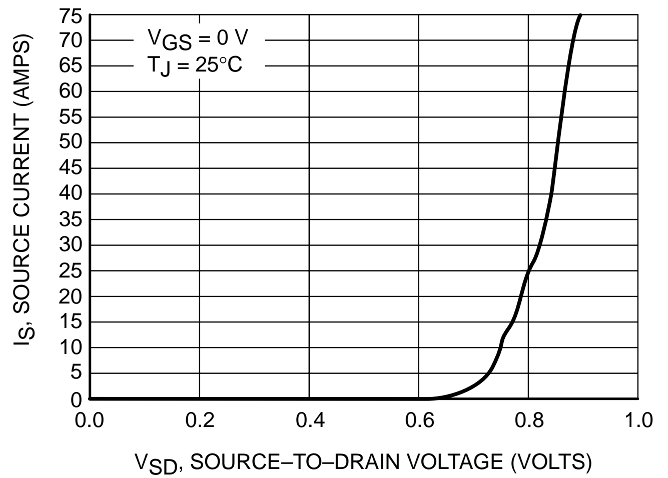



**Figure 10. Diode Forward Voltage vs. Current**

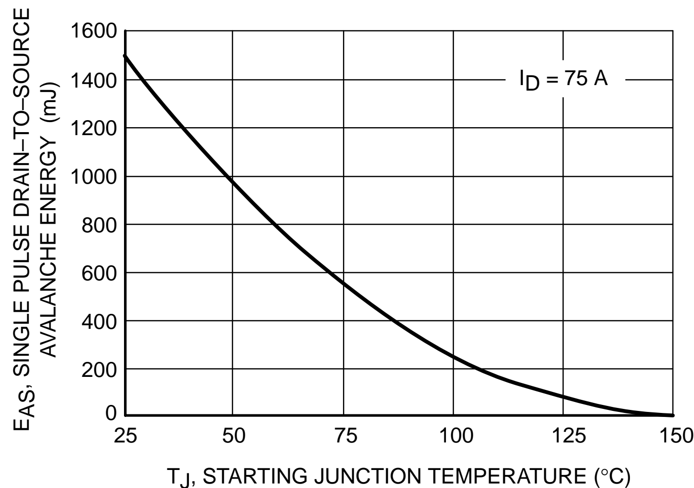



**Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature**

# NTP75N03L09, NTB75N03L09

# Power MOSFET 75 Amps, 30 Volts

## N–Channel TO–220 and D2PAK

This Logic Level Vertical Power MOSFET is a general purpose part that provides the “best of design” available today in a low cost power package. Avalanche energy issues make this part an ideal design in. The drain–to–source diode has a ideal fast but soft recovery.

**Features**

- Ultra–Low $R_{DS(on)}$, Single Base, Advanced Technology
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperatures
- High Avalanche Energy Specified
- ESD JEDAC Rated HBM Class 1, MM Class B, CDM Class 0

**Typical Applications**

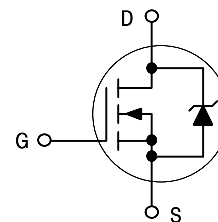
- Power Supplies
- Inductive Loads
- PWM Motor Controls
- Replaces MTP75N03HDL and MTB75N03HDL in Many Applications

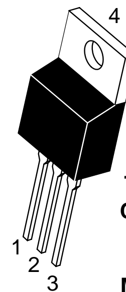
**ON Semiconductor™**

**http://onsemi.com**

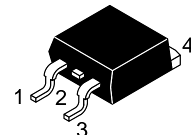
**75 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 9 mΩ**

**N–Channel**



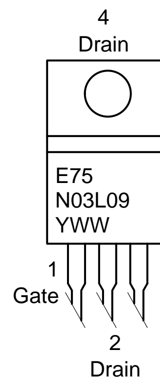



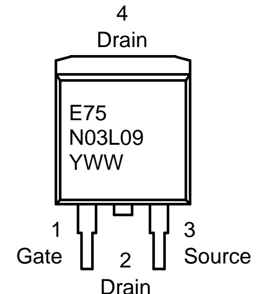

**TO–220AB CASE 221A STYLE 5**




**D2PAK CASE 418B STYLE 2**

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




N03L09 = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTP75N03L09 | TO–220 | 50 Units/Rail |
| NTB75N03L09 | D2PAK | 50 Units/Rail |
| NTB75N03L09T4 | D2PAK | 800 Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage<br>(RGS = 10 MΩ) | $V_{DGB}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Non–repetitive (tp ≤ 10 ms) | $V_{GS}$ | ±24 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>75<br>59<br>225 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 150<br>1.0<br>2.5 | W<br>W/°C<br>W |
| Operating and Storage Temperature Range | $T_J$ and $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 38 Vdc, $V_{GS}$ = 10 Vdc, L = 1 mH, $I_L$(pk) = 55 A, $V_{DS}$ = 40 Vdc) | $E_{AS}$ | 1500 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | <br>°C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage (Note 2.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{(BR)DSS}$ | 30<br>– | 34<br>–57 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current | ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Note 2.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.6<br>–6 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 2.) ($V_{GS}$ = 5.0 Vdc, $I_D$ = 37.5 Adc) | | $R_{DS(on)}$ | – | 7.5 | 9 | mΩ |
| Static Drain–to–Source On Resistance (Note 2.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 75 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 0.52<br>0.35 | 0.68<br>0.50 | Vdc |
| Forward Transconductance (Notes 2. & 4.) | ($V_{DS}$ = 3 Vdc, $I_D$ = 20 Adc) | $g_{FS}$ | – | 58 | – | mΩ |
| **DYNAMIC CHARACTERISTICS** (Note 4.) | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 4398 | 5635 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1160 | 1894 | |
| Transfer Capacitance | | $C_{rss}$ | – | 317 | 430 | |
| **SWITCHING CHARACTERISTICS** (Notes 3. & 4.) | | | | | | |
| Turn–On Delay Time | ($V_{GS}$ = 5.0 Vdc, $V_{DD}$ = 20 Vdc, $I_D$ = 75 Adc, $R_G$ = 4.7 Ω) (Note 2.) | $t_{d(on)}$ | – | 31 | 48 | ns |
| Rise Time | | $t_r$ | – | 510 | 986 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 99 | 120 | |
| Fall Time | | $t_f$ | – | 203 | 300 | |
| Gate Charge | ($V_{GS}$ = 5.0 Vdc, $I_D$ = 75 Adc, $V_{DS}$ = 24 Vdc) (Note 2.) | $Q_T$ | – | 52 | 122 | nC |
| | | $Q_1$ | – | 6.6 | 28 | |
| | | $Q_2$ | – | 28 | 66 | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) (Note 2.) | $V_{SD}$ | –<br>– | 1.19<br>1.09 | 1.25<br>– | Vdc |
| Reverse Recovery Time (Note 4.) | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 37 | – | ns |
| | | $t_a$ | – | 20 | – | |
| Reverse Recovery Stored Charge (Note 4.) | | $t_b$ | – | 17 | – | μC |
| | | $Q_{RR}$ | – | 0.023 | – | |

2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.
4. From characterization test data.

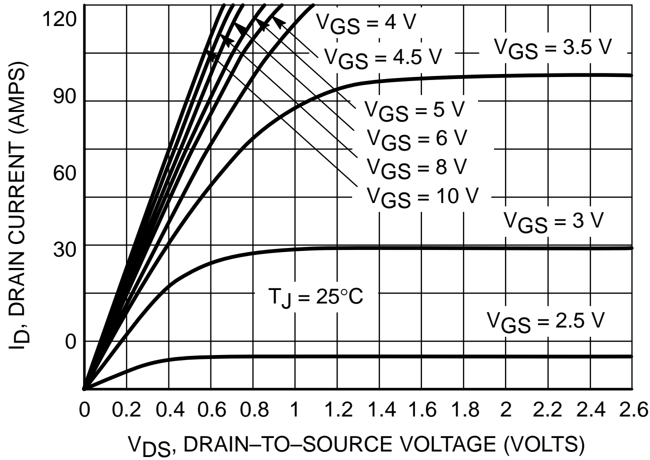


**Figure 1. On–Region Characteristics**

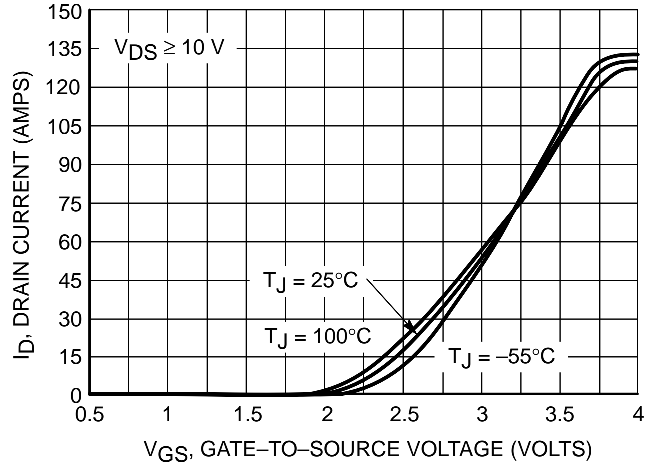


**Figure 2. Transfer Characteristics**

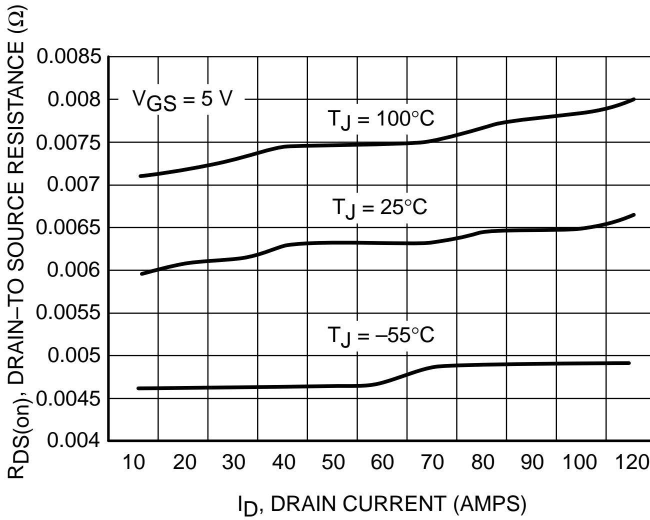


**Figure 3. On–Resistance vs. Drain Current and Temperature**

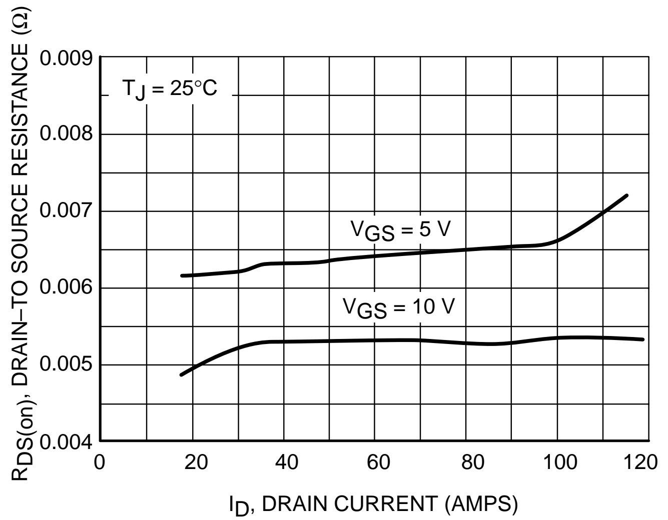


**Figure 4. On–Resistance vs. Drain Current and Gate Voltage**

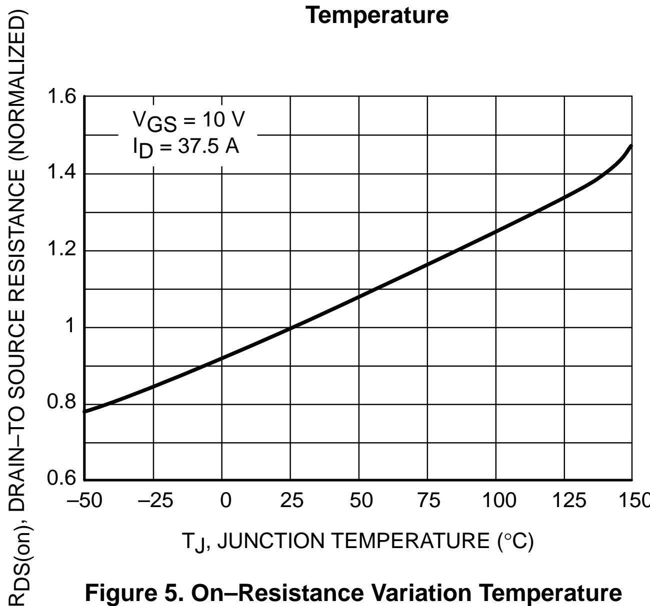


**Figure 5. On–Resistance Variation Temperature**

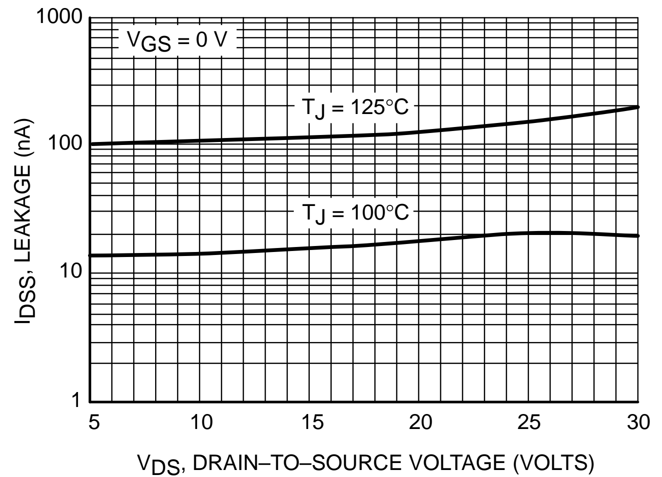


**Figure 6. Drain–to–Source Leakage Current vs. Voltage**

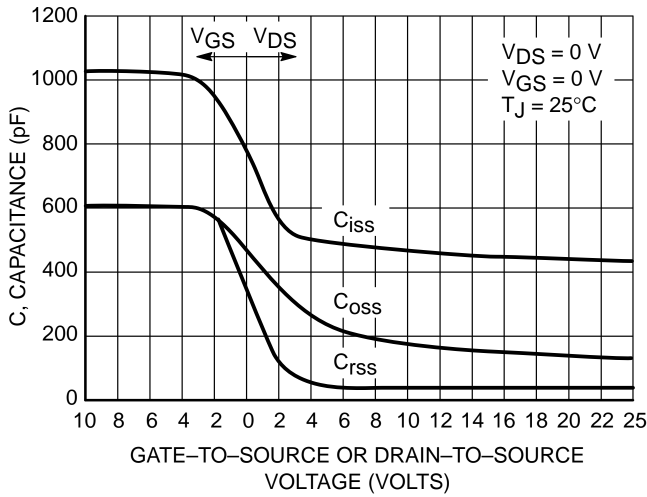


Figure 7. Capacitance Variation

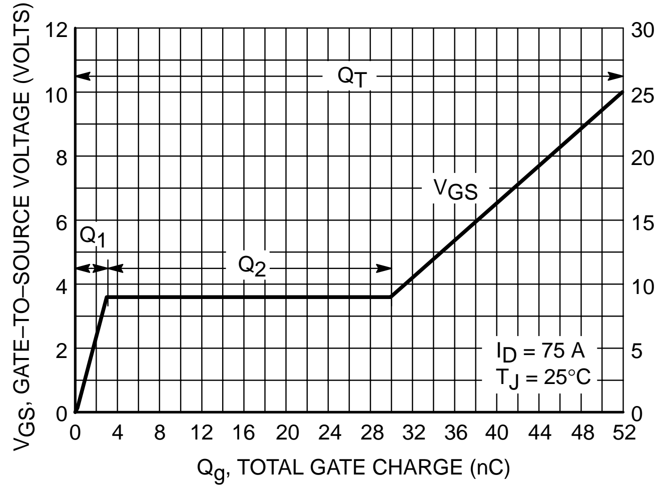


Figure 8. Gate–to–Source Voltage vs. Total Charge

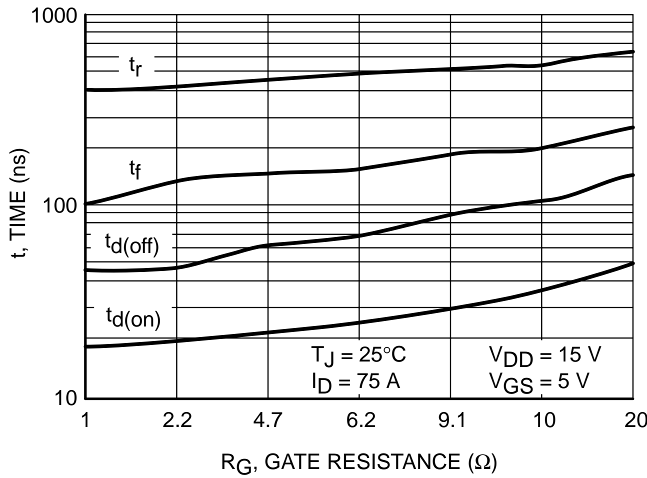


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

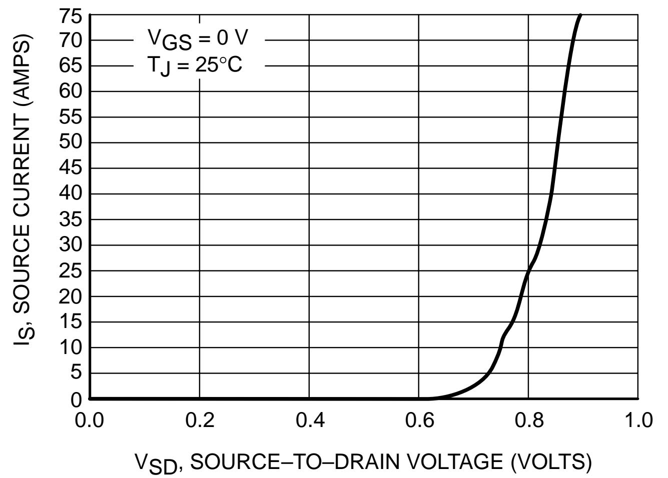


Figure 10. Diode Forward Voltage vs. Current

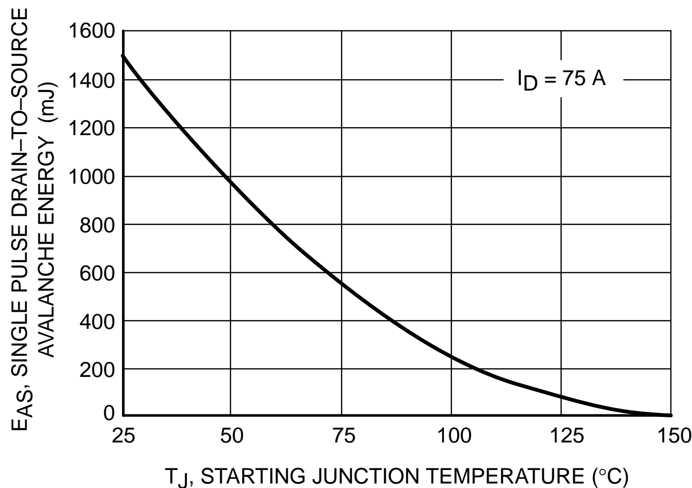


Figure 11. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTQD6866

**ON Semiconductor**

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*Product Preview*

## Power MOSFET
## 5.8 Amps, 20 Volts
### N–Channel TSSOP–8

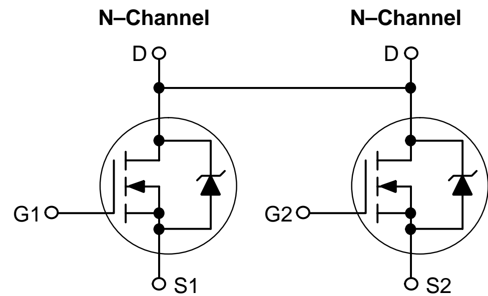
**5.8 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 30 mΩ**

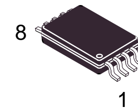
**Features**

- New Low Profile TSSOP–8 Package
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperatures

**Applications**

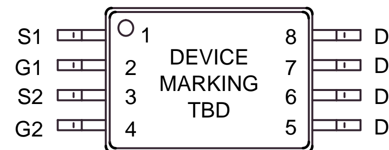
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones
- Lithium Ion Battery Applications
- Note Book PC




**TSSOP–8**
**CASE 948S**
**PLASTIC**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Top View

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Vdc |
| Drain Current – Continuous<br>– Continuous @ 70°C<br>– Single Pulse (tp ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5.8<br>TBD<br>20 | Adc |
| Total Power Dissipation | $P_D$ | 1.6 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5 Vdc, $I_L$ = 10 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 580 | mJ |
| Thermal Resistance –<br>Junction–to–Ambient (Note 1.)<br>Single Channel Steady State<br>Both Channels<br>Junction–to–Ambient (Note 2.)<br>Both Channels | $R_{\theta JA}$ | <br><br>180<br>176<br><br>100 | °C/W |
| Thermal Resistance – Junction–to–Lead<br>Single Channel<br>Both Channels Steady State | $R_{\theta JL}$ | <br>27<br>24 | °C/W |

1. Surface Mounted to Min Pad.
2. Surface Mounted to 1″ x 1″ FR4 Board.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTQD6866 | TSSOP–8 | 100 Units/Rail |
| NTQD6866R2 | TSSOP–8 | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | TBD | – | mV/°C |
| Zero Gate Voltage Collector Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 85°C) | | | – | – | 25 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS(f)}$ | – | – | 100 | nAdc |
| | | $I_{GSS(r)}$ | – | – | 100 | |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA) | | $V_{GS(th)}$ | 0.6 | 0.9 | 1.2 | Vdc |
| Temperature Coefficient (Negative) | | | – | TBD | – | mV/°C |
| Static Drain–to–Source On–State Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 7.0 Adc) | | $R_{DS(on)}$ | – | TBD | TBD | Ω |
| ($V_{GS}$ = 4.0 Vdc, $I_D$ = 7.0 Adc) | | | – | 0.026 | 0.030 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 3.5 Adc) | | | – | 0.031 | 0.040 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 7.0 Adc) | | $g_{FS}$ | TBD | 17 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 930 | TBD | pF |
| Output Capacitance | | $C_{oss}$ | – | 370 | TBD | |
| Transfer Capacitance | | $C_{rss}$ | – | 105 | TBD | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_L$ = 10, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 8.6 | TBD | ns |
| Rise Time | | $t_r$ | – | 14 | TBD | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 57 | TBD | |
| Fall Time | | $t_f$ | – | 54 | TBD | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 4.5 Vdc, $I_D$ = 5.8 Adc) | QT | – | 11 | 15 | nC |
| | | Q1 | – | 2.4 | – | |
| | | Q2 | – | 2.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 3.) | ($I_S$ = 1.8 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.7 | 1.0 | Vdc |
| | ($I_S$ = 1.8 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 85°C) | | – | TBD | – | |
| Reverse Recovery Time | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 30 | – | ns |
| | | $t_a$ | – | 14.5 | – | |
| | | $t_b$ | – | 15.5 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.01 | – | μC |

3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.
4. Switching characteristics are independent of operating junction temperature.

# NTQS6463

**ON Semiconductor**

http://onsemi.com

*Product Preview*

## Power MOSFET 6.2 Amps, 20 Volts

### P–Channel TSSOP–8

**Features**

- New Low Profile TSSOP–8 Package
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Diode Exhibits High Speed, Soft Recovery
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperatures

**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones
- Lithium Ion Battery Applications
- Note Book PC

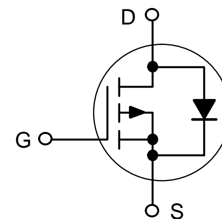
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | 10 secs | Steady State | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | –20 | | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 12 | | |
| Continuous Drain Current<br>– $T_J$ = 150°C (Note 1.)<br>– $T_A$ = 25°C<br>– $T_A$ = 70°C | $I_D$ | <br><br>± 7.4<br>± 5.9 | <br><br>± 6.2<br>± 4.9 | Adc |
| Pulsed Drain Current (10 µs Pulse Width) | $I_{DM}$ | ± 30 | | Apk |
| Continuous Source Current (Diode Conduction) (Note 1.) | $I_S$ | –1.35 | –0.95 | Adc |
| Maximum Power Dissipation (Note 1.)<br>– $T_A$ = 25°C<br>– $T_A$ = 70°C | $P_D$ | <br>1.5<br>1.0 | <br>1.05<br>0.67 | W |
| Operating Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$= 25°C ($V_{DD}$ = 50 V, $I_L$ = 16.3 Apk, L = 10 mH) | $E_{AS}$ | 1.38 | | J |

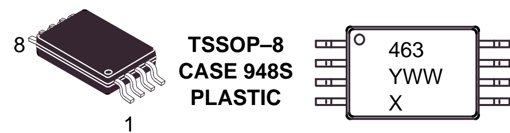
1. Surface mounted to 1″ x 1″ FR–4 board.

**6.2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 20 mΩ**

**P–Channel**

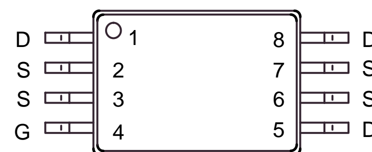



**MARKING DIAGRAM**




| | |
|---|---|
| 463 | = Device Code |
| Y | = Year |
| WW | = Work Week |
| X | = MOSFET |

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTQS6463 | TSSOP–8 | 100 Units/Rail |
| NTQS6463R2 | TSSOP–8 | 3000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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### THERMAL RESISTANCE RATINGS

| Rating | Symbol | Typical | Max | Unit |
|---|---|---|---|---|
| Maximum Junction–to–Ambient (Note 2.)<br>$t \leq 10$ sec<br>Steady State | $R_{\theta JA}$ | <br>65<br>100 | <br>83<br>120 | °C/W |
| Maximum Junction–to–Foot<br>Steady State | $R_{\theta JF}$ | <br>43 | <br>52 | °C/W |

### ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **STATIC** | | | | | | |
| Gate Threshold Voltage<br>($V_{DS} = V_{GS}$, $I_D$ = –250 μA) | | $V_{GS(th)}$ | –0.45 | –0.9 | – | Vdc |
| Gate–Body Leakage ($V_{GS}$ = 0 Vdc, $V_{GS}$ = ±8 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| Zero Gate Threshold Voltage Drain Current<br>($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>–1.0<br>–10 | μAdc |
| On–State Drain Current (Note 3.)<br>($V_{DS}$ = –5.0 Vdc, $V_{GS}$ = –4.5 Vdc) | | $I_{D(on)}$ | 20 | – | – | Adc |
| Drain–Source On–State Resistance (Note 3.)<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –7.4 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –6.3 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>0.018<br>0.025 | <br>0.020<br>0.027 | Ω |
| Forward Transconductance ($V_{DS}$ = –15 Vdc, $I_D$ = –7.4 Adc) (Note 3.) | | $g_{FS}$ | – | 21 | – | S |
| Diode Forward Voltage ($I_S$ = –1.3 Adc, $V_{GS}$ = 0 Vdc) (Note 3.) | | $V_{SD}$ | – | –0.71 | –1.1 | Vdc |
| **DYNAMIC** (Note 4.) | | | | | | |
| Total Gate Charge | ($V_{DS}$ = –10 Vdc, $V_{GS}$ = –5.0 Vdc, $I_D$ = –7.4 Adc) | $Q_g$ | – | 28 | 50 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 4.0 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 9.0 | – | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $R_L$ = 15 Ω, $I_D \cong$ –1.0 Adc, $V_{GEN}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 19 | 50 | ns |
| Rise Time | | $t_r$ | – | 20 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 95 | 120 | |
| Fall Time | | $t_f$ | – | 65 | 100 | |
| Source–Drain Reverse Recovery Time | ($I_F$ = –1.3 Adc, di/dt = 100 A/μs) | $t_{rr}$ | – | 45 | 80 | ns |

2. Surface mounted to 1″ x 1″ FR–4 board.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

# NTTD1P02R2

*Product Preview*

## Power MOSFET -1.45 Amps, -20 Volts

### P–Channel Enhancement Mode Dual Micro8 Package

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Dual Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

**Applications**

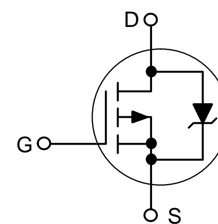
- Power Management in Portable and Battery–Powered Products, i.e.: Computers, Printers, PCMCIA Cards, Cellular and Cordless Telephones

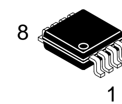
**ON Semiconductor™**

**http://onsemi.com**

**–1.45 AMPERES**
**–20 VOLTS**
**160 mΩ @ $V_{GS}$ = –4.5**

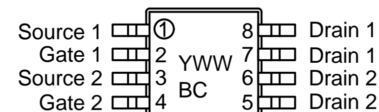
**Dual P–Channel**




**Micro8**
**CASE 846A**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




(Top View)

Y = Year
WW = Work Week
BC = Device Code

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 250 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.50 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –1.45 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.15 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –10 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 125 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.0 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.04 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.64 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –16 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –3.5 Apk, L = 5.6 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 35 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2%.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTTD1P02R2 | Micro8 | 4000/Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | –20<br>– | –<br>–12 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –8 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +8 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | –0.7<br>– | –0.95<br>2.3 | –1.4<br>– | Vdc |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.45 Adc)<br>($V_{GS}$ = –2.7 Vdc, $I_D$ = –0.7 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –0.7 Adc) | | $R_{DS(on)}$ | –<br>–<br>– | 0.130<br>0.175<br>0.190 | 0.160<br>0.250<br>– | Ω |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –0.7 Adc) | | $g_{FS}$ | – | 2.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 265 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 100 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 60 | – | |
| **SWITCHING CHARACTERISTICS** (Notes 5. & 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –16 Vdc, $I_D$ = –1.45 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | – | ns |
| Rise Time | | $t_r$ | – | 25 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | – | |
| Fall Time | | $t_f$ | – | 25 | – | |
| Turn–On Delay Time | ($V_{DD}$ = –16 Vdc, $I_D$ = –0.7 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | – | ns |
| Rise Time | | $t_r$ | – | 20 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | – | |
| Fall Time | | $t_f$ | – | 20 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –1.45 Adc) | $Q_{tot}$ | – | 5.0 | 10 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 2.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 5.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –1.45 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –1.45 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.91<br>–0.72 | –1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –1.45 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 25 | – | ns |
| | | $t_a$ | – | 13 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.015 | – | μC |

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

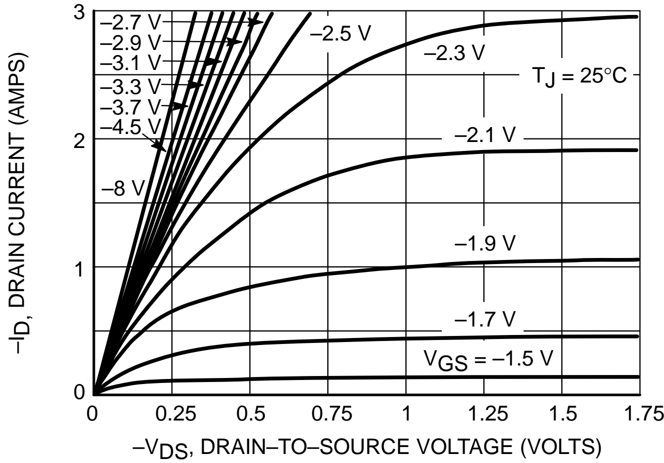



**Figure 1. On−Region Characteristics**

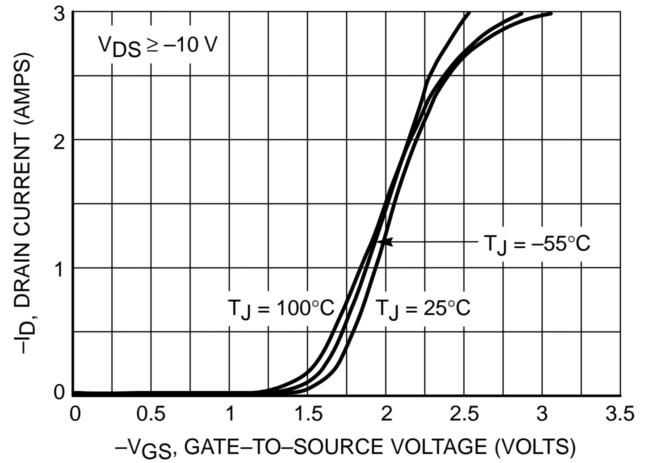



**Figure 2. Transfer Characteristics**

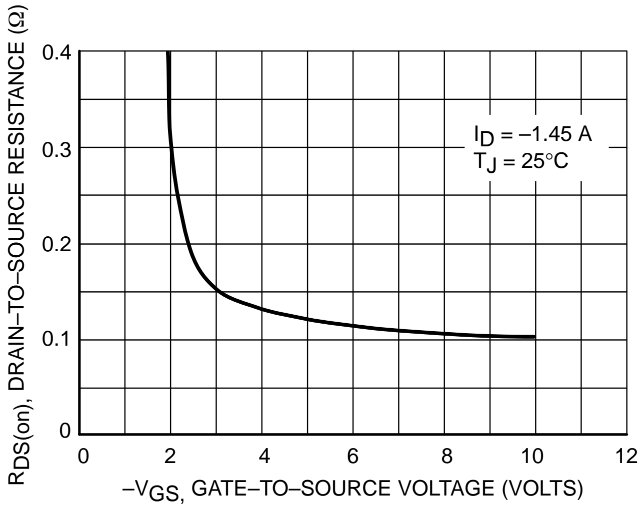



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

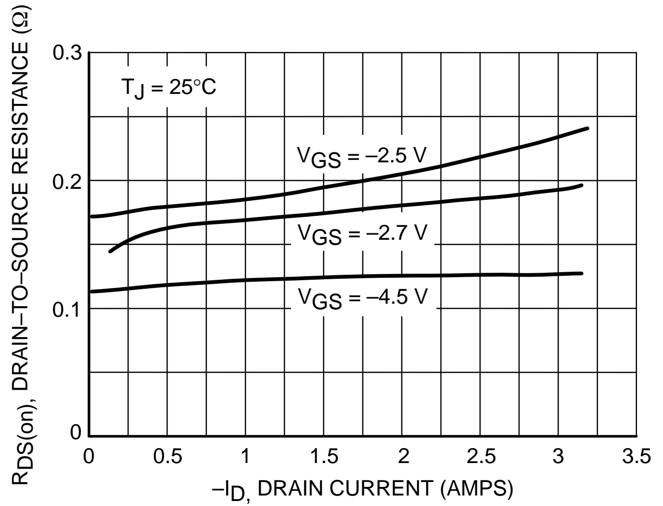



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

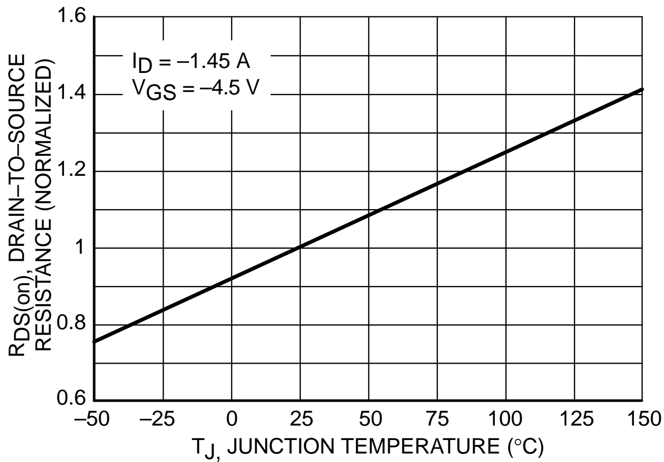



**Figure 5. On−Resistance Variation with Temperature**

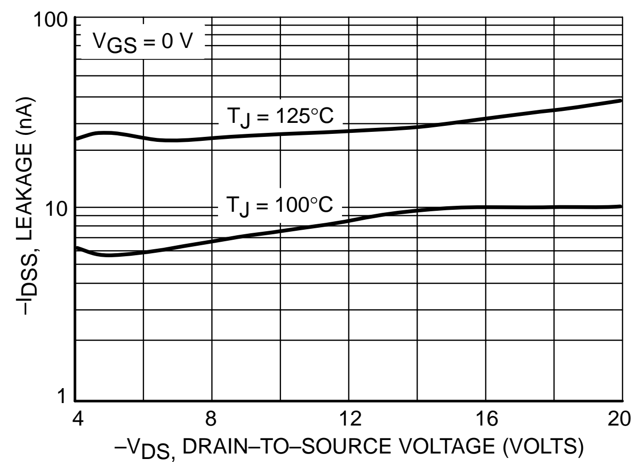



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

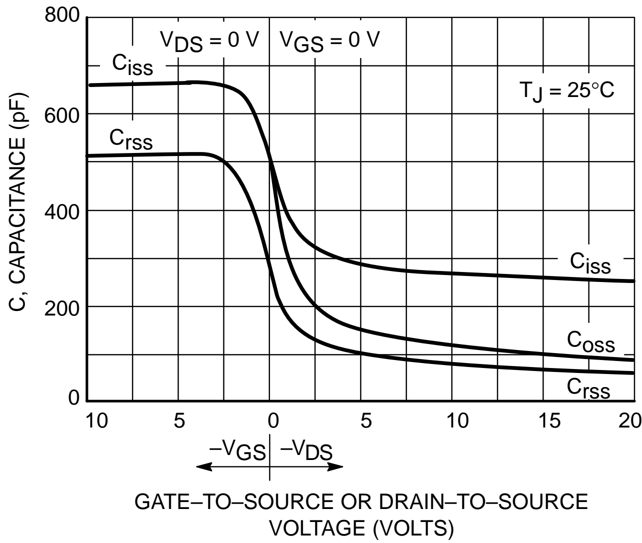



**Figure 7. Capacitance Variation**

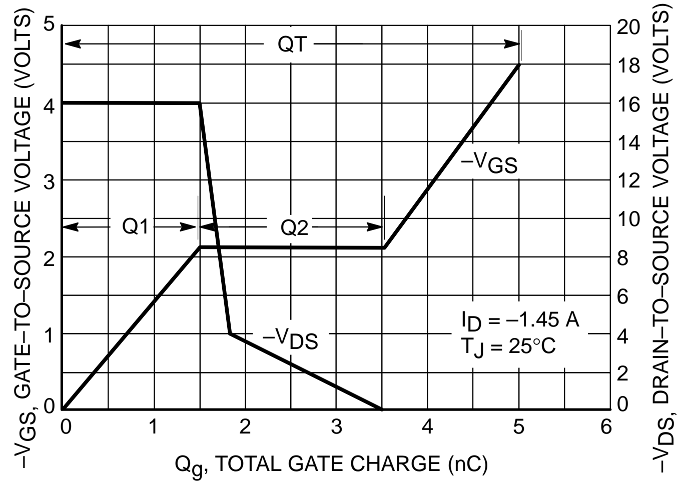



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

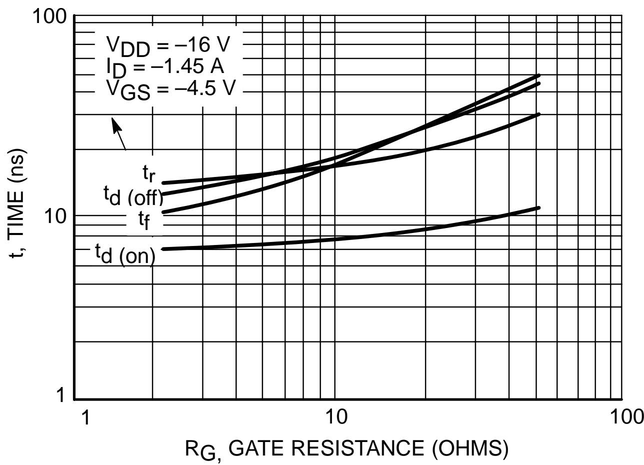



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

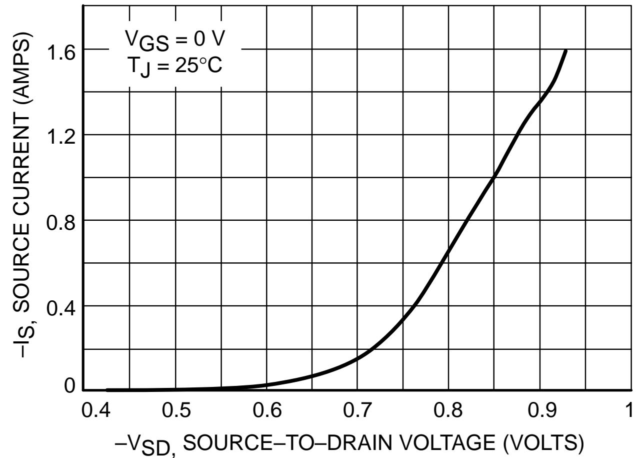



**Figure 10. Diode Forward Voltage versus Current**

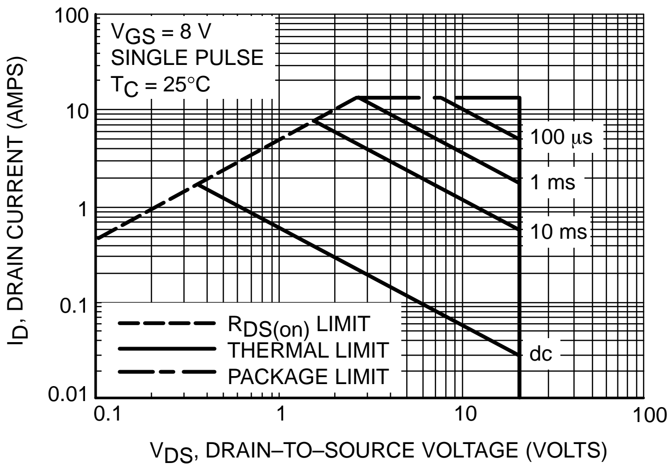



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

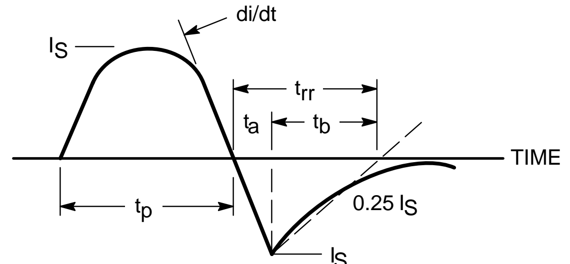



**Figure 12. Diode Reverse Recovery Waveform**

### TYPICAL ELECTRICAL CHARACTERISTICS

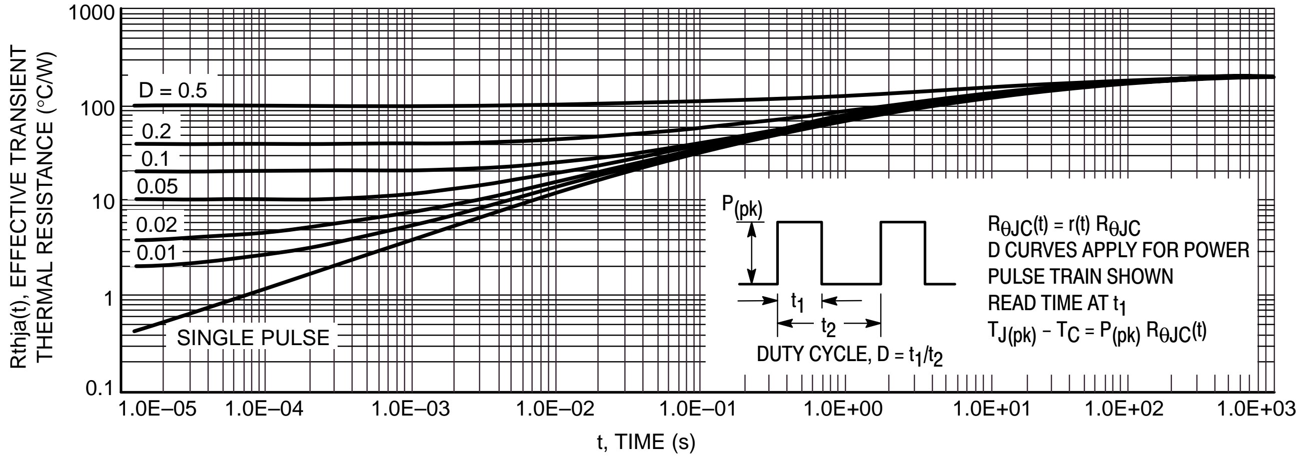
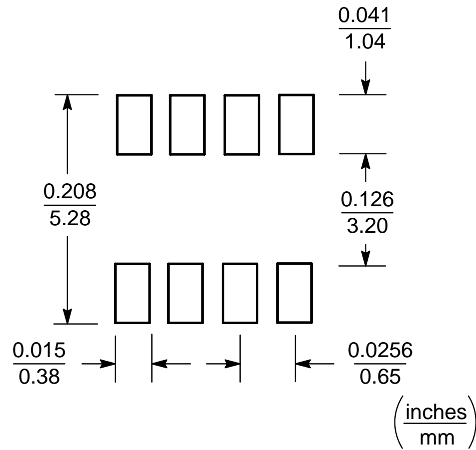



**Figure 13. Thermal Response**

## INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

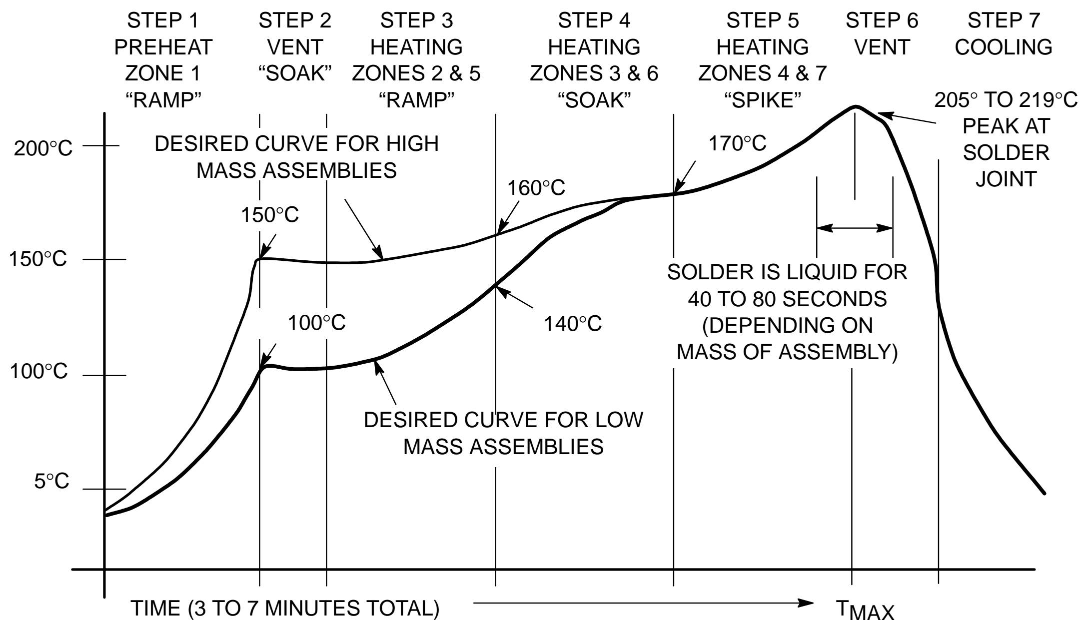
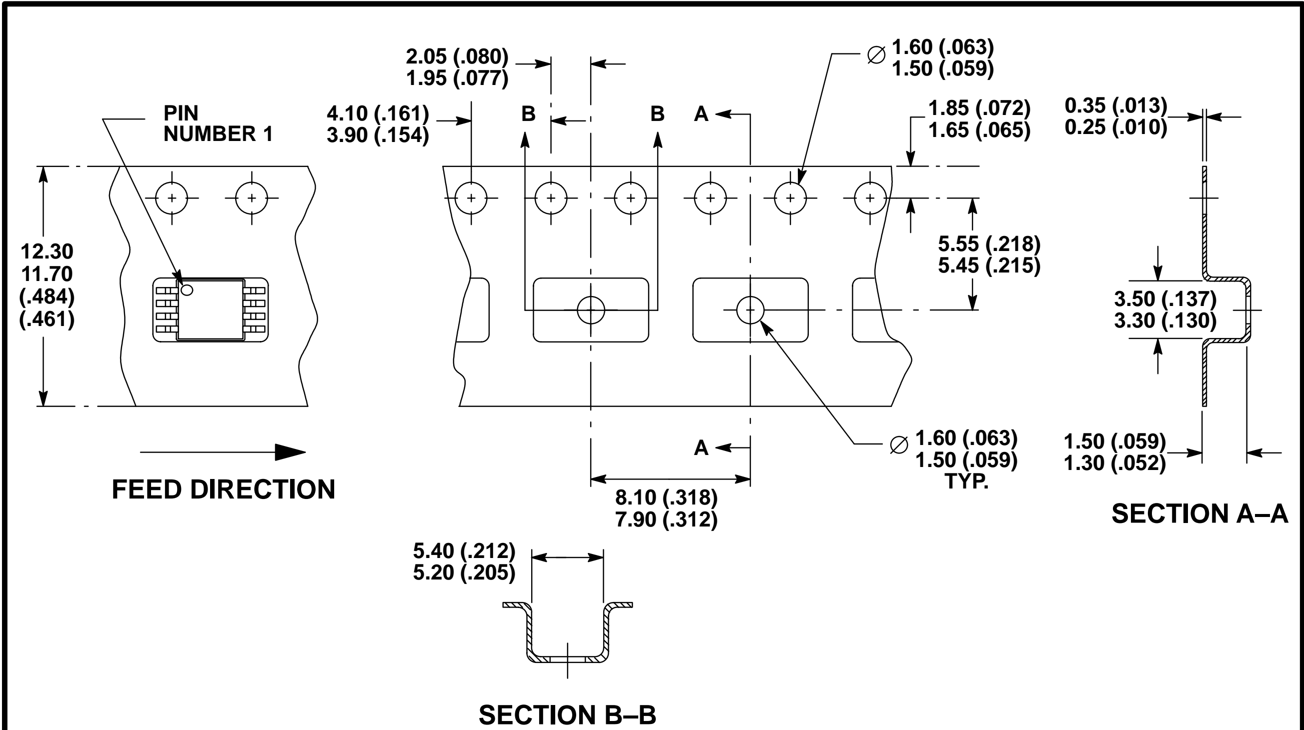



**Figure 14. Typical Solder Heating Profile**

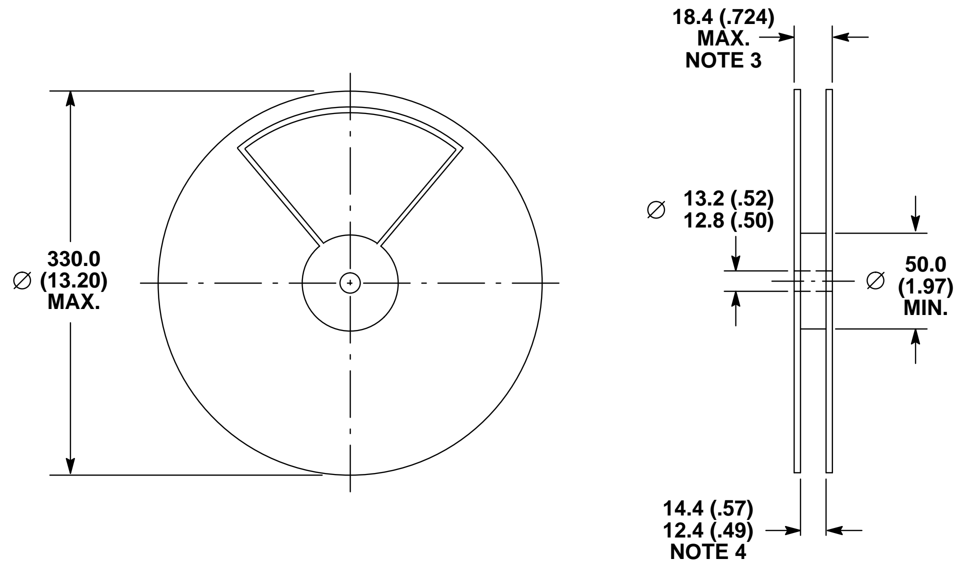
## TAPE & REEL INFORMATION

**Micro8**

Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# NTTD2P02R2

# Power MOSFET -2.4 Amps, -20 Volts

## Dual P–Channel Micro8

### Features

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Micro–8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

### Applications

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 160 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.78 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.4 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.92 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –20 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 88 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.42 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.25 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –2.6 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –30 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –5.0 Apk, L = 28 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 350 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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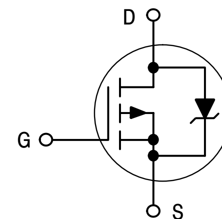
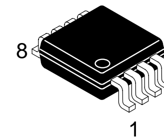
**–2.4 AMPERES**
**–20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ**

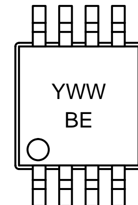
**P–Channel**



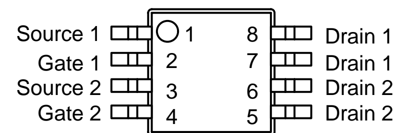

**Micro8**
**CASE 846A**
**STYLE 2**

**MARKING DIAGRAM**




Y = Year
WW = Work Week
BE = Device Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTTD2P02R2 | Micro8 | 4000/Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | –20<br>– | –<br>–12.7 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –16 Vdc, $T_J$ = 25°C)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –16 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–25 | μAdc |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C) | | $I_{DSS}$ | – | – | –5.0 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = –8 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = +8 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | –0.5<br>– | –0.90<br>2.5 | –1.4<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc)<br>($V_{GS}$ = –2.7 Vdc, $I_D$ = –1.2 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –1.2 Adc) | | $R_{DS(on)}$ | –<br>–<br>– | 0.070<br>0.100<br>0.110 | 0.090<br>0.130<br>– | Ω |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –1.2 Adc) | | $g_{FS}$ | 2.0 | 4.2 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 100 | – | |
| **SWITCHING CHARACTERISTICS** (Notes 5. & 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –2.4 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | – | ns |
| Rise Time | | $t_r$ | – | 31 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 33 | – | |
| Fall Time | | $t_f$ | – | 29 | – | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.2 Adc, $V_{GS}$ = –2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | – | ns |
| Rise Time | | $t_r$ | – | 40 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc) | $Q_{tot}$ | – | 10 | 18 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 5.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 5.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.88<br>–0.75 | –1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 37 | – | ns |
| | | $t_a$ | – | 16 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.025 | – | μC |

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

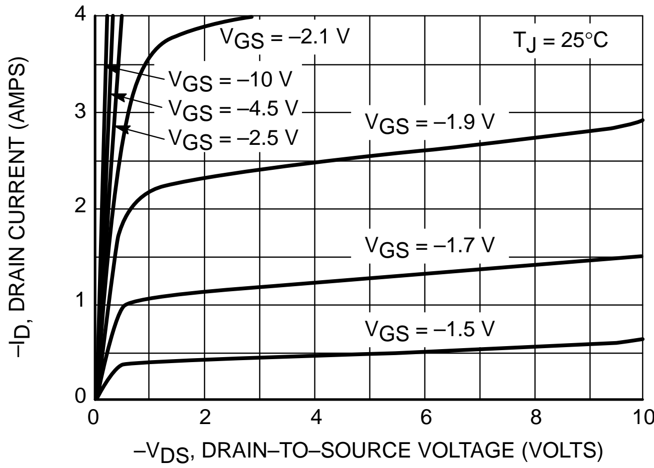



**Figure 1. On–Region Characteristics.**

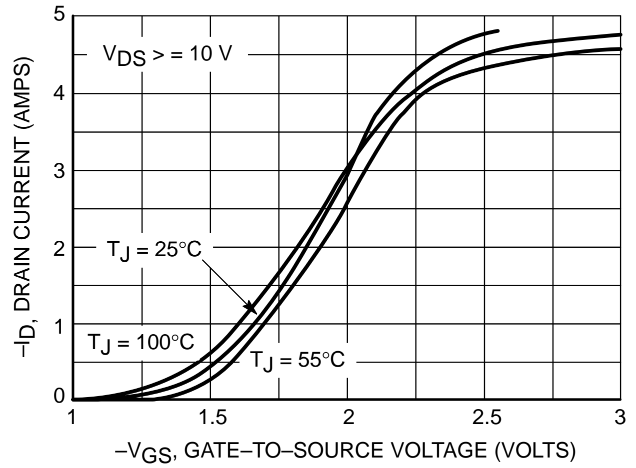



**Figure 2. Transfer Characteristics.**

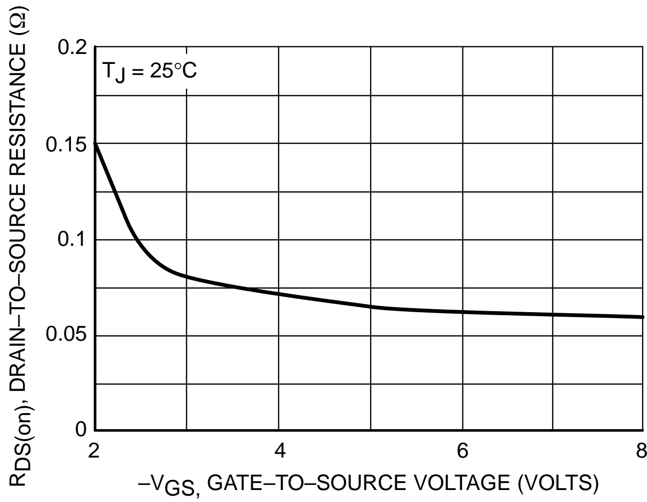



**Figure 3. On–Resistance vs. Gate–to–Source Voltage.**

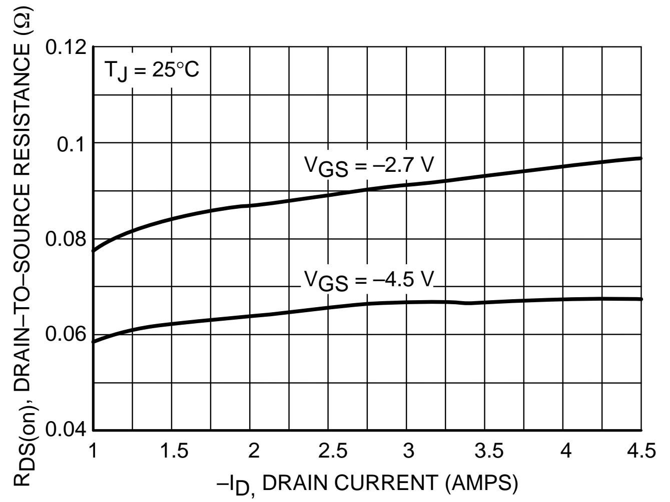



**Figure 4. On–Resistance vs. Drain Current and Gate Voltage.**

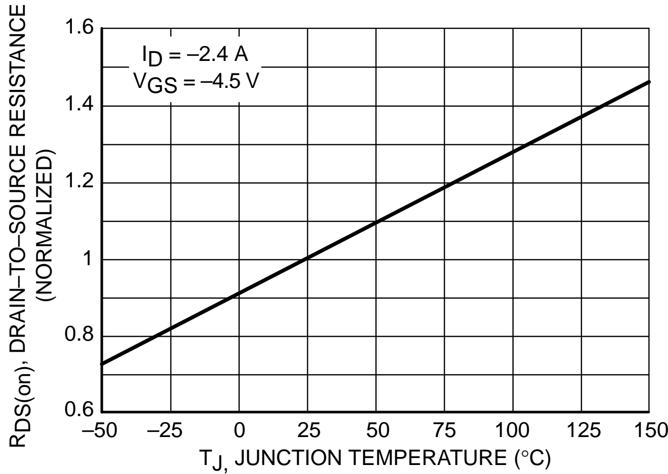



**Figure 5. On–Resistance Variation with Temperature.**

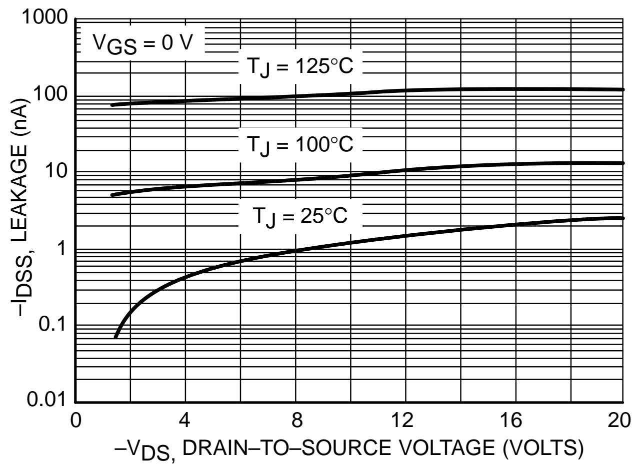



**Figure 6. Drain–to–Source Leakage Current vs. Voltage.**

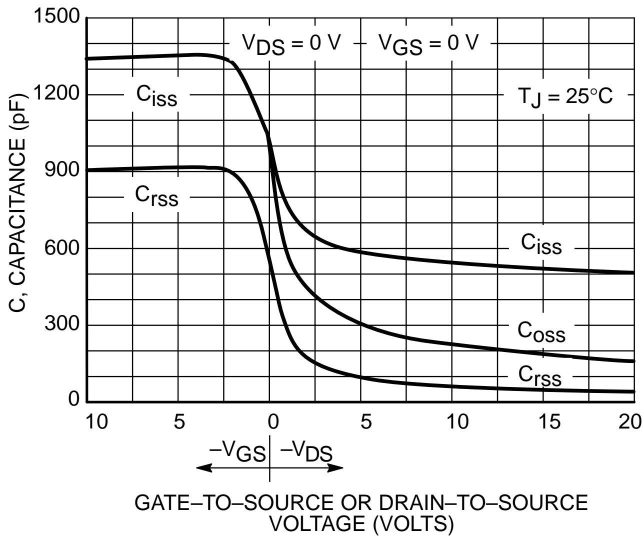



**Figure 7. Capacitance Variation**

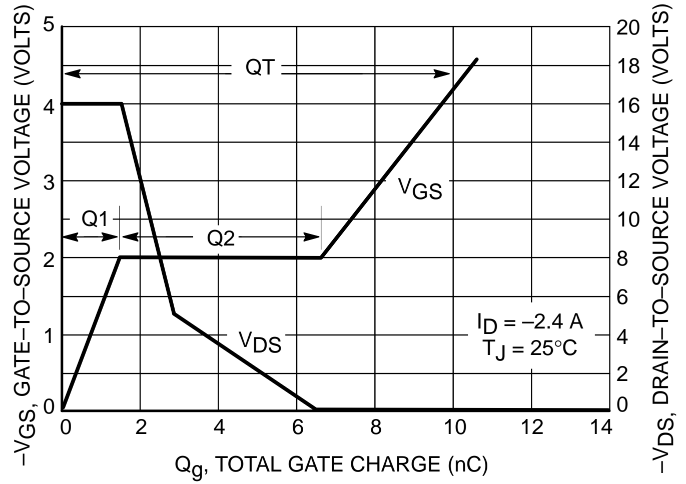



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

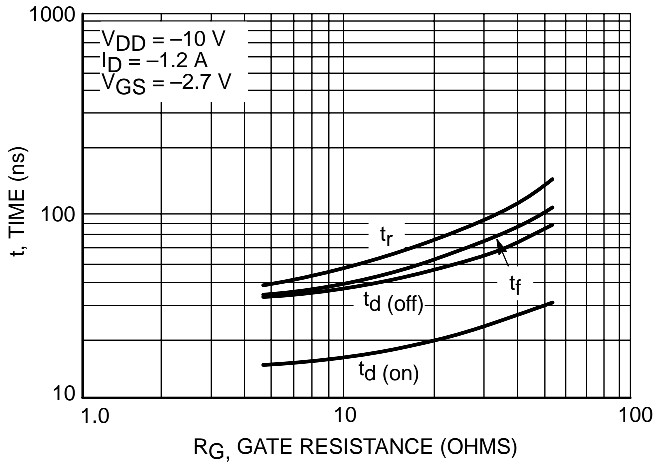



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

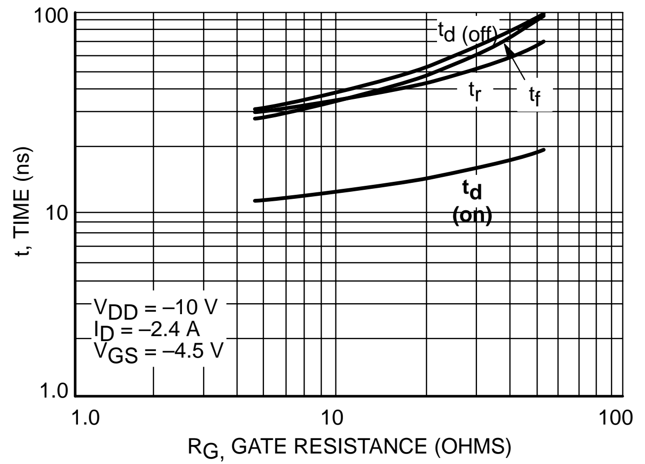



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

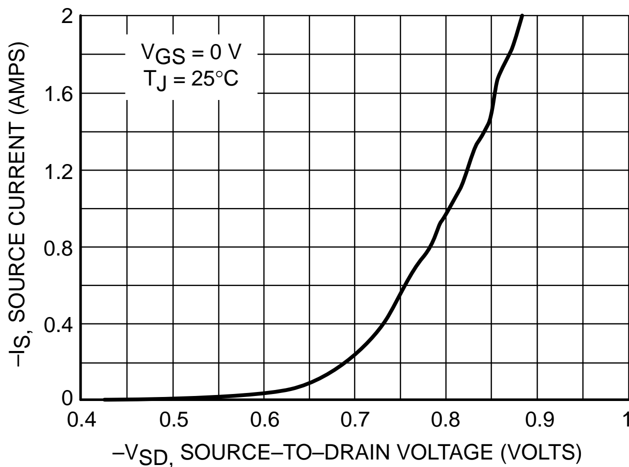



**Figure 11. Diode Forward Voltage versus Current**

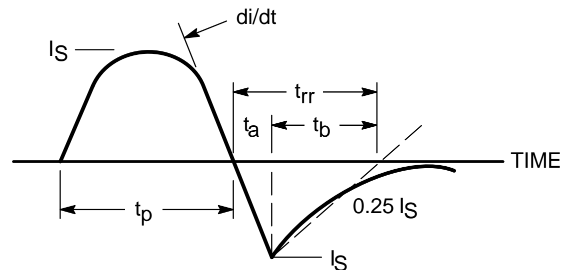



**Figure 12. Diode Reverse Recovery Waveform**

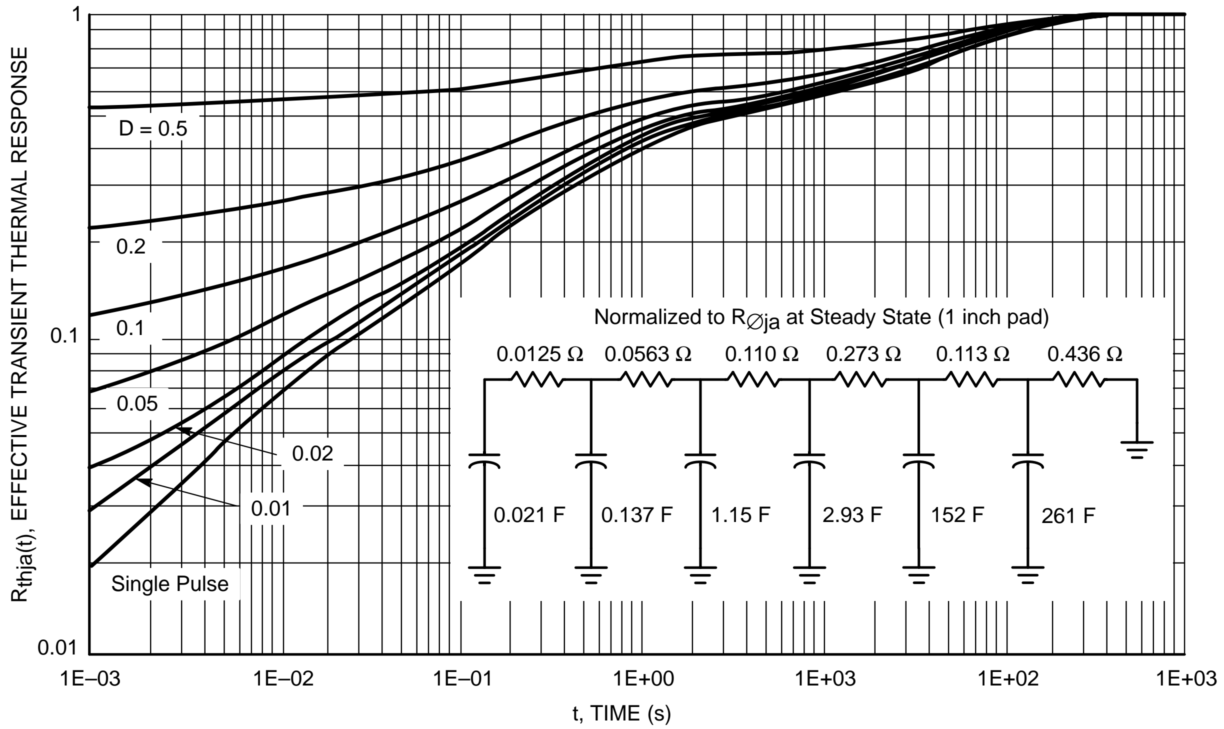
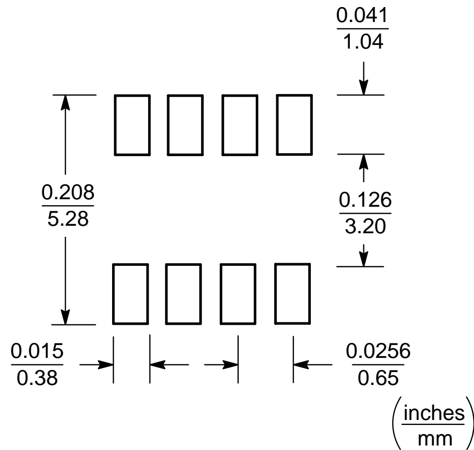



**Figure 13. FET Thermal Response.**

## INFORMATION FOR USING THE Micro–8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

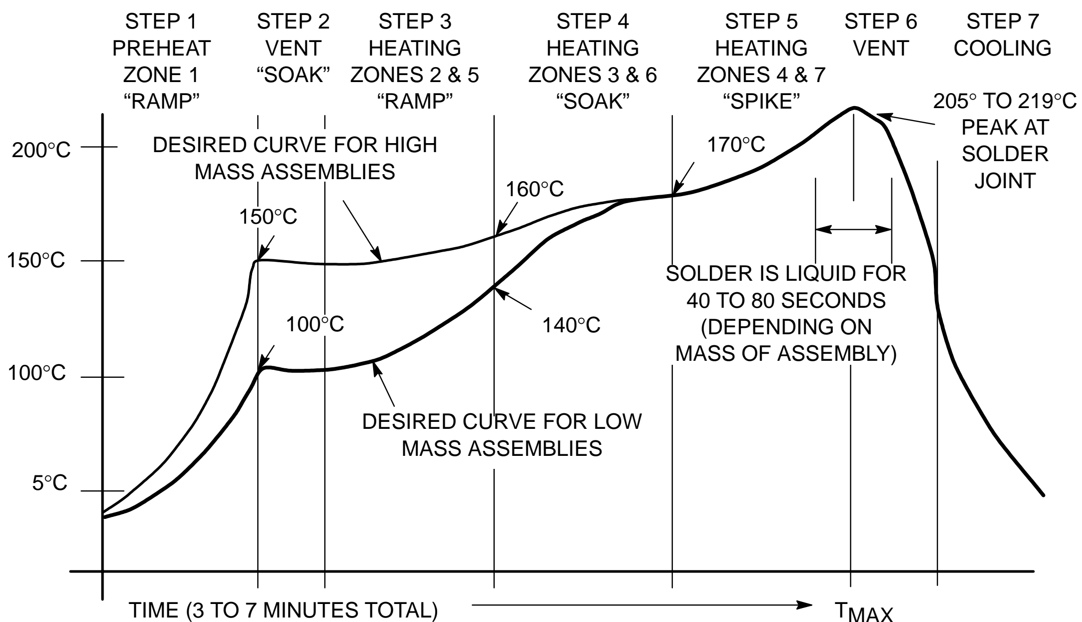
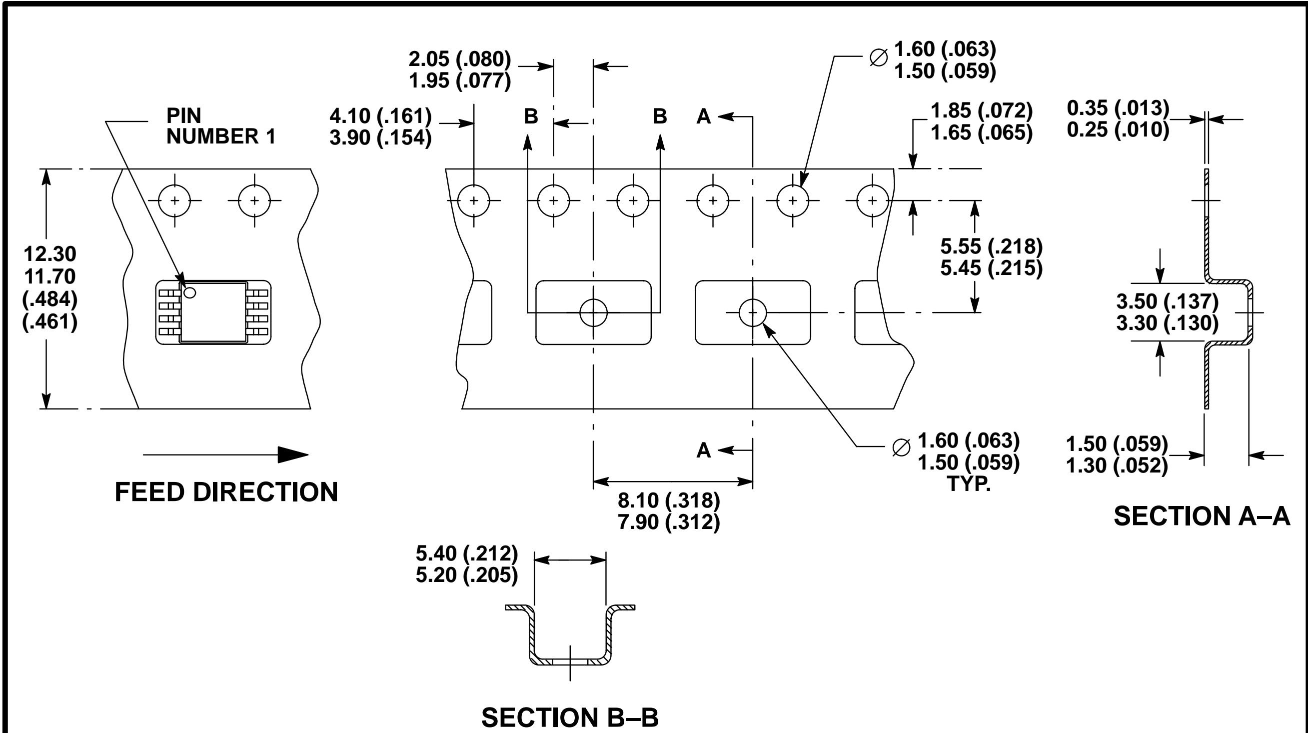



**Figure 14. Typical Solder Heating Profile**

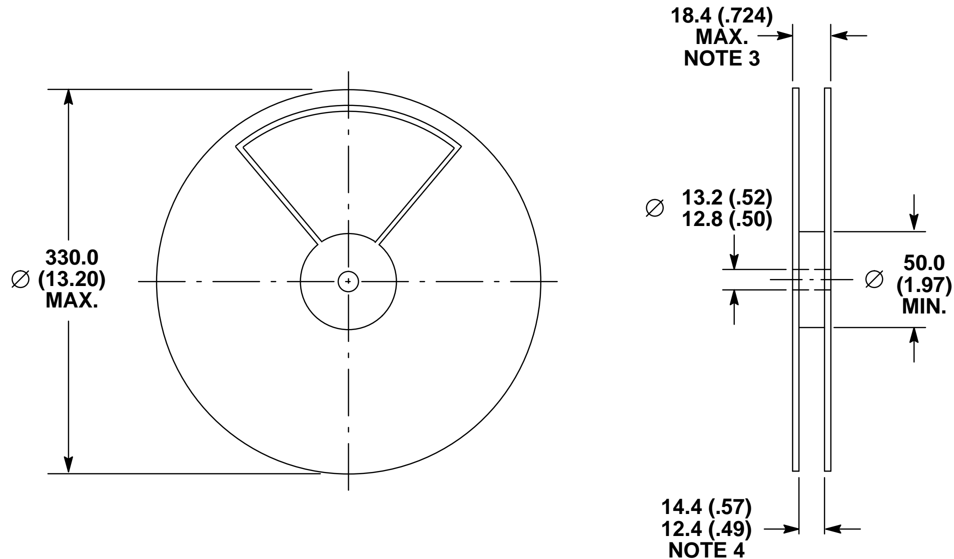
## TAPE & REEL INFORMATION

**Micro–8**

Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# NTTS2P02R2

## Power MOSFET -2.4 Amps, -20 Volts

### Single P–Channel Micro8™

**ON Semiconductor™**

**http://onsemi.com**

**–2.4 AMPERES**
**–20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ**

**Features**

- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Logic Level Gate Drive
- Miniature Micro–8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

**Applications**

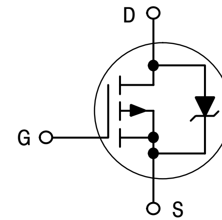
- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

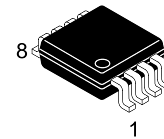
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –20 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±8.0 | V |
| Thermal Resistance – Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 160 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.78 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.4 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.92 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –20 | A |
| Thermal Resistance – Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 88 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.42 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.25 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –2.6 | A |
| Pulsed Drain Current (Note 3.) | $I_{DM}$ | –30 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –20 Vdc, $V_{GS}$ = –4.5 Vdc, Peak $I_L$ = –5.0 Apk, L = 28 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 350 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

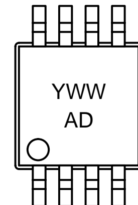
**Single P–Channel**



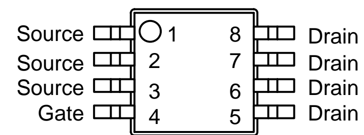

**Micro8**
**CASE 846A**
**STYLE 1**

**MARKING DIAGRAM**




Y = Year
WW = Work Week
AD = Device Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTTS2P02R2 | Micro8 | 4000/Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | –20<br>– | –<br>–12.7 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –16 Vdc, $T_J$ = 25°C)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –16 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–25 | μAdc |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –20 Vdc, $T_J$ = 25°C) | $I_{DSS}$ | – | – | –5.0 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = –8 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = +8 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | –0.5<br>– | –0.90<br>2.5 | –1.4<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc)<br>($V_{GS}$ = –2.7 Vdc, $I_D$ = –1.2 Adc)<br>($V_{GS}$ = –2.5 Vdc, $I_D$ = –1.2 Adc) | $R_{DS(on)}$ | –<br>–<br>– | 0.070<br>0.100<br>0.110 | 0.090<br>0.130<br>– | Ω |
| Forward Transconductance ($V_{DS}$ = –10 Vdc, $I_D$ = –1.2 Adc) | $g_{FS}$ | 2.0 | 4.2 | – | Mhos |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 100 | – | |

**SWITCHING CHARACTERISTICS** (Notes 5. & 6.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –2.4 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | – | ns |
| Rise Time | | $t_r$ | – | 31 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 33 | – | |
| Fall Time | | $t_f$ | – | 29 | – | |
| Turn–On Delay Time | ($V_{DD}$ = –10 Vdc, $I_D$ = –1.2 Adc, $V_{GS}$ = –2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | – | ns |
| Rise Time | | $t_r$ | – | 40 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Total Gate Charge | ($V_{DS}$ = –16 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –2.4 Adc) | $Q_{tot}$ | – | 10 | 18 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.5 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 5.0 | – | |

**BODY–DRAIN DIODE RATINGS** (Note 5.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Diode Forward On–Voltage | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.88<br>–0.75 | –1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –2.4 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 37 | – | ns |
| | | $t_a$ | – | 16 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.025 | – | μC |

4. Handling precautions to protect against electrostatic discharge is mandatory.
5. Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2%.
6. Switching characteristics are independent of operating junction temperature.

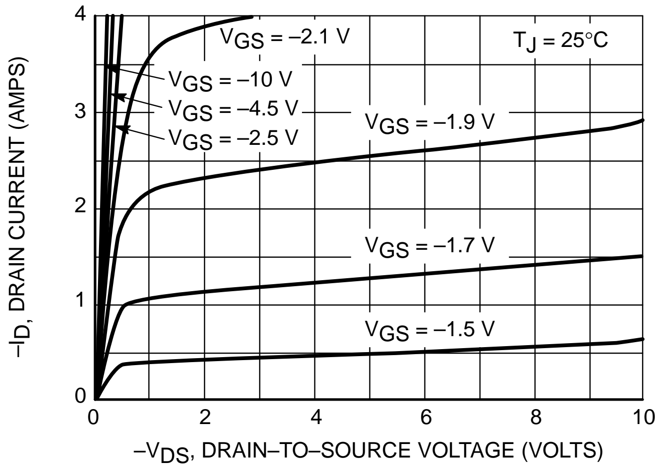



**Figure 1. On−Region Characteristics.**

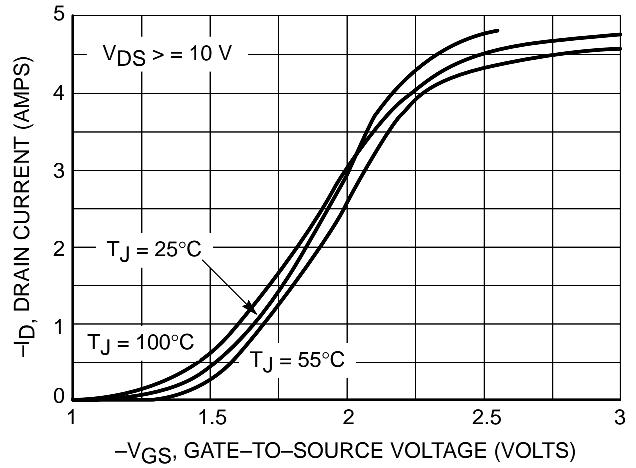



**Figure 2. Transfer Characteristics.**

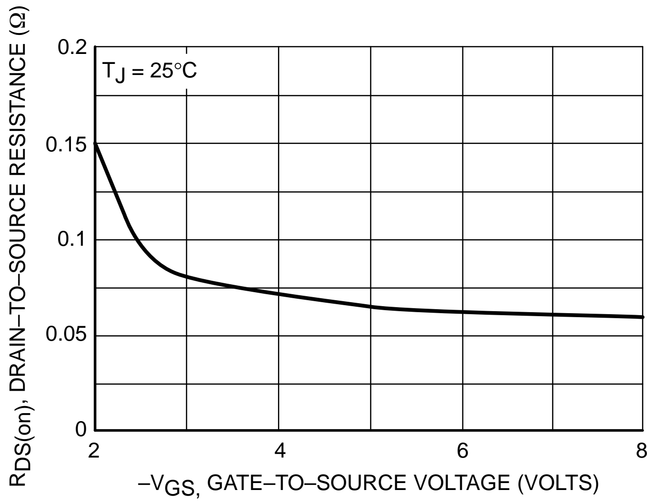



**Figure 3. On−Resistance vs. Gate−to−Source Voltage.**

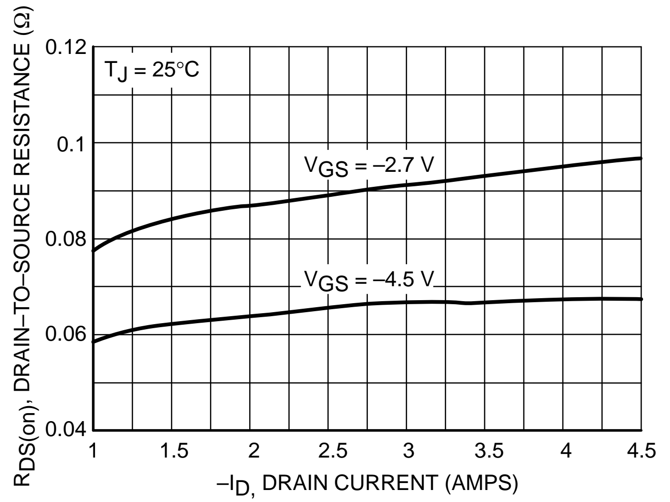



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage.**

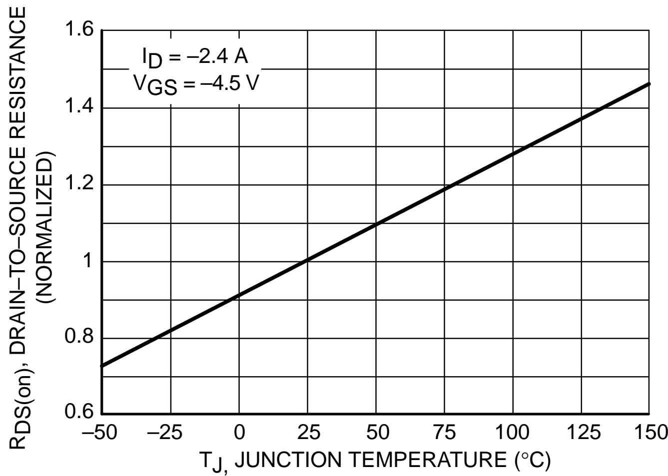



**Figure 5. On−Resistance Variation with Temperature.**

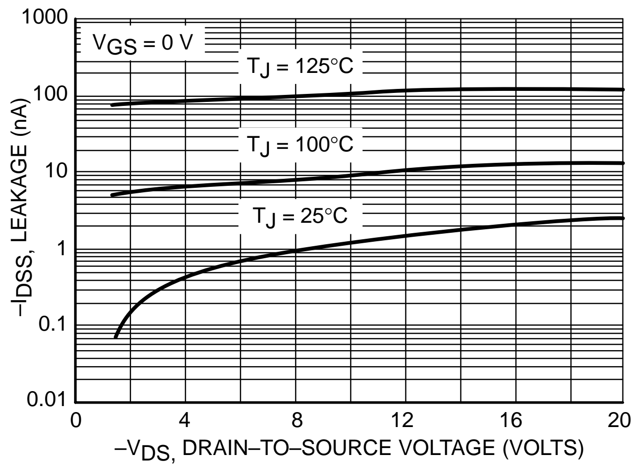



**Figure 6. Drain−to−Source Leakage Current vs. Voltage.**

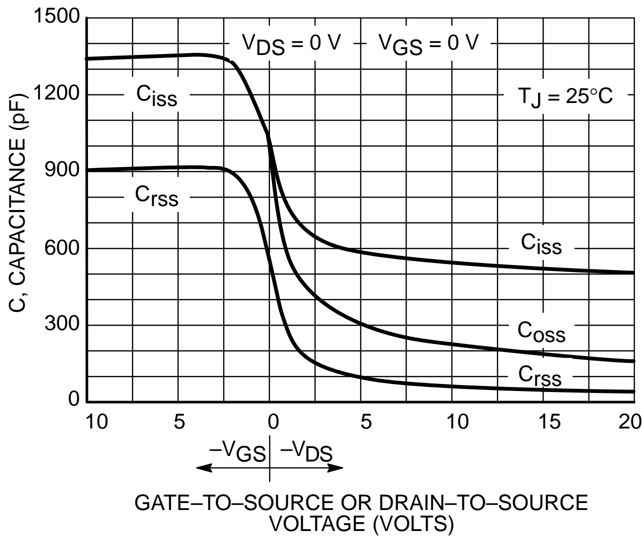



Figure 7. Capacitance Variation

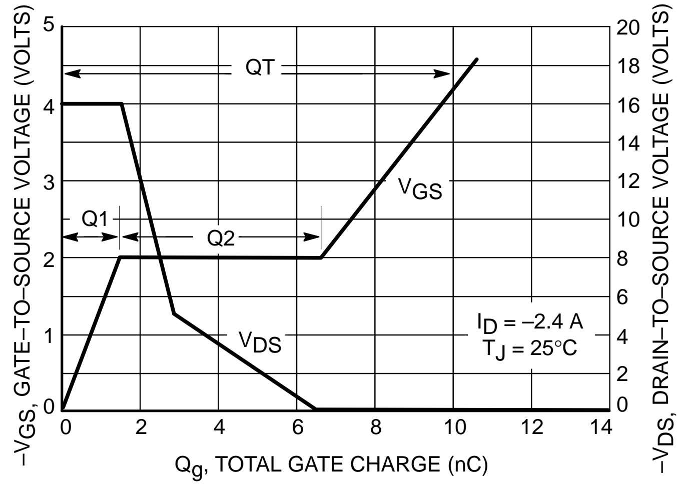



Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge

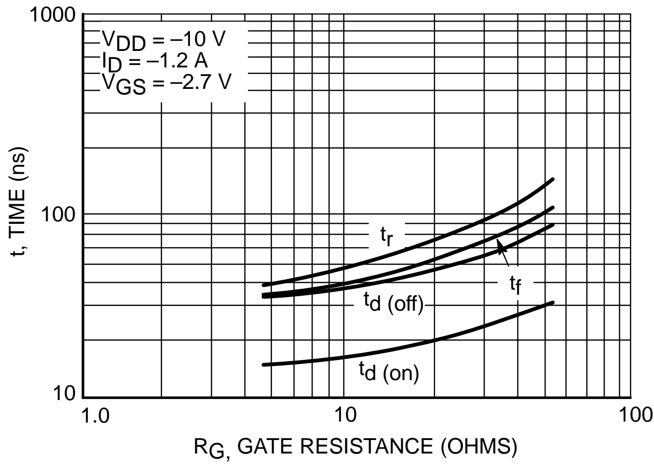



Figure 9. Resistive Switching Time Variation versus Gate Resistance

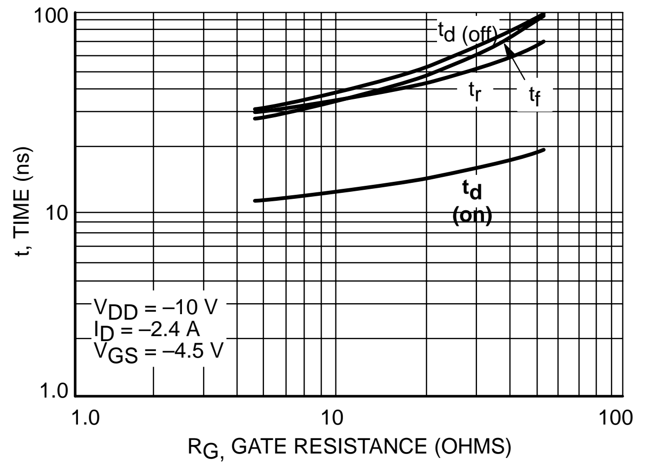



Figure 10. Resistive Switching Time Variation versus Gate Resistance

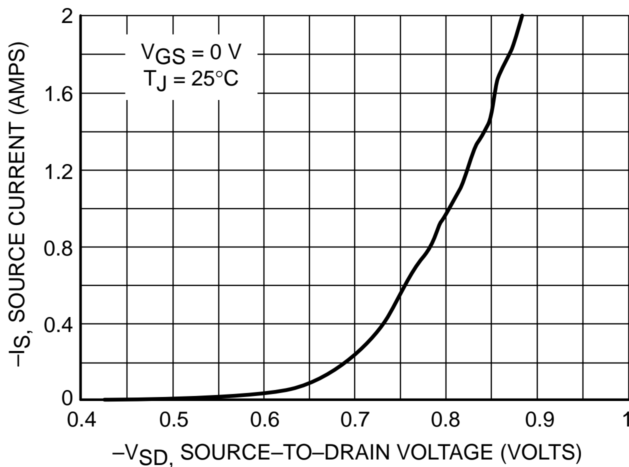



Figure 11. Diode Forward Voltage versus Current

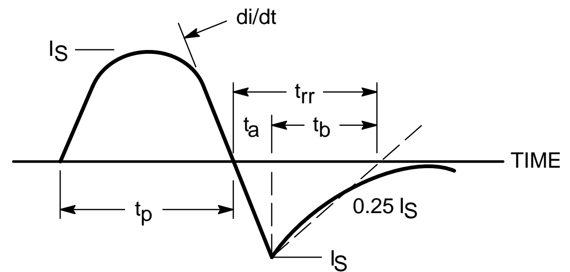



Figure 12. Diode Reverse Recovery Waveform

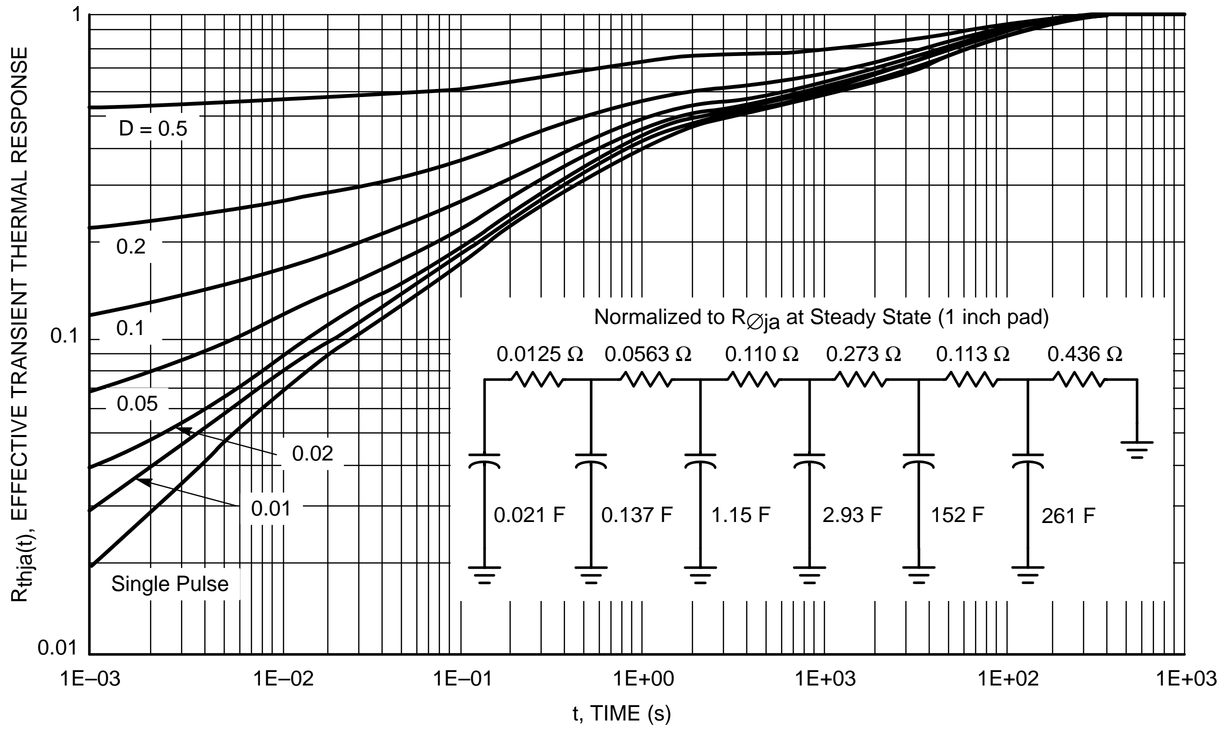
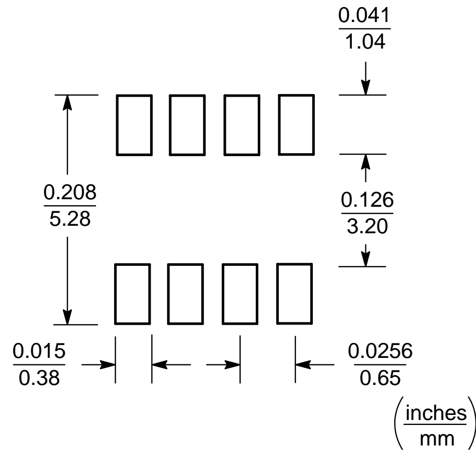



**Figure 13. FET Thermal Response.**

## INFORMATION FOR USING THE Micro–8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

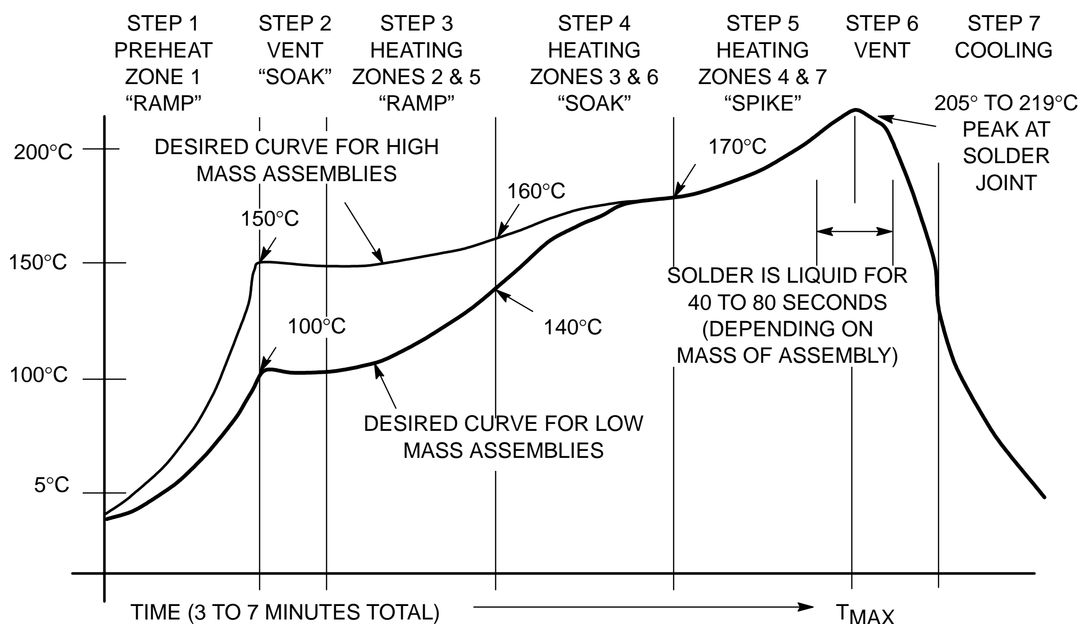
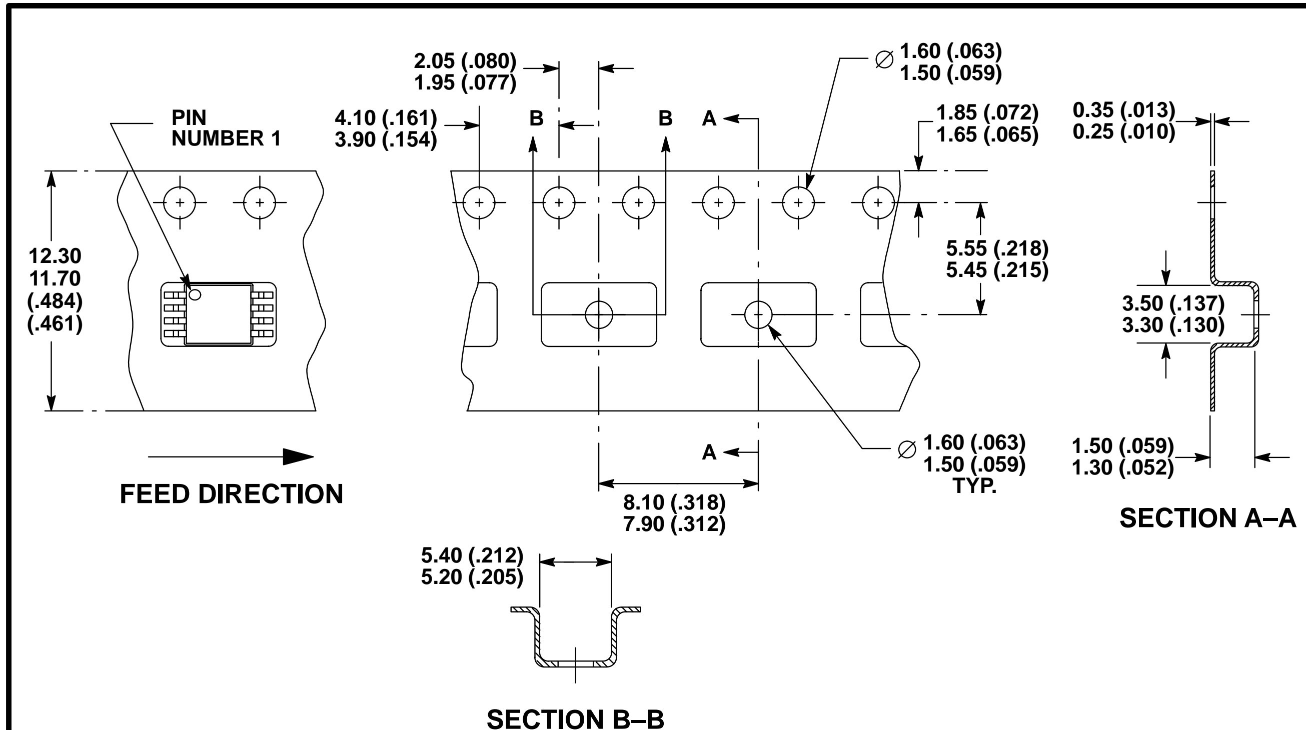


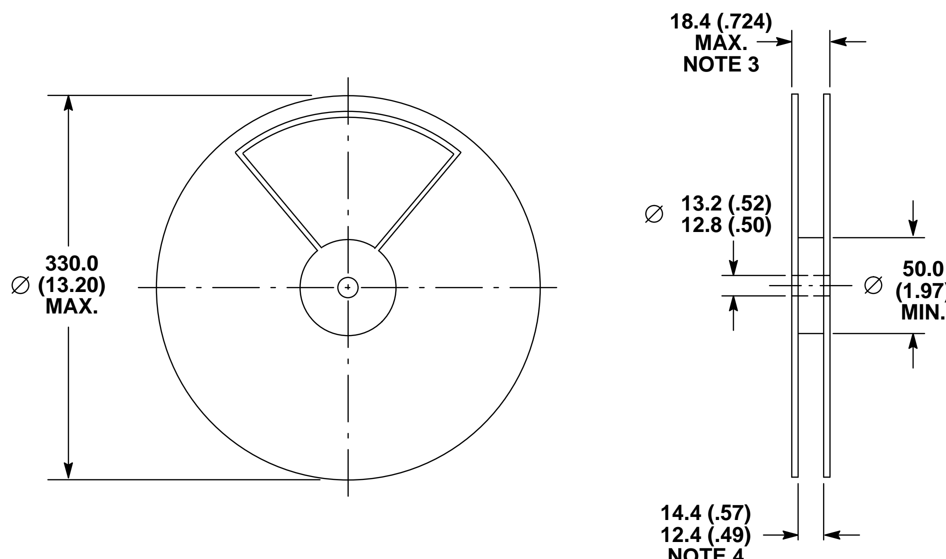

**Figure 14. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro–8**
Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# NTTS2P03R2

**ON Semiconductor™**

**http://onsemi.com**

*Product Preview*

## Power MOSFET -2.48 Amps, -30 Volts

### P–Channel Enhancement Mode Single Micro8™ Package

**Features**

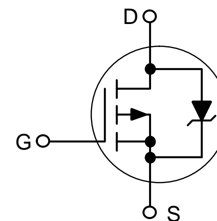
- Ultra Low $R_{DS(on)}$
- Higher Efficiency Extending Battery Life
- Miniature Micro8 Surface Mount Package
- Diode Exhibits High Speed, Soft Recovery
- Micro8 Mounting Information Provided

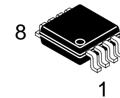
**Applications**

- Power Management in Portable and Battery–Powered Products, i.e.: Cellular and Cordless Telephones and PCMCIA Cards

**–2.48 AMPERES**
**–30 VOLTS**
**85 mΩ @ $V_{GS}$ = –10 V**

**Single P–Channel**



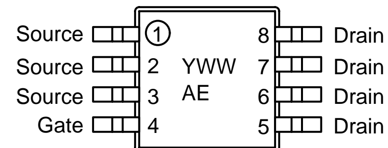

**Micro8**
**CASE 846A**
**STYLE 1**

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –30 | V |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | V |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 160 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.78 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.48 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.98 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | 70 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.78 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.75 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –3.0 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 3.) | $R_{\theta JA}$ | 210 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 0.60 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –2.10 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –1.67 | A |
| Pulsed Drain Current (Note 5.) | $I_{DM}$ | –17 | A |
| Thermal Resistance – | | | |
| Junction–to–Ambient (Note 4.) | $R_{\theta JA}$ | 100 | °C/W |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.25 | W |
| Continuous Drain Current @ $T_A$ = 25°C | $I_D$ | –3.02 | A |
| Continuous Drain Current @ $T_A$ = 70°C | $I_D$ | –2.42 | A |
| Pulsed Drain Current (Note 5.) | $I_{DM}$ | –24 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. Minimum FR–4 or G–10 PCB, Time ≤ 10 Seconds.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Time ≤ 10 Seconds.
3. Minimum FR–4 or G–10 PCB, Steady State.
4. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz Cu 0.06″ thick single sided), Steady State.
5. Pulse Test: Pulse Width = 300 µs, Duty Cycle = 2%.

**MARKING DIAGRAM & PIN ASSIGNMENT**




(Top View)

Y = Year
WW = Work Week
AE = Device Code

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTTS2P03R2 | Micro8 | 4000/Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (continued)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = –30 Vdc, $V_{GS}$ = –10 Vdc, Peak $I_L$ = –3.0 Apk, L = 65 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 292.5 | mJ |
| Maximum Lead Temperature for Soldering Purposes for 10 seconds | $T_L$ | 260 | °C |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | –30<br>– | –<br>–30 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –30 Vdc, $T_J$ = 25°C)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = –30 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | –1.0<br>–25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = –20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | –100 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = +20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = –250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | –1.0<br>– | –1.7<br>3.6 | –3.0<br>– | Vdc |
| Static Drain–to–Source On–State Resistance<br>($V_{GS}$ = –10 Vdc, $I_D$ = –2.48 Adc)<br>($V_{GS}$ = –4.5 Vdc, $I_D$ = –1.24 Adc) | | $R_{DS(on)}$ | –<br>– | 0.063<br>0.100 | 0.085<br>0.135 | Ω |
| Forward Transconductance ($V_{DS}$ = –15 Vdc, $I_D$ = –1.24 Adc) | | $g_{FS}$ | – | 3.1 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 500 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 160 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 65 | – | |
| **SWITCHING CHARACTERISTICS** (Notes 7. & 8.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –2.48 Adc, $V_{GS}$ = –10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | – | ns |
| Rise Time | | $t_r$ | – | 20 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 40 | – | |
| Fall Time | | $t_f$ | – | 35 | – | |
| Turn–On Delay Time | ($V_{DD}$ = –24 Vdc, $I_D$ = –1.24 Adc, $V_{GS}$ = –4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 40 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | – | |
| Fall Time | | $t_f$ | – | 30 | – | |
| Total Gate Charge | ($V_{DS}$ = –24 Vdc, $V_{GS}$ = –4.5 Vdc, $I_D$ = –2.48 Adc) | $Q_{tot}$ | – | 15 | 22 | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 3.2 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 4.0 | – | |
| **BODY–DRAIN DIODE RATINGS** (Note 7.) | | | | | | |
| Diode Forward On–Voltage | ($I_S$ = –2.48 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = –2.48 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | –0.92<br>–0.72 | –1.3<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = –1.45 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 18 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.04 | – | μC |

6. Handling precautions to protect against electrostatic discharge is mandatory.
7. Indicates Pulse Test: Pulse Width = 300 μsec max, Duty Cycle = 2%.
8. Switching characteristics are independent of operating junction temperature.

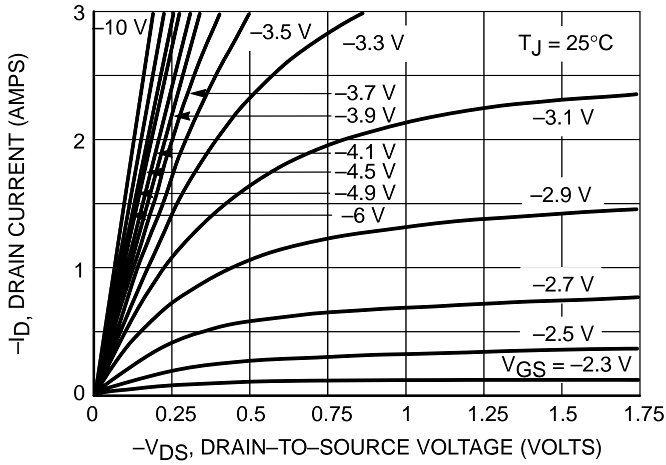



**Figure 1. On−Region Characteristics**

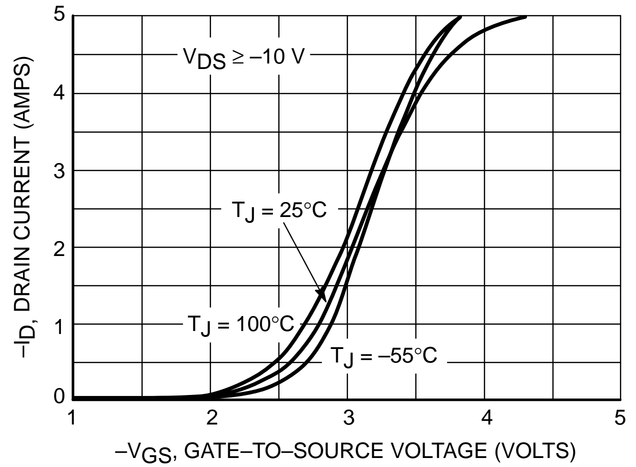



**Figure 2. Transfer Characteristics**

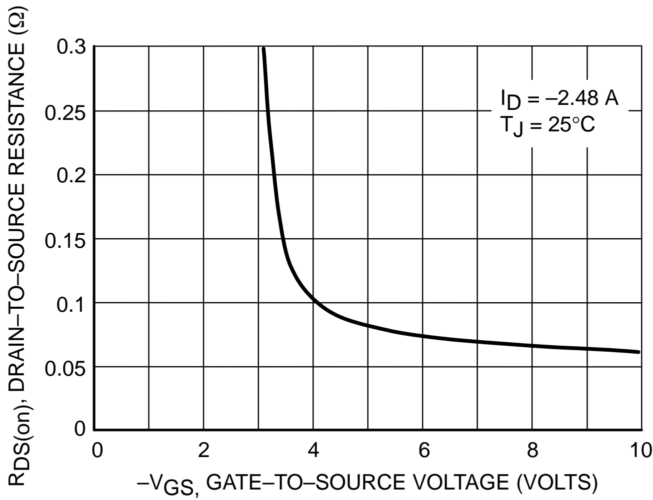



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

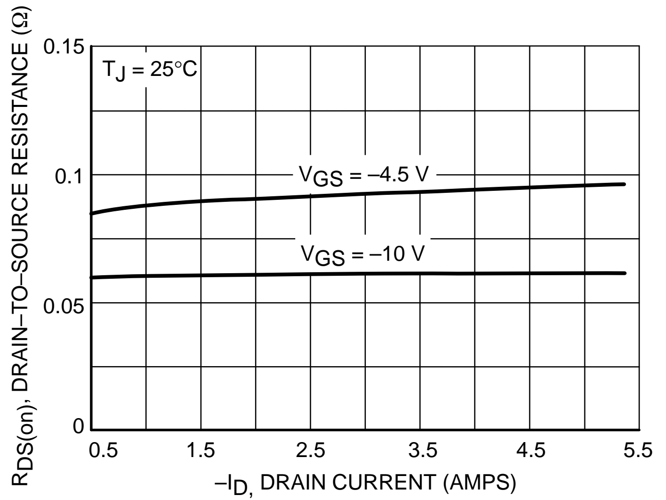



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

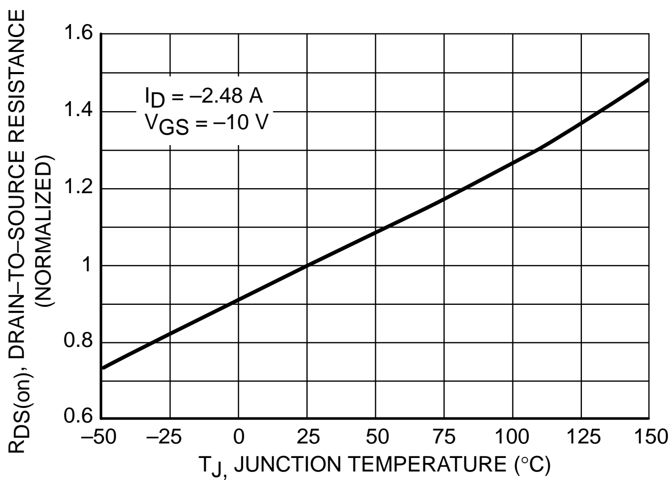



**Figure 5. On−Resistance Variation with Temperature**

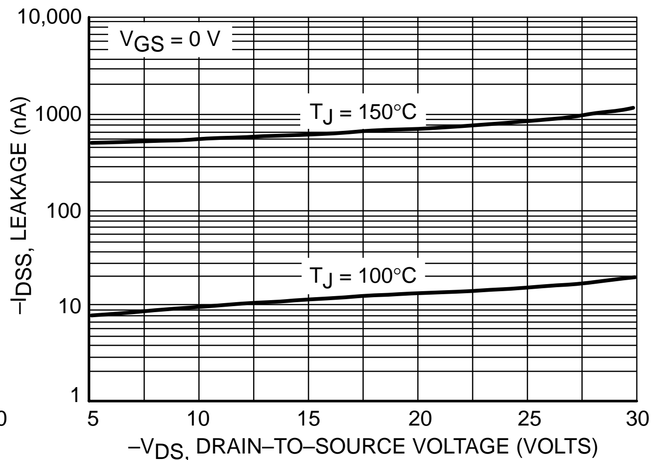



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

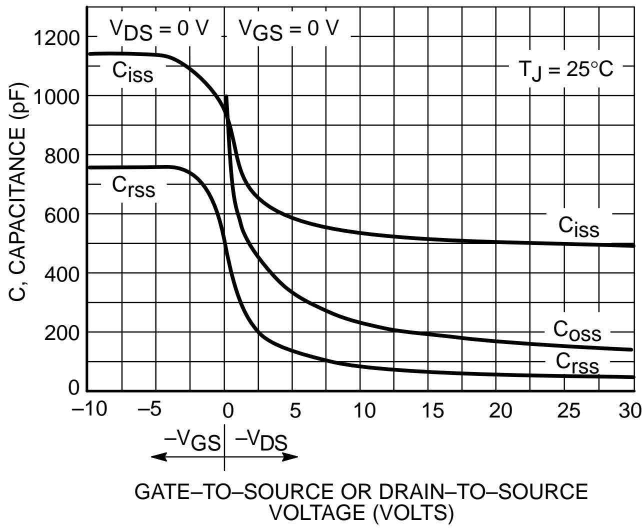



**Figure 7. Capacitance Variation**

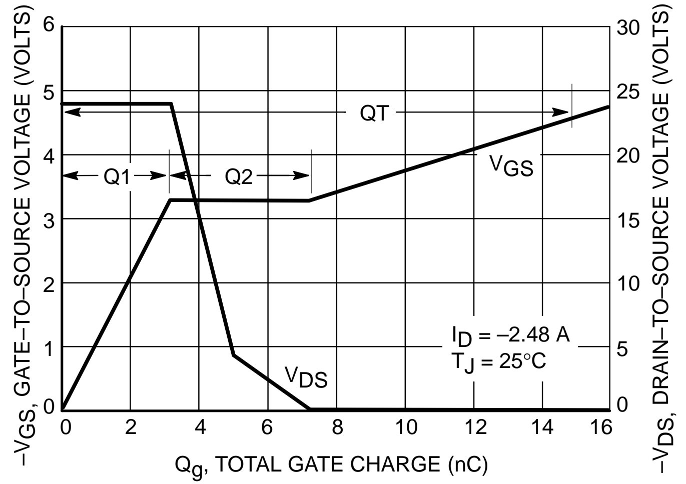



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

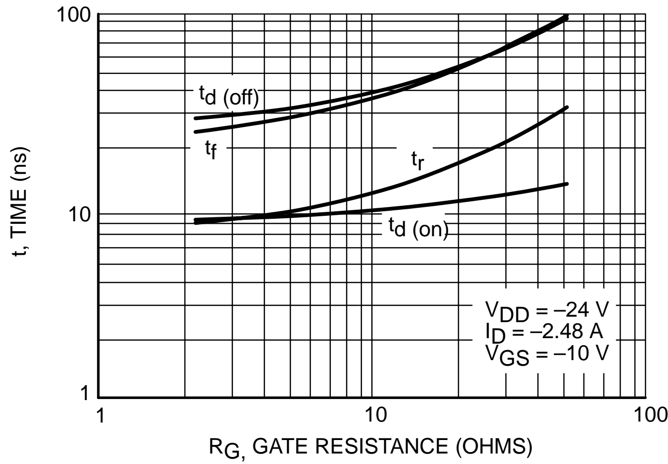



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

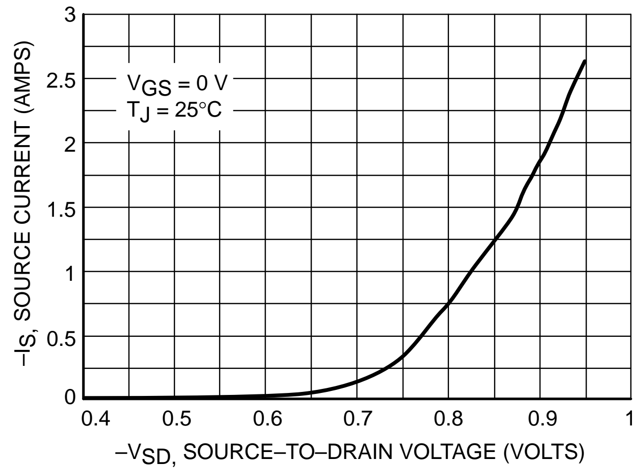



**Figure 10. Diode Forward Voltage versus Current**

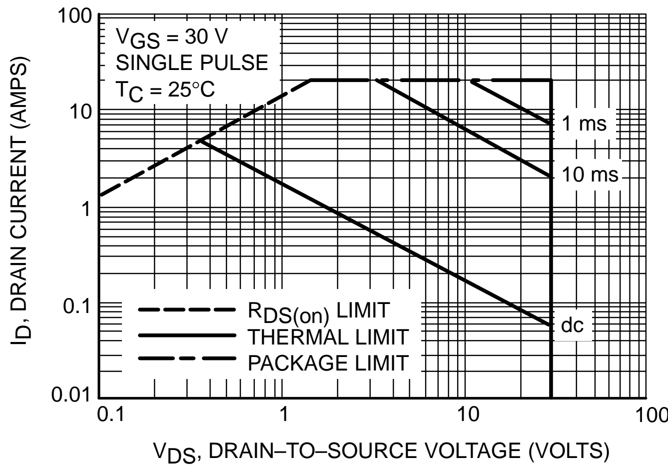



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

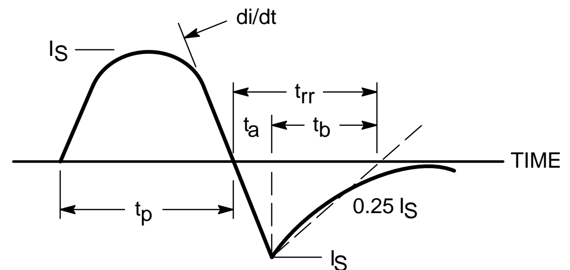



**Figure 12. Diode Reverse Recovery Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

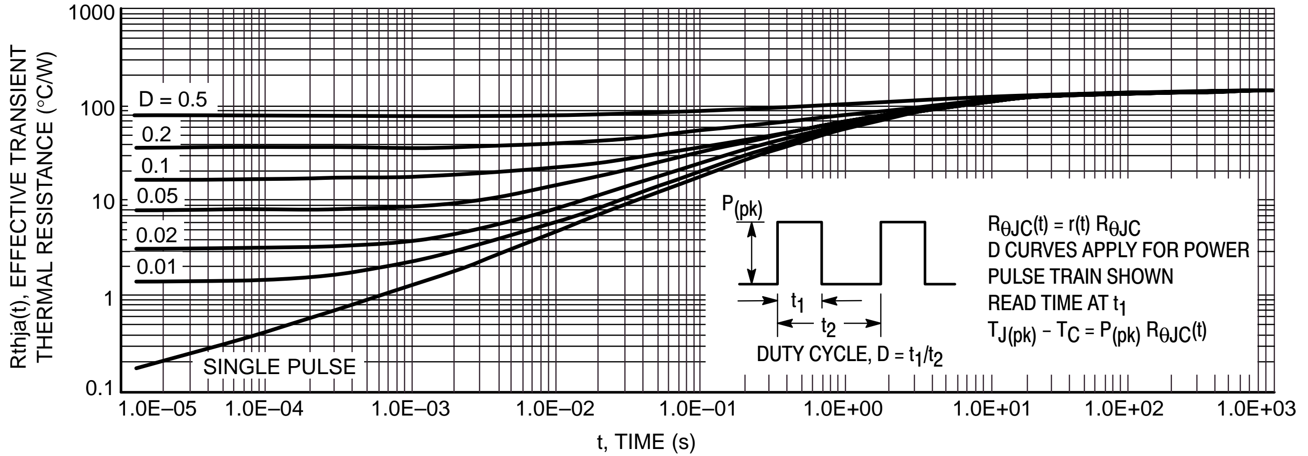
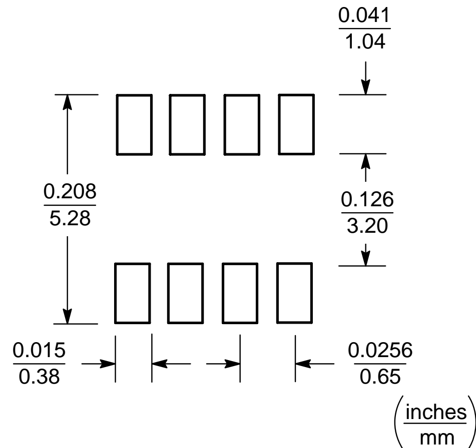



**Figure 13. Thermal Response**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.



## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

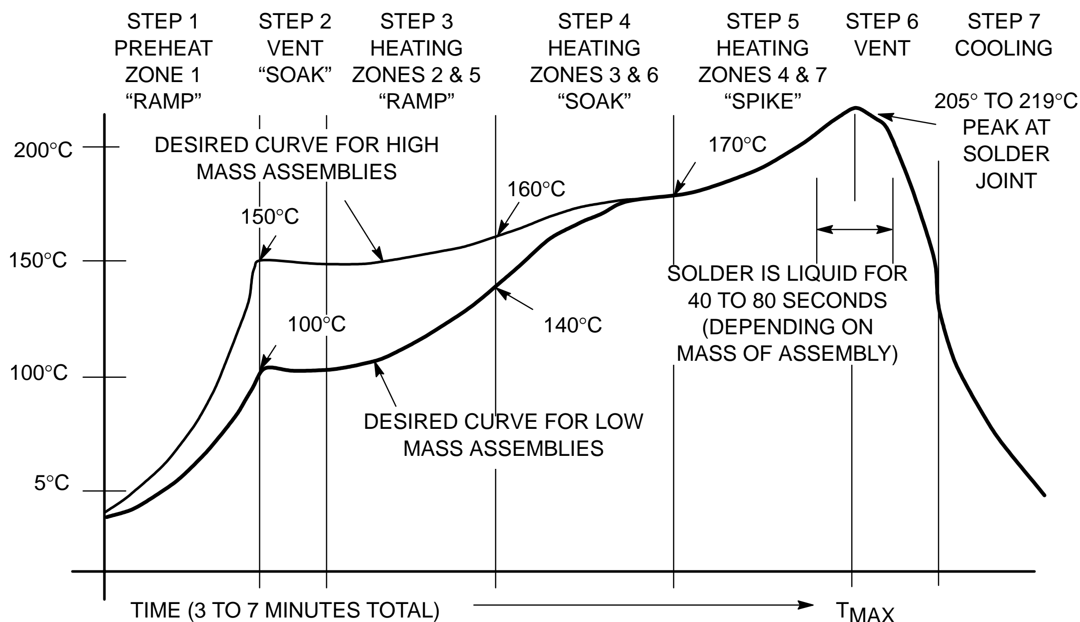
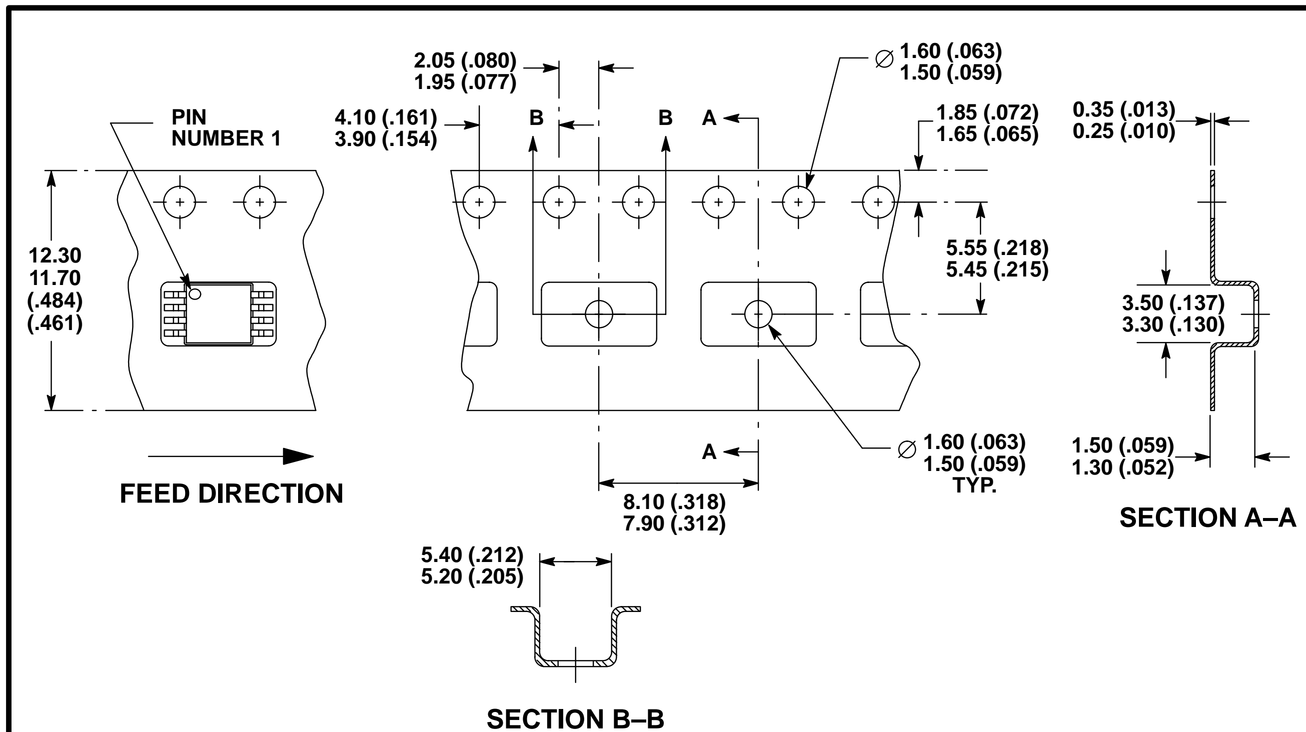


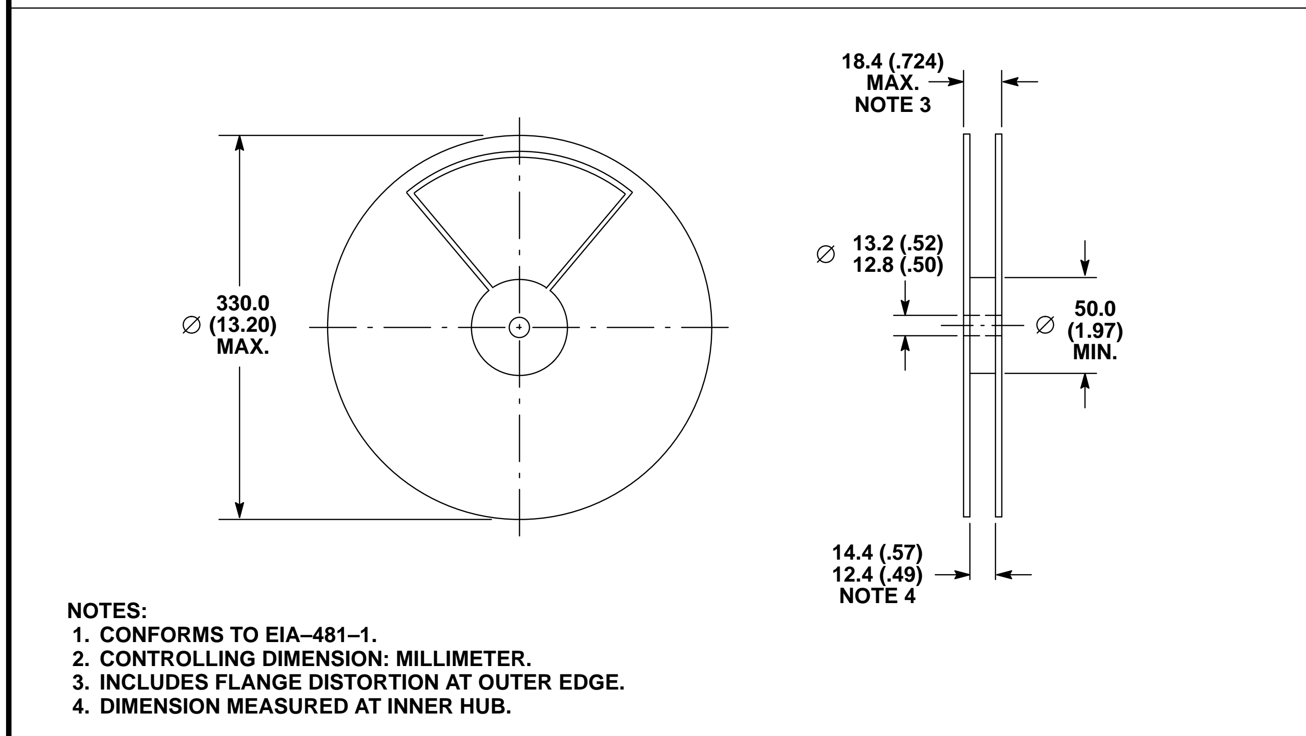

**Figure 14. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro–8**
Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# NTUD01N02

*Product Preview*

## Power MOSFET 100 mAmps, 20 Volts

### Dual N–Channel SC–88

- 2.5 V Gate Drive with Low On–Resistance
- Low Threshold Voltage: $V_{th}$ = 0.5 to 1.5 V, Ideal for Portable
- High Speed
- Enhancement Mode
- Small Package
- Easily Designed Drive Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

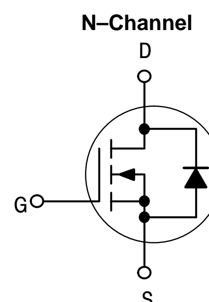
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GSS}$ | 10 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C | $I_D$ | 100 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 150 | mW |
| Channel Temperature | $T_{ch}$ | 150 | °C |
| Operating and Storage Temperature Range | $T_{stg}$ | – 55 to 150 | °C |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

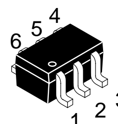
ON Semiconductor™

http://onsemi.com

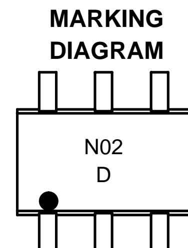
**100 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 10 Ω**




**MARKING DIAGRAM**

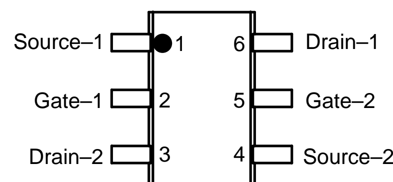



**SC–88/SOT–363**
**CASE 419B**
**STYLE 1**




N02 = Device Code
D = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| NTUD01N02 | SC–88 | 3000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 100 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Drain Cut–off Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 10 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 1.0 | μAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = 3.0 Vdc, $I_D$ = 0.1 mAdc) | | $V_{th}$ | 0.5 | – | 1.5 | Vdc |
| Drain–to–Source On–Resistance ($V_{GS}$ = 2.5 Vdc, $I_D$ = 10 mAdc) | | $R_{DS(on)}$ | – | 5.0 | 10 | Ω |
| Forward Transfer Admittance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 10 mAdc) | | $Y_{FS}$ | 20 | – | – | mS |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 3.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 5.5 | – | pF |
| Output Capacitance | ($V_{DS}$ = 3.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{oss}$ | – | 25 | – | |
| Reverse Transfer Capacitance | ($V_{DS}$ = 3.0 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{rss}$ | – | 1.6 | – | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 3.0 Vdc, $I_D$ = 10 mAdc, $V_{GS}$ = 0 to 2.5 Vdc) | $t_{on}$ | – | 0.14 | – | μs |
| Turn–Off Delay Time | | $t_{off}$ | – | 0.14 | – | |

# 2N7000

Preferred Device

# Small Signal MOSFET 200 mAmps, 60 Volts

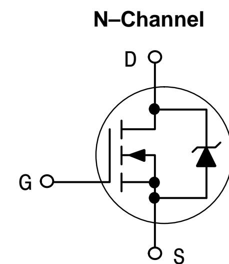
## N–Channel TO–92

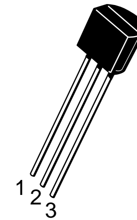
ON Semiconductor

http://onsemi.com

**200 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 5 Ω**

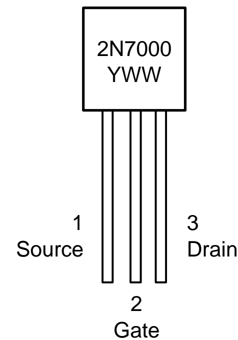
N–Channel




TO–92
CASE 29
Style 22

MARKING DIAGRAM & PIN ASSIGNMENT




Y = Year
WW = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le 50$ μs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Pulsed | <br>$I_D$<br>$I_{DM}$ | <br>200<br>500 | mAdc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 350<br>2.8 | mW<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 357 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds | $T_L$ | 300 | °C |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 266 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 µAdc) | | $V_{(BR)DSS}$ | 60 | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0) | | $I_{DSS}$ | – | 1.0 | µAdc |
| ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0, $T_J$ = 125°C) | | | – | 1.0 | mAdc |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | – | –10 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 0.8 | 3.0 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 0.5 Adc) | | $r_{DS(on)}$ | – | 5.0 | Ohm |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 75 mAdc) | | | – | 6.0 | |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 0.5 Adc) | | $V_{DS(on)}$ | – | 2.5 | Vdc |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 75 mAdc) | | | – | 0.45 | |
| On–State Drain Current ($V_{GS}$ = 4.5 Vdc, $V_{DS}$ = 10 Vdc) | | $I_{d(on)}$ | 75 | – | mAdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | $g_{fs}$ | 100 | – | µmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 60 | pF |
| Output Capacitance | | $C_{oss}$ | – | 25 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 5.0 | |
| **SWITCHING CHARACTERISTICS** (Note 1.) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 V, $I_D$ = 500 mA, $R_G$ = 25 Ω, $R_L$ = 30 Ω, $V_{gen}$ = 10 V) | $t_{on}$ | – | 10 | ns |
| Turn–Off Delay Time | | $t_{off}$ | – | 10 | |

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

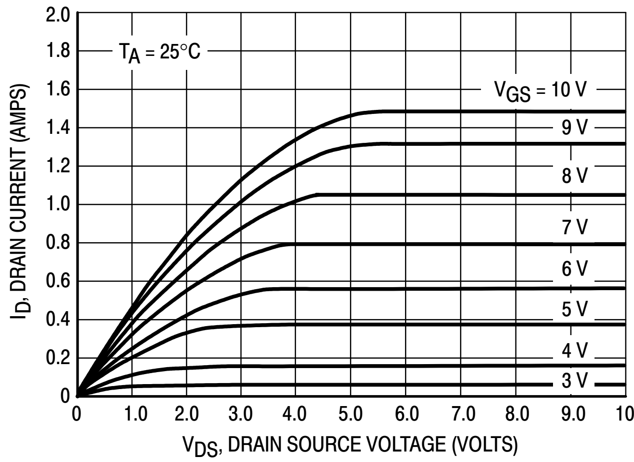



**Figure 1. Ohmic Region**

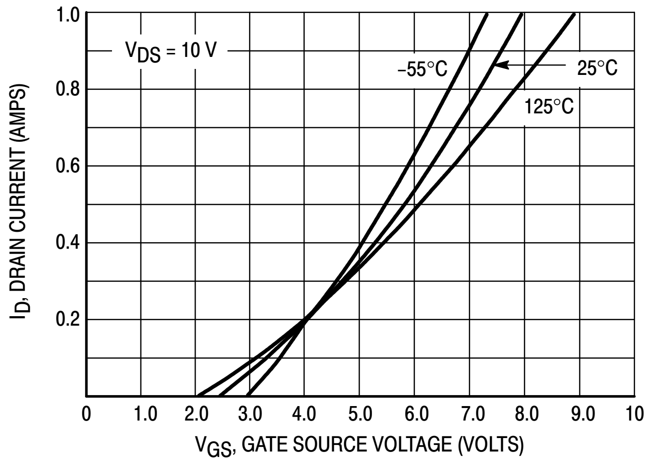



**Figure 2. Transfer Characteristics**

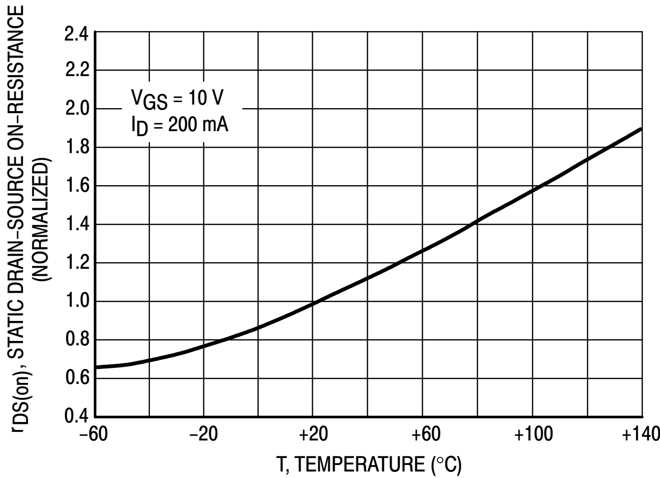



**Figure 3. Temperature versus Static Drain–Source On–Resistance**

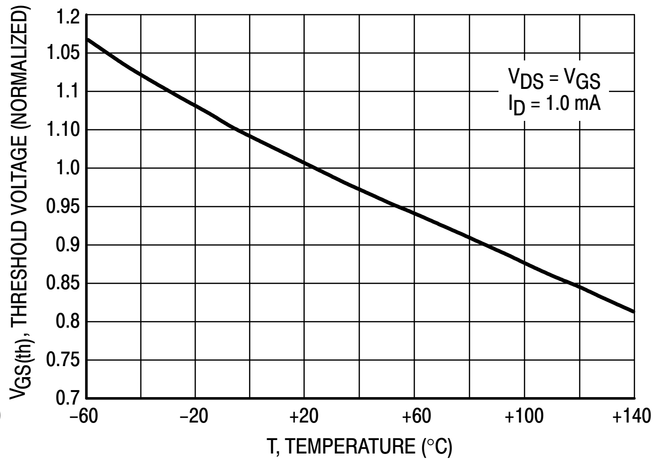



**Figure 4. Temperature versus Gate Threshold Voltage**

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| 2N7000 | TO–92 | 1000 Unit/Box |
| 2N7000RLRA | TO–92 | 2000 Tape & Reel |
| 2N7000RLRM | TO–92 | 2000 Ammo Pack |
| 2N7000RLRP | TO–92 | 2000 Ammo Pack |
| 2N7000ZL1 | TO–92 | 2000 Ammo Pack |

# 2N7002LT1

**Preferred Device**

# Small Signal MOSFET 115 mAmps, 60 Volts

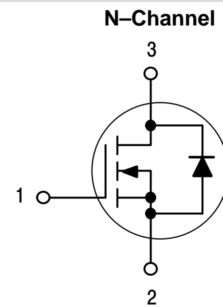
## N–Channel SOT–23

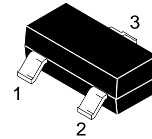
**ON Semiconductor™**

**http://onsemi.com**

**115 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 7.5 Ω**

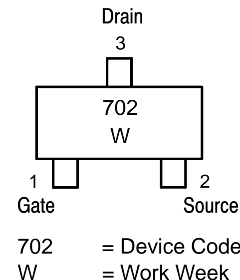
**N–Channel**




**SOT–23**
**CASE 318**
**STYLE 21**

**MARKING DIAGRAM & PIN ASSIGNMENT**




702 = Device Code
W = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Drain Current<br>– Continuous $T_C$ = 25°C (Note 1.)<br>$T_C$ = 100°C (Note 1.)<br>– Pulsed (Note 2.) | $I_D$<br>$I_D$<br>$I_{DM}$ | ±115<br>±75<br>±800 | mAdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p$ ≤ 50 μs) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR–5 Board (Note 3.) $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 225<br>1.8 | mW<br>mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Total Device Dissipation Alumina Substrate,(Note 4.) $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 300<br>2.4 | mW<br>mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 417 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. FR–5 = 1.0 x 0.75 x 0.062 in.
4. Alumina = 0.4 x 0.3 x 0.025 in 99.5% alumina.

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| 2N7002LT1 | SOT–23 | 3000 Tape & Reel |
| 2N7002LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 μAdc) | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0, $V_{DS}$ = 60 Vdc) $T_J$ = 25°C<br>$T_J$ = 125°C | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>500 | μAdc |
| Gate–Body Leakage Current, Forward ($V_{GS}$ = 20 Vdc) | $I_{GSSF}$ | – | – | 100 | nAdc |
| Gate–Body Leakage Current, Reverse ($V_{GS}$ = –20 Vdc) | $I_{GSSR}$ | – | – | –100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | $V_{GS(th)}$ | 1.0 | – | 2.5 | Vdc |
| On–State Drain Current ($V_{DS} \geq 2.0\ V_{DS(on)}$, $V_{GS}$ = 10 Vdc) | $I_{D(on)}$ | 500 | – | – | mA |
| Static Drain–Source On–State Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 500 mAdc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 50 mAdc) | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>3.75<br>0.375 | Vdc |
| Static Drain–Source On–State Resistance<br>($V_{GS}$ = 10 V, $I_D$ = 500 mAdc) $T_C$ = 25°C<br>$T_C$ = 125°C<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 50 mAdc) $T_C$ = 25°C<br>$T_C$ = 125°C | $r_{DS(on)}$ | <br>–<br>–<br>–<br>– | <br>–<br>–<br>–<br>– | <br>7.5<br>13.5<br>7.5<br>13.5 | Ohms |
| Forward Transconductance ($V_{DS} \geq 2.0\ V_{DS(on)}$, $I_D$ = 200 mAdc) | $g_{FS}$ | 80 | – | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | – | 50 | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | – | – | 25 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | – | – | 5.0 | pF |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | |
| Turn–On Delay Time ($V_{DD}$ = 25 Vdc, $I_D \cong$ 500 mAdc, $R_G$ = 25 Ω, $R_L$ = 50 Ω, $V_{gen}$ = 10 V) | $t_{d(on)}$ | – | – | 20 | ns |
| Turn–Off Delay Time ($V_{DD}$ = 25 Vdc, $I_D \cong$ 500 mAdc, $R_G$ = 25 Ω, $R_L$ = 50 Ω, $V_{gen}$ = 10 V) | $t_{d(off)}$ | – | – | 40 | ns |
| **BODY–DRAIN DIODE RATINGS** | | | | | |
| Diode Forward On–Voltage ($I_S$ = 11.5 mAdc, $V_{GS}$ = 0 V) | $V_{SD}$ | – | – | –1.5 | Vdc |
| Source Current Continuous (Body Diode) | $I_S$ | – | – | –115 | mAdc |
| Source Current Pulsed | $I_{SM}$ | – | – | –800 | mAdc |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

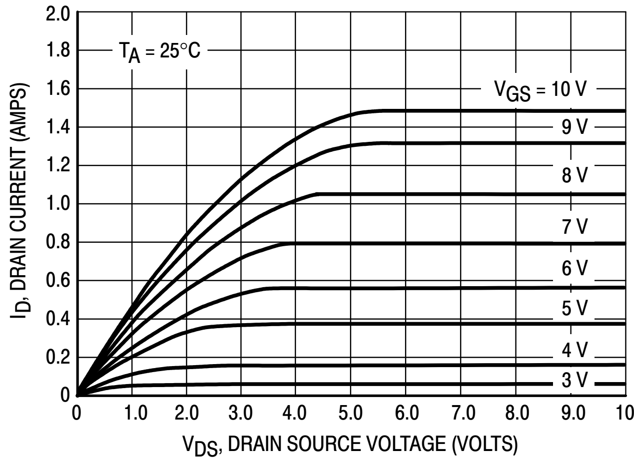



**Figure 1. Ohmic Region**

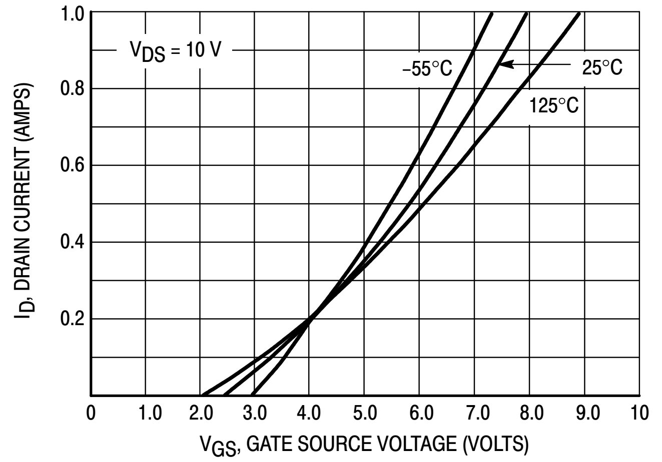



**Figure 2. Transfer Characteristics**

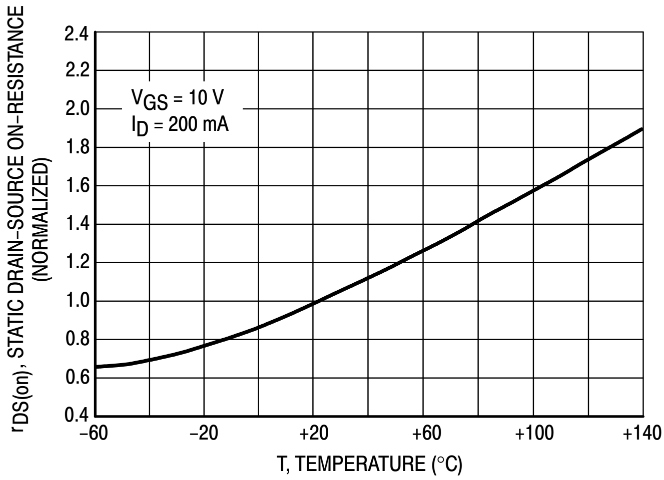



**Figure 3. Temperature versus Static Drain–Source On–Resistance**

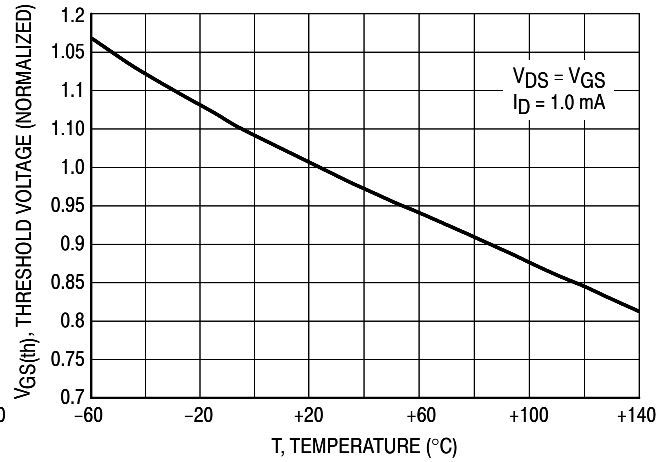
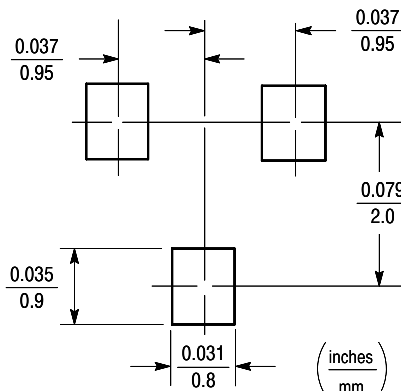



**Figure 4. Temperature versus Gate Threshold Voltage**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# BS107, BS107A

**Preferred Device**

# Small Signal MOSFET 250 mAmps, 200 Volts

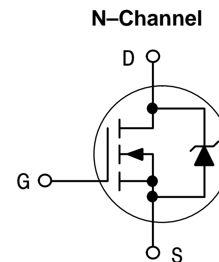
## N–Channel TO–92

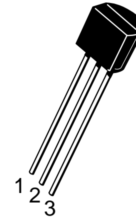
**ON Semiconductor**

**http://onsemi.com**

**250 mAMPS**
**200 VOLTS**
**$R_{DS(on)}$ = 14 Ω (BS107)**
**$R_{DS(on)}$ = 6.4 Ω (BS107A)**

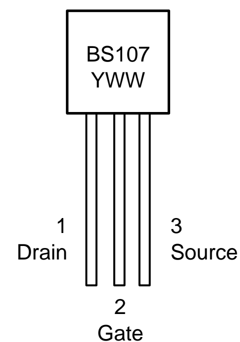
**N–Channel**




**TO–92**
**CASE 29**
**Style 30**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 274 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq 50\ \mu s$) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±30 | <br>Vdc<br>Vpk |
| Drain Current<br>Continuous (Note 1.)<br>Pulsed (Note 2.) | <br>$I_D$<br>$I_{DM}$ | <br>250<br>500 | mAdc |
| Total Device Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 350 | mW |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Zero–Gate–Voltage Drain Current ($V_{DS}$ = 130 Vdc, $V_{GS}$ = 0) | $I_{DSS}$ | – | – | 30 | nAdc |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 µAdc) | $V_{(BR)DSX}$ | 200 | – | – | Vdc |
| Gate Reverse Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | – | 0.01 | 10 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | |
| Gate Threshold Voltage ($I_D$ = 1.0 mAdc, $V_{DS}$ = $V_{GS}$) | $V_{GS(Th)}$ | 1.0 | – | 3.0 | Vdc |
| Static Drain–Source On Resistance | $r_{DS(on)}$ | | | | Ohms |
| BS107 ($V_{GS}$ = 2.6 Vdc, $I_D$ = 20 mAdc) | | – | – | 28 | |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | – | – | 14 | |
| BS107A ($V_{GS}$ = 10 Vdc) | | | | | |
| ($I_D$ = 100 mAdc) | | – | 4.5 | 6.0 | |
| ($I_D$ = 250 mAdc) | | – | 4.8 | 6.4 | |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 60 | – | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | – | 6.0 | – | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | – | 30 | – | pF |
| Forward Transconductance ($V_{DS}$ = 25 Vdc, $I_D$ = 250 mAdc) | $g_{fs}$ | 200 | 400 | – | mmhos |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Turn–On Time | $t_{on}$ | – | 6.0 | 15 | ns |
| Turn–Off Time | $t_{off}$ | – | 12 | 15 | ns |

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

## RESISTIVE SWITCHING

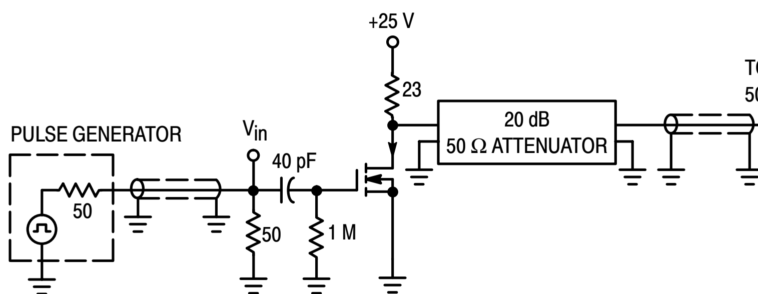



**Figure 1. Switching Test Circuit**

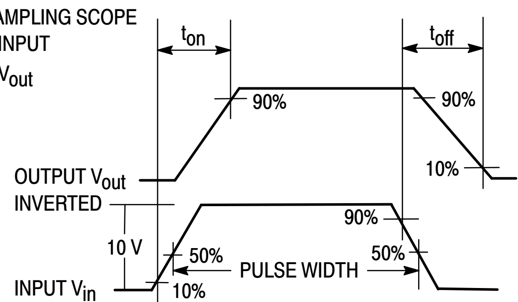



**Figure 2. Switching Waveforms**

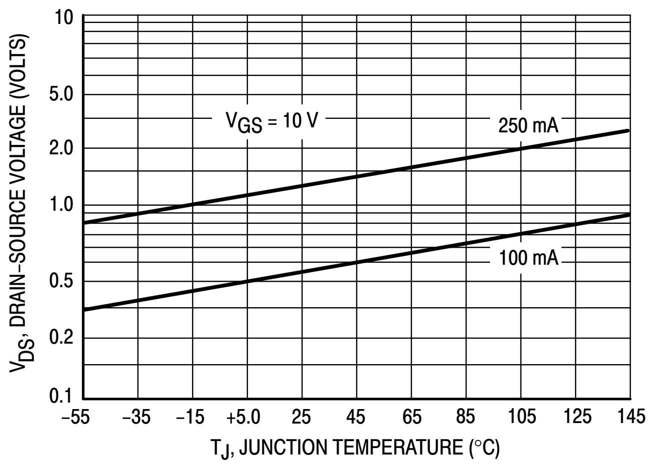



**Figure 3. On Voltage versus Temperature**

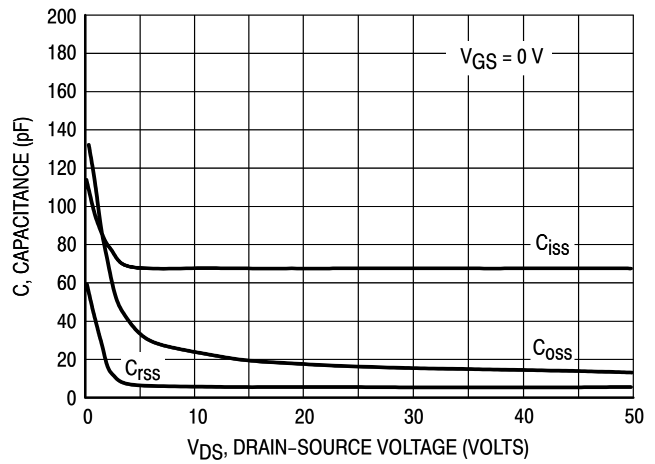



**Figure 4. Capacitance Variation**

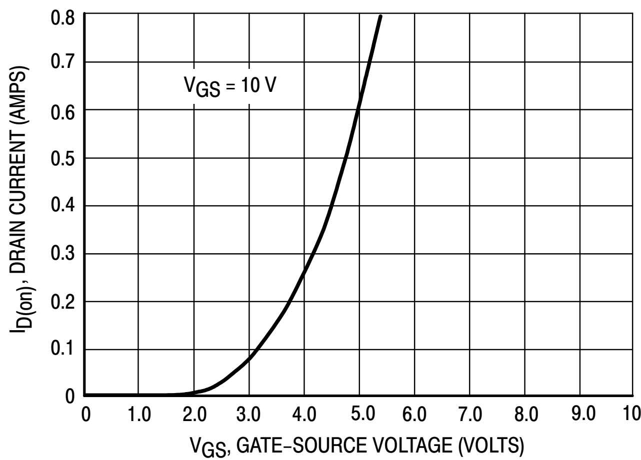



**Figure 5. Transfer Characteristic**

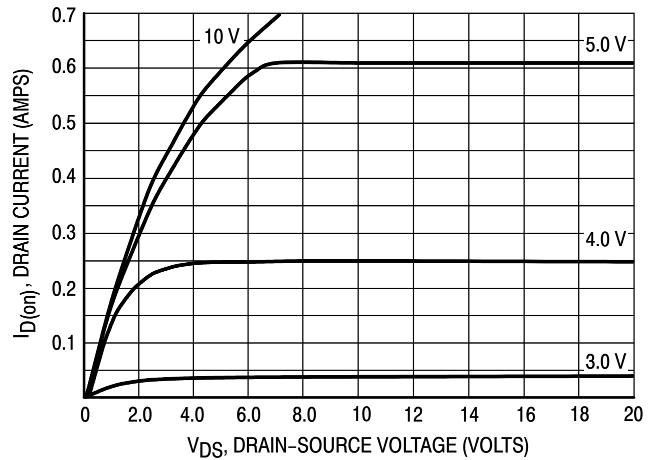



**Figure 6. Output Characteristic**

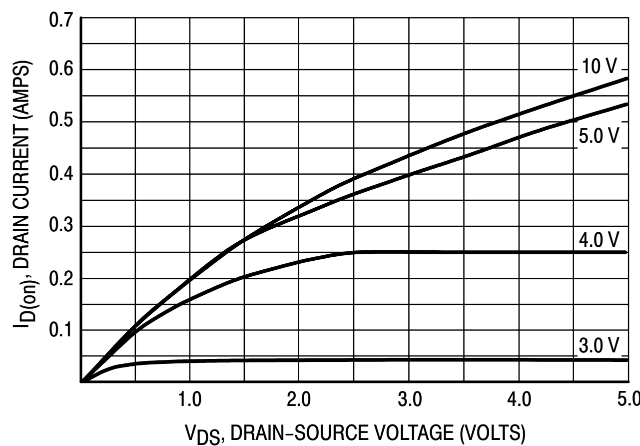



**Figure 7. Saturation Characteristic**

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| BS107 | TO–92 | 1000 Unit/Box |
| BS107RLRA | TO–92 | 2000 Tape & Reel |
| BS107RL1 | TO–92 | 2000 Tape & Reel |
| BS107A | TO–92 | 1000 Units/Box |
| BS107ARLRM | TO–92 | 2000 Ammo Pack |
| BS107ARLRP | TO–92 | 2000 Ammo Pack |
| BS107ARL1 | TO–92 | 2000 Tape & Reel |

# BS108

Preferred Device

# Small Signal MOSFET 250 mAmps, 200 Volts, Logic Level

## N–Channel TO–92

This MOSFET is designed for high voltage, high speed switching applications such as line drivers, relay drivers, CMOS logic, microprocessor or TTL to high voltage interface and high voltage display drivers.

- Low Drive Requirement, $V_{GS}$ = 3.0 V max
- Inherent Current Sharing Capability Permits Easy Paralleling of many Devices

**MAXIMUM RATINGS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | ±20 | Vdc |
| Drain Current<br>Continuous (Note 1.)<br>Pulsed (Note 2.) | <br>$I_D$<br>$I_{DM}$ | <br>250<br>500 | mAdc |
| Total Power Dissipation<br>@ $T_A$ = 25°C<br>Derate above $T_A$ = 25°C | $P_D$ | <br>350<br>6.4 | <br>mW<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

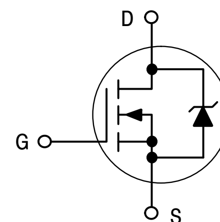
1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

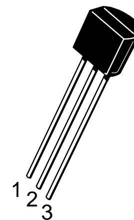
ON Semiconductor

http://onsemi.com

**250 mAMPS**
**200 VOLTS**
**$R_{DS(on)}$ = 8 Ω**

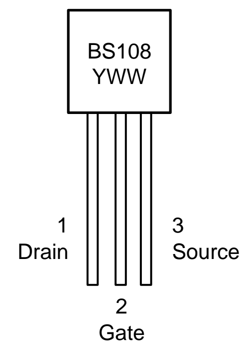
**N–Channel**




**TO–92**
**CASE 29**
**Style 30**

**MARKING DIAGRAM & PIN ASSIGNMENT**




BS108 = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| BS108 | TO–92 | 1000 Units/Box |
| BS108ZL1 | TO–92 | 2000 Ammo Pack |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 μA) | $V_{(BR)DS}$ | 200 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DSS}$ = 130 Vdc, $V_{GS}$ = 0) | $I_{DSS}$ | – | – | 30 | nAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | $I_{GSSF}$ | – | – | 10 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | |
| Gate Threshold Voltage ($I_D$ = 1.0 mA, $V_{DS}$ = $V_{GS}$) | $V_{GS(th)}$ | 0.5 | – | 1.5 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 2.0 Vdc, $I_D$ = 50 mA) ($V_{GS}$ = 2.8 Vdc, $I_D$ = 100 mA) | $r_{DS(on)}$ | –<br>– | –<br>– | 10<br>8.0 | Ohms |
| Drain Cutoff Current ($V_{GS}$ = 0.2 V, $V_{DS}$ = 70 V) | $I_{DSX}$ | – | – | 25 | μA |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | – | 150 | pF |
| Output Capacitance ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | – | – | 30 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | – | – | 10 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Turn–On Time (See Figure 1) | $t_{d(on)}$ | – | – | 15 | ns |
| Turn–Off Time (See Figure 1) | $t_{d(off)}$ | – | – | 15 | ns |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle = 2.0%.

## RESISTIVE SWITCHING

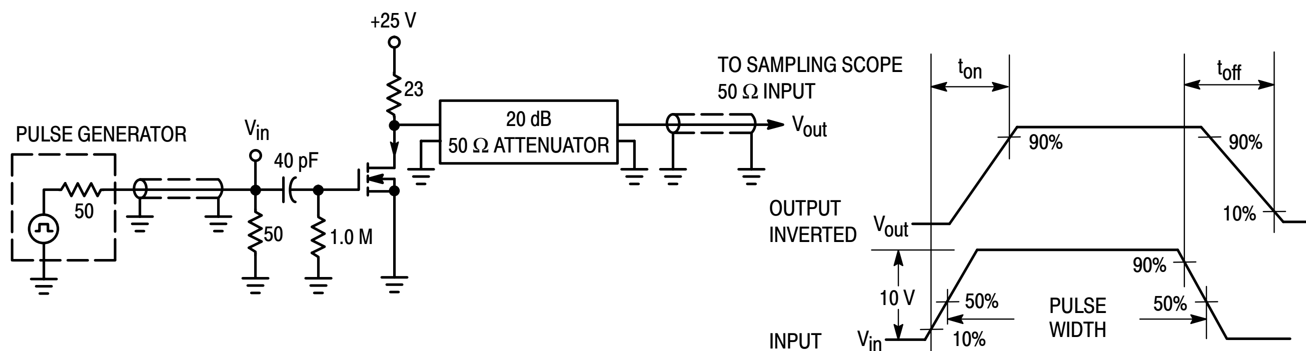



Figure 1. Switching Test Circuit

Figure 2. Switching Waveforms

# BS170

Preferred Device

# Small Signal MOSFET 500 mAmps, 60 Volts

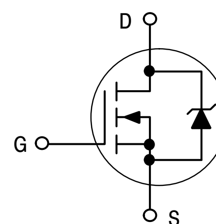
## N–Channel TO–92

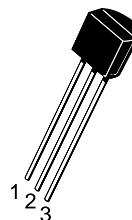
ON Semiconductor

http://onsemi.com

**500 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 5 Ω**

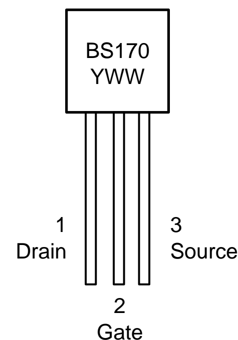
**N–Channel**




**TO–92**
**CASE 29**
**Style 30**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 278 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p$ ≤ 50 μs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current (Note 1.) | $I_D$ | 0.5 | Adc |
| Total Device Dissipation @ $T_A$ = 25°C | $P_D$ | 350 | mW |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. The Power Dissipation of the package may result in a lower continuous drain current.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Gate Reverse Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | – | 0.01 | 10 | nAdc |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 μAdc) | $V_{(BR)DSS}$ | 60 | 90 | – | Vdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | $V_{GS(Th)}$ | 0.8 | 2.0 | 3.0 | Vdc |
| Static Drain–Source On Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mAdc) | $r_{DS(on)}$ | – | 1.8 | 5.0 | Ω |
| Drain Cutoff Current ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc) | $I_{D(off)}$ | – | – | 0.5 | μA |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 250 mAdc) | $g_{fs}$ | – | 200 | – | mmhos |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | – | 60 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Turn–On Time ($I_D$ = 0.2 Adc) See Figure 1 | $t_{on}$ | – | 4.0 | 10 | ns |
| Turn–Off Time ($I_D$ = 0.2 Adc) See Figure 1 | $t_{off}$ | – | 4.0 | 10 | ns |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| BS170 | TO–92 | 1000 Unit/Box |
| BS170RLRA | TO–92 | 2000 Tape & Reel |
| BS170RLRM | TO–92 | 2000 Ammo Pack |
| BS170RLRP | TO–92 | 2000 Ammo Pack |
| BS170RL1 | TO–92 | 2000 Tape & Reel |
| BS170ZL1 | TO–92 | 2000 Ammo Pack |

## RESISTIVE SWITCHING

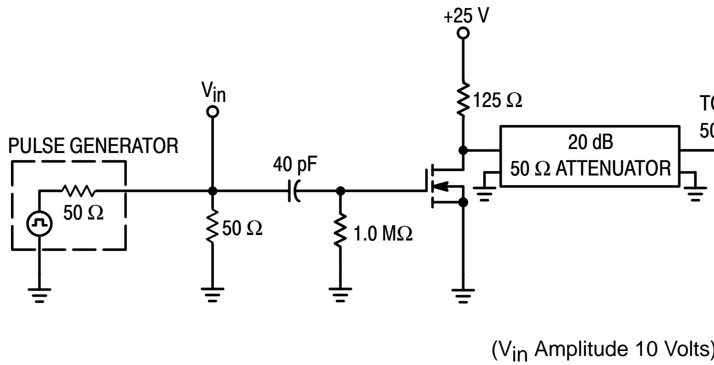



Figure 1. Switching Test Circuit

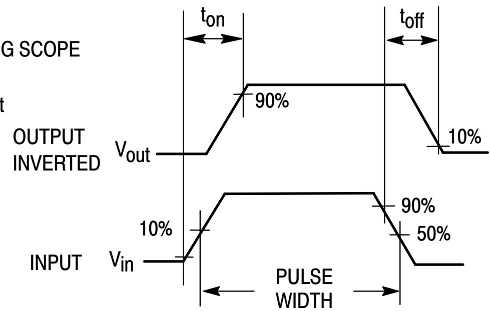



Figure 2. Switching Waveforms

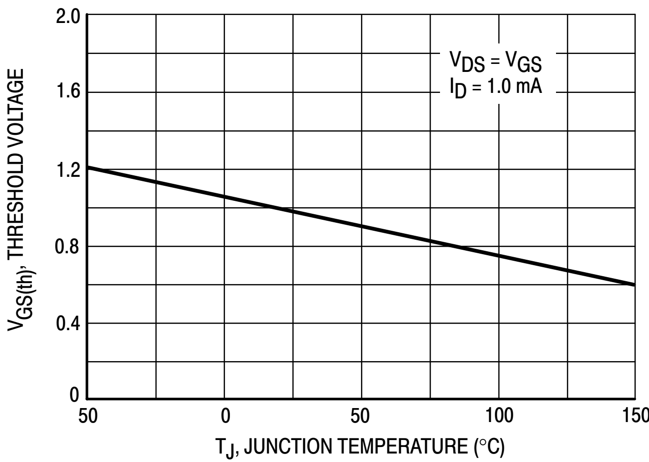



Figure 3. $V_{GS(th)}$ Normalized versus Temperature

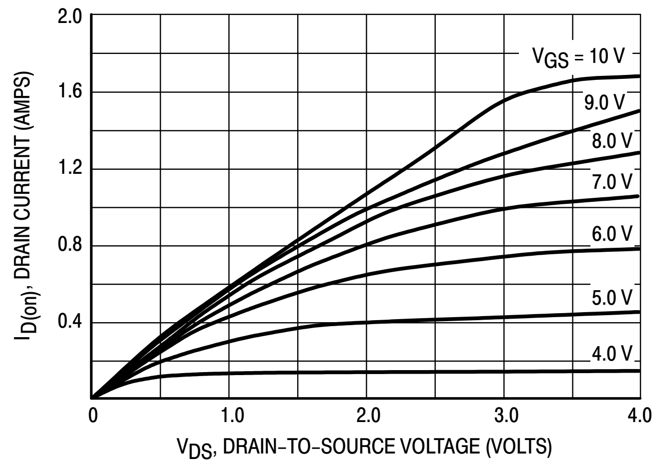



Figure 4. On–Region Characteristics

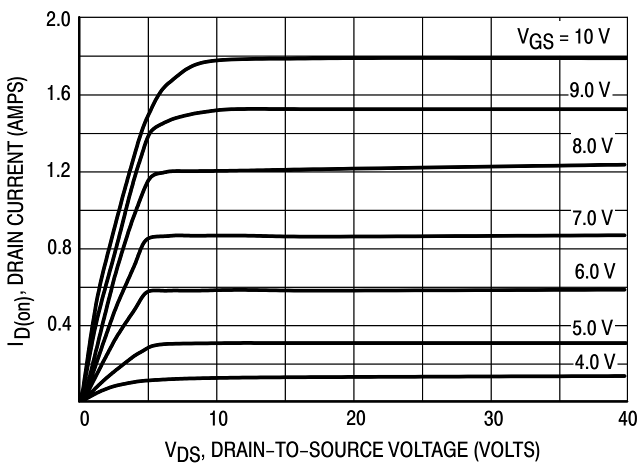



Figure 5. Output Characteristics

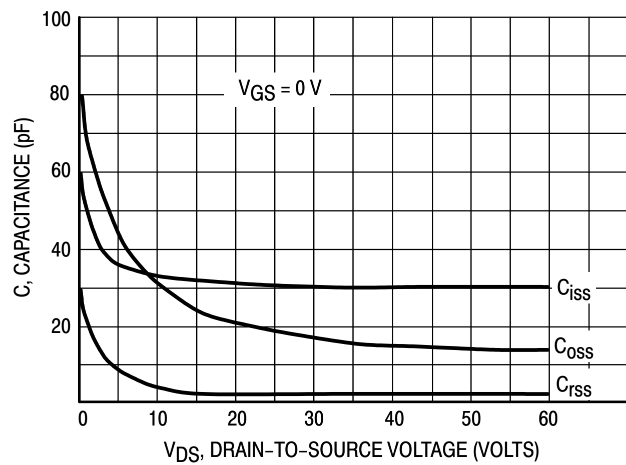



Figure 6. Capacitance versus Drain–To–Source Voltage

# BSS123LT1

**Preferred Device**

# Power MOSFET 170 mAmps, 100 Volts

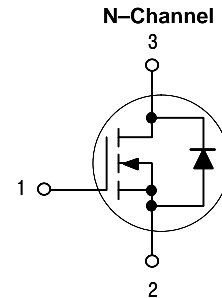
## N–Channel SOT–23

**ON Semiconductor™**

http://onsemi.com

**170 mAMPS**
**100 VOLTS**
**$R_{DS(on)}$ = 6 Ω**

**N–Channel**




### MAXIMUM RATINGS

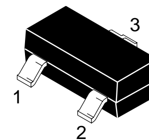
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq 50$ µs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current<br>Continuous (Note 1.)<br>Pulsed (Note 2.) | <br>$I_D$<br>$I_{DM}$ | <br>0.17<br>0.68 | Adc |

### THERMAL CHARACTERISTICS

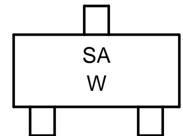
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR–5 Board (Note 3.)<br>$T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 225<br><br>1.8 | mW<br><br>mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
3. FR–5 = 1.0 × 0.75 × 0.062 in.

**MARKING DIAGRAM**

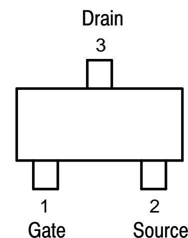



**SOT–23**
**CASE 318**
**STYLE 21**




SA = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| BSS123LT1 | SOT–23 | 3000 Tape & Reel |
| BSS123LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 100 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{GS}$ = 0, $V_{DS}$ = 100 Vdc) | | $I_{DSS}$ | | | | μAdc |
| | $T_J$ = 25°C | | – | – | 15 | |
| | $T_J$ = 125°C | | – | – | 60 | |
| Gate–Body Leakage Current ($V_{GS}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 50 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 0.8 | – | 2.8 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 100 mAdc) | | $r_{DS(on)}$ | – | 5.0 | 6.0 | Ω |
| Forward Transconductance ($V_{DS}$ = 25 Vdc, $I_D$ = 100 mAdc) | | $g_{fs}$ | 80 | – | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{iss}$ | – | 20 | – | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{oss}$ | – | 9.0 | – | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{rss}$ | – | 4.0 | – | pF |
| **SWITCHING CHARACTERISTICS**(4) | | | | | | |
| Turn–On Delay Time | ($V_{CC}$ = 30 Vdc, $I_C$ = 0.28 Adc, $V_{GS}$ = 10 Vdc, $R_{GS}$ = 50 Ω) | $t_{d(on)}$ | – | 20 | – | ns |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 40 | – | ns |
| **REVERSE DIODE** | | | | | | |
| Diode Forward On–Voltage ($I_D$ = 0.34 Adc, $V_{GS}$ = 0 Vdc) | | $V_{SD}$ | – | – | 1.3 | V |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

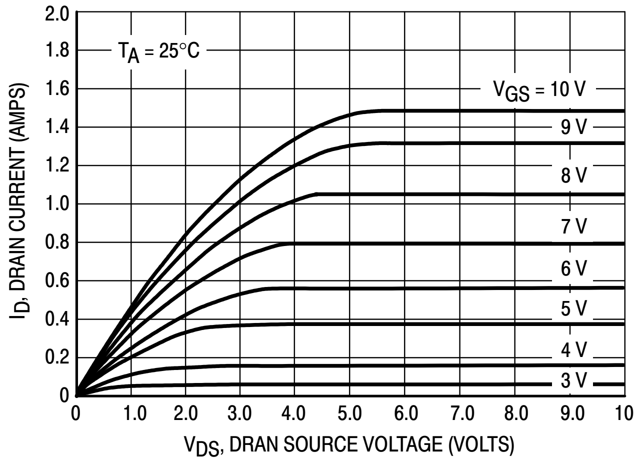



**Figure 1. Ohmic Region**

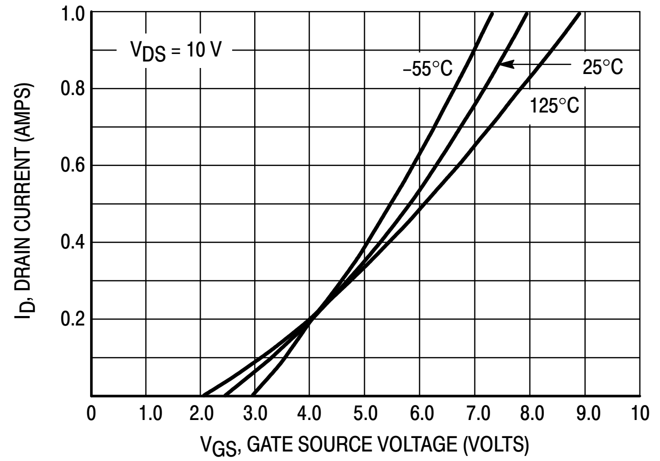



**Figure 2. Transfer Characteristics**

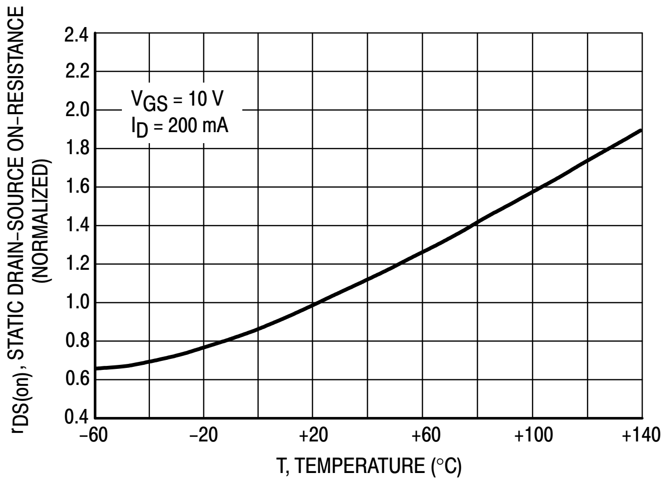



**Figure 3. Temperature versus Static Drain–Source On–Resistance**

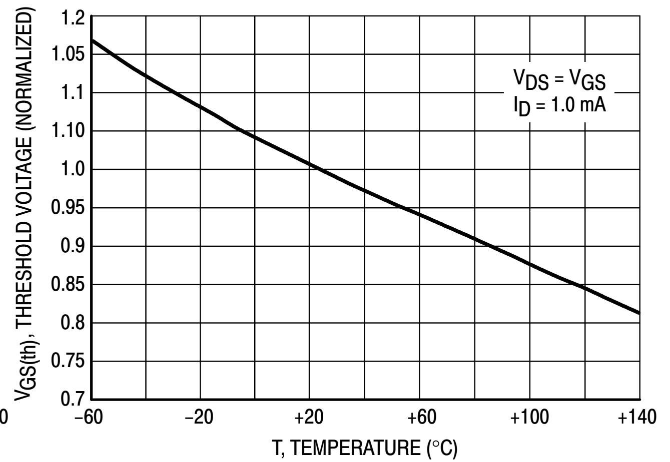
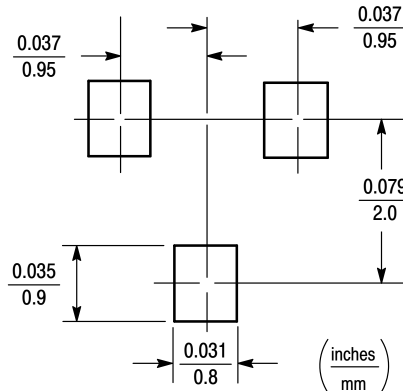



**Figure 4. Temperature versus Gate Threshold Voltage**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




**SOT–23**

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# BSS138LT1

Preferred Device

# Power MOSFET 200 mAmps, 50 Volts

## N–Channel SOT–23

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Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

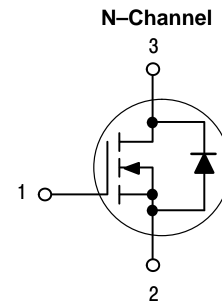
- Low Threshold Voltage ($V_{GS(th)}$: 0.5V...1.5V) makes it ideal for low voltage applications
- Miniature SOT–23 Surface Mount Package saves board space

**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

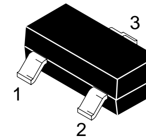
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 50 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \leq 10\ \mu s$) | <br>$I_D$<br>$I_{DM}$ | <br>200<br>800 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 225 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

**200 mAMPS**
**50 VOLTS**
**$R_{DS(on)}$ = 3.5 Ω**

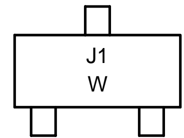
**N–Channel**




**MARKING DIAGRAM**

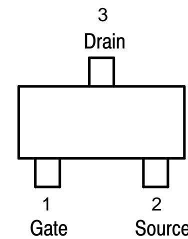



**SOT–23**
**CASE 318**
**STYLE 21**




J1 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| BSS138LT1 | SOT–23 | 3000 Tape & Reel |
| BSS138LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 50 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 0.1 | |
| ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 0.5 | |
| Gate–Source Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±0.1 | μAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate–Source Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 0.5 | – | 1.5 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 2.75 Vdc, $I_D$ < 200 mAdc, $T_A$ = –40°C to +85°C) | | | – | 5.6 | 10 | |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 200 mAdc) | | | – | – | 3.5 | |
| Forward Transconductance ($V_{DS}$ = 25 Vdc, $I_D$ = 200 mAdc, f = 1.0 kHz) | | $g_{fs}$ | 100 | – | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{iss}$ | – | 40 | 50 | pF |
| Output Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{oss}$ | – | 12 | 25 | |
| Transfer Capacitance | ($V_{DG}$ = 25 Vdc, $V_{GS}$ = 0, f = 1 MHz) | $C_{rss}$ | – | 3.5 | 5.0 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 0.2 Adc,) | $t_{d(on)}$ | – | – | 20 | ns |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | – | 20 | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

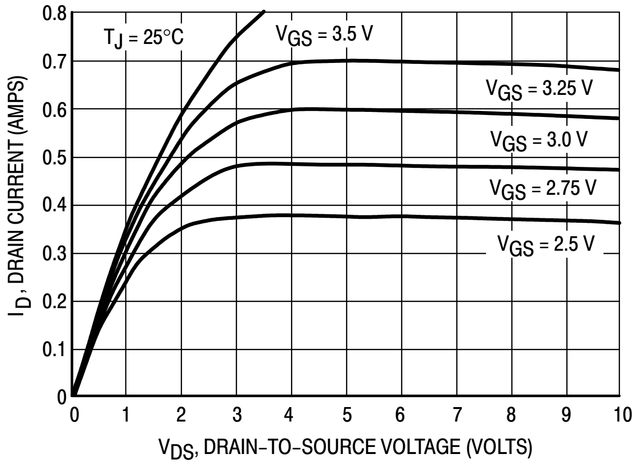



**Figure 1. On–Region Characteristics**

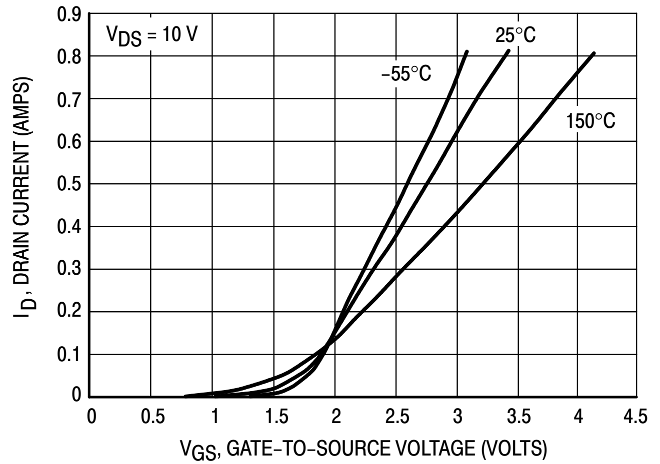



**Figure 2. Transfer Characteristics**

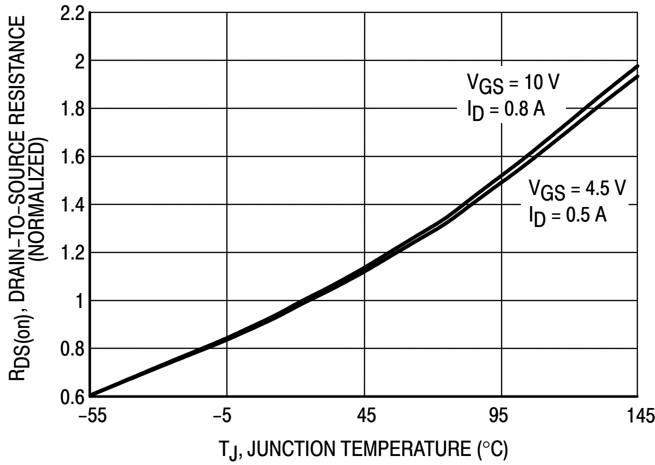



**Figure 3. On–Resistance Variation with Temperature**

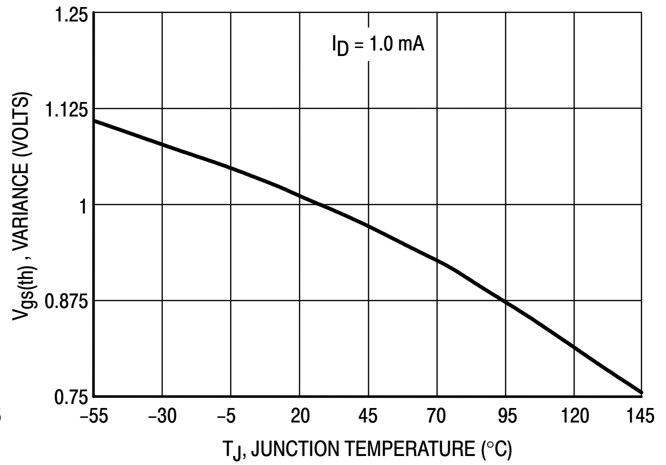



**Figure 4. Threshold Voltage Variation with Temperature**

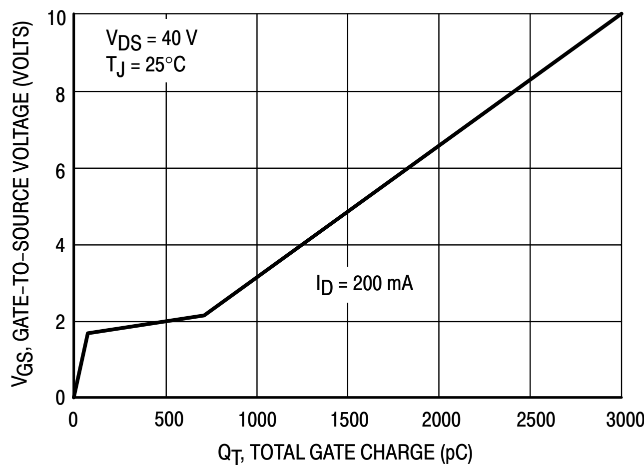



**Figure 5. Gate Charge**

## TYPICAL ELECTRICAL CHARACTERISTICS

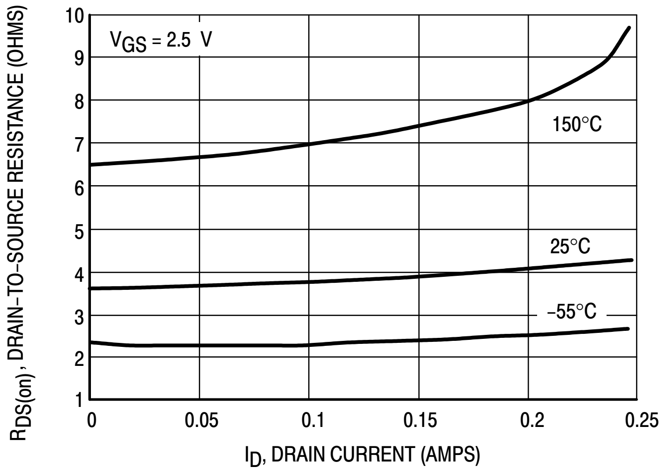



**Figure 6. On−Resistance versus Drain Current**

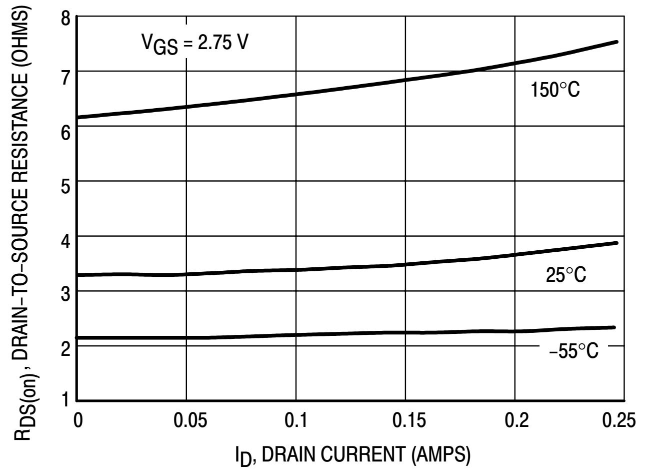



**Figure 7. On−Resistance versus Drain Current**

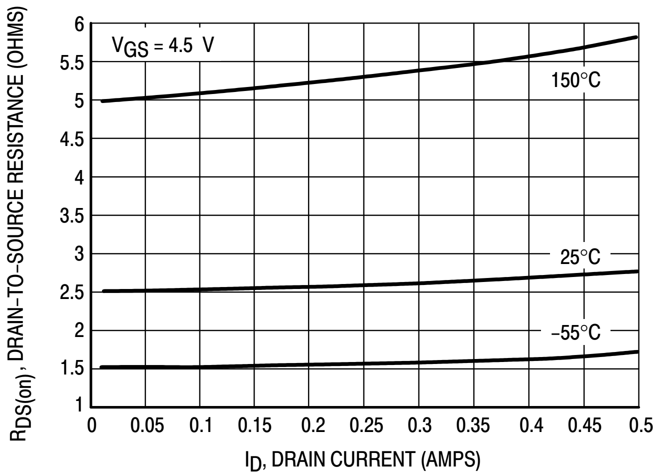



**Figure 8. On−Resistance versus Drain Current**

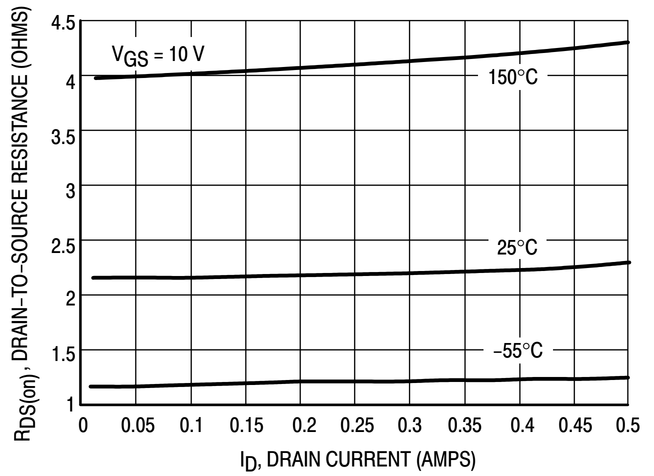



**Figure 9. On−Resistance versus Drain Current**

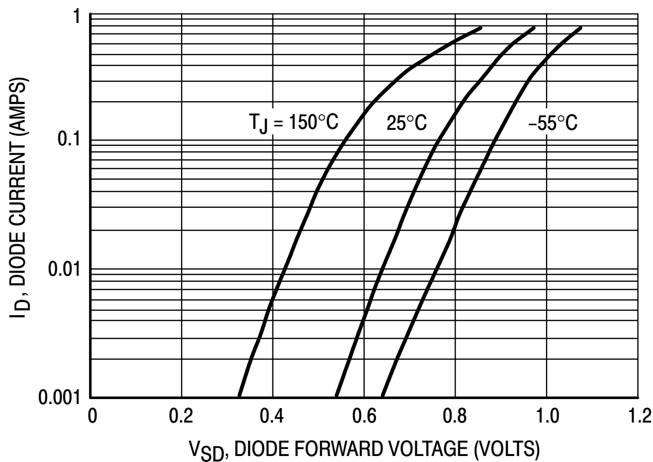



**Figure 10. Body Diode Forward Voltage**

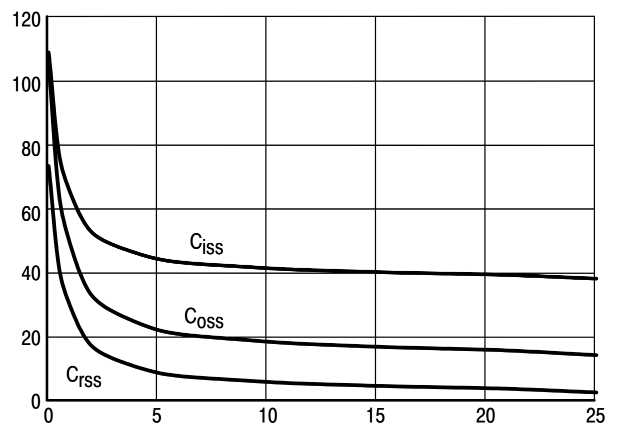
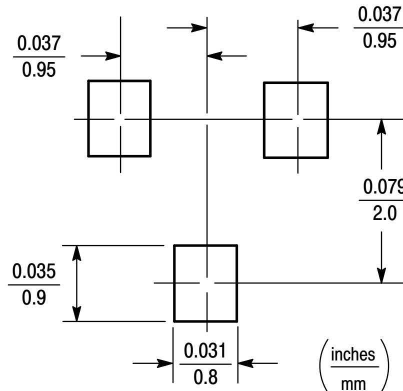



**Figure 11. Capacitance**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# BSS84LT1

**Preferred Device**

# Power MOSFET 130 mAmps, 50 Volts

## P–Channel SOT–23

These miniature surface mount MOSFETs reduce power loss conserve energy, making this device ideal for use in small power management circuitry. Typical applications are dc–dc converters, load switching, power management in portable and battery–powered products such as computers, printers, cellular and cordless telephones.

- Energy Efficient
- Miniature SOT–23 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 50 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_{DM}$ | <br>130<br>520 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 225 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

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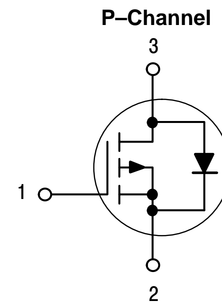
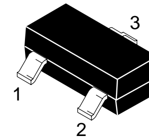
**130 mAMPS**
**50 VOLTS**
**$R_{DS(on)}$ = 10 Ω**

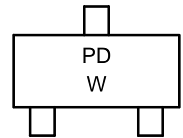
**P–Channel**




**MARKING DIAGRAM**

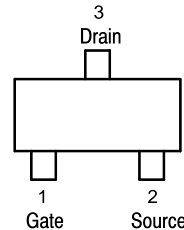



**SOT–23**
**CASE 318**
**STYLE 21**




PD = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| BSS84LT1 | SOT–23 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | $V_{(BR)DSS}$ | 50 | – | – | Vdc |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc) | | – | – | 0.1 | |
| ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | | – | – | 15 | |
| ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | – | 60 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | ±60 | μAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate–Source Threaded Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | $V_{GS(th)}$ | 0.8 | – | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 100 mAdc) | $r_{DS(on)}$ | – | 5.0 | 10 | Ohms |
| Transfer Admittance ($V_{DS}$ = 25 Vdc, $I_D$ = 100 mAdc, f = 1.0 kHz) | $\|y_{fs}\|$ | 50 | – | – | mS |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{iss}$ | – | 30 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{oss}$ | – | 10 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc) | $C_{rss}$ | – | 5.0 | – | |

**SWITCHING CHARACTERISTICS** (Note 2.)

| Characteristic | Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | ($V_{DD}$ = –15 Vdc, $I_D$ = –2.5 Adc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge | | $Q_T$ | – | 6000 | – | pC |

**SOURCE–DRAIN DIODE CHARACTERISTICS**

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Continuous Current | $I_S$ | – | – | 0.130 | A |
| Pulsed Current | $I_{SM}$ | – | – | 0.520 | |
| Forward Voltage (Note 2.) | $V_{SD}$ | – | 2.5 | – | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

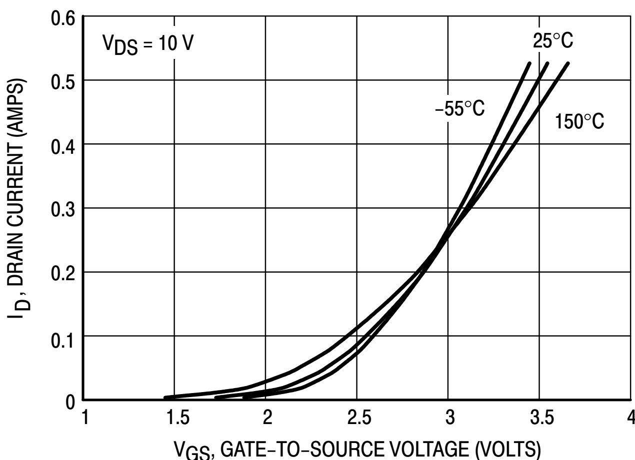



**Figure 1. Transfer Characteristics**

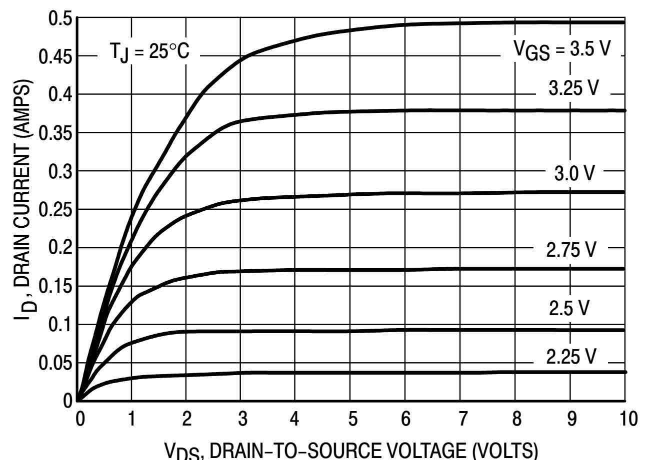



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

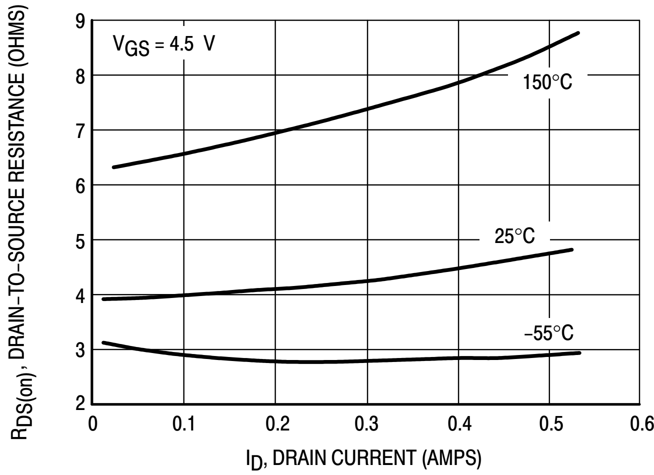



**Figure 3. On−Resistance versus Drain Current**

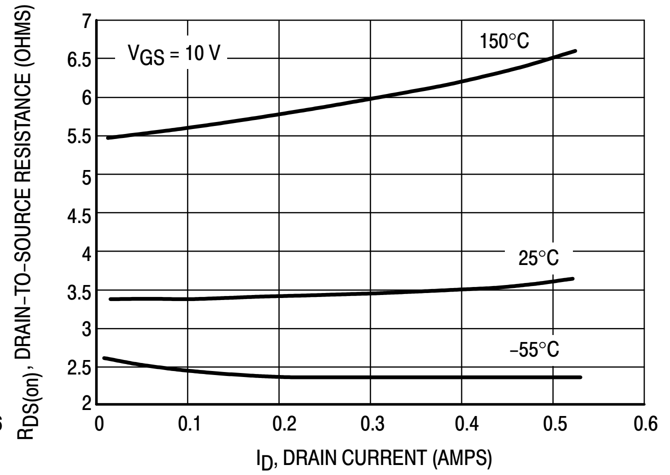



**Figure 4. On−Resistance versus Drain Current**

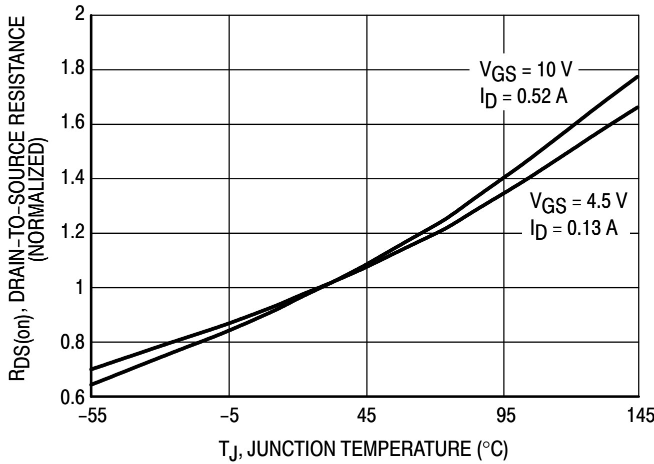



**Figure 5. On−Resistance Variation with Temperature**

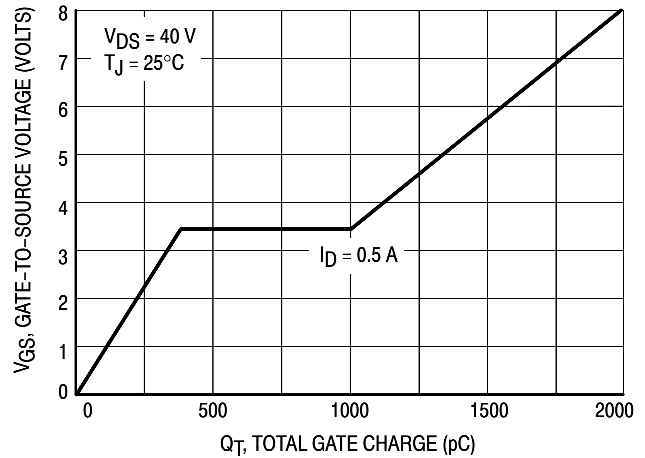



**Figure 6. Gate Charge**

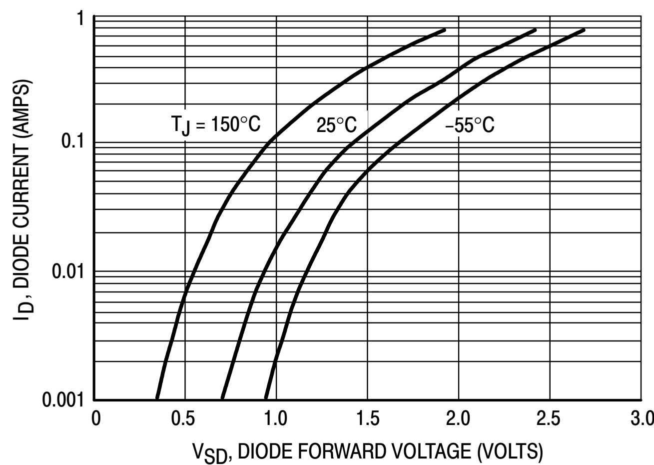
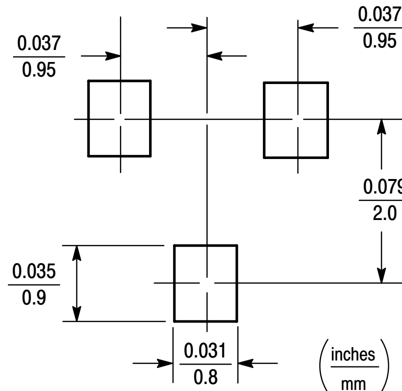



**Figure 7. Body Diode Forward Voltage**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGP15N35CL, MGB15N35CL

**Preferred Device**

# Ignition IGBT 15 Amps, 350 Volts

## N–Channel TO–220 and D2PAK

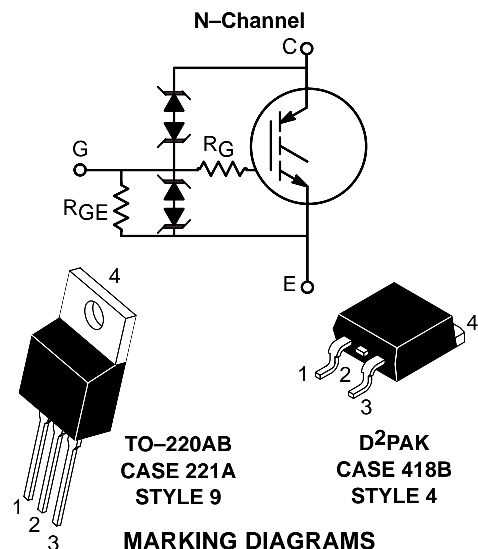
**ON Semiconductor**™

**http://onsemi.com**

**15 AMPERES**
**350 VOLTS (Clamped)**
**$V_{CE(on)}$ @ 10 A = 1.8 V Max**

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

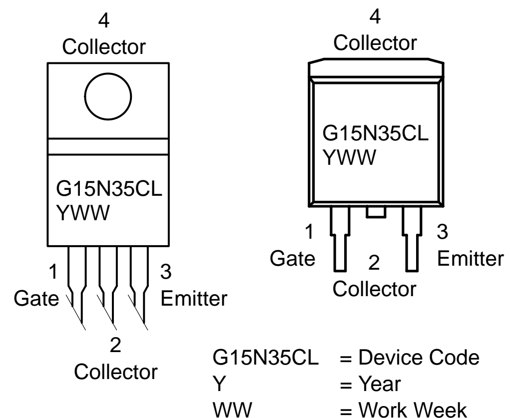
- Ideal for Coil–On–Plug, IGBT–On–Coil, or Distributorless Ignition System Applications
- High Pulsed Current Capability up to 50 A
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- Optional Gate Resistor ($R_G$)




**TO–220AB CASE 221A STYLE 9**

**D2PAK CASE 418B STYLE 4**

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




G15N35CL = Device Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** (–55°C ≤ $T_J$ ≤ 175°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CES}$ | 380 | $V_{DC}$ |
| Collector–Gate Voltage | $V_{CER}$ | 380 | $V_{DC}$ |
| Gate–Emitter Voltage | $V_{GE}$ | 22 | $V_{DC}$ |
| Collector Current–Continuous @ $T_C$ = 25°C – Pulsed | $I_C$ | 15<br>50 | $A_{DC}$<br>$A_{AC}$ |
| ESD (Human Body Model) R = 1500 Ω, C = 100 pF | ESD | 8.0 | kV |
| ESD (Machine Model) R = 0 Ω, C = 200 pF | ESD | 800 | V |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |

**UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS** (–55°C ≤ $T_J$ ≤ 175°C)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Collector–to–Emitter Avalanche Energy<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 17.4 A, L = 2.0 mH, Starting $T_J$ = 25°C<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 14.2 A, L = 2.0 mH, Starting $T_J$ = 150°C | $E_{AS}$ | <br>300<br>200 | mJ |
| Reverse Avalanche Energy<br>$V_{CC}$ = 100 V, $V_{GE}$ = 20 V, L = 3.0 mH, Pk $I_L$ = 25.8 A, Starting $T_J$ = 25°C | $E_{AS(R)}$ | 1000 | mJ |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGP15N35CL | TO–220 | 50 Units/Rail |
| MGB15N35CLT4 | D2PAK | 800 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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### THERMAL CHARACTERISTICS

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Case | | $R_{\theta JC}$ | 1.0 | °C/W |
| Thermal Resistance, Junction to Ambient | TO–220 | $R_{\theta JA}$ | 62.5 | |
| | $D^2$PAK (Note 1.) | $R_{\theta JA}$ | 50 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | | $T_L$ | 275 | °C |

### ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Collector–Emitter Clamp Voltage | $BV_{CES}$ | $I_C$ = 2.0 mA | $T_J$ = –40°C to 150°C | 320 | 350 | 380 | $V_{DC}$ |
| | | $I_C$ = 10 mA | $T_J$ = –40°C to 150°C | 330 | 360 | 380 | |
| Zero Gate Voltage Collector Current | $I_{CES}$ | $V_{CE}$ = 300 V, $V_{GE}$ = 0 V | $T_J$ = 25°C | – | 1.5 | 20 | $\mu A_{DC}$ |
| | | | $T_J$ = 150°C | – | 10 | 40* | |
| | | | $T_J$ = –40°C | – | 0.7 | 1.5 | |
| Reverse Collector–Emitter Leakage Current | $I_{ECS}$ | $V_{CE}$ = –24 V | $T_J$ = 25°C | – | 0.35 | 1.0 | mA |
| | | | $T_J$ = 150°C | – | 8.0 | 15* | |
| | | | $T_J$ = –40°C | – | 0.05 | 0.5 | |
| Reverse Collector–Emitter Clamp Voltage | $B_{VCES(R)}$ | $I_C$ = –75 mA | $T_J$ = 25°C | 25 | 33 | 50 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 25 | 36 | 50 | |
| | | | $T_J$ = –40°C | 25 | 30 | 50 | |
| Gate–Emitter Clamp Voltage | $BV_{GES}$ | $I_G$ = 5.0 mA | $T_J$ = –40°C to 150°C | 17 | 20 | 22 | $V_{DC}$ |
| Gate–Emitter Leakage Current | $I_{GES}$ | $V_{GE}$ = 10 V | $T_J$ = –40°C to 150°C | 384 | 600 | 1000 | $\mu A_{DC}$ |
| Gate Resistor (Optional) | $R_G$ | – | $T_J$ = –40°C to 150°C | – | 70 | – | Ω |
| Gate Emitter Resistor | $R_{GE}$ | – | $T_J$ = –40°C to 150°C | 10 | 16 | 26 | kΩ |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | | |
| Gate Threshold Voltage | $V_{GE(th)}$ | $I_C$ = 1.0 mA, $V_{GE}$ = $V_{CE}$ | $T_J$ = 25°C | 1.4 | 1.7 | 2.0 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.75 | 1.1 | 1.4 | |
| | | | $T_J$ = –40°C | 1.6 | 1.9 | 2.1* | |
| Threshold Temperature Coefficient (Negative) | – | – | – | – | 4.4 | – | mV/°C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width ≤ 300 µS, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ON CHARACTERISTICS (continued)** (Note 3.) | | | | | | | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 6.0 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.0 | 1.3 | 1.6 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.9 | 1.2 | 1.5 | |
| | | | $T_J$ = –40°C | 1.1 | 1.4 | 1.7* | |
| | | $I_C$ = 10 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.3 | 1.6 | 1.9 | |
| | | | $T_J$ = 150°C | 1.2 | 1.5 | 1.8 | |
| | | | $T_J$ = –40°C | 1.3 | 1.6 | 1.9* | |
| | | $I_C$ = 15 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.6 | 1.95 | 2.25 | |
| | | | $T_J$ = 150°C | 1.7 | 2.0 | 2.3* | |
| | | | $T_J$ = –40°C | 1.6 | 1.9 | 2.2 | |
| | | $I_C$ = 20 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.9 | 2.2 | 2.5 | |
| | | | $T_J$ = 150°C | 2.1 | 2.4 | 2.7* | |
| | | | $T_J$ = –40°C | 1.85 | 2.15 | 2.45 | |
| | | $I_C$ = 25 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 2.1 | 2.5 | 2.9 | |
| | | | $T_J$ = 150°C | 2.5 | 2.9 | 3.3* | |
| | | | $T_J$ = –40°C | 2.0 | 2.4 | 2.8 | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 10 A, $V_{GE}$ = 4.5 V | $T_J$ = 150°C | – | 1.5 | 1.8 | $V_{DC}$ |
| Forward Transconductance | gfs | $V_{CE}$ = 5.0 V, $I_C$ = 6.0 A | $T_J$ = –40°C to 150°C | 8.0 | 15 | 25 | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{CC}$ = 25 V, $V_{GE}$ = 0 V f = 1.0 MHz | $T_J$ = –40°C to 150°C | – | 1000 | 1300 | pF |
| Output Capacitance | $C_{OSS}$ | | | – | 100 | 130 | |
| Transfer Capacitance | $C_{RSS}$ | | | – | 5.0 | 8.0 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | | |
| Turn–Off Delay Time (Inductive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 4.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 4.5 | 10 | |
| Fall Time (Inductive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 7.0 | 10 | |
| | | | $T_J$ = 150°C | – | 10 | 15* | |
| Turn–Off Delay Time (Resistive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω, | $T_J$ = 25°C | – | 4.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 4.5 | 10 | |
| Fall Time (Resistive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω, | $T_J$ = 25°C | – | 13 | 20 | |
| | | | $T_J$ = 150°C | – | 16 | 20 | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 1.0 | 1.5 | μSec |
| | | | $T_J$ = 150°C | – | 1.0 | 1.5 | |
| Rise Time | $t_r$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 4.5 | 6.0 | |
| | | | $T_J$ = 150°C | – | 5.0 | 6.0 | |

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
*Maximum Value of Characteristic across Temperature Range.

**TYPICAL ELECTRICAL CHARACTERISTICS** (unless otherwise noted)

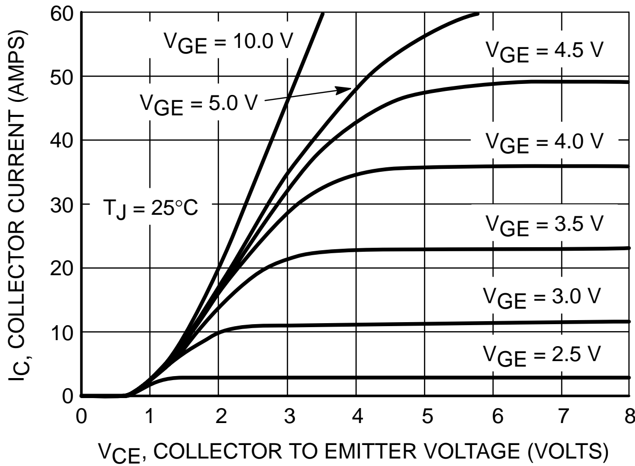


**Figure 1. Output Characteristics**

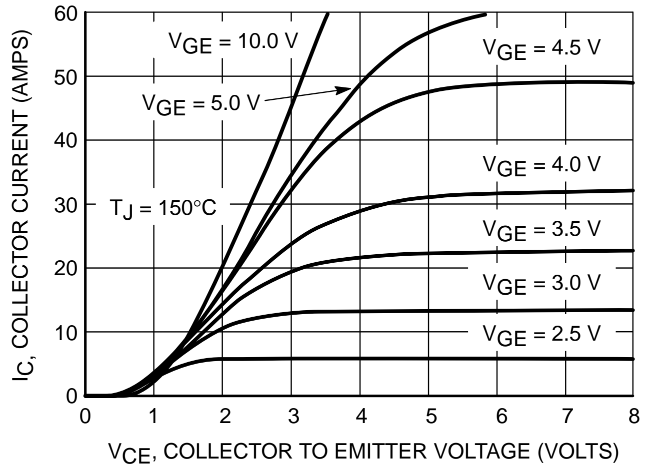


**Figure 2. Output Characteristics**

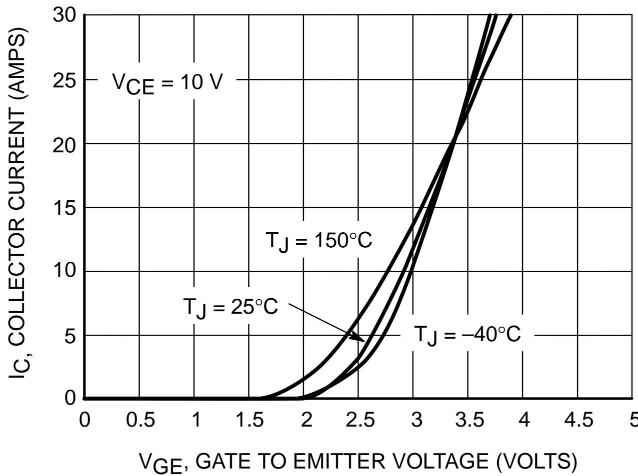


**Figure 3. Transfer Characteristics**

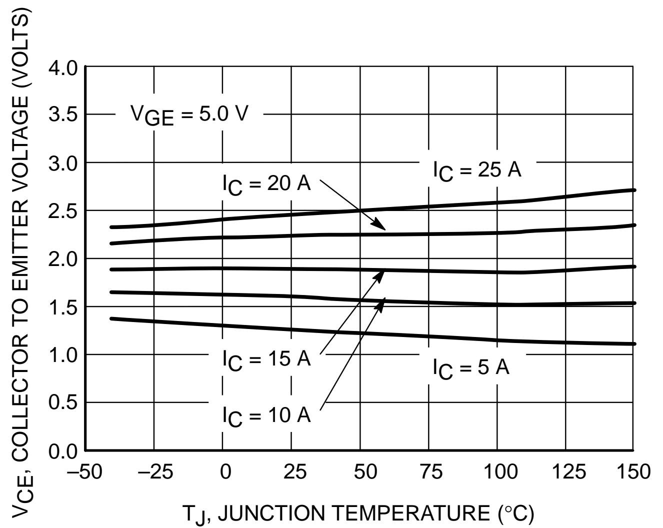


**Figure 4. Collector–to–Emitter Saturation Voltage vs. Junction Temperature**

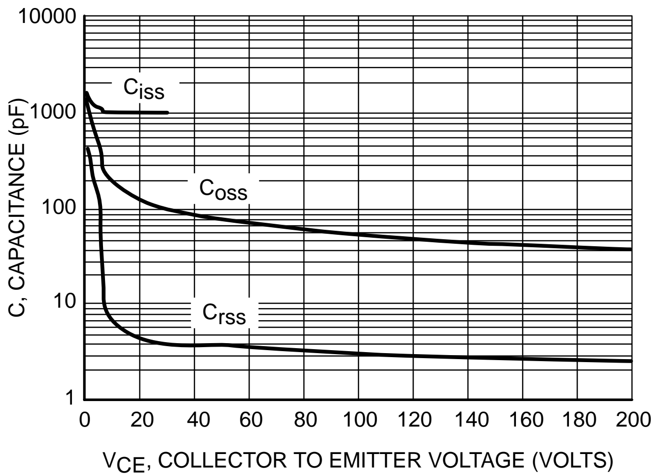


**Figure 5. Capacitance Variation**

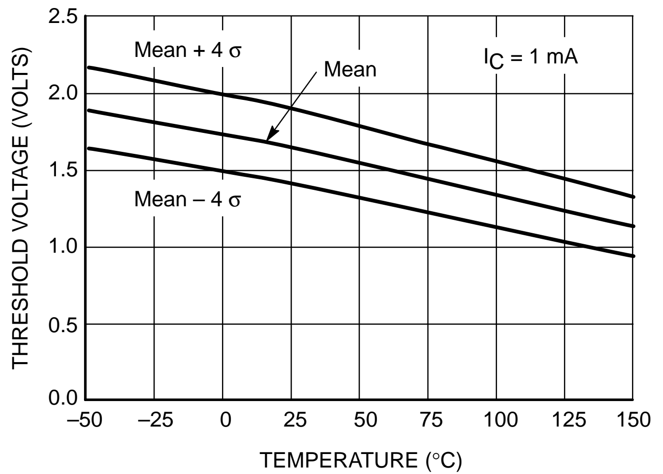


**Figure 6. Threshold Voltage vs. Temperature**

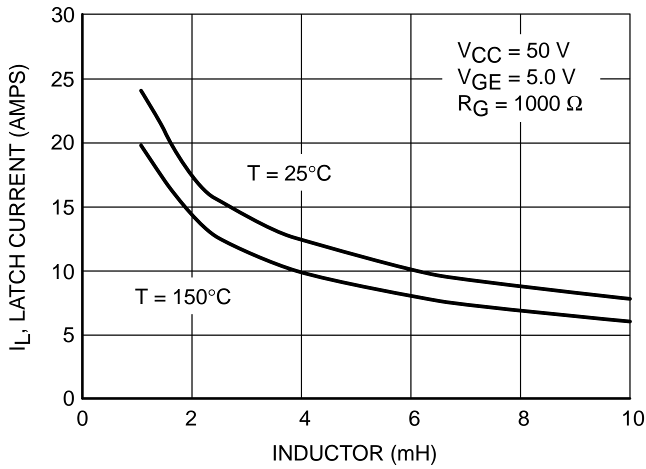


**Figure 7. Minimum Open Secondary Latch Current vs. Inductor**

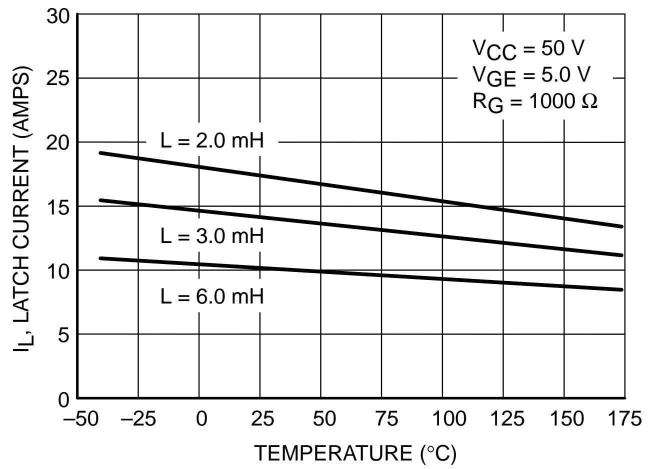


**Figure 8. Minimum Open Secondary Latch Current vs. Temperature**

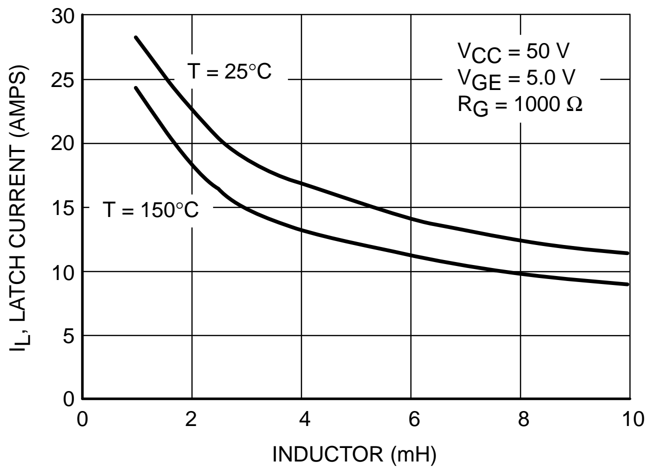


**Figure 9. Typical Open Secondary Latch Current vs. Inductor**

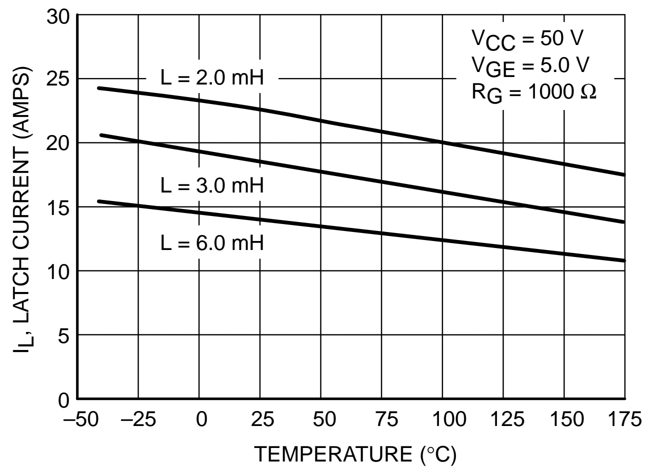


**Figure 10. Typical Open Secondary Latch Current vs. Temperature**

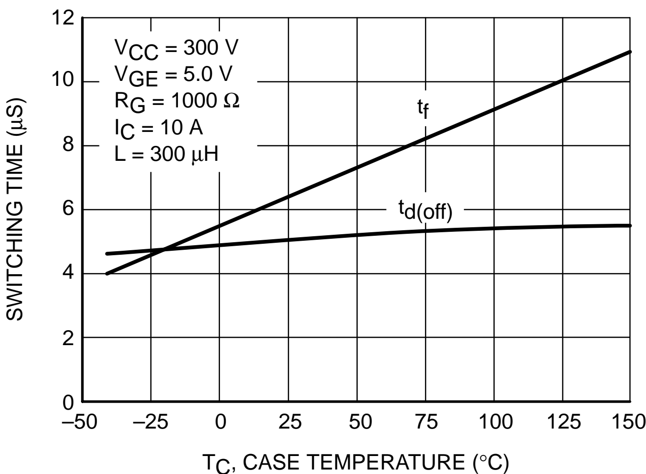


**Figure 11. Switching Speed vs. Case Temperature**

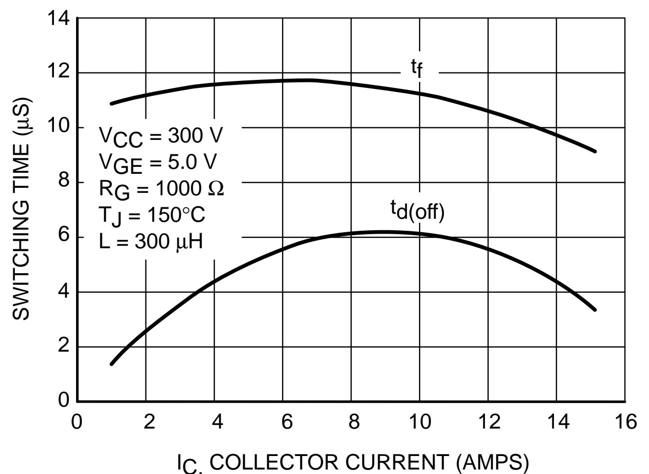


**Figure 12. Switching Speed vs. Collector Current**

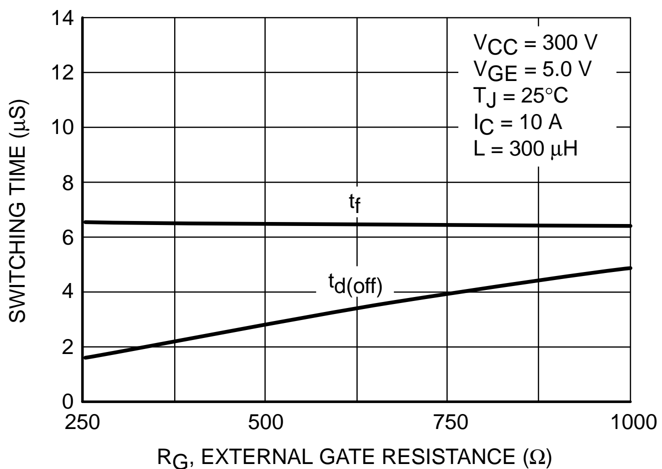


**Figure 13. Switching Speed vs. External Gate Resistance**

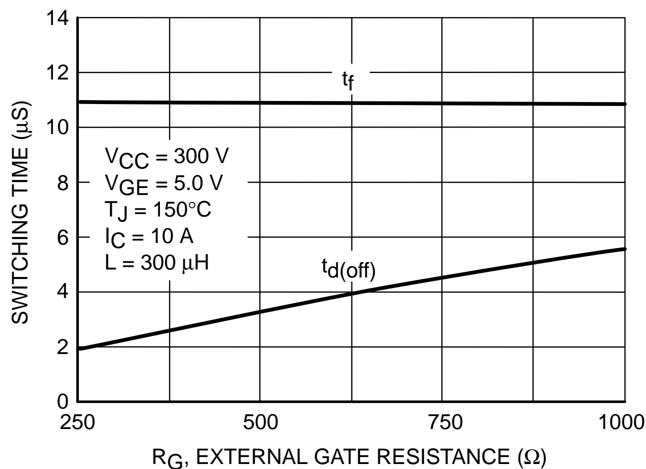


**Figure 14. Switching Speed vs. External Gate Resistance**

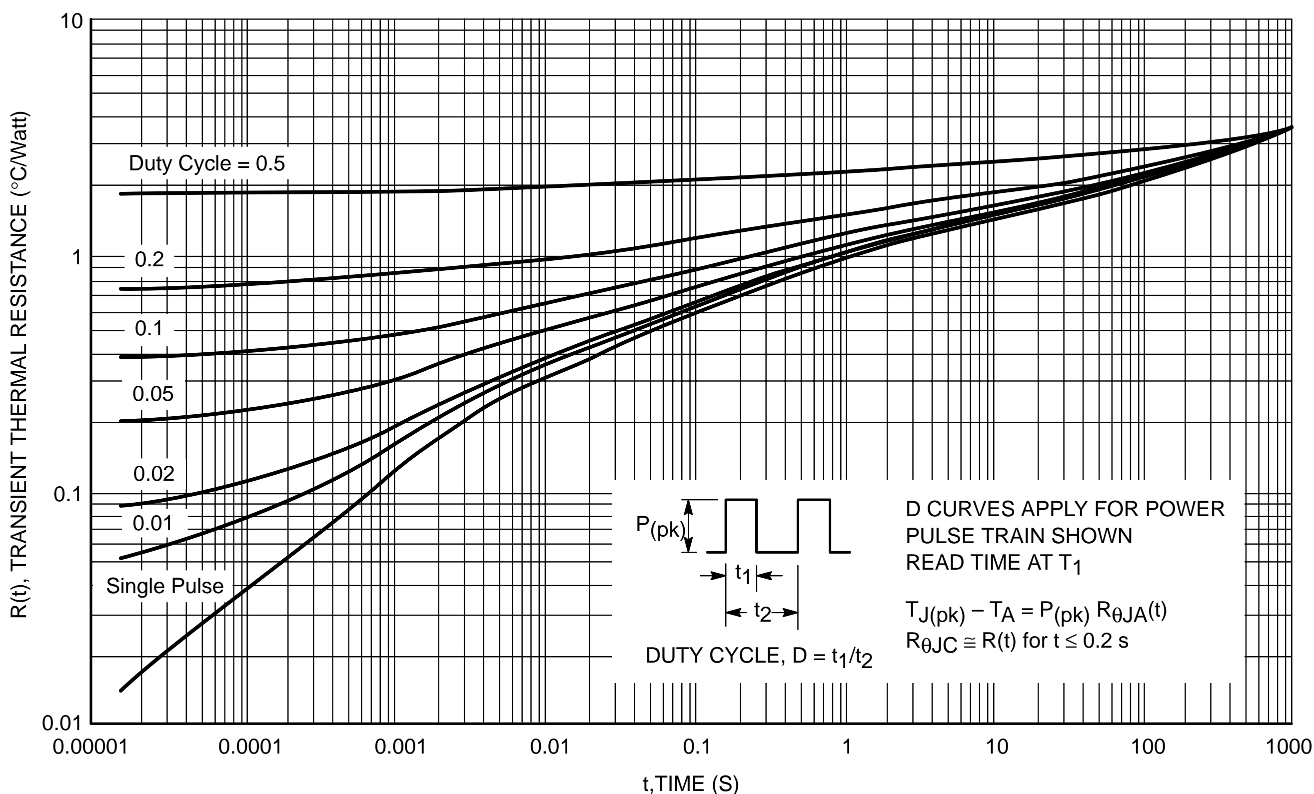


**Figure 15. Transient Thermal Resistance (Non–normalized Junction–to–Ambient mounted on fixture in Figure 16)**

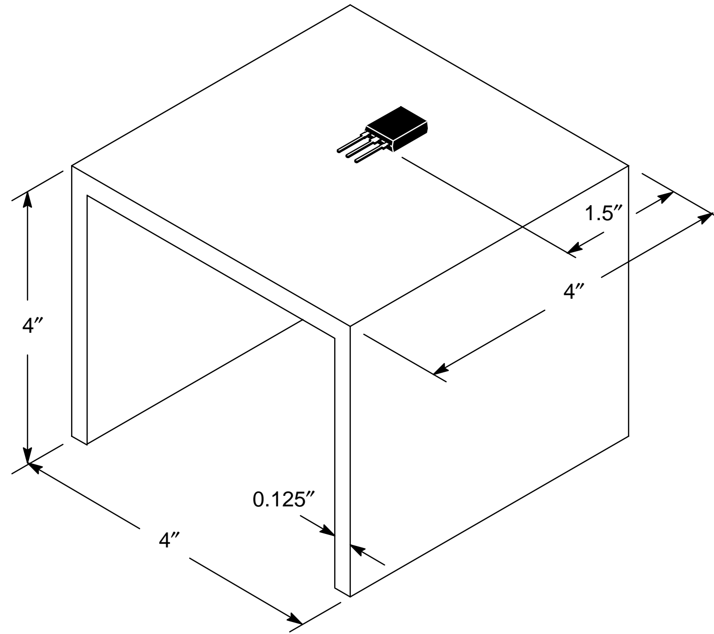


**Figure 16. Test Fixture for Transient Thermal Curve (48 square inches of 1/8″ thick aluminum)**

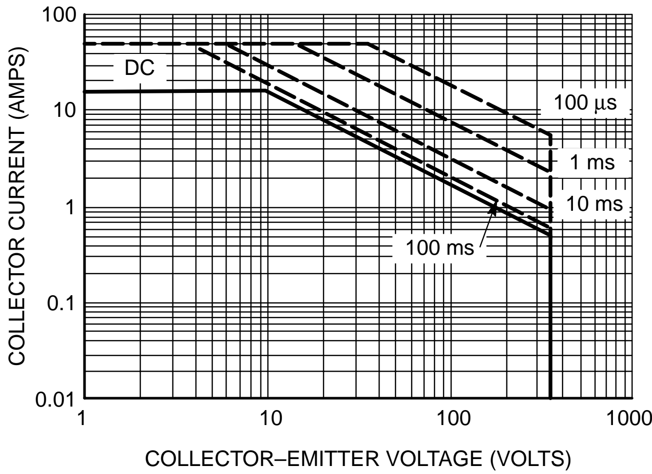


**Figure 17. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

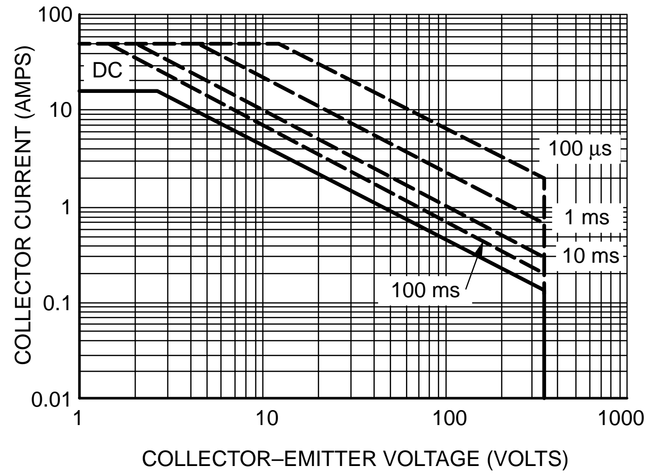


**Figure 18. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

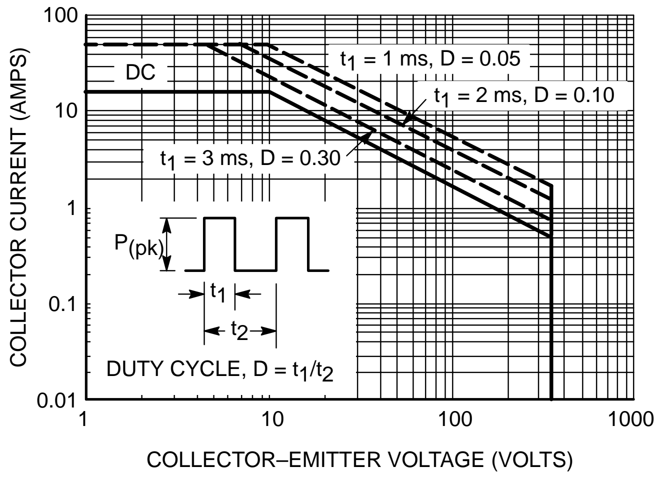


**Figure 19. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

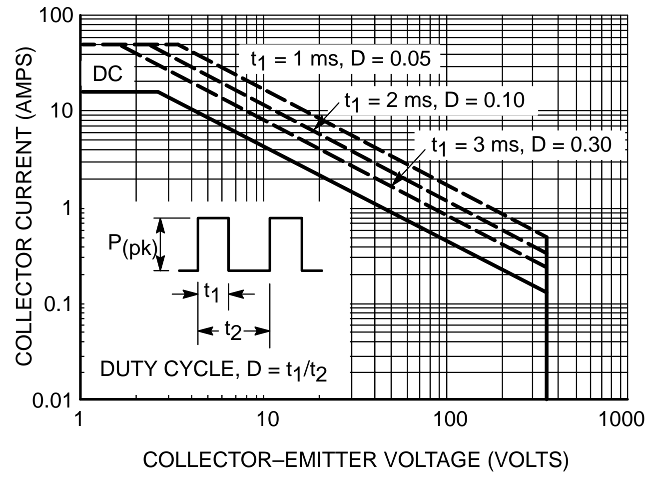


**Figure 20. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

# MGP15N40CL, MGB15N40CL

**Preferred Device**

# Ignition IGBT 15 Amps, 410 Volts

## N–Channel TO–220 and D2PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

- Ideal for Coil–On–Plug, IGBT–On–Coil, or Distributorless Ignition System Applications
- High Pulsed Current Capability up to 50 A
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- Optional Gate Resistor ($R_G$)

**MAXIMUM RATINGS** (–55°C ≤ $T_J$ ≤ 175°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CES}$ | 380 | $V_{DC}$ |
| Collector–Gate Voltage | $V_{CER}$ | 380 | $V_{DC}$ |
| Gate–Emitter Voltage | $V_{GE}$ | 22 | $V_{DC}$ |
| Collector Current–Continuous<br>@ $T_C$ = 25°C – Pulsed | $I_C$ | 15<br>50 | $A_{DC}$<br>$A_{AC}$ |
| ESD (Human Body Model)<br>R = 1500 Ω, C = 100 pF | ESD | <br>8.0 | kV |
| ESD (Machine Model) R = 0 Ω, C = 200 pF | ESD | 800 | V |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |

**UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS** (–55°C ≤ $T_J$ ≤ 175°C)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Collector–to–Emitter Avalanche Energy<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 17.4 A, L = 2.0 mH, Starting $T_J$ = 25°C<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 14.2 A, L = 2.0 mH, Starting $T_J$ = 150°C | $E_{AS}$ | <br>300<br><br>200 | mJ |
| Reverse Avalanche Energy<br>$V_{CC}$ = 100 V, $V_{GE}$ = 20 V, L = 3.0 mH, Pk $I_L$ = 25.8 A, Starting $T_J$ = 25°C | $E_{AS(R)}$ | 1000 | mJ |

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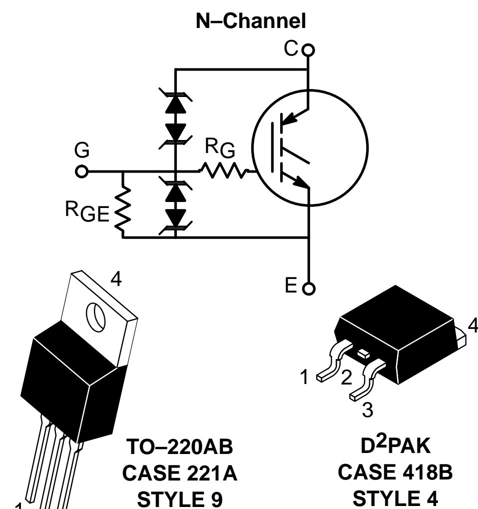
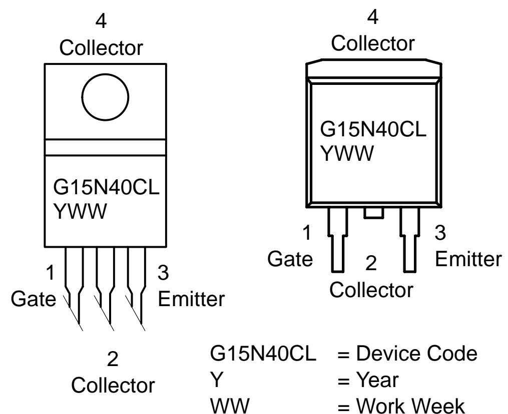
**15 AMPERES**
**410 VOLTS (Clamped)**
**$V_{CE(on)}$ @ 10 A = 1.8 V Max**




**TO–220AB CASE 221A STYLE 9**

**D2PAK CASE 418B STYLE 4**

**MARKING DIAGRAMS & PIN ASSIGNMENTS**




G15N40CL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGP15N40CL | TO–220 | 50 Units/Rail |
| MGB15N40CLT4 | D2PAK | 800 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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March, 2001 – Rev. 5

Publication Order Number:
MGP15N40CL/D

## THERMAL CHARACTERISTICS

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Case | | $R_{\theta JC}$ | 1.0 | °C/W |
| Thermal Resistance, Junction to Ambient | TO–220 | $R_{\theta JA}$ | 62.5 | |
| | $D^2PAK$ (Note 1.) | $R_{\theta JA}$ | 50 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | | $T_L$ | 275 | °C |

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Collector–Emitter Clamp Voltage | $BV_{CES}$ | $I_C$ = 2.0 mA | $T_J$ = –40°C to 150°C | 320 | 350 | 380 | $V_{DC}$ |
| | | $I_C$ = 10 mA | $T_J$ = –40°C to 150°C | 330 | 360 | 380 | |
| Zero Gate Voltage Collector Current | $I_{CES}$ | $V_{CE}$ = 300 V, $V_{GE}$ = 0 V | $T_J$ = 25°C | – | 1.5 | 20 | μ$A_{DC}$ |
| | | | $T_J$ = 150°C | – | 10 | 40* | |
| | | | $T_J$ = –40°C | – | 0.7 | 1.5 | |
| Reverse Collector–Emitter Leakage Current | $I_{ECS}$ | $V_{CE}$ = –24 V | $T_J$ = 25°C | – | 0.35 | 1.0 | mA |
| | | | $T_J$ = 150°C | – | 8.0 | 15* | |
| | | | $T_J$ = –40°C | – | 0.05 | 0.5 | |
| Reverse Collector–Emitter Clamp Voltage | $B_{VCES(R)}$ | $I_C$ = –75 mA | $T_J$ = 25°C | 25 | 33 | 50 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 25 | 36 | 50 | |
| | | | $T_J$ = –40°C | 25 | 30 | 50 | |
| Gate–Emitter Clamp Voltage | $BV_{GES}$ | $I_G$ = 5.0 mA | $T_J$ = –40°C to 150°C | 17 | 20 | 22 | $V_{DC}$ |
| Gate–Emitter Leakage Current | $I_{GES}$ | $V_{GE}$ = 10 V | $T_J$ = –40°C to 150°C | 384 | 600 | 1000 | μ$A_{DC}$ |
| Gate Resistor (Optional) | $R_G$ | – | $T_J$ = –40°C to 150°C | – | 70 | – | Ω |
| Gate Emitter Resistor | $R_{GE}$ | – | $T_J$ = –40°C to 150°C | 10 | 16 | 26 | kΩ |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | | |
| Gate Threshold Voltage | $V_{GE(th)}$ | $I_C$ = 1.0 mA, $V_{GE}$ = $V_{CE}$ | $T_J$ = 25°C | 1.4 | 1.7 | 2.0 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.75 | 1.1 | 1.4 | |
| | | | $T_J$ = –40°C | 1.6 | 1.9 | 2.1* | |
| Threshold Temperature Coefficient (Negative) | – | – | – | – | 4.4 | – | mV/°C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ON CHARACTERISTICS (continued)** (Note 3.) | | | | | | | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 6.0 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.0 | 1.3 | 1.6 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.9 | 1.2 | 1.5 | |
| | | | $T_J$ = –40°C | 1.1 | 1.4 | 1.7* | |
| | | $I_C$ = 10 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.3 | 1.6 | 1.9 | |
| | | | $T_J$ = 150°C | 1.2 | 1.5 | 1.8 | |
| | | | $T_J$ = –40°C | 1.3 | 1.6 | 1.9* | |
| | | $I_C$ = 15 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.6 | 1.95 | 2.25 | |
| | | | $T_J$ = 150°C | 1.7 | 2.0 | 2.3* | |
| | | | $T_J$ = –40°C | 1.6 | 1.9 | 2.2 | |
| | | $I_C$ = 20 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.9 | 2.2 | 2.5 | |
| | | | $T_J$ = 150°C | 2.1 | 2.4 | 2.7* | |
| | | | $T_J$ = –40°C | 1.85 | 2.15 | 2.45 | |
| | | $I_C$ = 25 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 2.1 | 2.5 | 2.9 | |
| | | | $T_J$ = 150°C | 2.5 | 2.9 | 3.3* | |
| | | | $T_J$ = –40°C | 2.0 | 2.4 | 2.8 | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 10 A, $V_{GE}$ = 4.5 V | $T_J$ = 150°C | – | 1.5 | 1.8 | $V_{DC}$ |
| Forward Transconductance | gfs | $V_{CE}$ = 5.0 V, $I_C$ = 6.0 A | $T_J$ = –40°C to 150°C | 8.0 | 15 | 25 | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{CC}$ = 25 V, $V_{GE}$ = 0 V f = 1.0 MHz | $T_J$ = –40°C to 150°C | – | 1000 | 1300 | pF |
| Output Capacitance | $C_{OSS}$ | | | – | 100 | 130 | |
| Transfer Capacitance | $C_{RSS}$ | | | – | 5.0 | 8.0 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | | |
| Turn–Off Delay Time (Inductive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 4.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 4.5 | 10 | |
| Fall Time (Inductive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 7.0 | 10 | |
| | | | $T_J$ = 150°C | – | 10 | 15* | |
| Turn–Off Delay Time (Resistive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω, | $T_J$ = 25°C | – | 4.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 4.5 | 10 | |
| Fall Time (Resistive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω, | $T_J$ = 25°C | – | 13 | 20 | |
| | | | $T_J$ = 150°C | – | 16 | 20 | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 1.0 | 1.5 | μSec |
| | | | $T_J$ = 150°C | – | 1.0 | 1.5 | |
| Rise Time | $t_r$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 4.5 | 6.0 | |
| | | | $T_J$ = 150°C | – | 5.0 | 6.0 | |

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
*Maximum Value of Characteristic across Temperature Range.

## TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

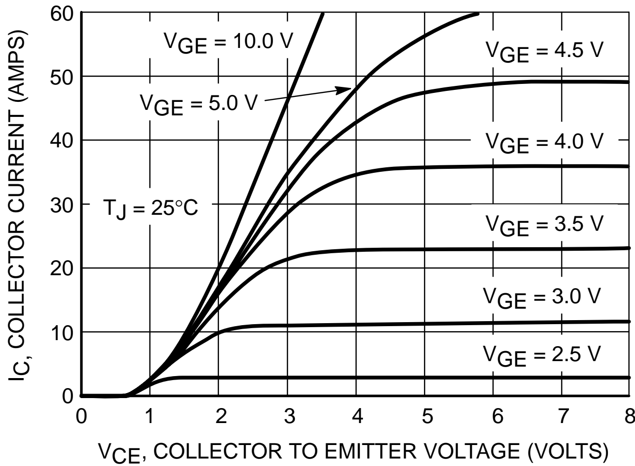


**Figure 1. Output Characteristics**

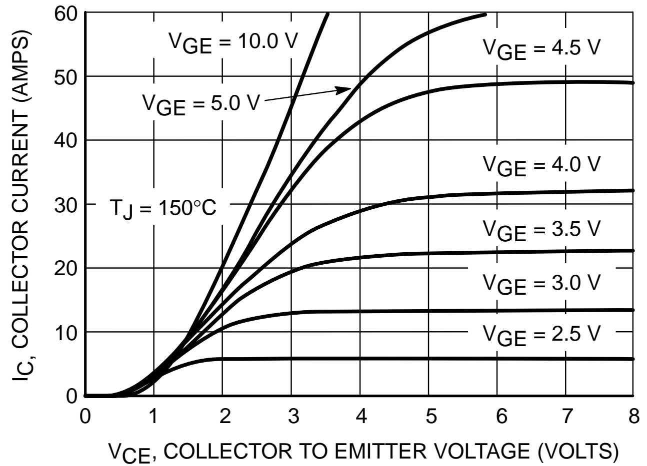


**Figure 2. Output Characteristics**

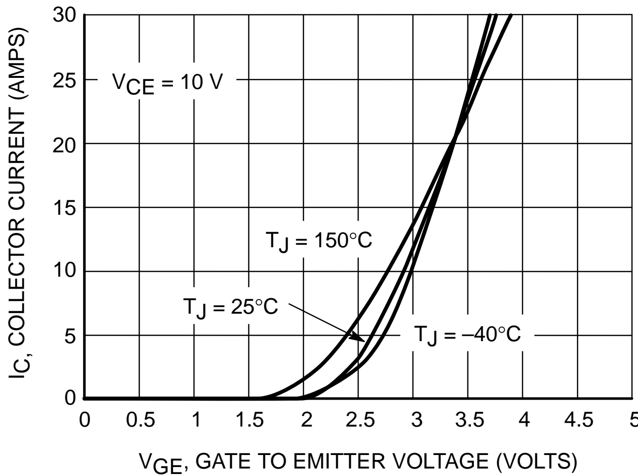


**Figure 3. Transfer Characteristics**

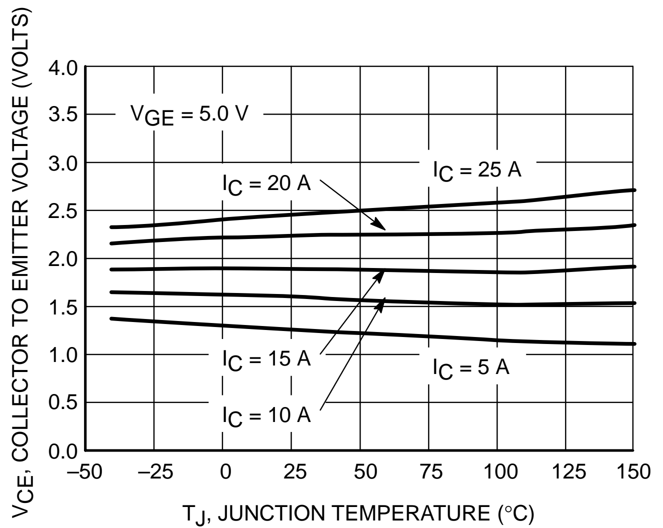


**Figure 4. Collector–to–Emitter Saturation Voltage vs. Junction Temperature**

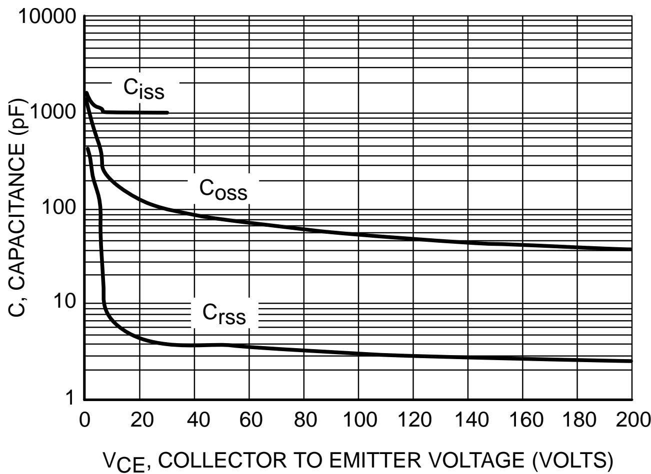


**Figure 5. Capacitance Variation**

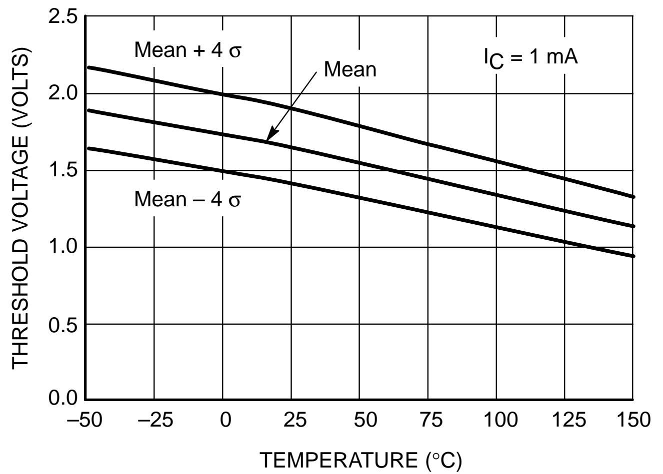


**Figure 6. Threshold Voltage vs. Temperature**

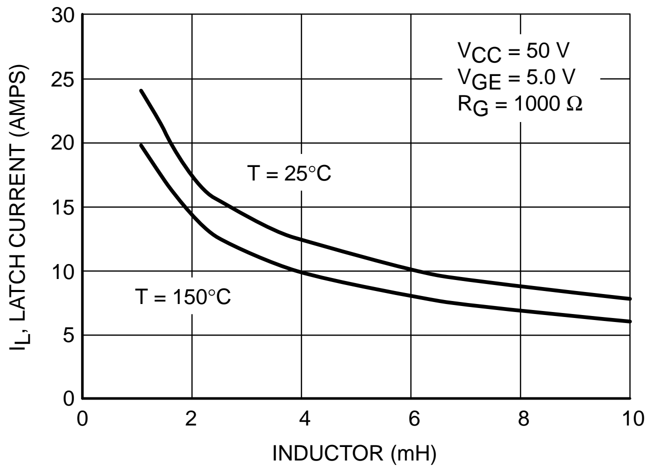


**Figure 7. Minimum Open Secondary Latch Current vs. Inductor**

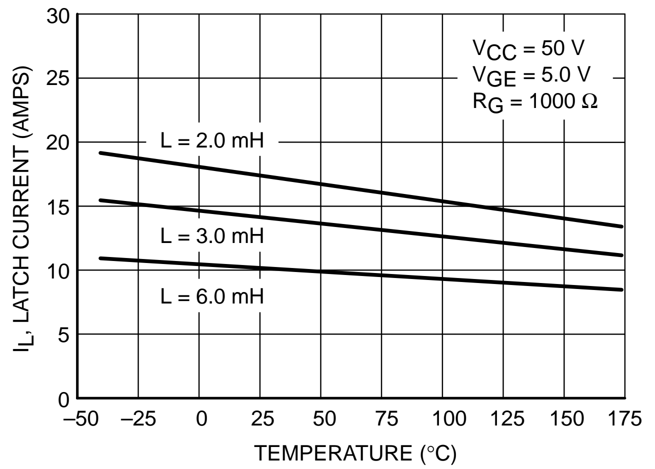


**Figure 8. Minimum Open Secondary Latch Current vs. Temperature**

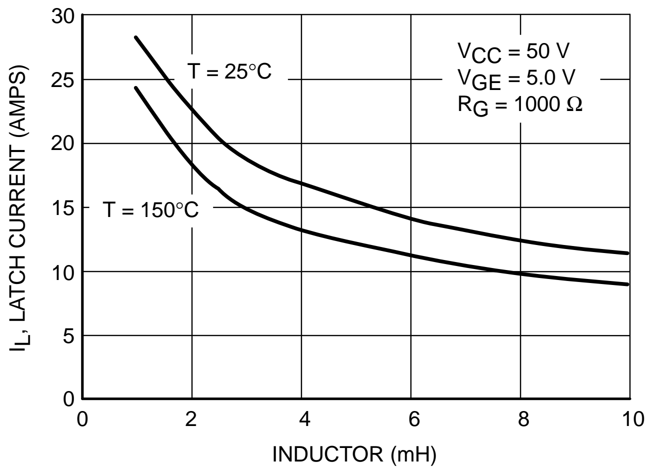


**Figure 9. Typical Open Secondary Latch Current vs. Inductor**

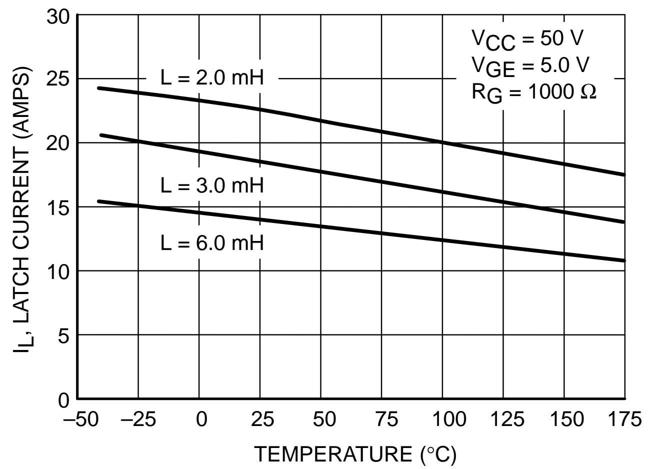


**Figure 10. Typical Open Secondary Latch Current vs. Temperature**

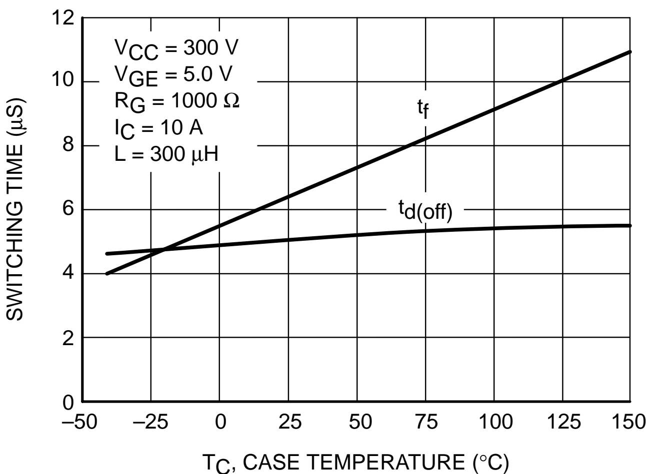


**Figure 11. Switching Speed vs. Case Temperature**

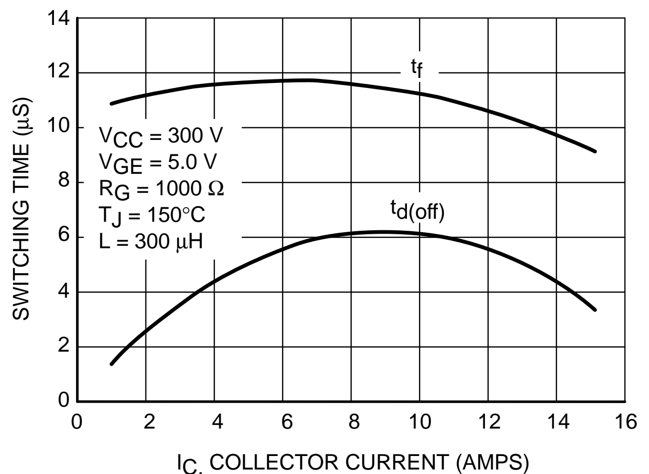


**Figure 12. Switching Speed vs. Collector Current**

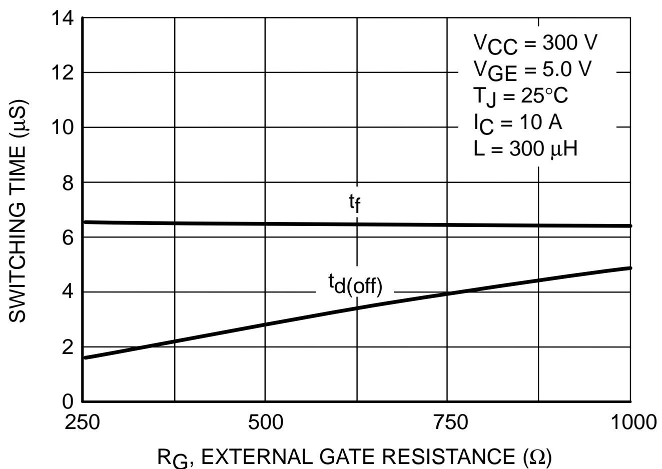


**Figure 13. Switching Speed vs. External Gate Resistance**

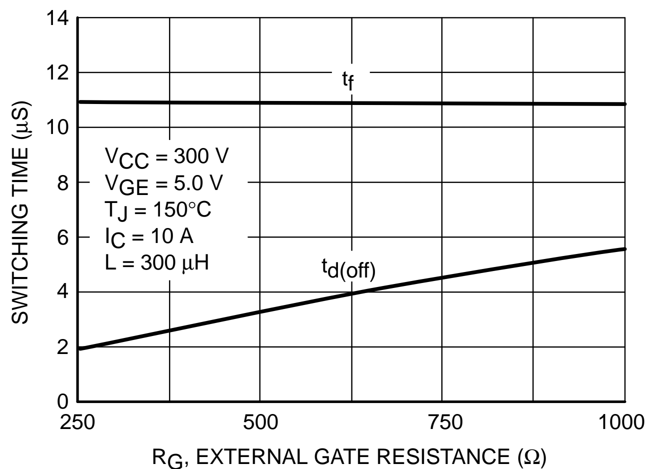


**Figure 14. Switching Speed vs. External Gate Resistance**

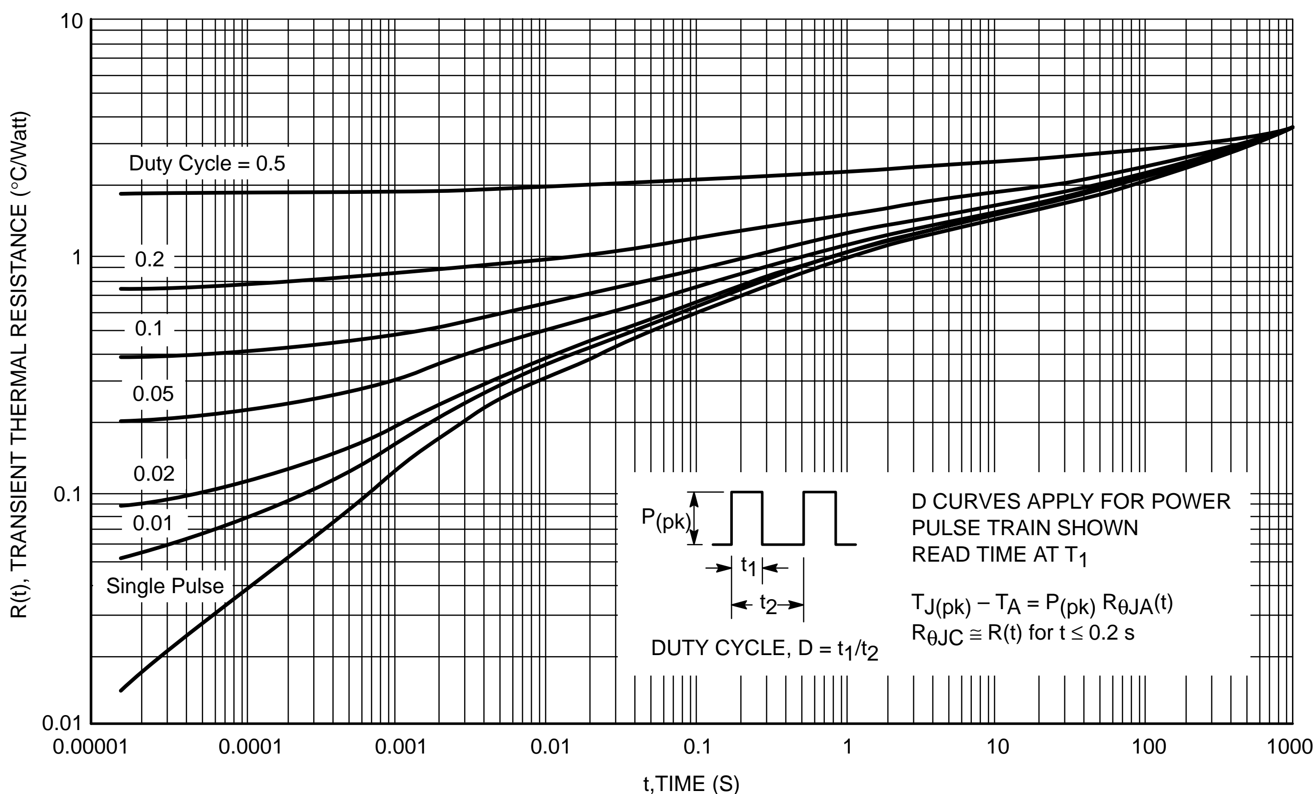


**Figure 15. Transient Thermal Resistance (Non–normalized Junction–to–Ambient mounted on fixture in Figure 16)**

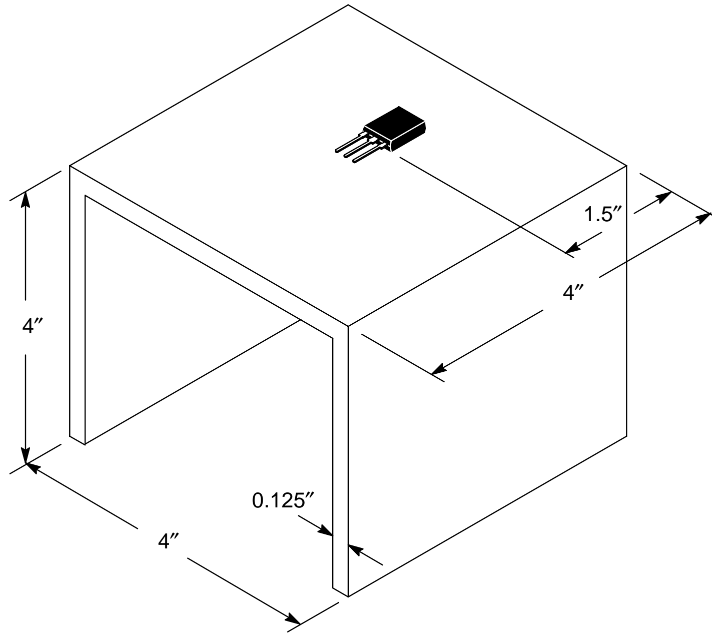


**Figure 16. Test Fixture for Transient Thermal Curve (48 square inches of 1/8″ thick aluminum)**

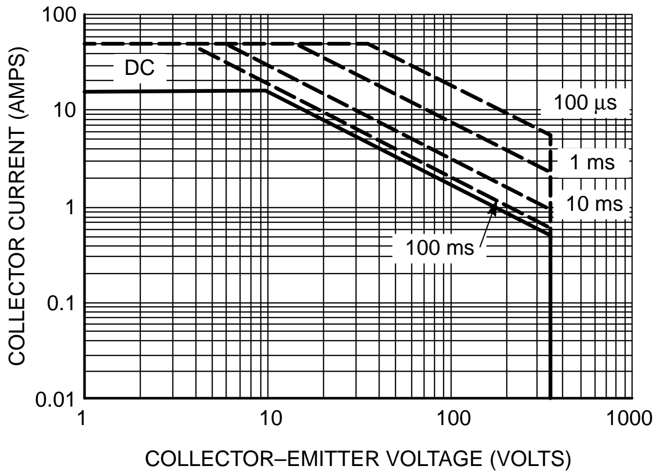


**Figure 17. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

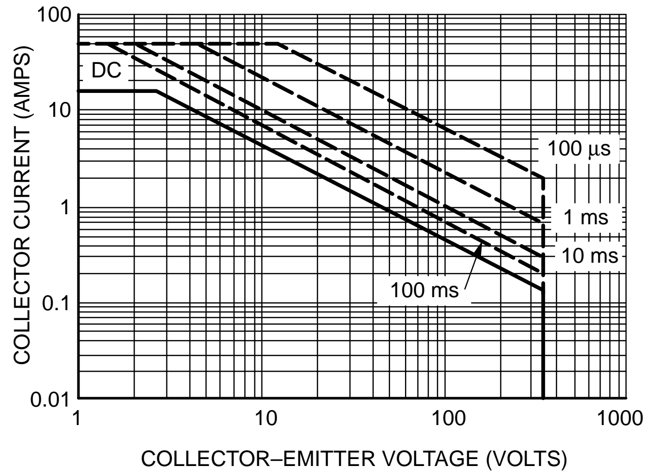


**Figure 18. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

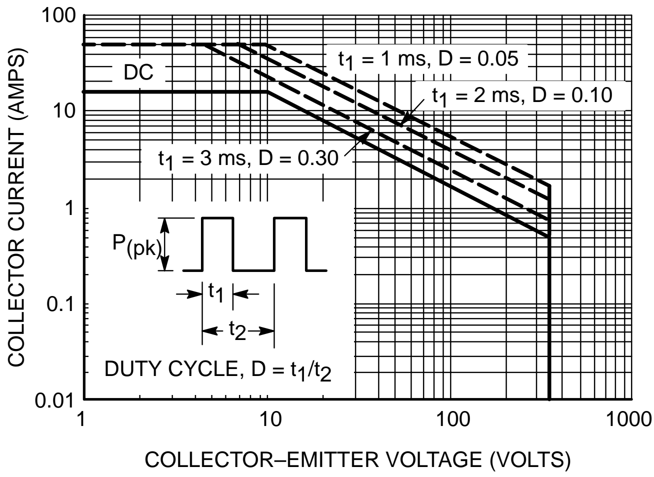


**Figure 19. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

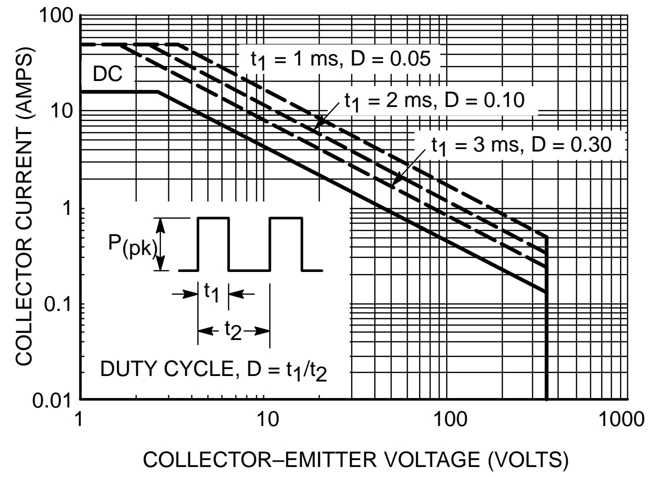


**Figure 20. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

# MGP19N35CL, MGB19N35CL

**Preferred Device**

# Ignition IGBT
# 19 Amps, 350 Volts
## N–Channel TO–220 and D2PAK

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over–Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

- Ideal for IGBT–On–Coil or Distributorless Ignition System Applications
- High Pulsed Current Capability up to 50 A
- Gate–Emitter ESD Protection
- Temperature Compensated Gate–Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- Optional Gate Resistor ($R_G$)

**MAXIMUM RATINGS** (–55°C ≤ $T_J$ ≤ 175°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Collector–Emitter Voltage | $V_{CES}$ | 380 | $V_{DC}$ |
| Collector–Gate Voltage | $V_{CER}$ | 380 | $V_{DC}$ |
| Gate–Emitter Voltage | $V_{GE}$ | 22 | $V_{DC}$ |
| Collector Current – Continuous<br>@ $T_C$ = 25°C – Pulsed | $I_C$ | 19<br>50 | $A_{DC}$<br>$A_{AC}$ |
| ESD (Human Body Model)<br>R = 1500 Ω, C = 100 pF | ESD | 8.0 | kV |
| ESD (Machine Model) R = 0 Ω, C = 200 pF | ESD | 800 | V |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 165<br>1.1 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |

**UNCLAMPED COLLECTOR–TO–EMITTER AVALANCHE CHARACTERISTICS** (–55°C ≤ $T_J$ ≤ 175°C)

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Collector–to–Emitter Avalanche Energy<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 22.4 A, L = 2.0 mH, Starting $T_J$ = 25°C<br>$V_{CC}$ = 50 V, $V_{GE}$ = 5.0 V, Pk $I_L$ = 17.4 A, L = 2.0 mH, Starting $T_J$ = 150°C | $E_{AS}$ | <br>500<br>300 | mJ |
| Reverse Avalanche Energy<br>$V_{CC}$ = 100 V, $V_{GE}$ = 20 V, L = 3.0 mH, Pk $I_L$ = 25.8 A, Starting $T_J$ = 25°C | $E_{AS(R)}$ | 1000 | mJ |

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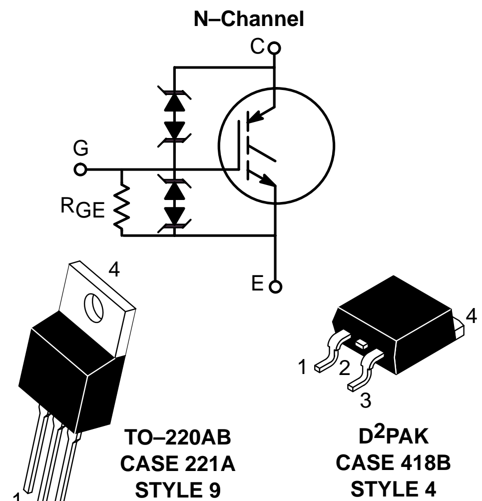
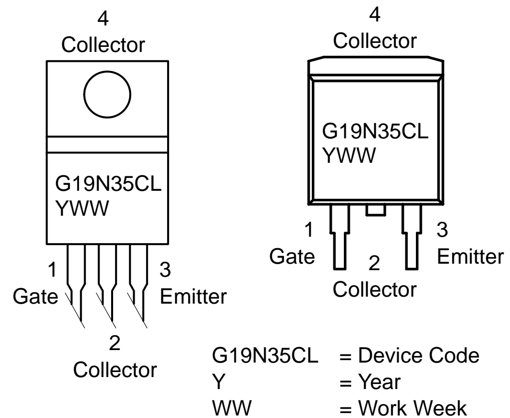
**19 AMPERES**
**350 VOLTS (Clamped)**
**$V_{CE(on)}$ @ 10 A = 1.8 V Max**




**MARKING DIAGRAMS & PIN ASSIGNMENTS**




| | |
|---|---|
| G19N35CL | = Device Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGP19N35CL | TO–220 | 50 Units/Rail |
| MGB19N35CLT4 | D2PAK | 800 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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## THERMAL CHARACTERISTICS

| Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|
| Thermal Resistance, Junction to Case | | $R_{\theta JC}$ | 0.9 | °C/W |
| Thermal Resistance, Junction to Ambient | TO–220 | $R_{\theta JA}$ | 62.5 | |
| | $D^2PAK$ (Note 1.) | $R_{\theta JA}$ | 50 | |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | | $T_L$ | 275 | °C |

## ELECTRICAL CHARACTERISTICS

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Collector–Emitter Clamp Voltage | $BV_{CES}$ | $I_C$ = 2.0 mA | $T_J$ = –40°C to 150°C | 320 | 350 | 380 | $V_{DC}$ |
| | | $I_C$ = 10 mA | $T_J$ = –40°C to 150°C | 330 | 360 | 380 | |
| Zero Gate Voltage Collector Current | $I_{CES}$ | $V_{CE}$ = 300 V, $V_{GE}$ = 0 V | $T_J$ = 25°C | – | 1.5 | 20 | $\mu A_{DC}$ |
| | | | $T_J$ = 150°C | – | 15 | 40* | |
| | | | $T_J$ = –40°C | – | 0.7 | 1.5 | |
| Reverse Collector–Emitter Leakage Current | $I_{ECS}$ | $V_{CE}$ = –24 V | $T_J$ = 25°C | – | 0.35 | 1.0 | mA |
| | | | $T_J$ = 150°C | – | 10 | 20* | |
| | | | $T_J$ = –40°C | – | 0.05 | 0.5 | |
| Reverse Collector–Emitter Clamp Voltage | $B_{VCES(R)}$ | $I_C$ = –75 mA | $T_J$ = 25°C | 25 | 33 | 50 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 25 | 36 | 50 | |
| | | | $T_J$ = –40°C | 25 | 30 | 50 | |
| Gate–Emitter Clamp Voltage | $BV_{GES}$ | $I_G$ = 5.0 mA | $T_J$ = –40°C to 150°C | 17 | 20 | 22 | $V_{DC}$ |
| Gate–Emitter Leakage Current | $I_{GES}$ | $V_{GE}$ = 10 V | $T_J$ = –40°C to 150°C | 384 | 500 | 1000 | $\mu A_{DC}$ |
| Gate Resistor (Optional) | $R_G$ | – | $T_J$ = –40°C to 150°C | – | 70 | – | Ω |
| Gate Emitter Resistor | $R_{GE}$ | – | $T_J$ = –40°C to 150°C | 10 | 20 | 26 | kΩ |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | | |
| Gate Threshold Voltage | $V_{GE(th)}$ | $I_C$ = 1.0 mA, $V_{GE}$ = $V_{CE}$ | $T_J$ = 25°C | 1.4 | 1.7 | 2.0 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.75 | 1.1 | 1.4 | |
| | | | $T_J$ = –40°C | 1.6 | 1.9 | 2.1* | |
| Threshold Temperature Coefficient (Negative) | – | – | – | – | 4.4 | – | mV/°C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.
2. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.

*Maximum Value of Characteristic across Temperature Range.

**ELECTRICAL CHARACTERISTICS (continued)**

| Characteristic | Symbol | Test Conditions | Temperature | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **ON CHARACTERISTICS (continued)** (Note 3.) | | | | | | | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 6.0 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.0 | 1.25 | 1.6 | $V_{DC}$ |
| | | | $T_J$ = 150°C | 0.8 | 1.05 | 1.4 | |
| | | | $T_J$ = –40°C | 1.15 | 1.4 | 1.75* | |
| | | $I_C$ = 10 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.2 | 1.5 | 1.8 | |
| | | | $T_J$ = 150°C | 1.0 | 1.3 | 1.6 | |
| | | | $T_J$ = –40°C | 1.3 | 1.6 | 1.9* | |
| | | $I_C$ = 15 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.5 | 1.75 | 2.1 | |
| | | | $T_J$ = 150°C | 1.35 | 1.65 | 1.95 | |
| | | | $T_J$ = –40°C | 1.5 | 1.8 | 2.1* | |
| | | $I_C$ = 20 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 1.7 | 2.0 | 2.3 | |
| | | | $T_J$ = 150°C | 1.6 | 1.9 | 2.2 | |
| | | | $T_J$ = –40°C | 1.7 | 2.0 | 2.3* | |
| | | $I_C$ = 25 A, $V_{GE}$ = 4.0 V | $T_J$ = 25°C | 2.0 | 2.25 | 2.6 | |
| | | | $T_J$ = 150°C | 2.0 | 2.3 | 2.7* | |
| | | | $T_J$ = –40°C | 2.0 | 2.2 | 2.6 | |
| Collector–to–Emitter On–Voltage | $V_{CE(on)}$ | $I_C$ = 10 A, $V_{GE}$ = 4.5 V | $T_J$ = 150°C | – | 1.3 | 1.8 | $V_{DC}$ |
| Forward Transconductance | gfs | $V_{CE}$ = 5.0 V, $I_C$ = 6.0 A | $T_J$ = –40°C to 150°C | 8.0 | 15 | 25 | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{CC}$ = 25 V, $V_{GE}$ = 0 V f = 1.0 MHz | $T_J$ = –40°C to 150°C | – | 1500 | 1800 | pF |
| Output Capacitance | $C_{OSS}$ | | | – | 130 | 160 | |
| Transfer Capacitance | $C_{RSS}$ | | | – | 6.0 | 8.0 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | | |
| Turn–Off Delay Time (Inductive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 10 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 5.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 6.0 | 10 | |
| Fall Time (Inductive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 10 A $R_G$ = 1.0 kΩ, L = 300 μH | $T_J$ = 25°C | – | 6.0 | 10 | |
| | | | $T_J$ = 150°C | – | 11 | 15* | |
| Turn–Off Delay Time (Resistive) | $t_{d(off)}$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω | $T_J$ = 25°C | – | 6.0 | 10 | μSec |
| | | | $T_J$ = 150°C | – | 7.0 | 10 | |
| Fall Time (Resistive) | $t_f$ | $V_{CC}$ = 300 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 46 Ω | $T_J$ = 25°C | – | 12 | 20 | |
| | | | $T_J$ = 150°C | – | 18 | 22* | |
| Turn–On Delay Time | $t_{d(on)}$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 1.5 | 2.0 | μSec |
| | | | $T_J$ = 150°C | – | 1.5 | 2.0 | |
| Rise Time | $t_r$ | $V_{CC}$ = 10 V, $I_C$ = 6.5 A $R_G$ = 1.0 kΩ, $R_L$ = 1.5 Ω | $T_J$ = 25°C | – | 4.0 | 6.0 | |
| | | | $T_J$ = 150°C | – | 5.0 | 6.0 | |

3. Pulse Test: Pulse Width ≤ 300 μS, Duty Cycle ≤ 2%.
*Maximum Value of Characteristic across Temperature Range.

## TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)

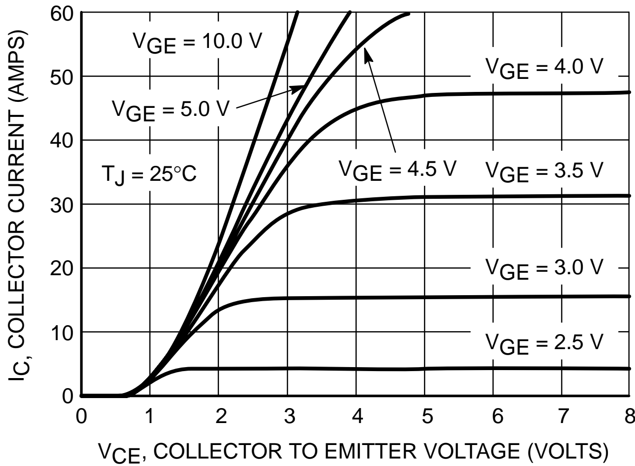



**Figure 1. Output Characteristics**

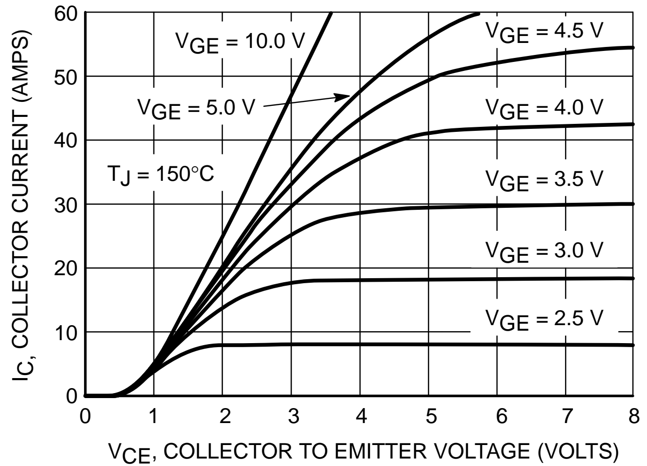



**Figure 2. Output Characteristics**

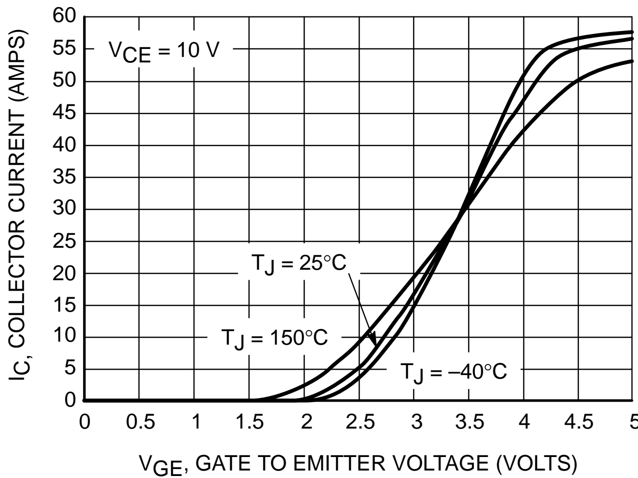



**Figure 3. Transfer Characteristics**

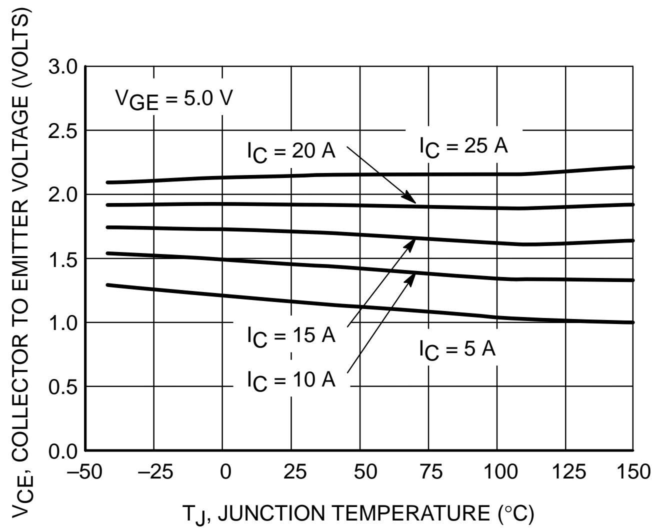



**Figure 4. Collector–to–Emitter Saturation Voltage vs. Junction Temperature**

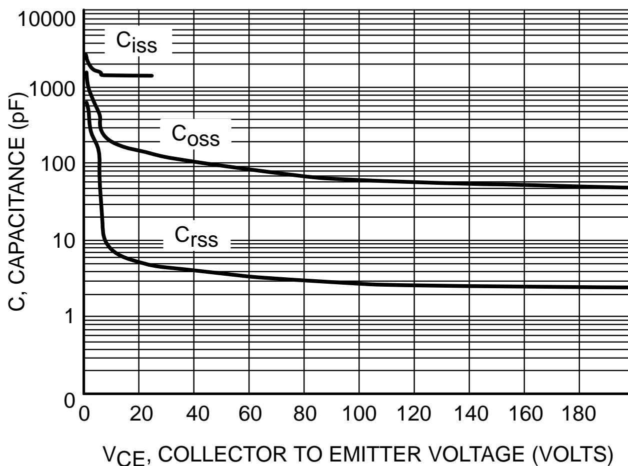



**Figure 5. Capacitance Variation**

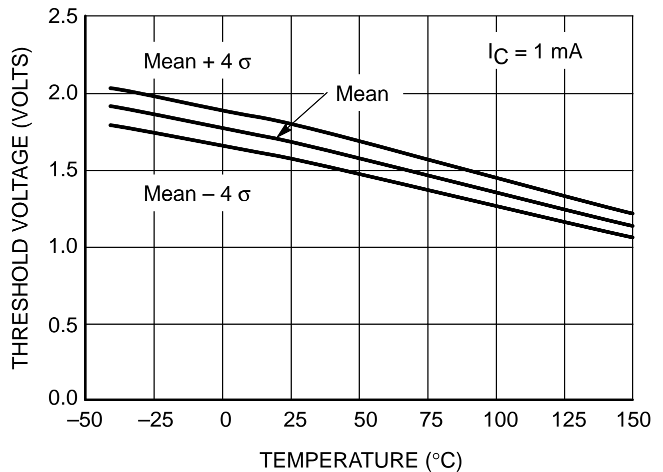



**Figure 6. Threshold Voltage vs. Temperature**

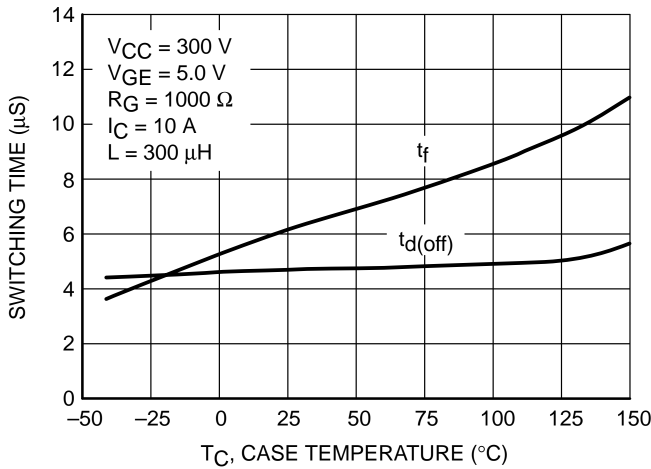



**Figure 7. Switching Speed vs. Case Temperature**

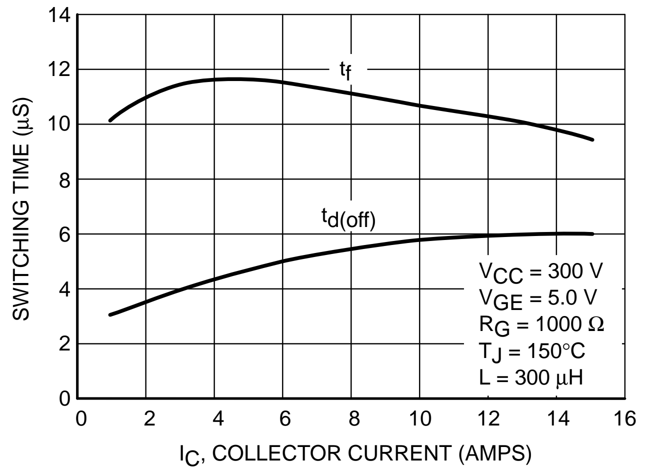



**Figure 8. Switching Speed vs. Collector Current**

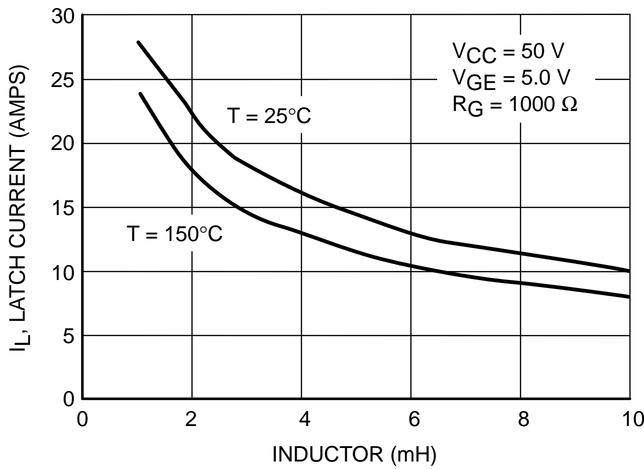



**Figure 9. Minimum Open Secondary Latch Current vs. Inductor**

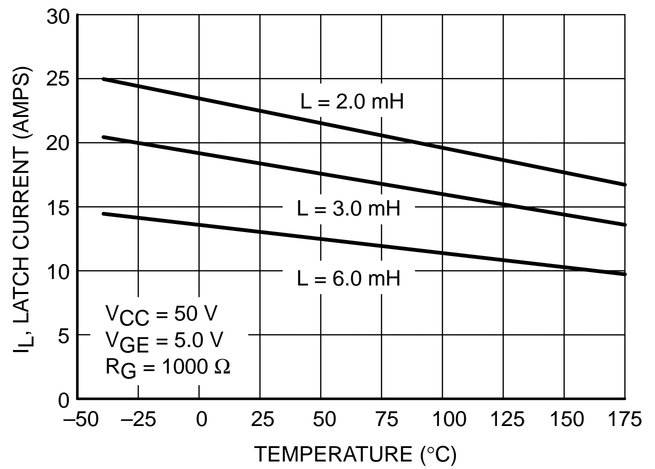



**Figure 10. Minimum Open Secondary Latch Current vs. Temperature**

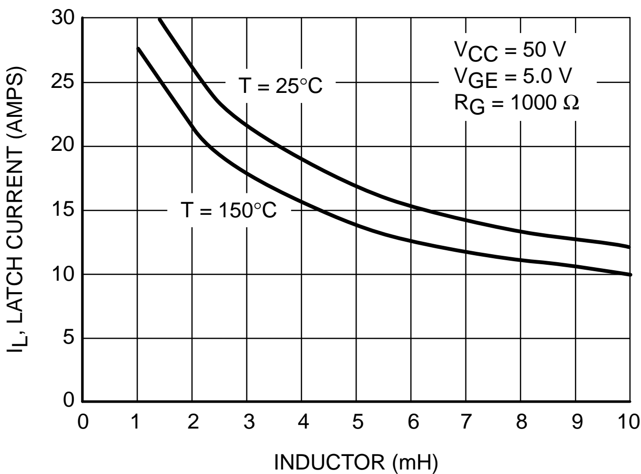



**Figure 11. Typical Open Secondary Latch vs. Inductor**

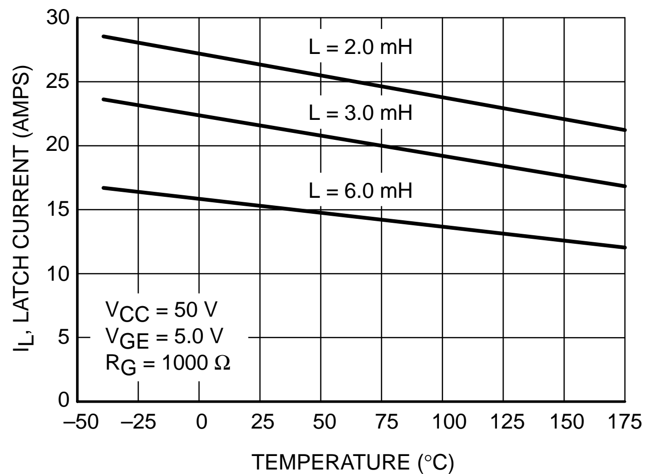



**Figure 12. Typical Open Secondary Latch vs. Temperature**

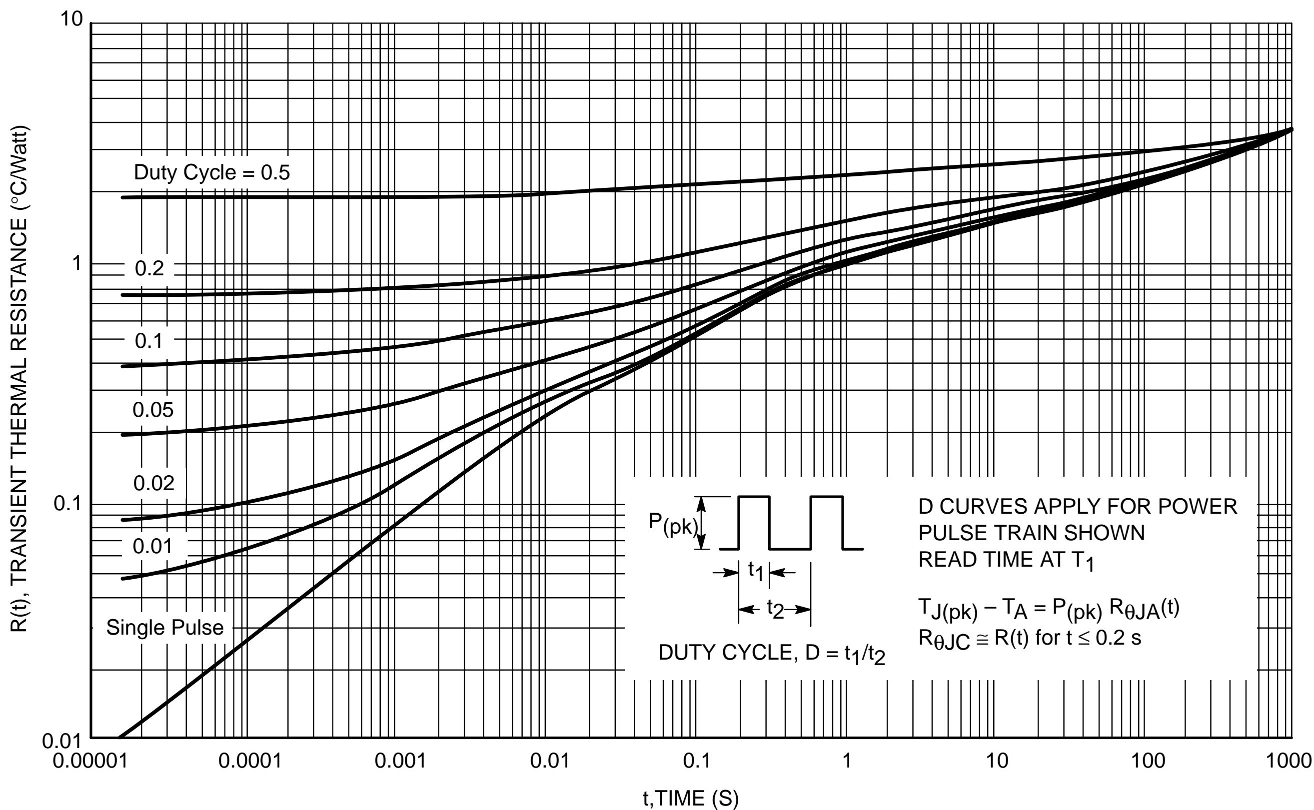



**Figure 13. Transient Thermal Resistance (Non–normalized Junction–to–Ambient mounted on fixture in Figure 14)**

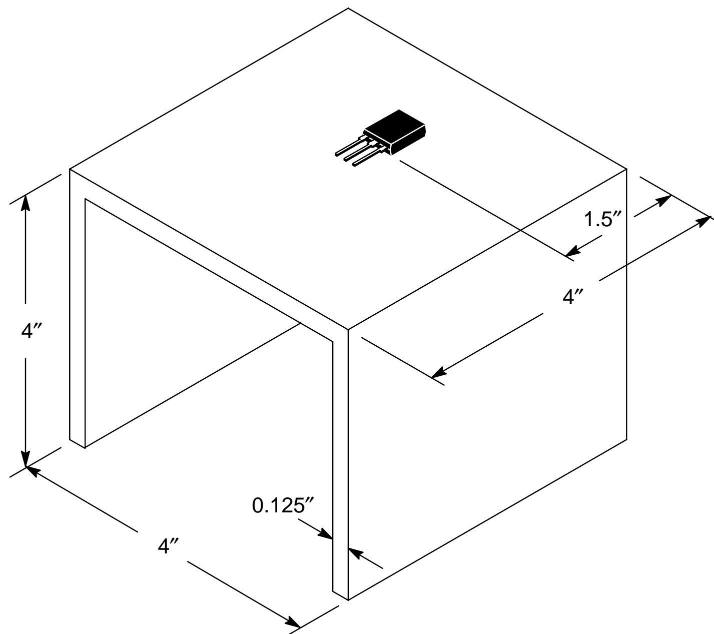



**Figure 14. Test Fixture for Transient Thermal Curve (48 square inches of 1/8″ thick aluminum)**

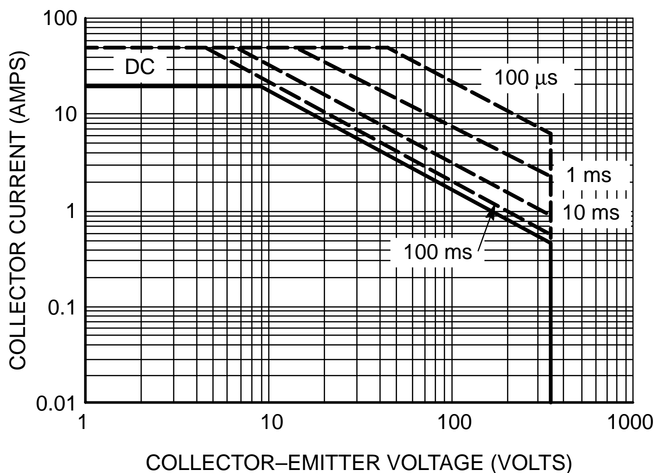



**Figure 15. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

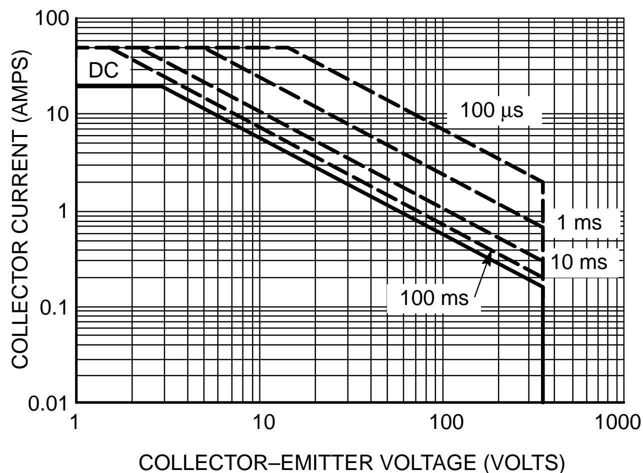



**Figure 16. Single Pulse Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

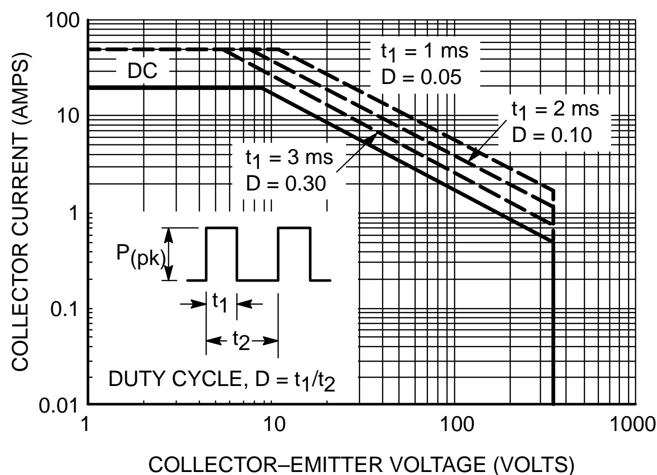



**Figure 17. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 25°C)**

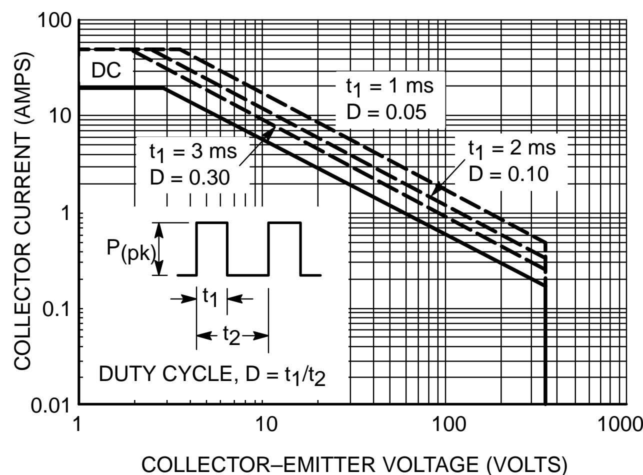



**Figure 18. Pulse Train Safe Operating Area (Mounted on an Infinite Heatsink at $T_C$ = 125°C)**

# MGSF1N02ELT1

**Preferred Device**

# Power MOSFET 750 mAmps, 20 Volts

## N–Channel SOT–23

**ON Semiconductor™**

**http://onsemi.com**

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

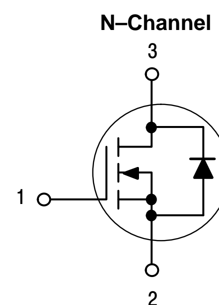
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

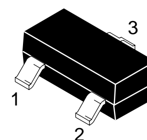
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \le 10\ \mu s$) | <br>$I_D$<br>$I_{DM}$ | <br>750<br>2000 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 400 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 300 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**750 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 85 mΩ**

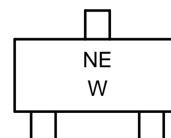
**N–Channel**




**MARKING DIAGRAM**

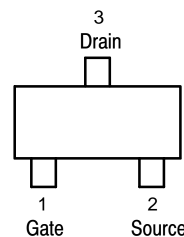



**SOT–23**
**CASE 318**
**STYLE 21**




NE = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF1N02ELT1 | SOT–23 | 3000 Tape & Reel |
| MGSF1N02ELT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Source Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±0.1 | μAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate–Source Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.5 | – | 1.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 A) ($V_{GS}$ = 2.5 Vdc, $I_D$ = 0.75 A) | | $r_{DS(on)}$ | –<br>– | –<br>– | 0.085<br>0.115 | Ohms |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc, $V_{GS}$ = 0 V, f = 1.0 Mhz) | $C_{iss}$ | – | 160 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc, $V_{GS}$ = 0 V, f = 1.0 Mhz) | $C_{oss}$ | – | 130 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc, $V_{GS}$ = 0 V, f = 1.0 Mhz) | $C_{rss}$ | – | 60 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 5 Vdc, $I_D$ = 1.0 Adc, $R_L$ = 5 Ω, $R_G$ = 6 Ω) | $t_{d(on)}$ | – | 6.0 | – | ns |
| Rise Time | | $t_r$ | – | 26 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 117 | – | |
| Fall Time | | $t_f$ | – | 105 | – | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 1.2 Adc, $V_{GS}$ = 4.0 Vdc) | $Q_T$ | – | 6500 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.6 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) ($V_{GS}$ = 0 Vdc, $I_S$ = 0.6 Adc) | | $V_{SD}$ | – | – | 1.2 | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

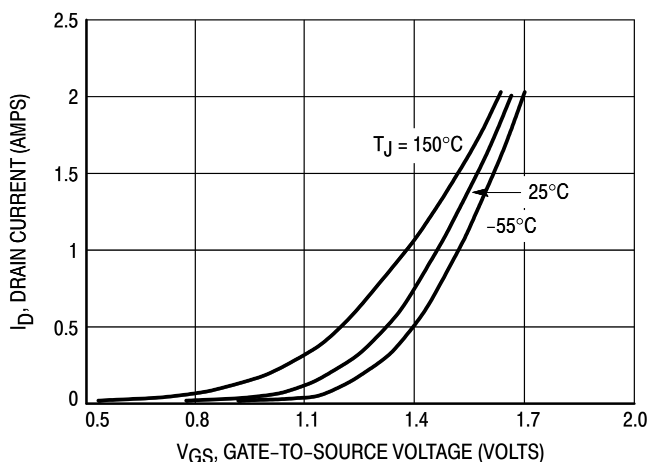



**Figure 1. Transfer Characteristics**

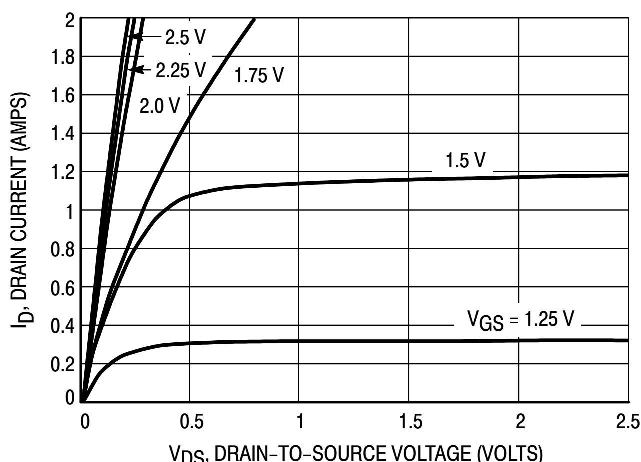



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

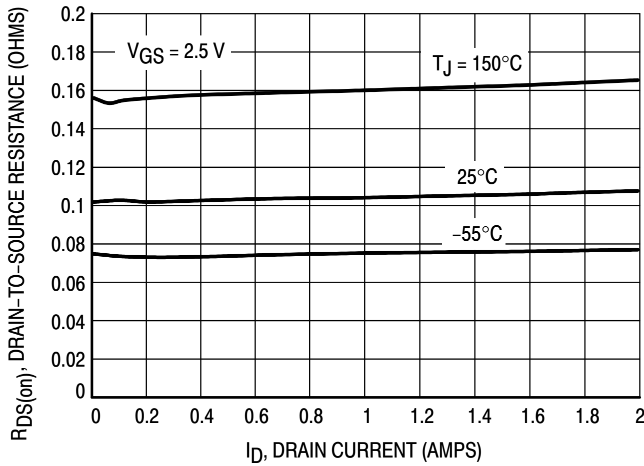



**Figure 3. On–Resistance versus Drain Current**

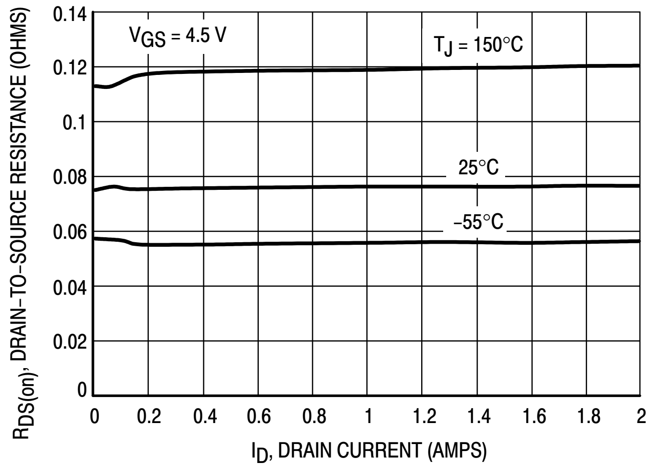



**Figure 4. On–Resistance versus Drain Current**

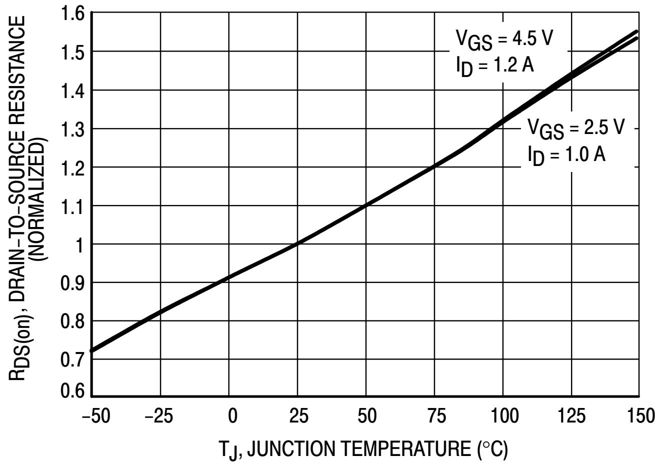



**Figure 5. On–Resistance Variation Over Temperature**

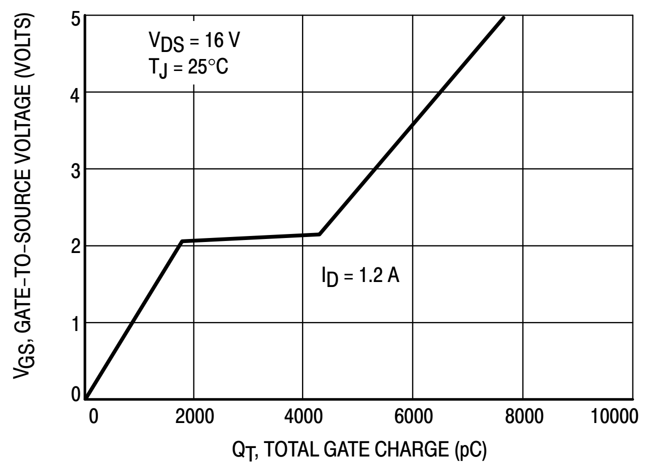



**Figure 6. Gate Charge**

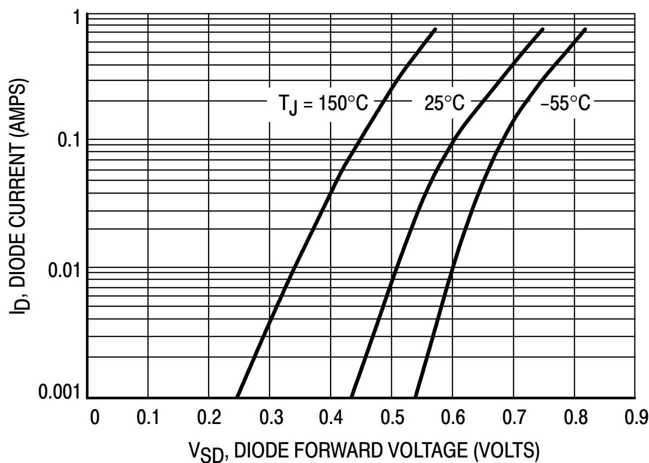



**Figure 7. Body Diode Forward Voltage**

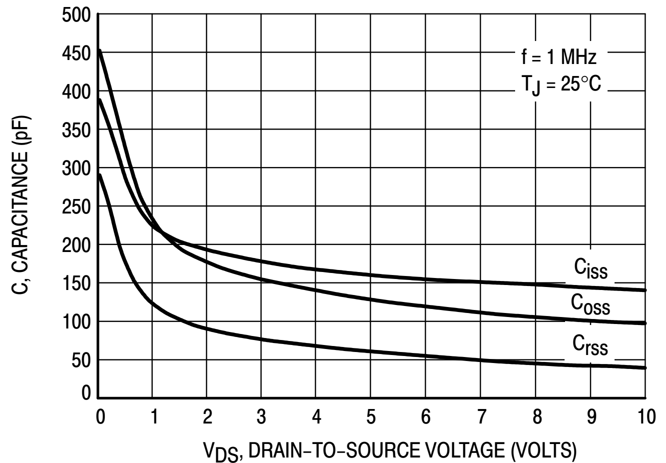
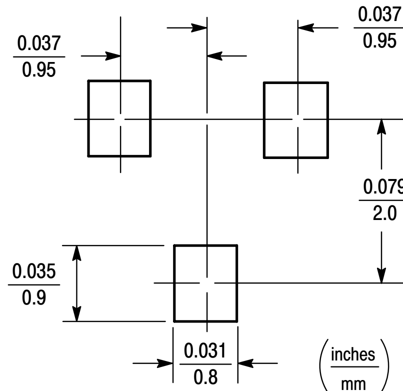



**Figure 8. Capacitance Variation**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 416 milliwatts.

$$P_D = \frac{150°C - 25°C}{300°C/W} = 416 \text{ milliwatts}$$

The 300°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 416 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF1N02LT1

**Preferred Device**

# Power MOSFET 750 mAmps, 20 Volts

## N–Channel SOT–23

**ON Semiconductor™**

**http://onsemi.com**

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

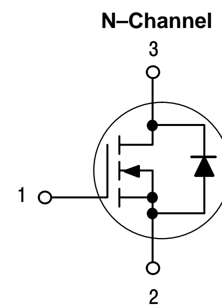
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**750 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ**

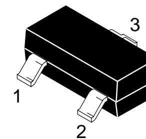
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \le$ 10 µs) | $I_D$<br>$I_{DM}$ | 750<br>2000 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 400 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 300 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

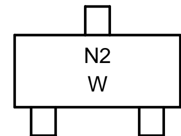
**N–Channel**




**MARKING DIAGRAM**

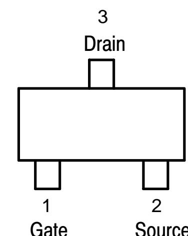



**SOT–23**
**CASE 318**
**STYLE 21**




N2 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF1N02LT1 | SOT–23 | 3000 Tape & Reel |
| MGSF1N02LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 1.2 Adc) | | | – | 0.075 | 0.090 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | | – | 0.115 | 0.130 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{iss}$ | – | 125 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{oss}$ | – | 120 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc) | $C_{rss}$ | – | 45 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 1.0 Adc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge (See Figure 6) | | $Q_T$ | – | 6000 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.6 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | 0.8 | – | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

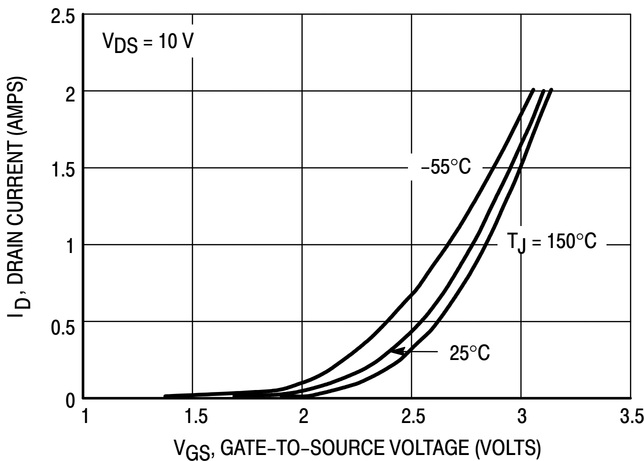



**Figure 1. Transfer Characteristics**

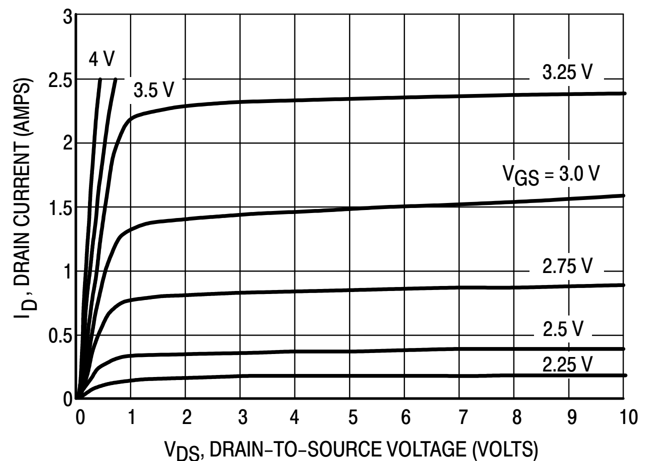



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

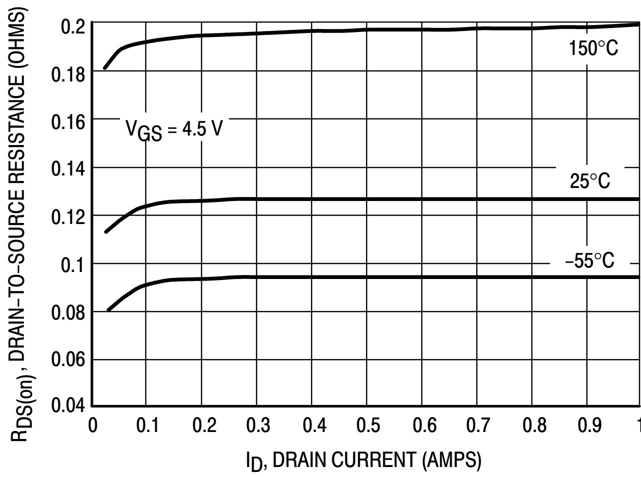
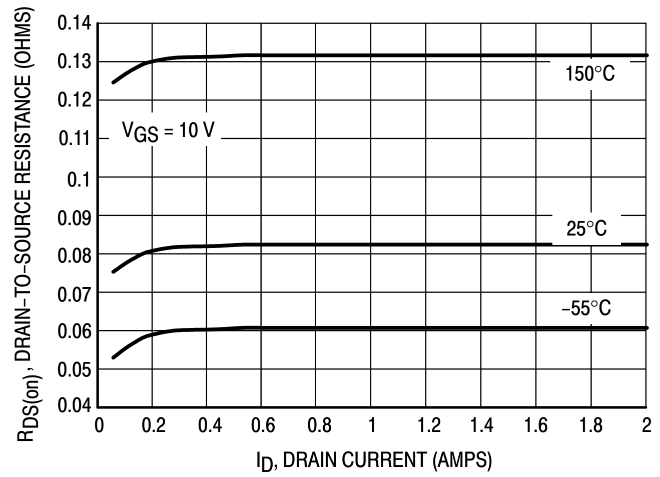



**Figure 3. On−Resistance versus Drain Current**

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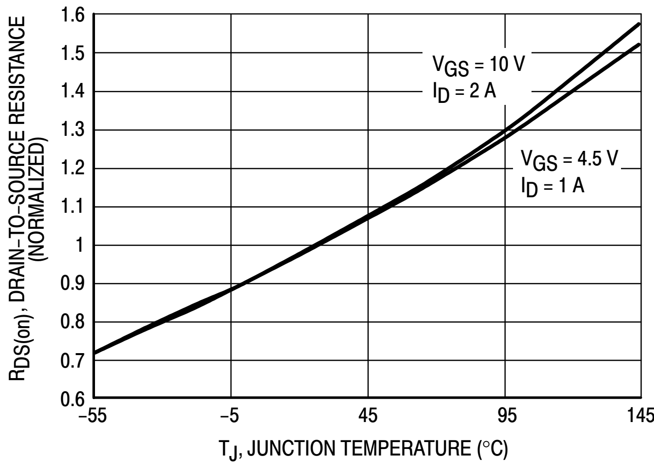


**Figure 5. On−Resistance Variation with Temperature**

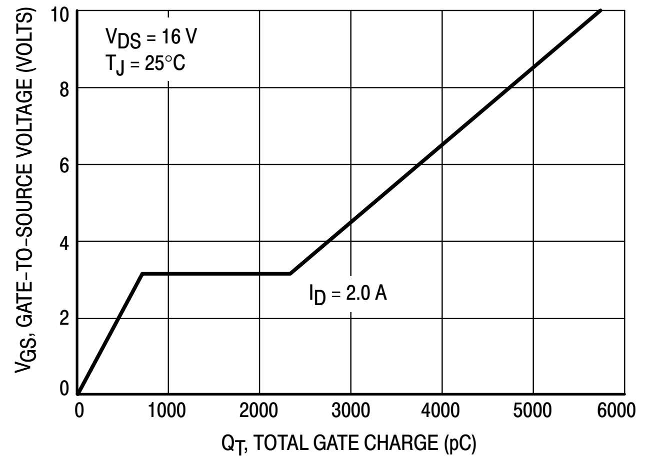


**Figure 6. Gate Charge**

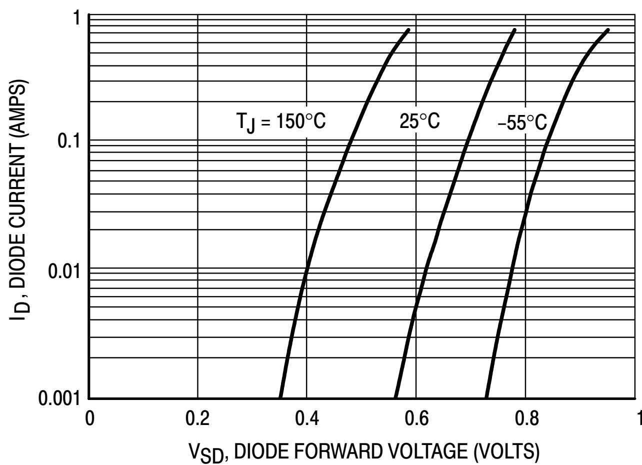


**Figure 7. Body Diode Forward Voltage**

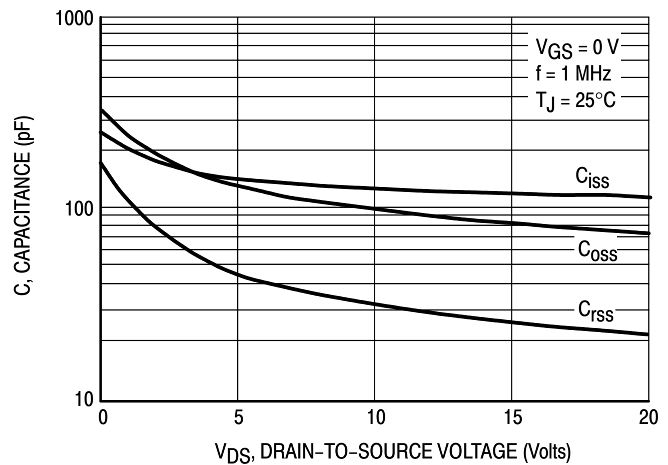


**Figure 8. Capacitance**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

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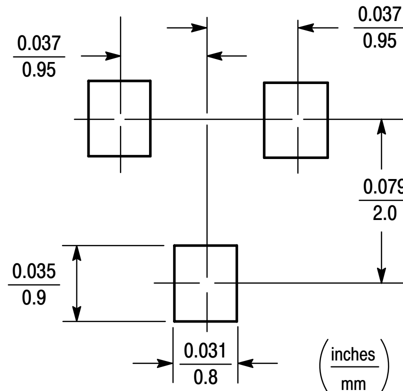


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The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 416 milliwatts.

$$P_D = \frac{150°C - 25°C}{300°C/W} = 416 \text{ milliwatts}$$

The 300°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 416 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF1N03LT1

**Preferred Device**

# Power MOSFET 750 mAmps, 30 Volts

## N–Channel SOT–23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

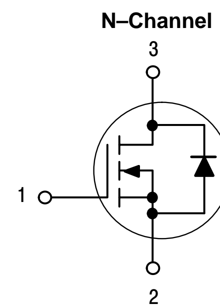
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \le$ 10 μs) | <br>$I_D$<br>$I_{DM}$ | <br>750<br>2000 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 400 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 300 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor**™

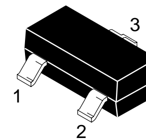
http://onsemi.com

**750 mAMPS**
**30 VOLTS**
**$R_{DS(on)}$ = 100 mΩ**

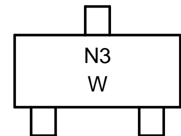
**N–Channel**




**MARKING DIAGRAM**

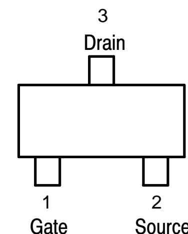



**SOT–23**
**CASE 318**
**STYLE 21**




N3 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF1N03LT1 | SOT–23 | 3000 Tape & Reel |
| MGSF1N03LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 1.2 Adc) | | | – | 0.08 | 0.10 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | | – | 0.125 | 0.145 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{iss}$ | – | 140 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{oss}$ | – | 100 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc) | $C_{rss}$ | – | 40 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 1.0 Adc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge (See Figure 6) | | $Q_T$ | – | 6000 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.6 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | 0.8 | – | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

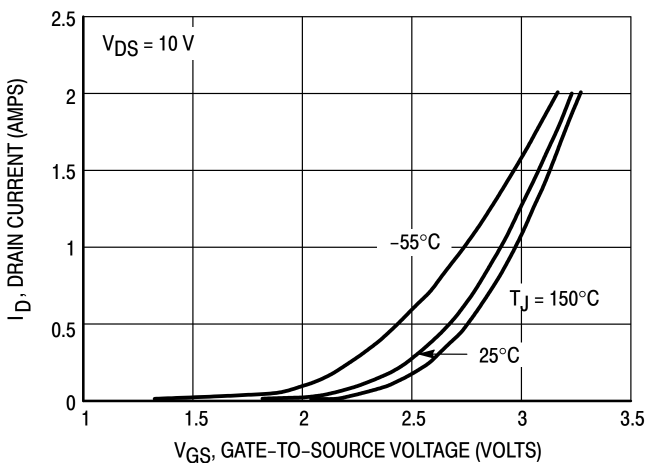



**Figure 1. Transfer Characteristics**

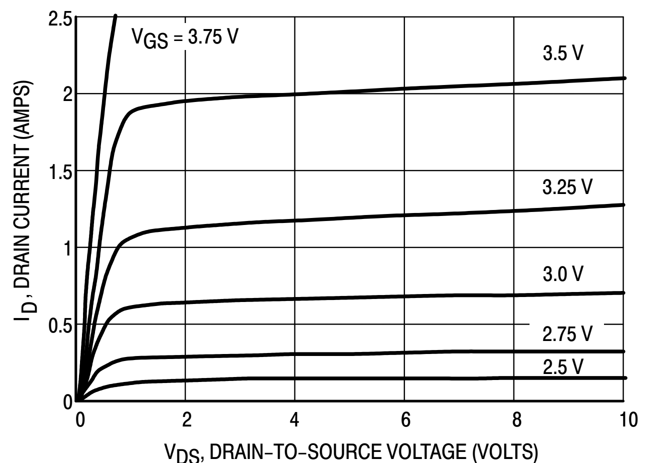



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

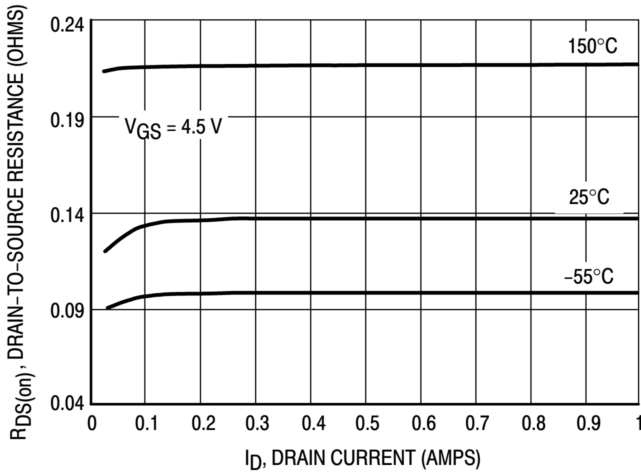
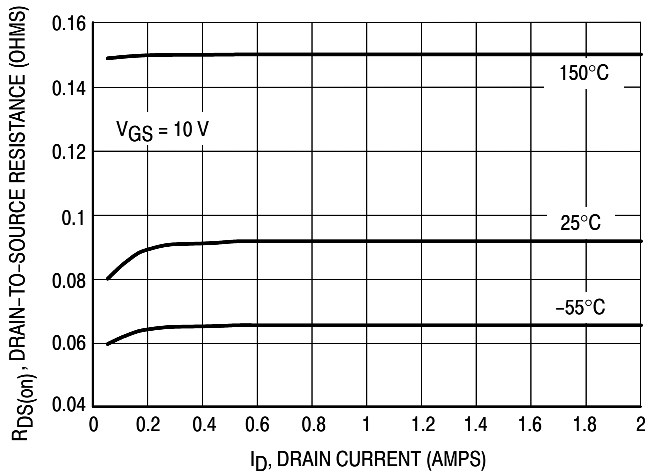



**Figure 3. On−Resistance versus Drain Current**

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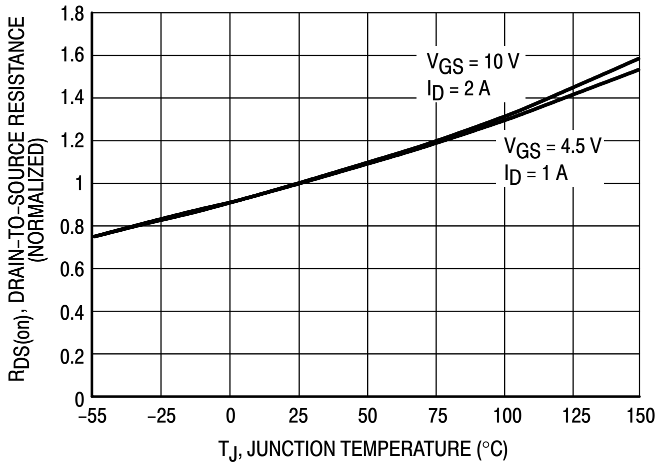


**Figure 5. On−Resistance Variation with Temperature**

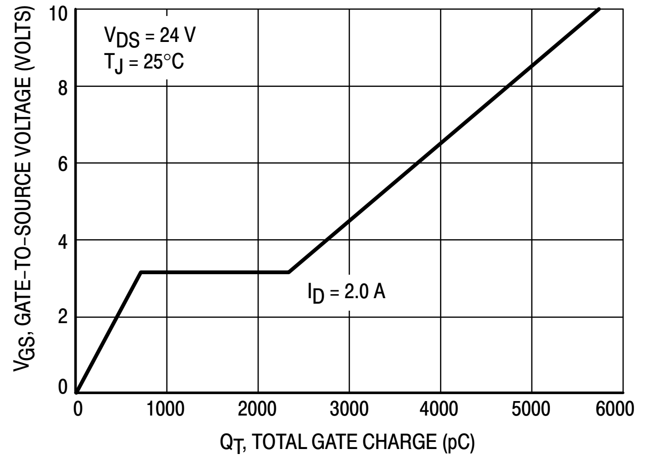


**Figure 6. Gate Charge**

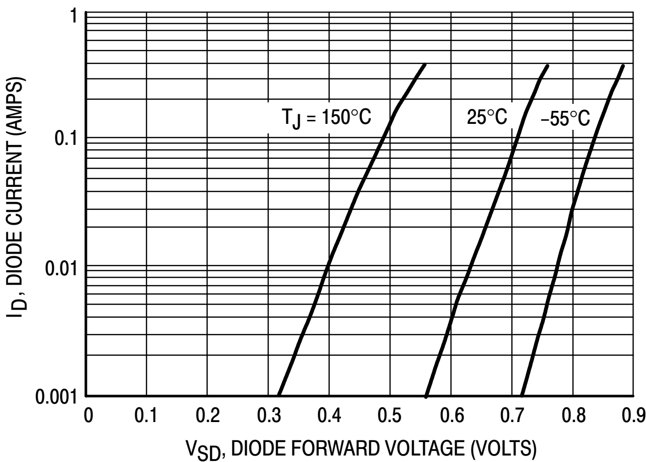


**Figure 7. Body Diode Forward Voltage**

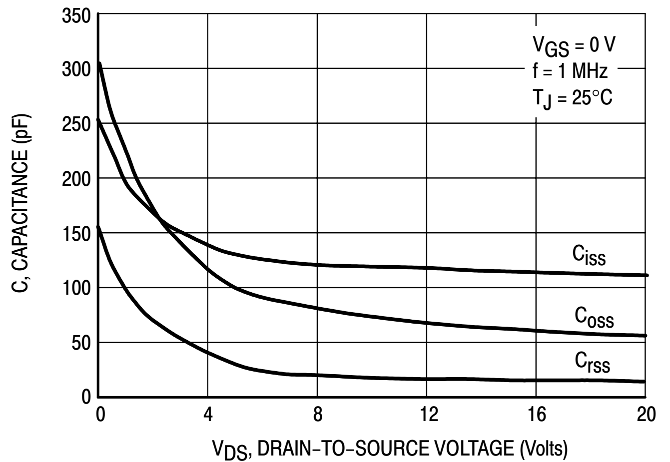


**Figure 8. Capacitance**

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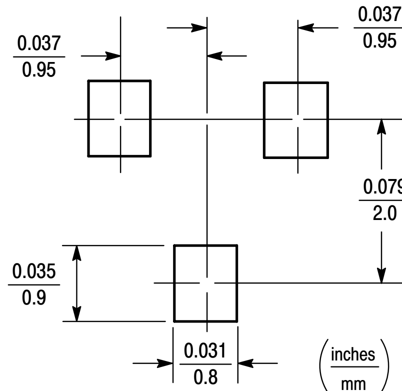


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$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 416 milliwatts.

$$P_D = \frac{150°C - 25°C}{300°C/W} = 416 \text{ milliwatts}$$

The 300°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 416 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF1P02ELT1

**Preferred Device**

# Power MOSFET 750 mAmps, 20 Volts

## P–Channel SOT–23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

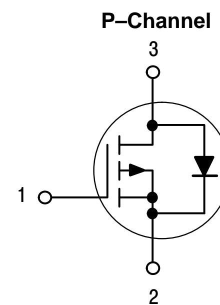
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \leq 10\ \mu s$) | <br>$I_D$<br>$I_{DM}$ | <br>750<br>2000 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 400 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 300 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

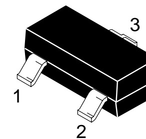
**http://onsemi.com**

**750 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 260 mΩ**

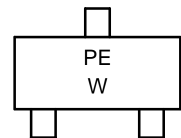
**P–Channel**




**MARKING DIAGRAM**

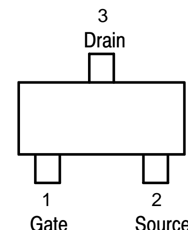



**SOT–23**
**CASE 318**
**STYLE 21**




PE = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF1P02ELT1 | SOT–23 | 3000 Tape & Reel |
| MGSF1P02ELT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.7 | 1.0 | 1.25 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 0.75 Adc) | | | – | 0.22 | 0.26 | |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 0.5 Adc) | | | – | 0.40 | 0.50 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{iss}$ | – | 140 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{oss}$ | – | 130 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc) | $C_{rss}$ | – | 50 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 5 Vdc, $I_D$ = 1.0 Adc, $R_L$ = 5 Ω, $R_G$ = 6 Ω) | $t_{d(on)}$ | – | 9.5 | – | ns |
| Rise Time | | $t_r$ | – | 32 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 200 | – | |
| Fall Time | | $t_f$ | – | 200 | – | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 1.5 Adc, $V_{GS}$ = 4.0 Vdc) | $Q_T$ | – | 5500 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.6 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) ($V_{GS}$ = 0 Vdc, $I_S$ = 0.6 Adc) | | $V_{SD}$ | – | – | 1.0 | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

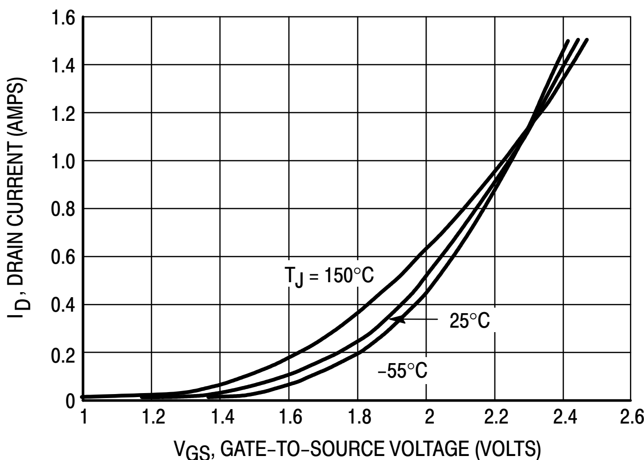



**Figure 1. Transfer Characteristics**

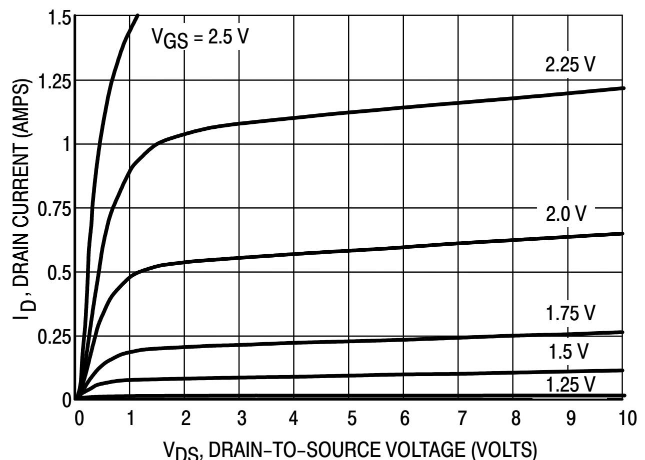



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

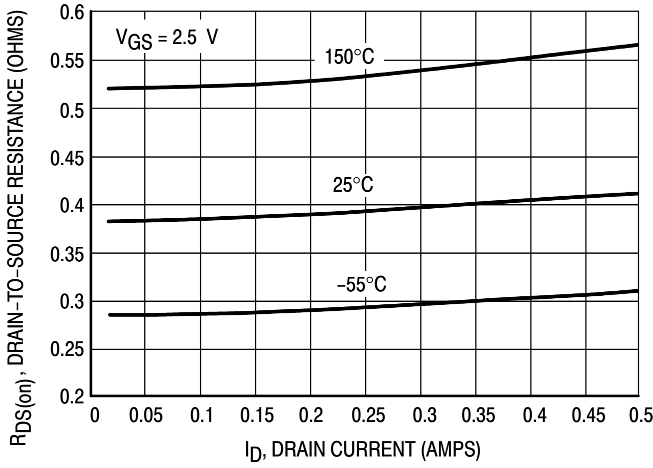



**Figure 3. On−Resistance versus Drain Current**

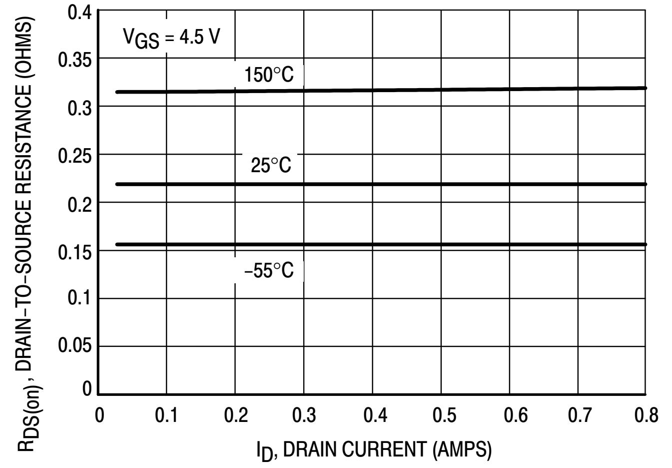



**Figure 4. On−Resistance versus Drain Current**

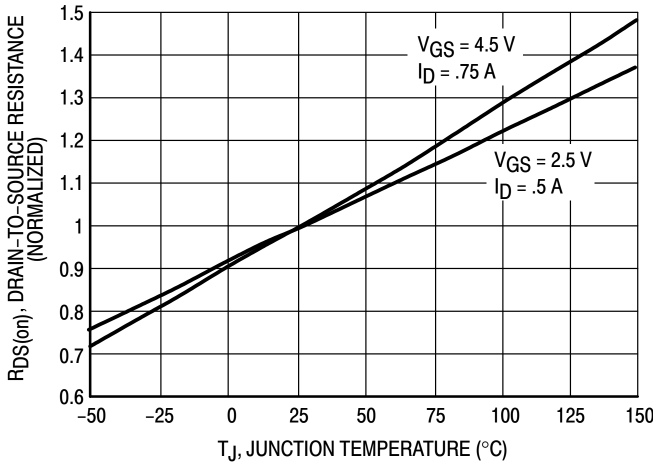



**Figure 5. On−Resistance Variation with Temperature**

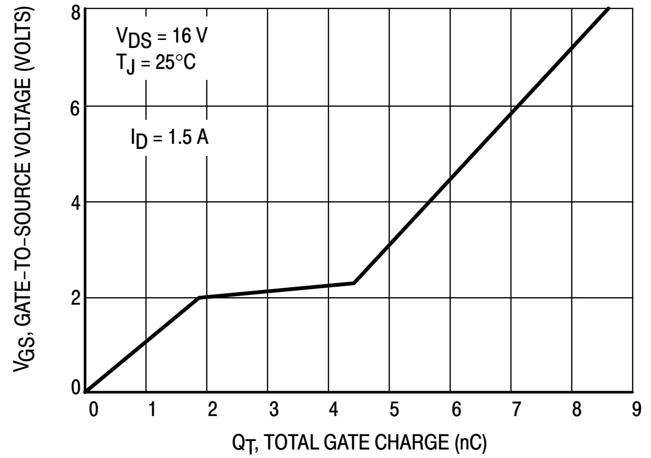



**Figure 6. Gate Charge**

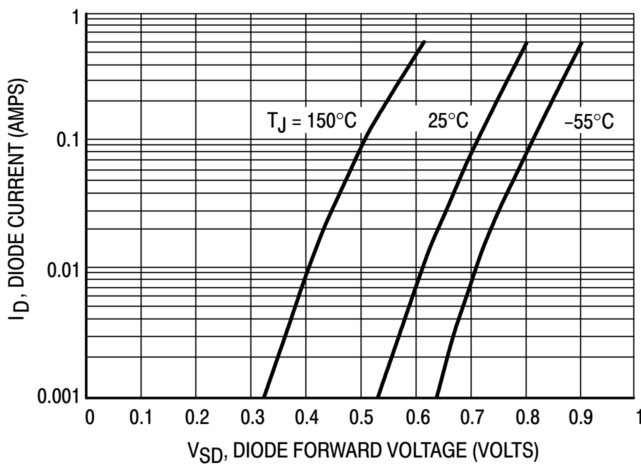



**Figure 7. Body Diode Forward Voltage**

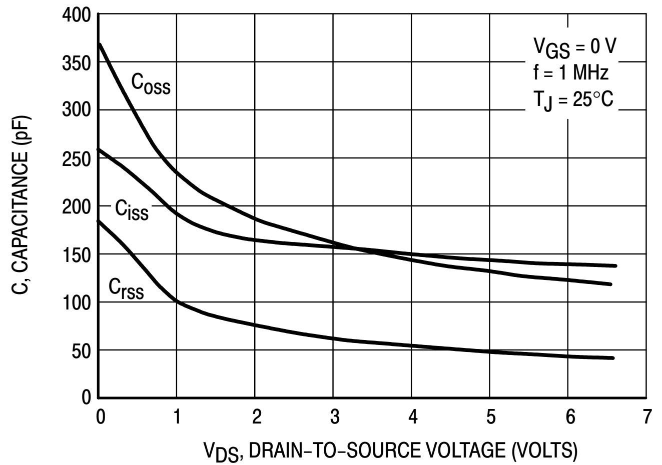
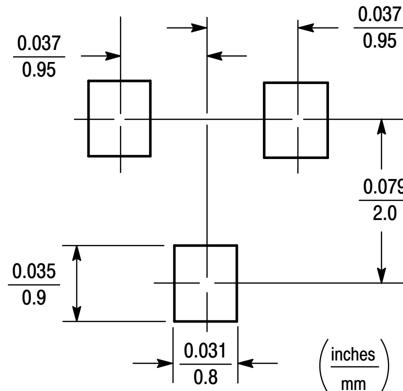



**Figure 8. Capacitance Variation**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 416 milliwatts.

$$P_D = \frac{150°C - 25°C}{300°C/W} = 416 \text{ milliwatts}$$

The 300°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 416 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF1P02LT1

**Preferred Device**

# Power MOSFET 750 mAmps, 20 Volts

## P–Channel SOT–23

**ON Semiconductor™**

**http://onsemi.com**

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in space sensitive power management circuitry. Typical applications are dc–dc converters and power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

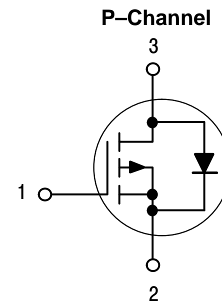
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**750 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 350 mΩ**

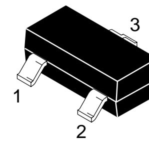
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \leq$ 10 µs) | <br>$I_D$<br>$I_{DM}$ | <br>750<br>2000 | mA |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 400 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 300 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

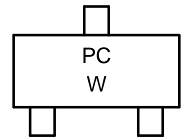
**P–Channel**




**MARKING DIAGRAM**

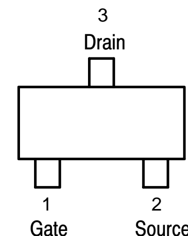



**SOT–23**
**CASE 318**
**STYLE 21**




PC = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF1P02LT1 | SOT–23 | 3000 Tape & Reel |
| MGSF1P02LT3 | SOT–23 | 10,000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc) | | | – | 0.235 | 0.350 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 0.75 Adc) | | | – | 0.375 | 0.500 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{iss}$ | – | 130 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 Vdc) | $C_{oss}$ | – | 120 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 Vdc) | $C_{rss}$ | – | 60 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 1.0 Adc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge (See Figure 6) | | $Q_T$ | – | 6000 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.6 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | 1.5 | – | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

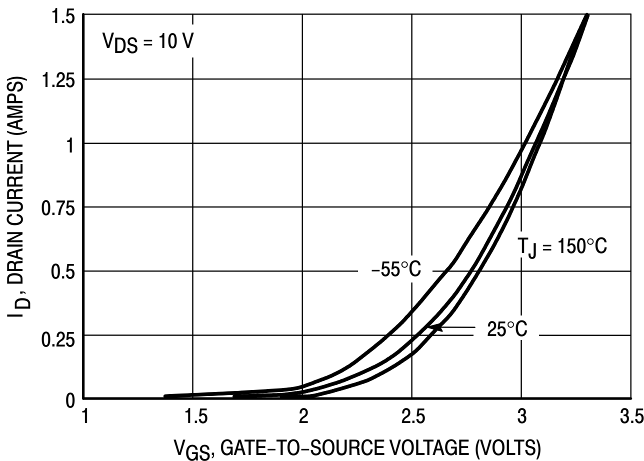



**Figure 1. Transfer Characteristics**

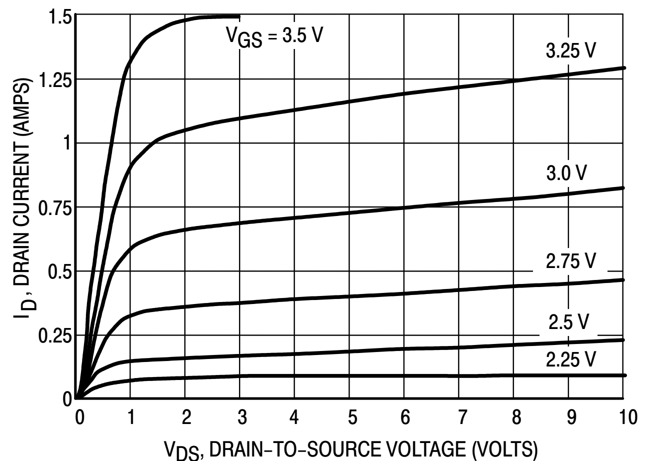



**Figure 2. On–Region Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

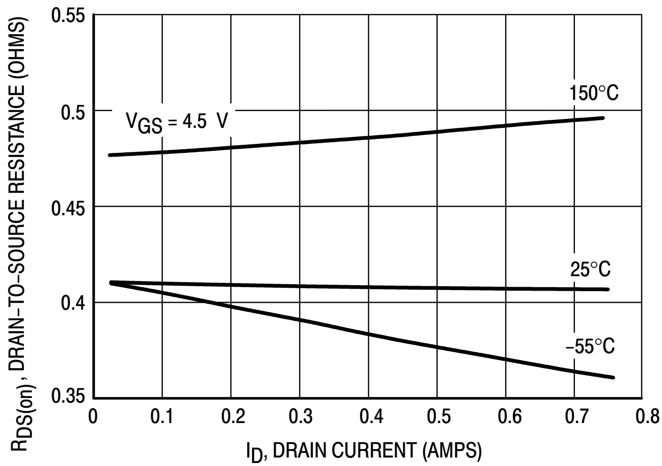



**Figure 3. On−Resistance versus Drain Current**

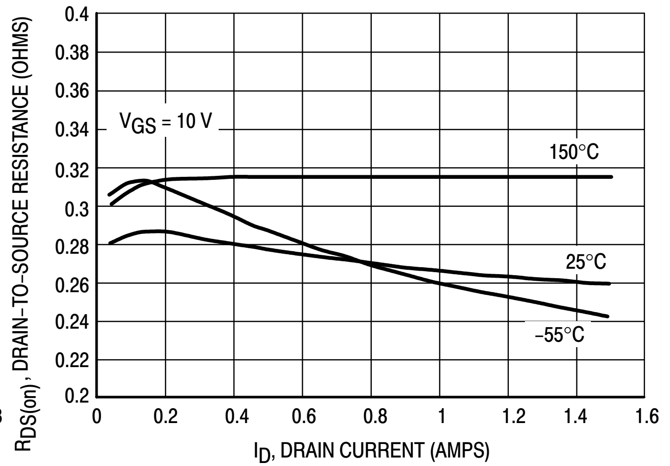



**Figure 4. On−Resistance versus Drain Current**

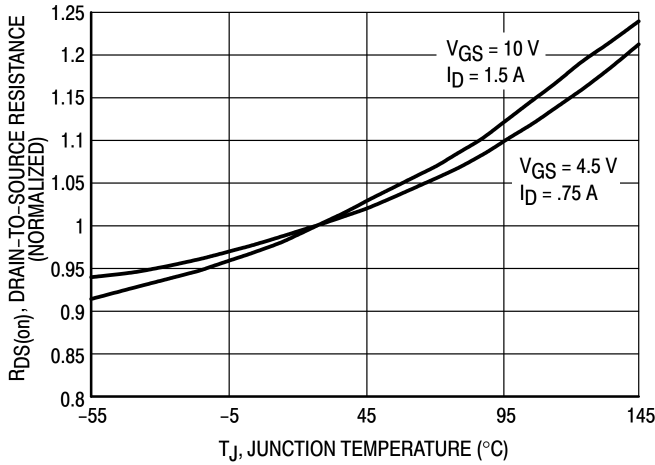



**Figure 5. On−Resistance Variation with Temperature**

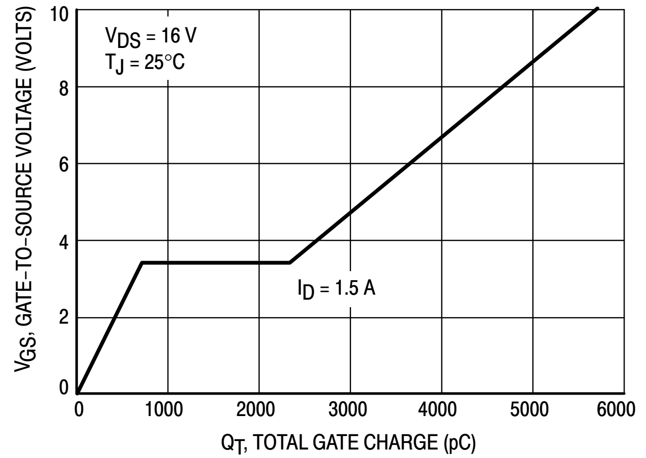



**Figure 6. Gate Charge**

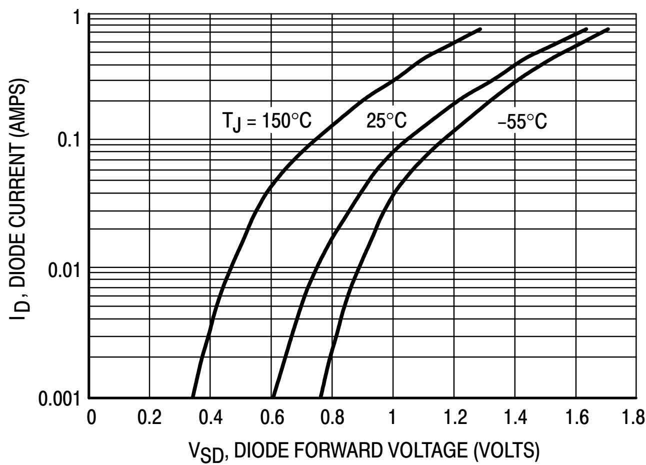



**Figure 7. Body Diode Forward Voltage**

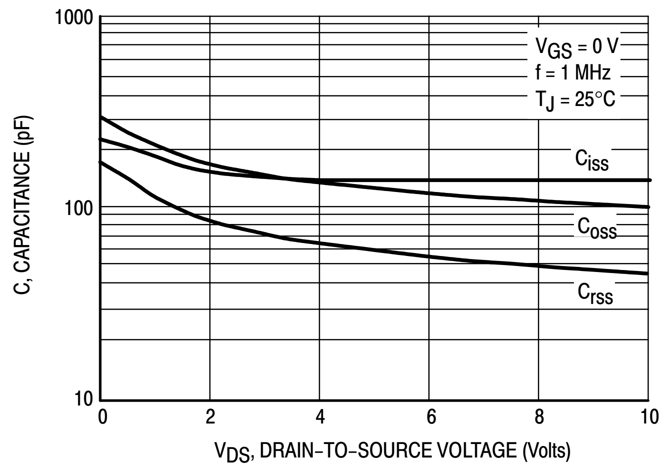
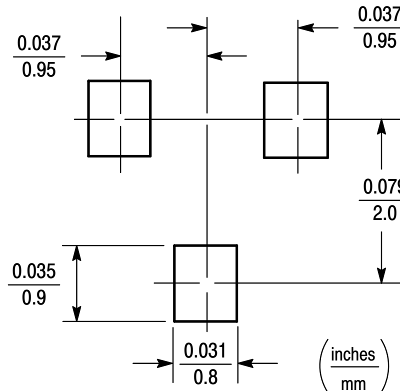



**Figure 8. Capacitance**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 416 milliwatts.

$$P_D = \frac{150°C - 25°C}{300°C/W} = 416 \text{ milliwatts}$$

The 300°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 416 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF2P02HD

*Product Preview*

## Power MOSFET 2 Amps, 20 Volts

### P–Channel TSOP–6

This device represents a series of Power MOSFETs which are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Miniature TSOP–6 Surface Mount Package – Saves Board Space
- Low Profile for Thin Applications such as PCMCIA Cards
- Very Low $R_{DS(on)}$ Provides Higher Efficiency and Expands Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperatures
- Avalanche Energy Specified
- Package Mounting Information Provided

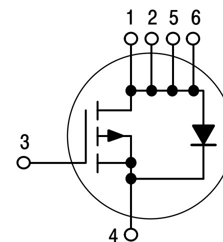
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

ON Semiconductor™

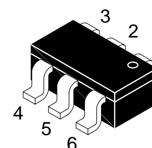
http://onsemi.com

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 175 mΩ**

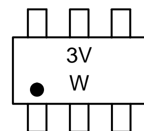
**P–Channel**




**MARKING DIAGRAM**

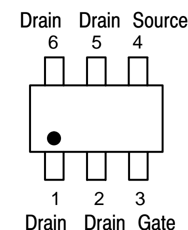



**TSOP–6**
**CASE 318G**
**STYLE 1**




3V = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF2P02HDT1 | TSOP–6 | 3000 Tape & Reel |
| MGSF2P02HDT3 | TSOP–6 | 10,000 Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
| --- | --- | --- | --- |
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | V |
| Gate–to–Source Voltage | $V_{GS}$ | ±9 | V |
| Drain Current – Continuous<br>– Single Pulse ($t_p \leq$ 10 μs)<br>Total Power Dissipation @ $T_C$ = 25°C<br>Total Power Dissipation @ $T_C$ = 85°C<br>Thermal Resistance – Junction to Ambient (Note 1.) | $I_D$<br>$I_{DM}$<br>$P_D$<br>$P_D$<br>$R_{\theta JA}$ | 1.3<br>10<br>400<br>210<br>312 | A<br><br>mW<br>mW<br>°C/W |
| Drain Current – Continuous<br>– Single Pulse ($t_p \leq$ 10 μs)<br>Total Power Dissipation @ $T_C$ = 25°C<br>Total Power Dissipation @ $T_C$ = 85°C<br>Thermal Resistance – Junction to Ambient (Note 2.) | $I_D$<br>$I_{DM}$<br>$P_D$<br>$P_D$<br>$R_{\theta JA}$ | 2.9<br>15<br>2.0<br>1.0<br>62.5 | A<br><br>W<br>W<br>°C/W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to<br>150 | °C |
| Single Pulse Drain Source Avalanche Energy $V_{DD}$ = 20 V, $V_{GS}$ = 4.5 Vpk,<br>$I_L$ = 3.6 Apk, L = 25 mH, $R_G$ = 25 Ω | $E_{AS}$ | 160 | mJ |

**THERMAL CHARACTERISTICS**

| | | | |
| --- | --- | --- | --- |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds | $T_L$ | 260 | °C |

1. Minimum FR–4 or G–10 PCB, Operating to Steady State.
2. Mounted onto a 2″ square FR–4 Board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Operating time ≤5 seconds.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | µA |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–to–Source Leakage Current ($V_{GS}$ = ±9.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | | $V_{GS(th)}$ | 0.7 | 0.95 | 1.4 | Vdc |
| Temperature Coefficient (Negative) | | | – | 2.2 | – | mV/°C |
| Drain–to–Source On–Voltage ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.3 Adc) | | $R_{DS(on)}$ | – | 145 | 175 | mΩ |
| (VGS = 2.7 Vdc, $I_D$ = 0.8 Adc) | | | – | 220 | 280 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 0.6 Adc) | | $g_{FS}$ | 1.3 | 2.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 225 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 150 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 60 | – | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 1.2 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | – | nsec |
| Rise Time | | $t_r$ | – | 27 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 60 | – | |
| Fall Time | | $t_f$ | – | 72 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 0.6 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | – | |
| Rise Time | | $t_r$ | – | 94 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 49 | – | |
| Fall Time | | $t_f$ | – | 76 | – | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 1.2 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 5.3 | 7.5 | nC |
| | | $Q_1$ | – | 0.7 | – | |
| | | $Q_2$ | – | 2.6 | – | |
| | | $Q_3$ | – | 1.9 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.2 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.89 | 1.1 | Vdc |
| | | | – | 0.72 | – | |
| Reverse Recovery Time | ($I_S$ = 1.2 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 86 | – | nsec |
| | | $t_a$ | – | 27 | – | |
| | | $t_b$ | – | 59 | – | |
| | | $Q_{RR}$ | – | 0.115 | – | µC |

NOTE: Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

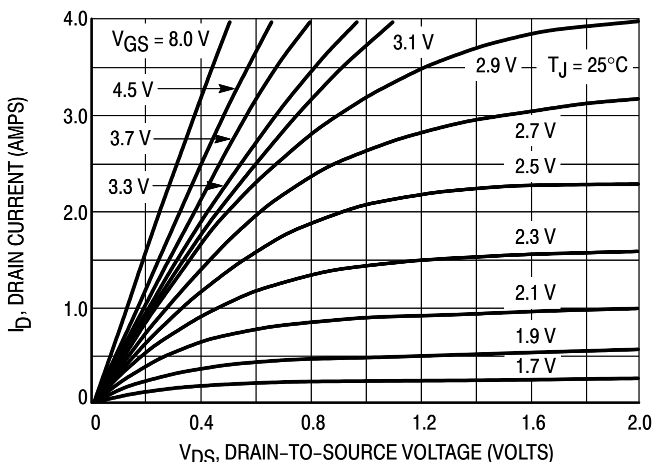



**Figure 1. On–Region Characteristics**

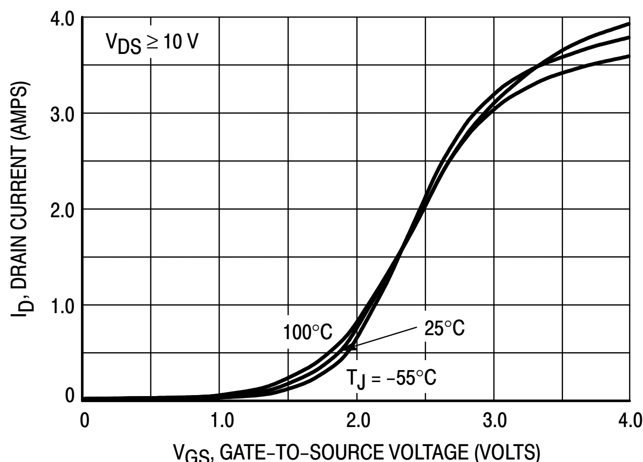



**Figure 2. Transfer Characteristics**

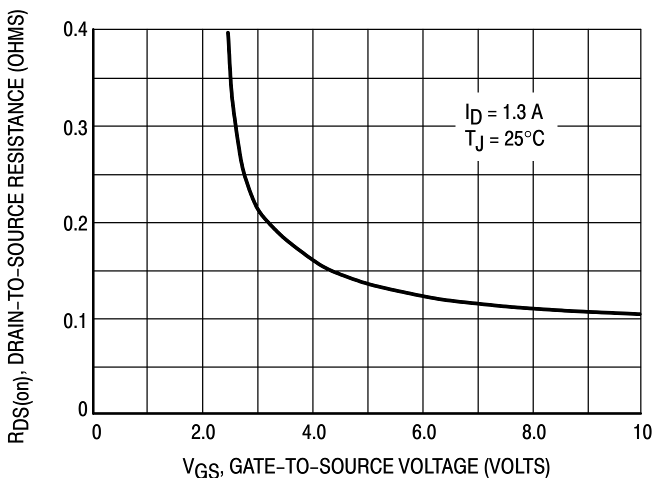



**Figure 3. On–Resistance versus Drain Current**

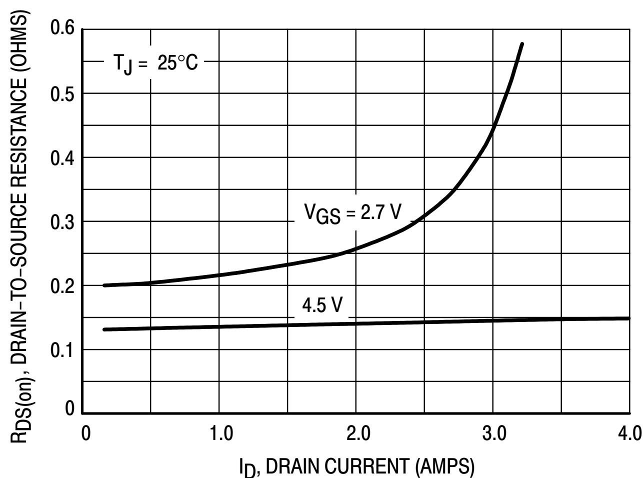



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

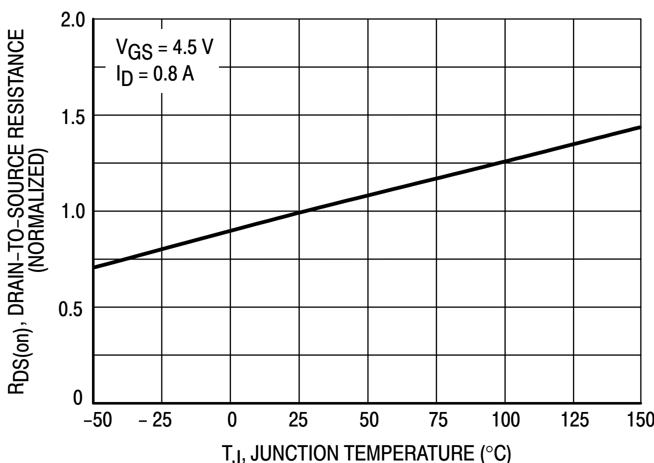



**Figure 5. On–Resistance versus Temperature**

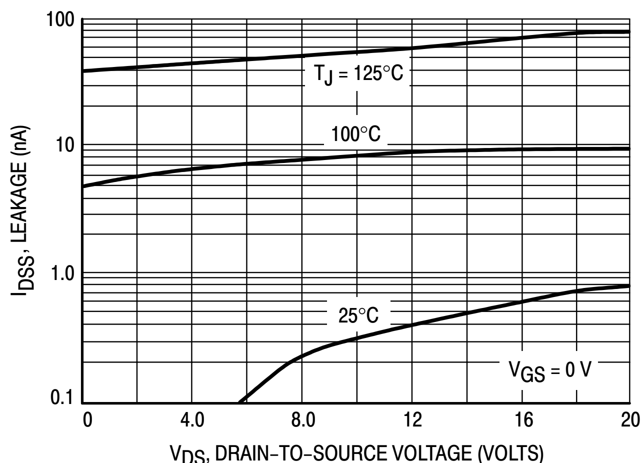



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

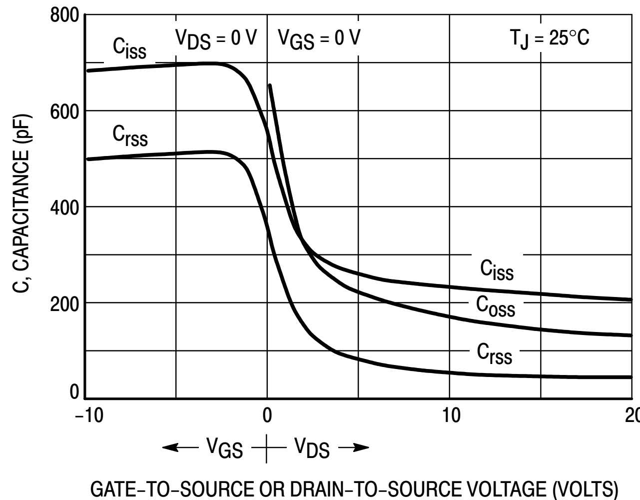



**Figure 7. Capacitance Variation**

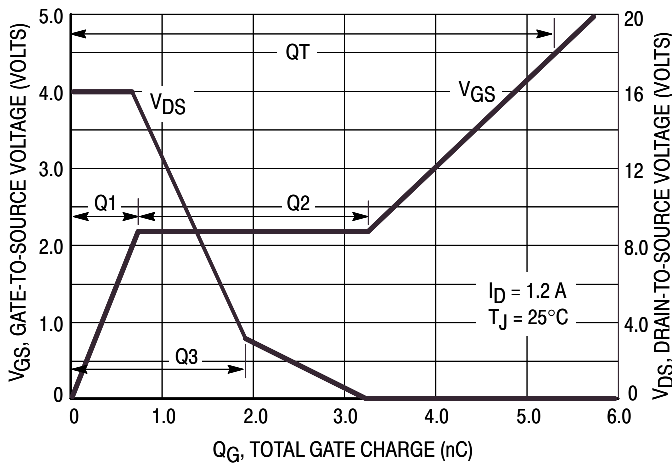



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

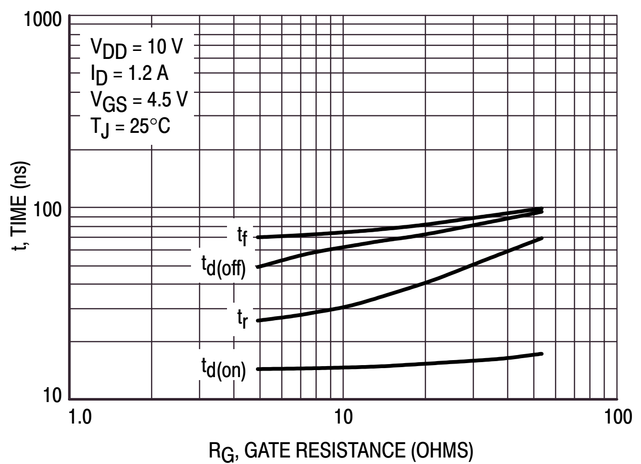



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

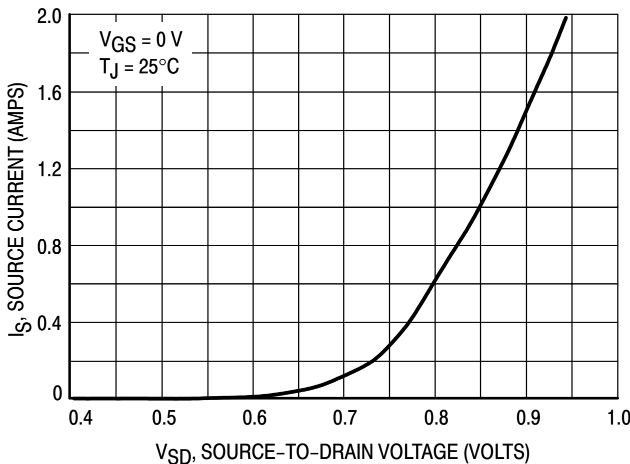



**Figure 10. Diode Forward Voltage versus Current**

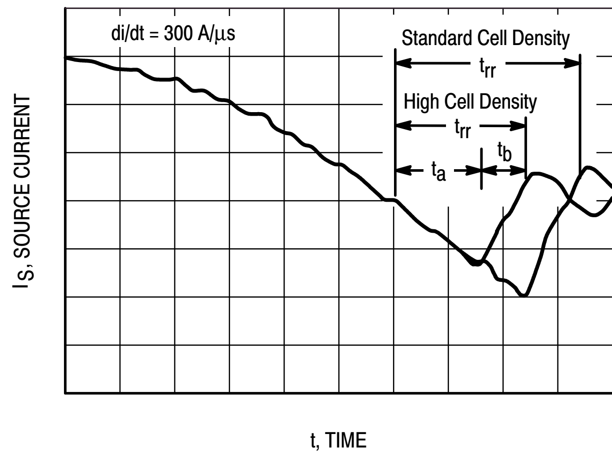



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## TYPICAL ELECTRICAL CHARACTERISTICS

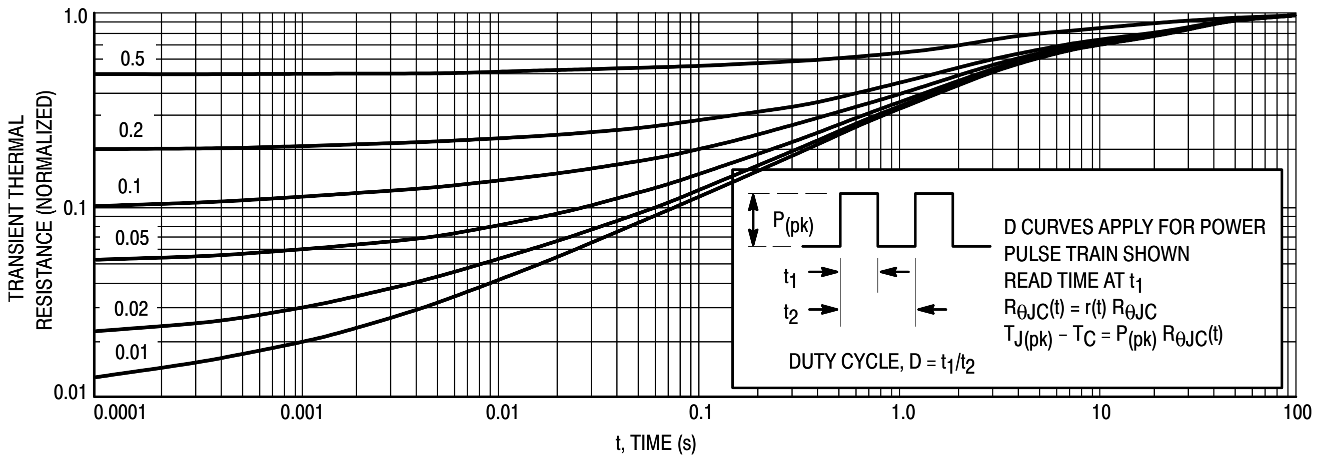



**Figure 12. Thermal Response**

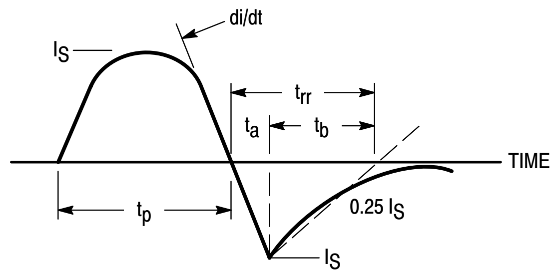
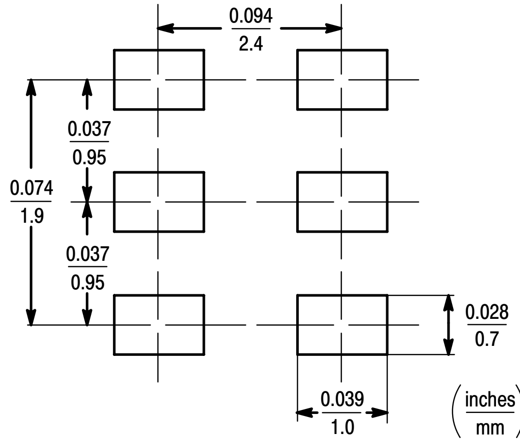



**Figure 13. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## TSOP–6 POWER DISSIPATION

The power dissipation of the TSOP–6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the TSOP–6 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 400 milliwatts.

$$P_D = \frac{150°C - 25°C}{312°C/W} = 400 \text{ milliwatts}$$

The 312°C/W for the TSOP–6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 400 milliwatts. There are other alternatives to achieving higher power dissipation from the TSOP–6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF3442VT1

Preferred Device

# Power MOSFET 4 Amps, 20 Volts

## N–Channel TSOP–6

**ON Semiconductor™**

http://onsemi.com

**4 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 70 mΩ**

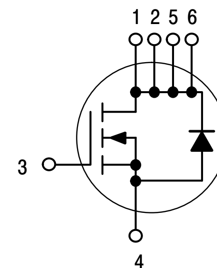
These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TSOP–6 Surface Mount Package Saves Board Space

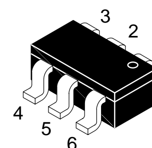
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p \le 10\ \mu s$) | <br>$I_D$<br>$I_{DM}$ | <br>4.0<br>20 | A |
| Total Power Dissipation @ $T_A$ = 25°C<br>Mounted on FR4 $t \le 5$ sec | $P_D$ | 2.0 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

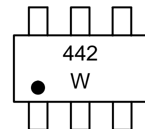
N–Channel




**MARKING DIAGRAM**

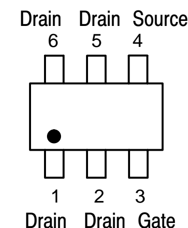



**TSOP–6**
**CASE 318G**
**STYLE 1**




442 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF3442VT1 | TSOP–6 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | | | – | – | 5.0 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.6 | – | – | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.0 A) | | $r_{DS(on)}$ | – | 0.058 | 0.070 | Ohms |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 3.4 A) | | | – | 0.072 | 0.095 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 90 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 50 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 10 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 A, $V_{GEN}$ = 10 V, $R_L$ = 10 Ω) | $t_{d(on)}$ | – | 8.0 | 20 | ns |
| Rise Time | | $t_r$ | – | 24 | 40 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 36 | 60 | |
| Fall Time | | $t_f$ | – | 10 | 20 | |
| Gate Charge | | $Q_T$ | – | – | – | nC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 1.0 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 5.0 | A |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | – | 1.2 | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

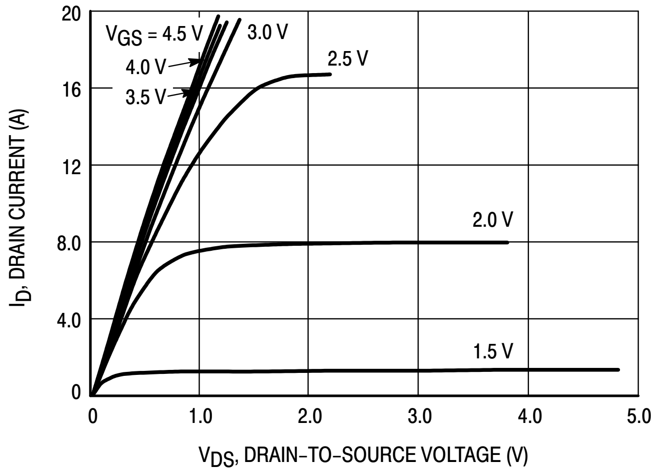



**Figure 1. Output Characteristics**

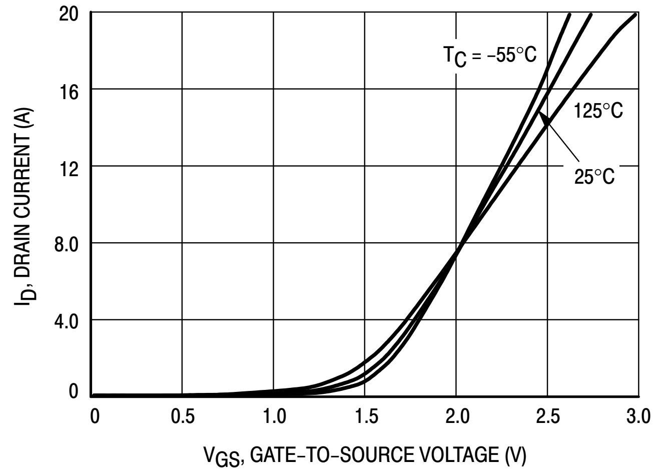



**Figure 2. Transfer Characteristics**

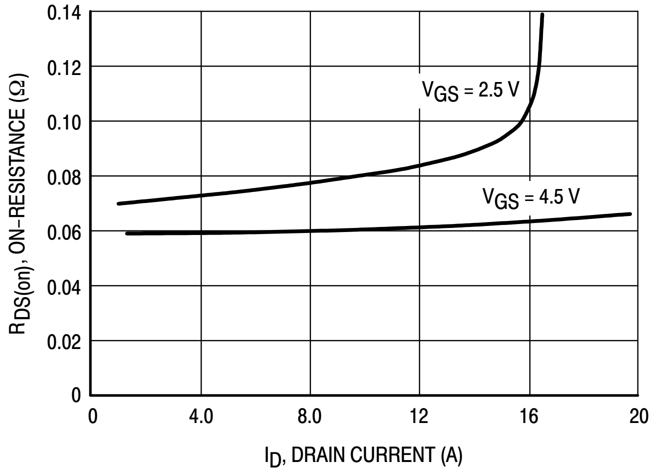



**Figure 3. On–Resistance versus Drain Current**

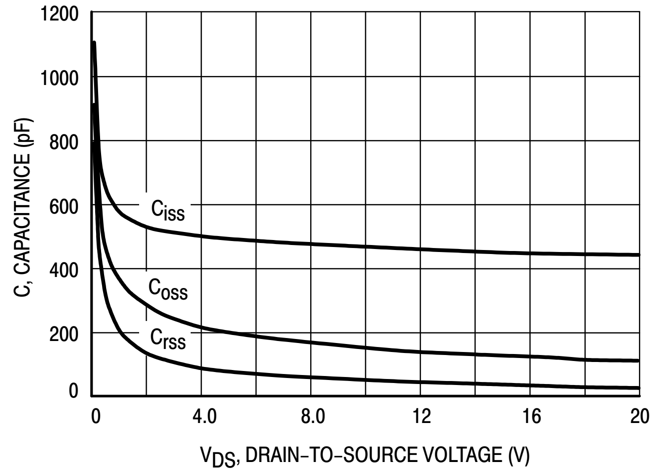



**Figure 4. Capacitance**

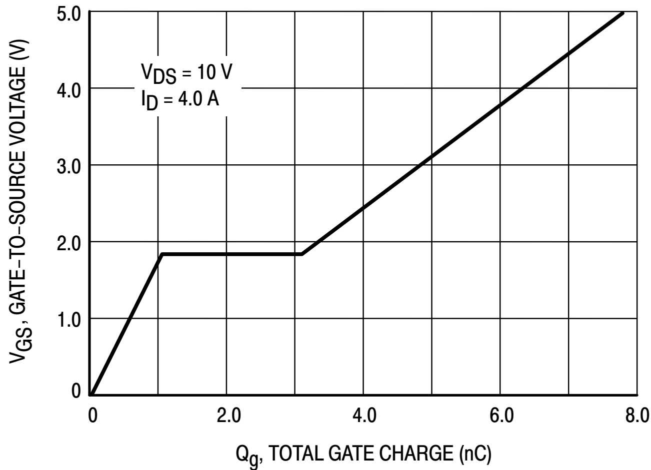



**Figure 5. Gate Charge**

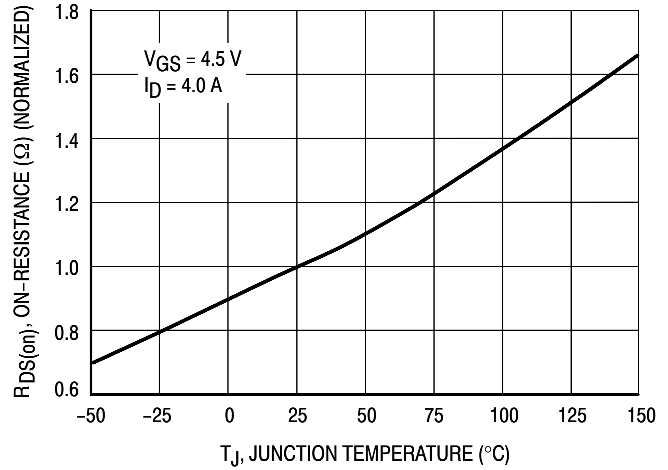



**Figure 6. On–Resistance versus Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

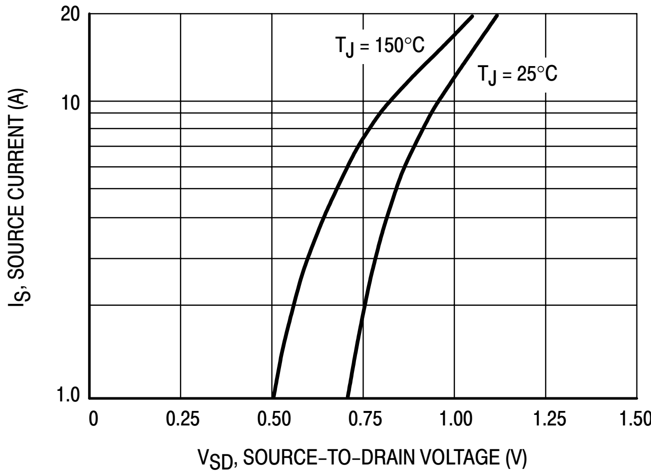



**Figure 7. Source–Drain Diode Forward Voltage**

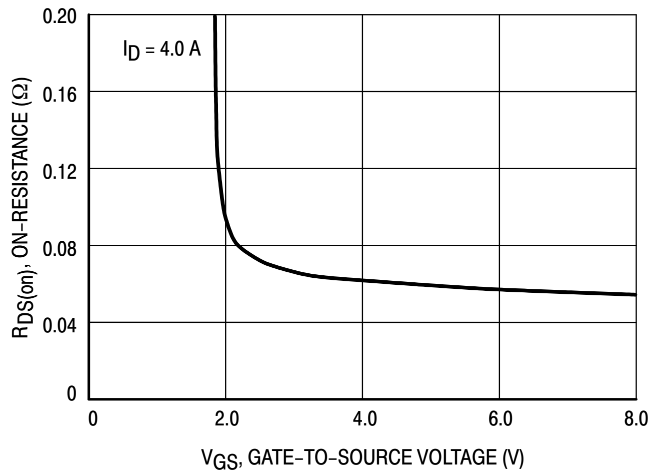



**Figure 8. On–Resistance versus Gate–to–Source Voltage**

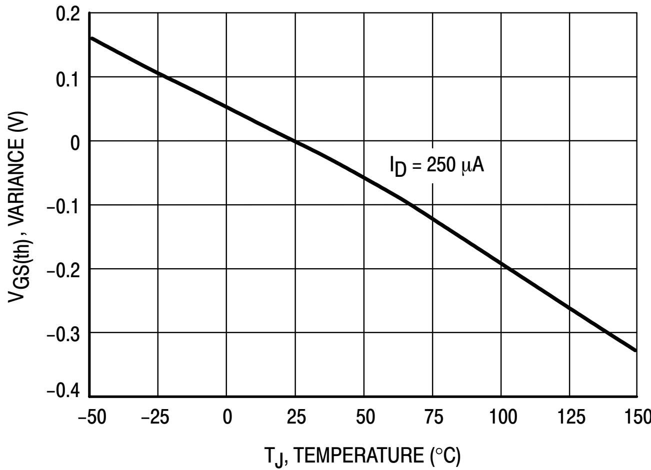



**Figure 9. Threshold Voltage**

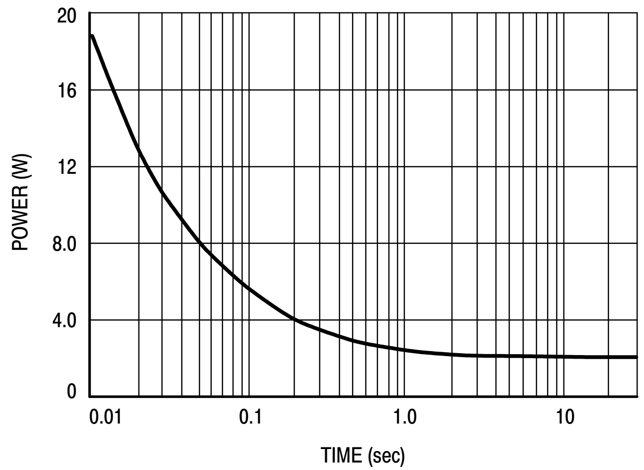



**Figure 10. Single Pulse Power**

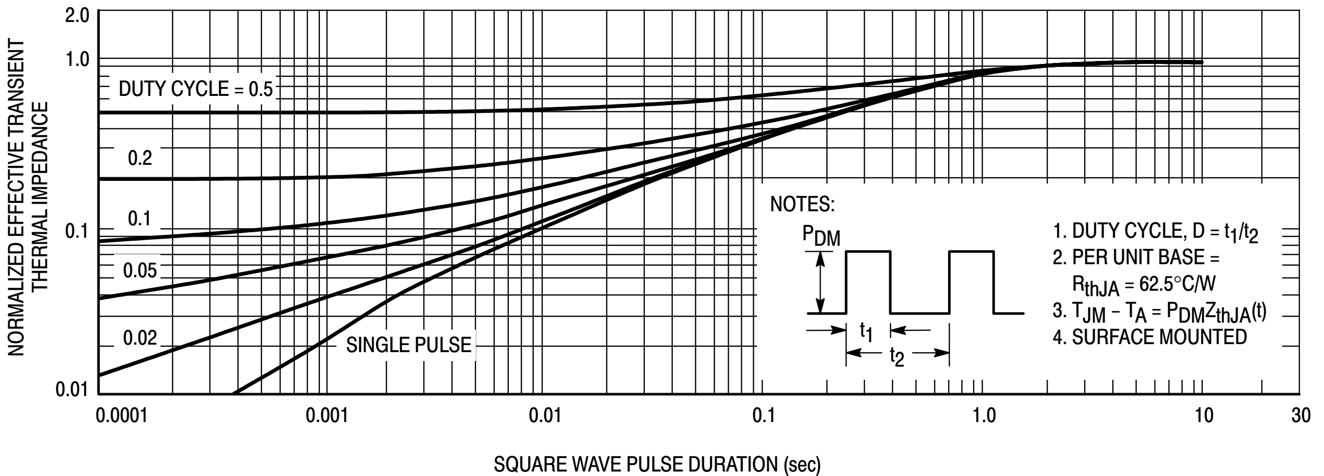
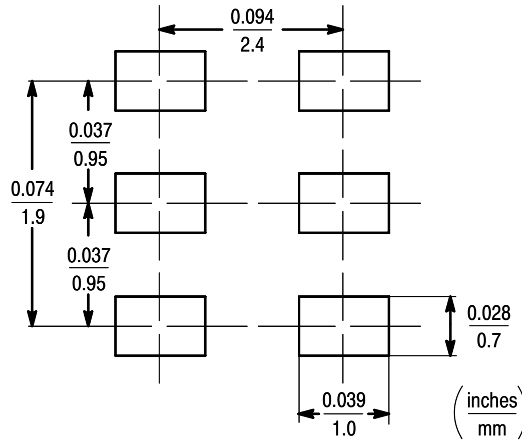



**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

# INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## TSOP–6 POWER DISSIPATION

The power dissipation of the TSOP–6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the TSOP–6 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ watts}$$

The 62.5°C/W for the TSOP–6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 watts. There are other alternatives to achieving higher power dissipation from the TSOP–6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MGSF3454VT1

**Preferred Device**

# Power MOSFET 4 Amps, 30 Volts

## N–Channel TSOP–6

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature TSOP–6 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Pulsed Drain Current ($t_p$ ≤ 10 µs) | <br>$I_D$<br>$I_{DM}$ | <br>4.2<br>20 | A |
| Total Power Dissipation @ $T_A$ = 25°C Mounted on FR4 t ≤ 5 sec | $P_D$ | 2.0 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

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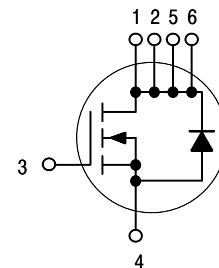
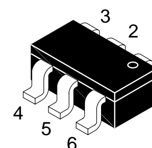
**4 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 65 mΩ**

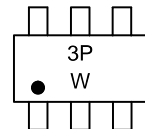
**N–Channel**




**MARKING DIAGRAM**

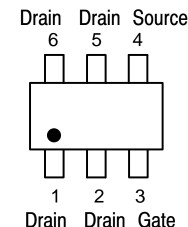



**TSOP–6**
**CASE 318G**
**STYLE 1**




3P = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MGSF3454VT1 | TSOP–6 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 70°C) | | | – | – | 25 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | – | – | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 4.2 A) | | $r_{DS(on)}$ | – | 0.05 | 0.065 | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.4 A) | | | – | 0.07 | 0.095 | |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 90 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 50 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 10 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 A, $V_{GEN}$ = 10 V, $R_L$ = 10 Ω) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 15 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 20 | 35 | |
| Fall Time | | $t_f$ | – | 10 | 20 | |
| Gate Charge | | $Q_T$ | – | – | 15 | nC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 1.0 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 5.0 | A |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | – | 1.2 | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

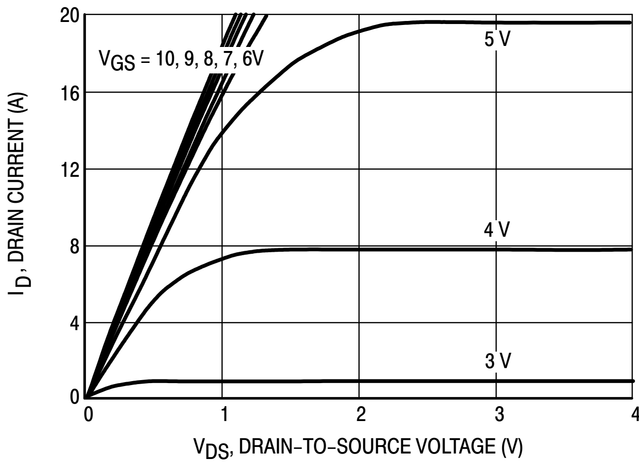



**Figure 1. Output Characteristics**

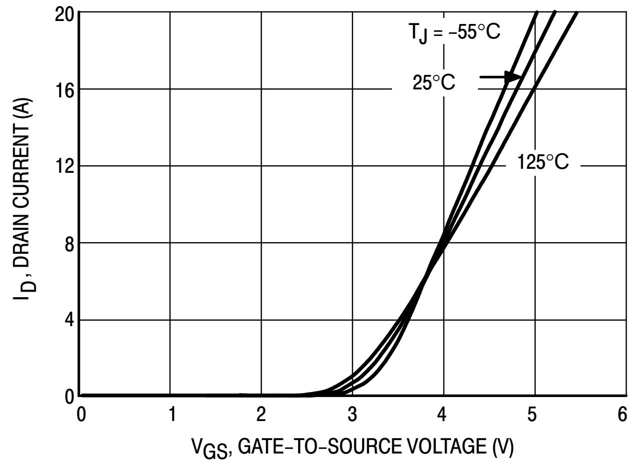



**Figure 2. Transfer Characteristics**

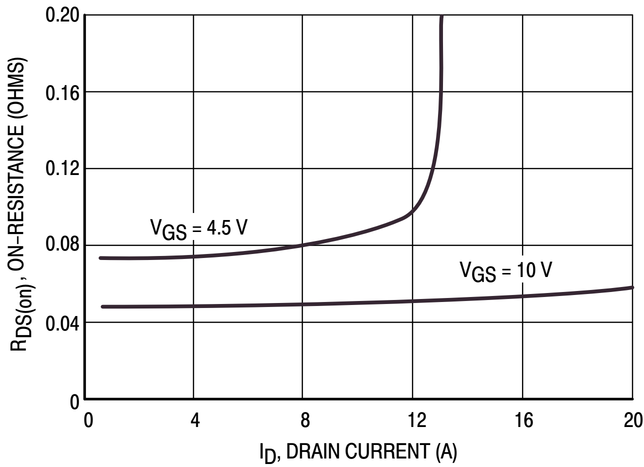



**Figure 3. On–Resistance vs. Drain Current**

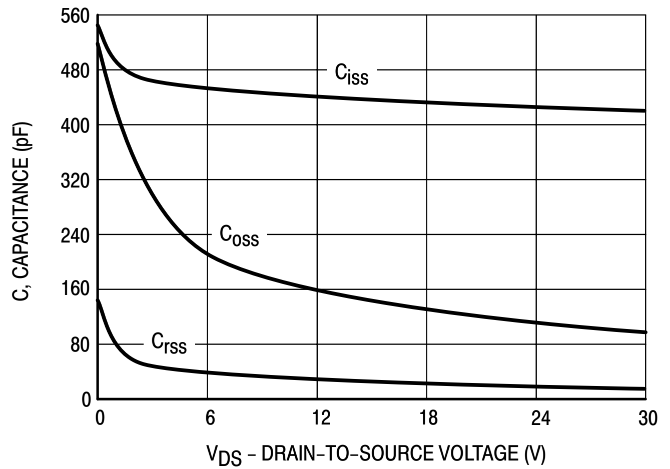



**Figure 4. Capacitance**

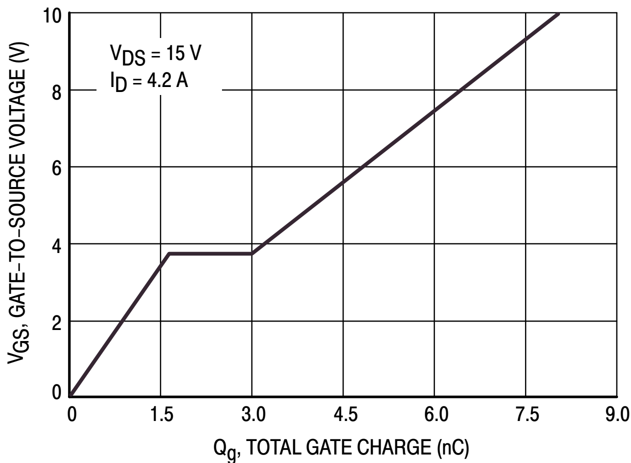



**Figure 5. Gate Charge**

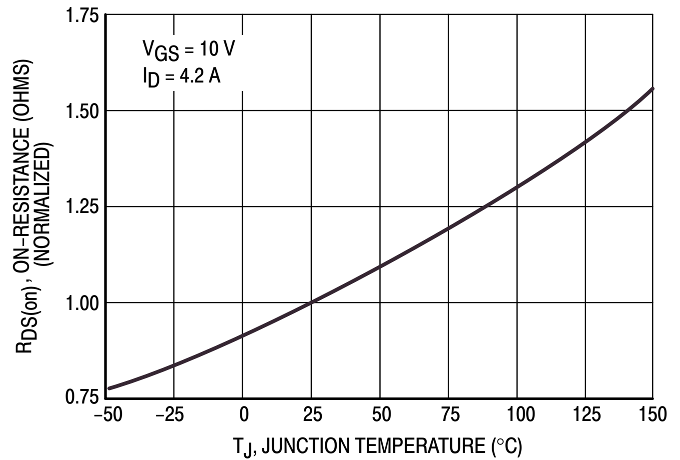



**Figure 6. On–Resistance vs. Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

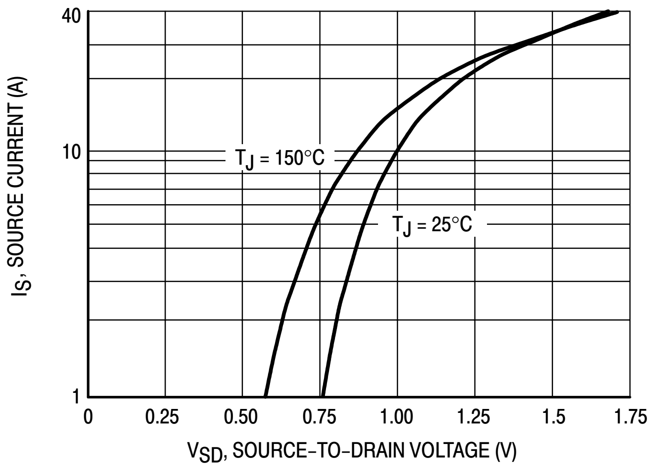



**Figure 7. Source–Drain Diode Forward Voltage**

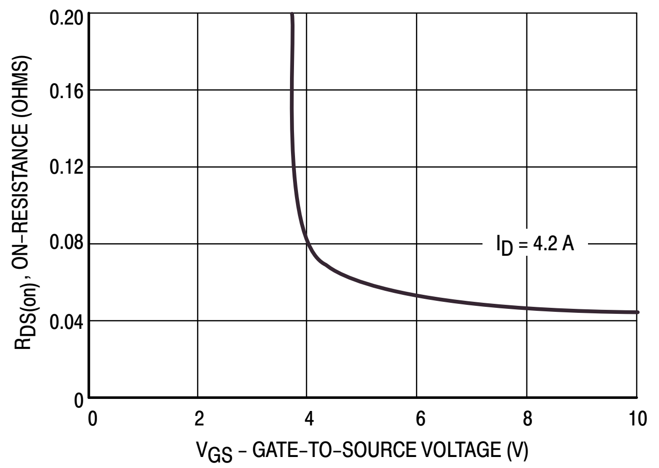



**Figure 8. On–Resistance vs. Gate–to–Source Voltage**

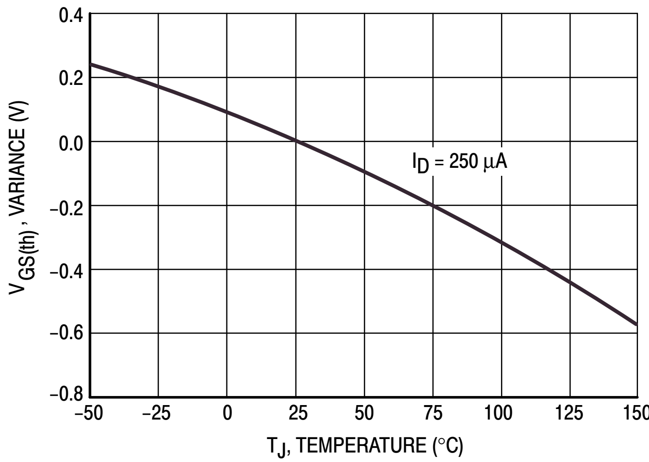



**Figure 9. Threshold Voltage**

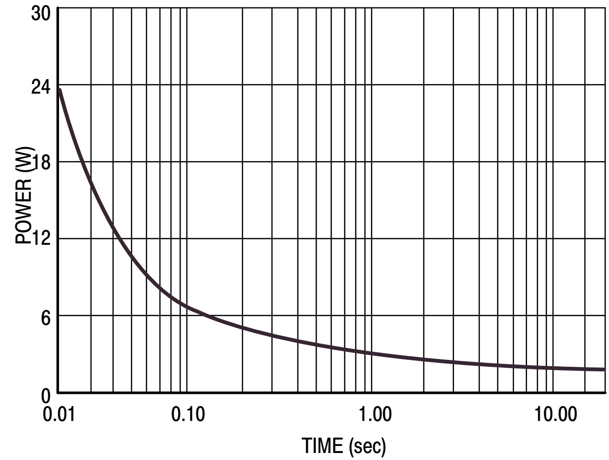



**Figure 10. Single Pulse Power**

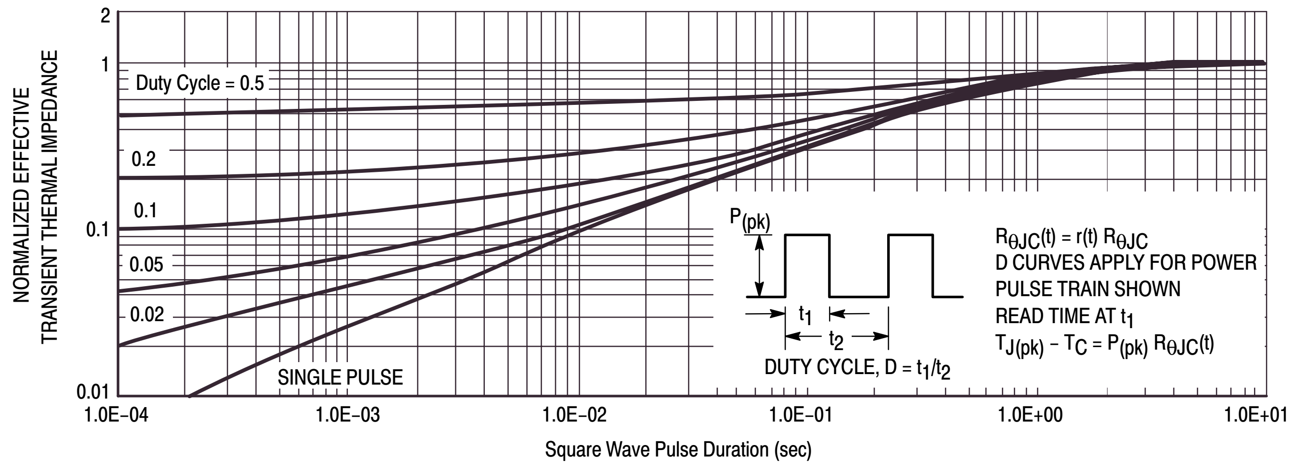
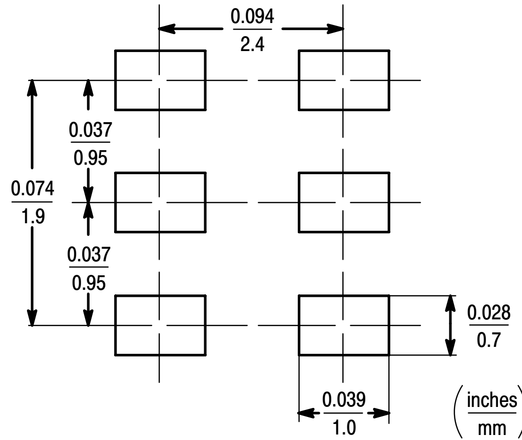



**Figure 11. Normalized Thermal Transient Impedance, Junction–to–Ambient**

# INFORMATION FOR USING THE TSOP–6 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## TSOP–6 POWER DISSIPATION

The power dissipation of the TSOP–6 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the TSOP–6 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ watts}$$

The 62.5°C/W for the TSOP–6 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 watts. There are other alternatives to achieving higher power dissipation from the TSOP–6 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MLD1N06CL

**Preferred Device**

# SMARTDISCRETES™ MOSFET 1 Amp, 62 Volts, Logic Level

## N–Channel DPAK

The MLD1N06CL is designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontrol unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

This Logic Level Power MOSFET features current limiting for short circuit protection, integrated Gate–Source clamping for ESD protection and integral Gate–Drain clamping for over–voltage protection and Sensefet technology for low on–resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate–Source and Gate–Drain clamps allow the device to be applied without use of external transient suppression components. The Gate–Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate–Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | Clamped | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | Clamped | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | Vdc |
| Drain Current – Continuous<br>– Single Pulse | $I_D$<br>$I_{DM}$ | Self–limited<br>1.8 | Adc<br>Apk |
| Total Power Dissipation | $P_D$ | 40 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –50 to 150 | °C |
| Electrostatic Discharge Voltage (Human Model) | ESD | 2.0 | kV |

**THERMAL CHARACTERISTICS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{θJC}$<br>$R_{θJA}$<br>$R_{θJA}$ | <br>3.12<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 sec. | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

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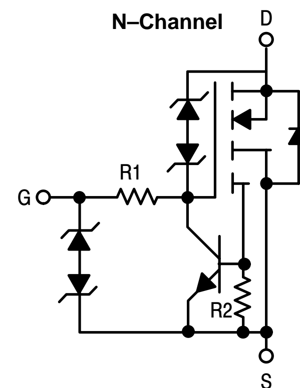
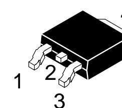
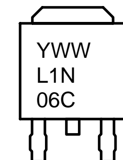
**1 AMPERE**
**62 VOLTS (Clamped)**
**$R_{DS(on)}$ = 750 mΩ**




**MARKING DIAGRAM**

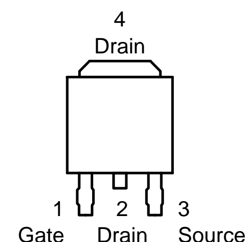



**CASE 369A**
**DPAK**
**STYLE 2**




L1N06C = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MLD1N06CLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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## UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche Energy<br>Starting $T_J$ = 25°C | $E_{AS}$ | 80 | mJ |

## ELECTRICAL CHARACTERISTICS ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage (Internally Clamped)<br>($I_D$ = 20 mAdc, $V_{GS}$ = 0 Vdc)<br>($I_D$ = 20 mAdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{(BR)DSS}$ | <br>59<br>59 | <br>62<br>62 | <br>65<br>65 | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 45 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 45 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $I_{DSS}$ | <br>–<br>– | <br>0.6<br>6.0 | <br>5.0<br>20 | μAdc |
| Gate–Source Leakage Current<br>($V_G$ = 5.0 Vdc, $V_{DS}$ = 0 Vdc)<br>($V_G$ = 5.0 Vdc, $V_{DS}$ = 0 Vdc, $T_J$ = 150°C) | $I_{GSS}$ | <br>–<br>– | <br>0.5<br>1.0 | <br>5.0<br>20 | μAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage<br>($I_D$ = 250 μAdc, $V_{DS}$ = $V_{GS}$)<br>($I_D$ = 250 μAdc, $V_{DS}$ = $V_{GS}$, $T_J$ = 150°C) | $V_{GS(th)}$ | <br>1.0<br>0.6 | <br>1.5<br>– | <br>2.0<br>1.6 | Vdc |
| Static Drain–to–Source On–Resistance<br>($I_D$ = 1.0 Adc, $V_{GS}$ = 4.0 Vdc)<br>($I_D$ = 1.0 Adc, $V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 1.0 Adc, $V_{GS}$ = 4.0 Vdc, $T_J$ = 150°C)<br>($I_D$ = 1.0 Adc, $V_{GS}$ = 5.0 Vdc, $T_J$ = 150°C) | $R_{DS(on)}$ | <br>–<br>–<br>–<br>– | <br>0.63<br>0.59<br>1.1<br>1.0 | <br>0.75<br>0.75<br>1.9<br>1.8 | Ohms |
| Static Source–to–Drain Diode Voltage ($I_S$ = 1.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.1 | 1.5 | Vdc |
| Static Drain Current Limit<br>($V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 10 Vdc)<br>($V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 10 Vdc, $T_J$ = 150°C) | $I_{D(lim)}$ | <br>2.0<br>1.1 | <br>2.3<br>1.3 | <br>2.75<br>1.8 | Adc |
| Forward Transconductance ($I_D$ = 1.0 Adc, $V_{DS}$ = 10 Vdc) | $g_{FS}$ | 1.0 | 1.4 | – | mhos |
| **RESISTIVE SWITCHING CHARACTERISTICS** (Note 3.) | | | | | |
| Turn–On Delay Time ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, $R_{GS}$ = 50 Ohms) | $t_{d(on)}$ | – | 1.2 | 2.0 | ns |
| Rise Time | $t_r$ | – | 4.0 | 6.0 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 4.0 | 6.0 | |
| Fall Time | $t_f$ | – | 3.0 | 5.0 | |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from drain lead 0.25″ from package to center of die) | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

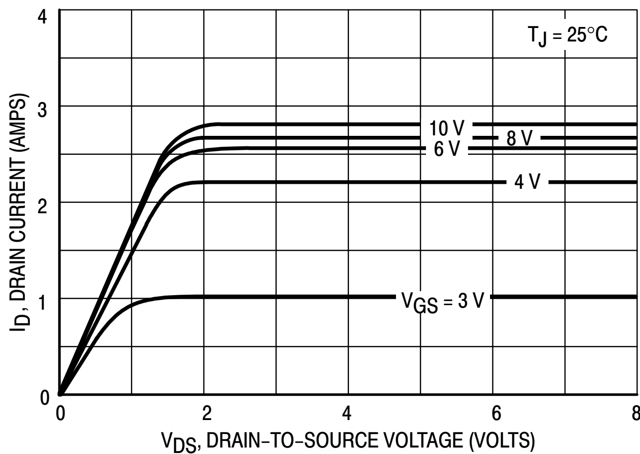



**Figure 1. Output Characteristics**

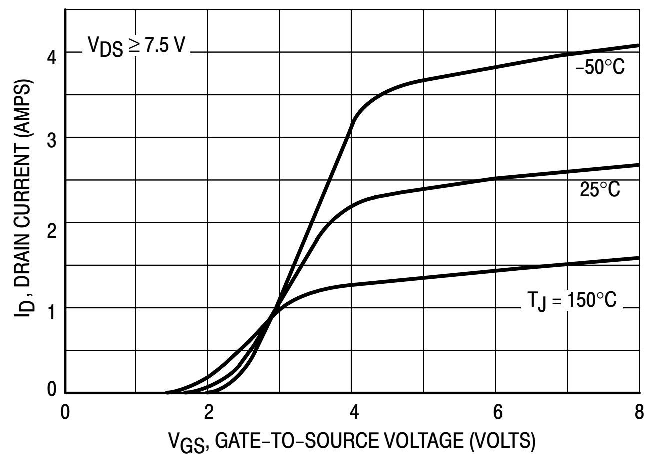



**Figure 2. Transfer Function**

### THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

### OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLD1N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

### SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLD1N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

Since the MLD1N06CL continues to conduct current and dissipate power during a shorted load condition, it is important to provide sufficient heatsinking to limit the device junction temperature to a maximum of 150°C.

The metal current sense resistor R2 adds about 0.4 ohms to the power MOSFET's on–resistance, but the effect of temperature on the combination is less than on a standard MOSFET due to the lower temperature coefficient of R2. The on–resistance variation with temperature for gate voltages of 4 and 5 Volts is shown in Figure 5.

Back–to–back polysilicon diodes between gate and source provide ESD protection to greater than 2 kV, HBM. This on–chip protection feature eliminates the need for an external Zener diode for systems with potentially heavy line transients.

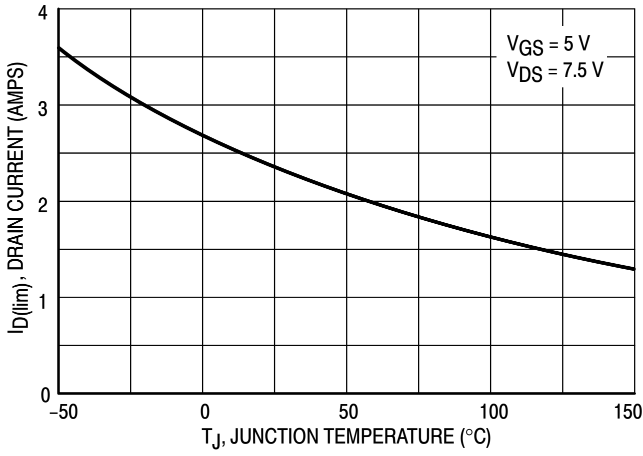



**Figure 3. $I_{D(lim)}$ Variation With Temperature**

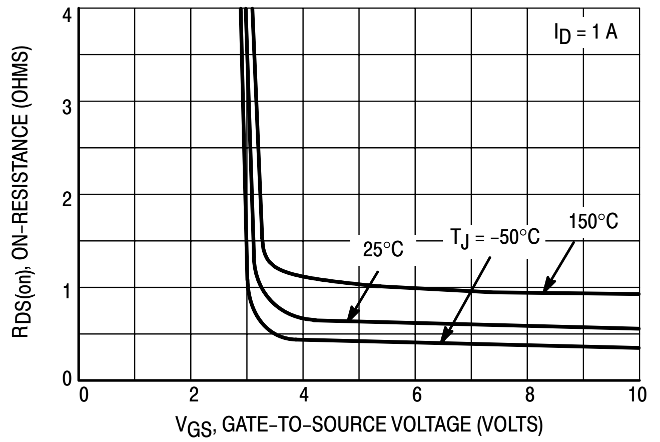



**Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage**

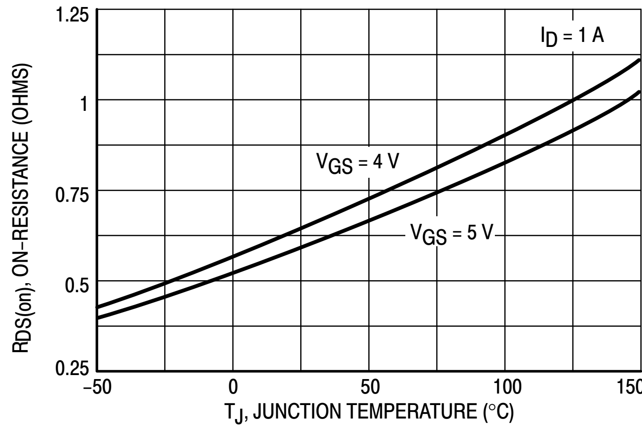



**Figure 5. On–Resistance Variation With Temperature**

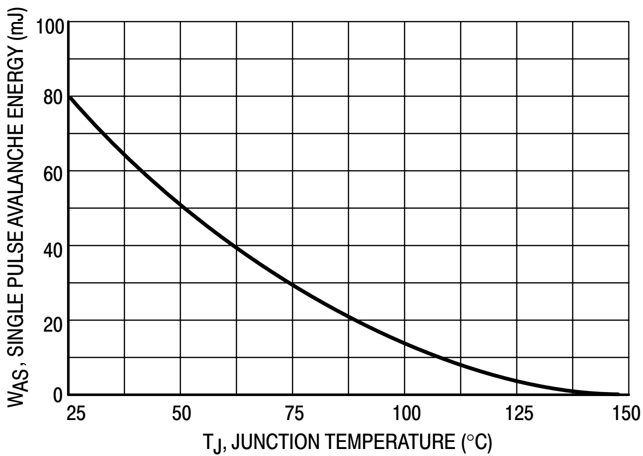



**Figure 6. Single Pulse Avalanche Energy versus Junction Temperature**

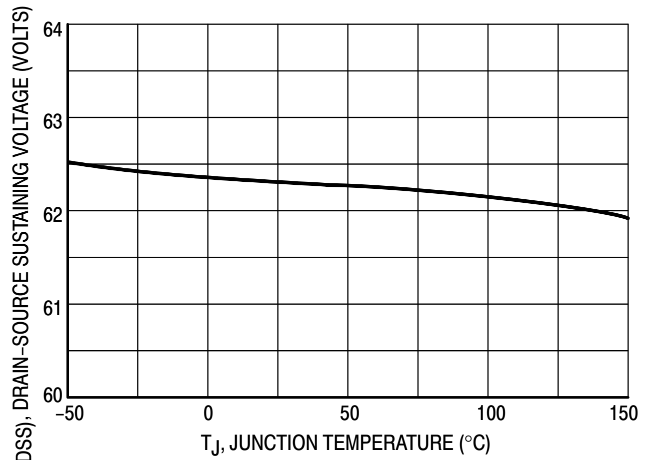



**Figure 7. Drain–Source Sustaining Voltage Variation With Temperature**

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance – General Data and Its Use” provides detailed instructions.

### MAXIMUM DC VOLTAGE CONSIDERATIONS

The maximum drain–to–source voltage that can be continuously applied across the MLD1N06CL when it is in current limit is a function of the power that must be dissipated. This power is determined by the maximum current limit at maximum rated operating temperature (1.8 A at 150°C) and not the $R_{DS(on)}$. The maximum voltage can be calculated by the following equation:

$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)}\,(R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

### DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of $V_{DS}$ applied when operating in a duty cycle mode can be approximated by:

$$V_{DS} = \frac{150 - T_C}{I_{D(lim)} \times DC \times R_{\theta JC}}$$

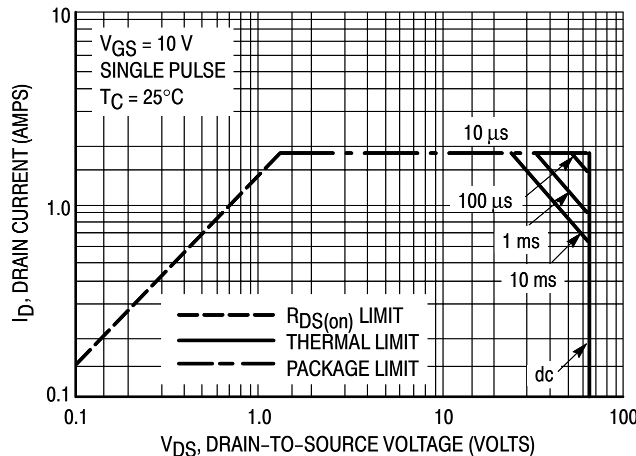



**Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLD1N06CL)**

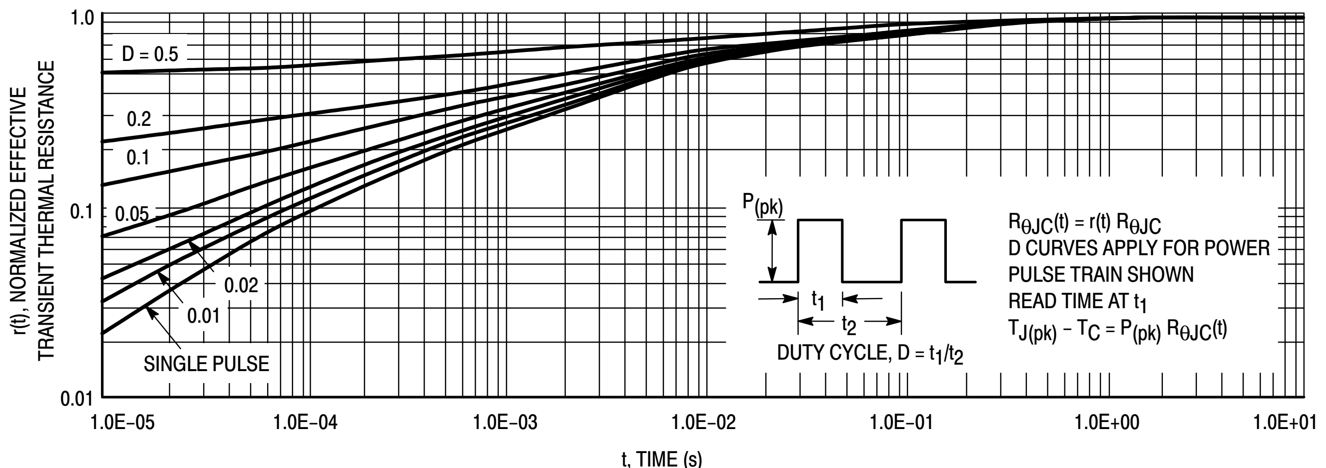



**Figure 9. Thermal Response (MLD1N06CL)**

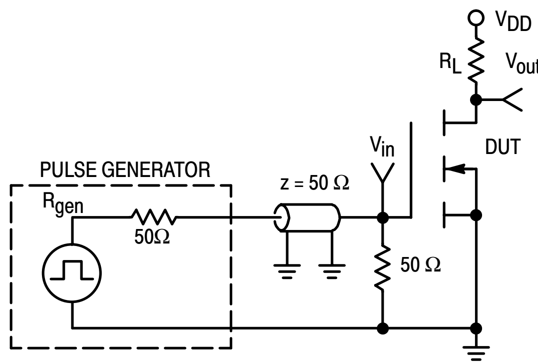



Figure 10. Switching Test Circuit

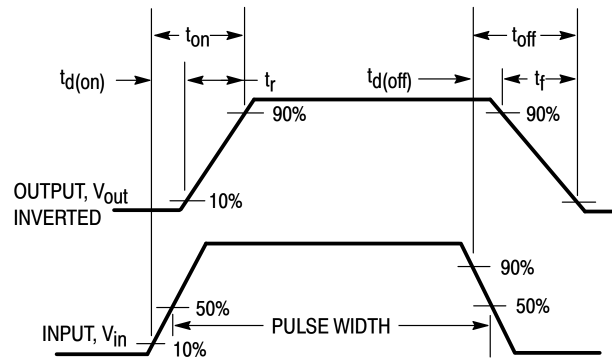



Figure 11. Switching Waveforms

**ACTIVE CLAMPING**

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

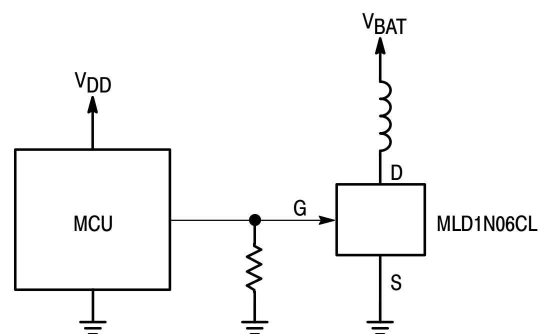
To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLD1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLD1N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

The gate–to–drain voltage clamp technique is particularly useful for snubbing loads where the inductive energy would otherwise avalanche the power device. An improvement in ruggedness of at least four times has been observed when inductive energy is dissipated in the gate–to–drain clamped conduction mode rather than in the more stressful gate–to–source avalanche mode.

**TYPICAL APPLICATIONS: INJECTOR DRIVER, SOLENOIDS, LAMPS, RELAY COILS**

The MLD1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



# MLP1N06CL

**Preferred Device**

# SMARTDISCRETES™ MOSFET 1 Amp, 62 Volts, Logic Level

## N–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

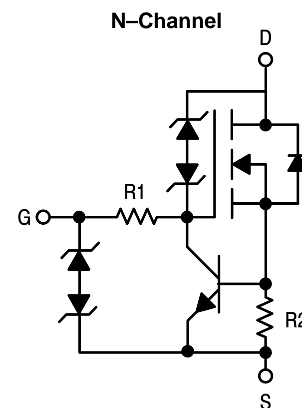
**1 AMPERE**
**62 VOLTS (Clamped)**
**$R_{DS(on)}$ = 750 mΩ**

These SMARTDISCRETES devices feature current limiting for short circuit protection, an integral gate–to–source clamp for ESD protection and gate–to–drain clamp for over–voltage protection. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal gate–to–source and gate–to–drain clamps allow the devices to be applied without use of external transient suppression components. The gate–to–source clamp protects the MOSFET input from electrostatic gate voltage stresses up to 2.0 kV. The gate–to–drain clamp protects the MOSFET drain from drain avalanche stresses that occur with inductive loads. This unique design provides voltage clamping that is essentially independent of operating temperature.

- Temperature Compensated Gate–to–Drain Clamp Limits Voltage Stress Applied to the Device and Protects the Load From Overvoltage
- Integrated ESD Diode Protection
- Controlled Switching Minimizes RFI
- Low Threshold Voltage Enables Interfacing Power Loads to Microprocessors

**N–Channel**



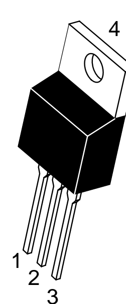

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | Clamped | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | Clamped | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | Vdc |
| Drain Current – Continuous<br>– Single Pulse | $I_D$<br>$I_{DM}$ | Self–limited<br>1.8 | Adc |
| Total Power Dissipation | $P_D$ | 40 | Watts |
| Electrostatic Discharge Voltage (Human Body Model) | ESD | 2.0 | kV |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | –50 to 150 | °C |

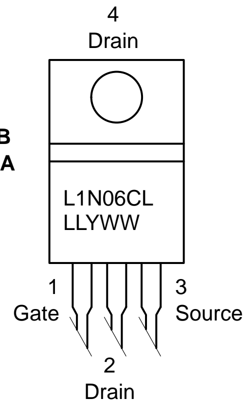
**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance, Junction to Case<br>Thermal Resistance, Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 3.12<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| L1N06CL | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MLP1N06CL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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## UNCLAMPED DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche Energy (Starting $T_J$ = 25°C, $I_D$ = 2.0 A, L = 40 mH) (Figure 6) | $E_{AS}$ | 80 | mJ |

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Sustaining Voltage (Internally Clamped) | $V_{(BR)DSS}$ | | | | Vdc |
| ($I_D$ = 20 mA, $V_{GS}$ = 0) | | 59 | 62 | 65 | |
| ($I_D$ = 20 mA, $V_{GS}$ = 0, $T_J$ = 150°C) | | 59 | 62 | 65 | |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 45 V, $V_{GS}$ = 0) | | – | 0.6 | 5.0 | |
| ($V_{DS}$ = 45 V, $V_{GS}$ = 0, $T_J$ = 150°C) | | – | 6.0 | 20 | |
| Gate–Body Leakage Current | $I_{GSS}$ | | | | μAdc |
| ($V_G$ = 5.0 V, $V_{DS}$ = 0) | | – | 0.5 | 5.0 | |
| ($V_G$ = 5.0 V, $V_{DS}$ = 0, $T_J$ = 150°C) | | – | 1.0 | 20 | |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage | $V_{GS(th)}$ | | | | Vdc |
| ($I_D$ = 250 μA, $V_{DS}$ = $V_{GS}$) | | 1.0 | 1.5 | 2.0 | |
| ($I_D$ = 250 μA, $V_{DS}$ = $V_{GS}$, $T_J$ = 150°C) | | 0.6 | – | 1.6 | |
| Static Drain–to–Source On–Resistance | $R_{DS(on)}$ | | | | Ohms |
| ($I_D$ = 1.0 A, $V_{GS}$ = 4.0 V) | | – | 0.63 | 0.75 | |
| ($I_D$ = 1.0 A, $V_{GS}$ = 5.0 V) | | – | 0.59 | 0.75 | |
| ($I_D$ = 1.0 A, $V_{GS}$ = 4.0 V, $T_J$ = 150°C) | | – | 1.1 | 1.9 | |
| ($I_D$ = 1.0 A, $V_{GS}$ = 5.0 V, $T_J$ = 150°C) | | – | 1.0 | 1.8 | |
| Forward Transconductance ($I_D$ = 1.0 A, $V_{DS}$ = 10 V) | $g_{FS}$ | 1.0 | 1.4 | – | mhos |
| Static Source–to–Drain Diode Voltage ($I_S$ = 1.0 A, $V_{GS}$ = 0) | $V_{SD}$ | – | 1.1 | 1.5 | Vdc |
| Static Drain Current Limit | $I_{D(lim)}$ | | | | A |
| ($V_{GS}$ = 5.0 V, $V_{DS}$ = 10 V) | | 2.0 | 2.3 | 2.75 | |
| ($V_{GS}$ = 5.0 V, $V_{DS}$ = 10 V, $T_J$ = 150°C) | | 1.1 | 1.3 | 1.8 | |

**RESISTIVE SWITCHING CHARACTERISTICS** (Note 1.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 1.0 A, $V_{GS}$ = 5.0 V, $R_G$ = 50 Ohms) | $t_{d(on)}$ | – | 1.2 | 2.0 | μs |
| Rise Time | | $t_r$ | – | 4.0 | 6.0 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 4.0 | 6.0 | |
| Fall Time | | $t_f$ | – | 3.0 | 5.0 | |

1. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

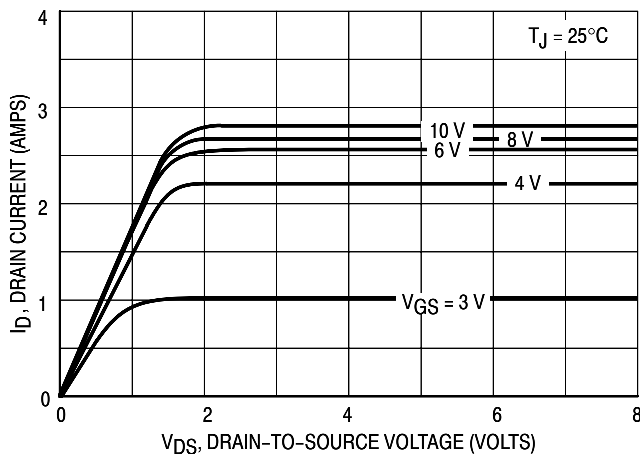
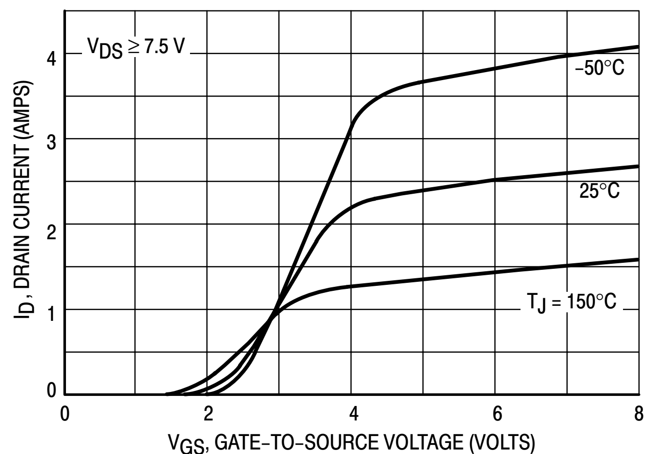



**Figure 1. Output Characteristics**

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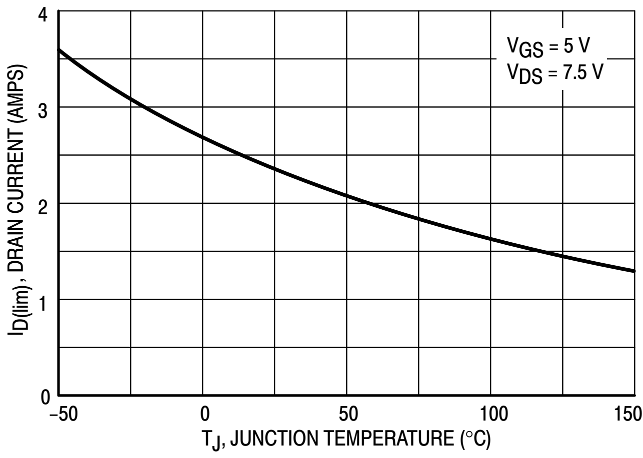


**Figure 3. $I_{D(lim)}$ Variation With Temperature**

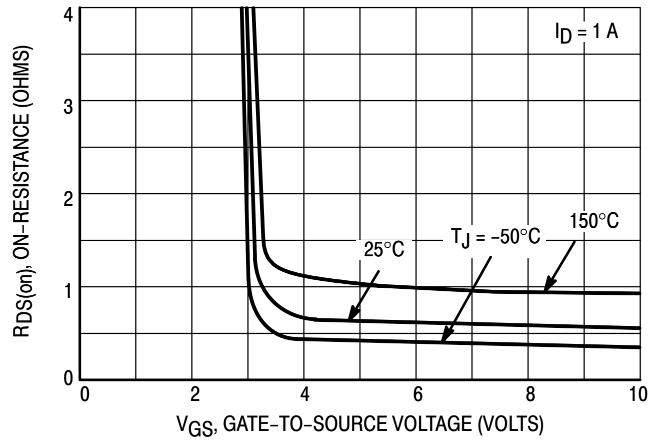


**Figure 4. $R_{DS(on)}$ Variation With Gate–To–Source Voltage**

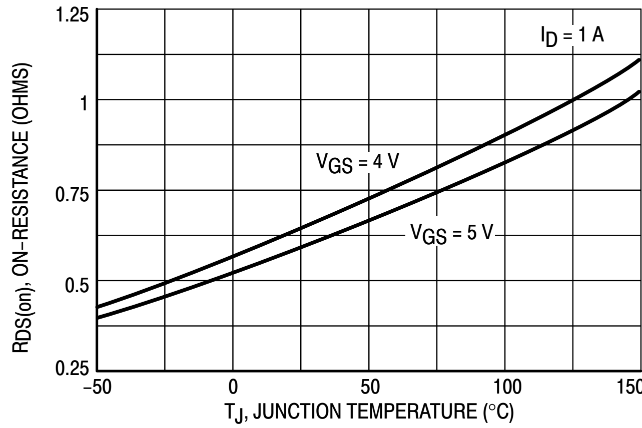


**Figure 5. On–Resistance Variation With Temperature**

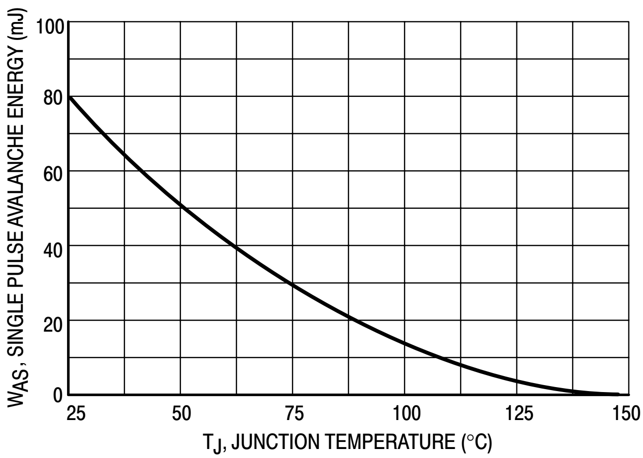


**Figure 6. Single Pulse Avalanche Energy versus Junction Temperature**

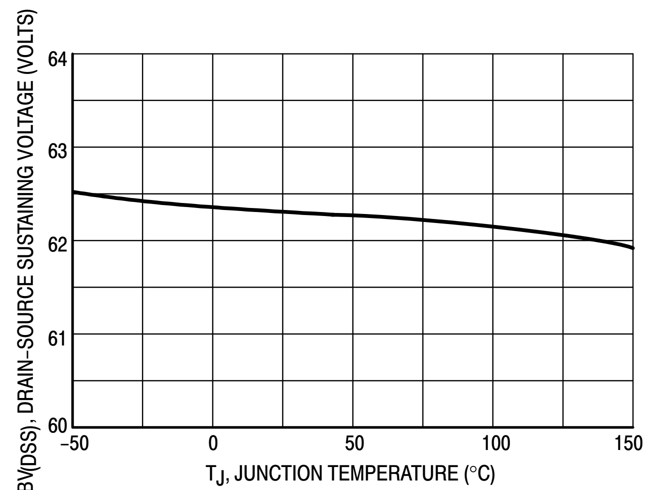


**Figure 7. Drain–Source Sustaining Voltage Variation With Temperature**

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$$V_{supply} = \frac{(150 - T_A)}{I_{D(lim)}\,(R_{\theta JC} + R_{\theta CA})}$$

where the value of $R_{\theta CA}$ is determined by the heatsink that is being used in the application.

## DUTY CYCLE OPERATION

When operating in the duty cycle mode, the maximum drain voltage can be increased. The maximum operating temperature is related to the duty cycle (DC) by the following equation:

$$T_C = (V_{DS} \times I_D \times DC \times R_{\theta CA}) + T_A$$

The maximum value of $V_{DS}$ applied when operating in a duty cycle mode can be approximated by:

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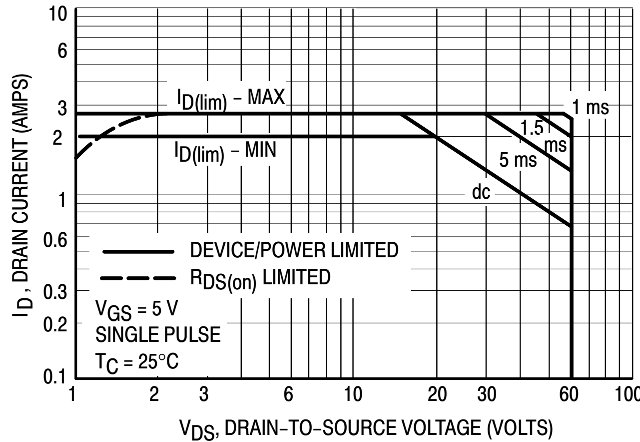



**Figure 8. Maximum Rated Forward Bias Safe Operating Area (MLP1N06CL)**

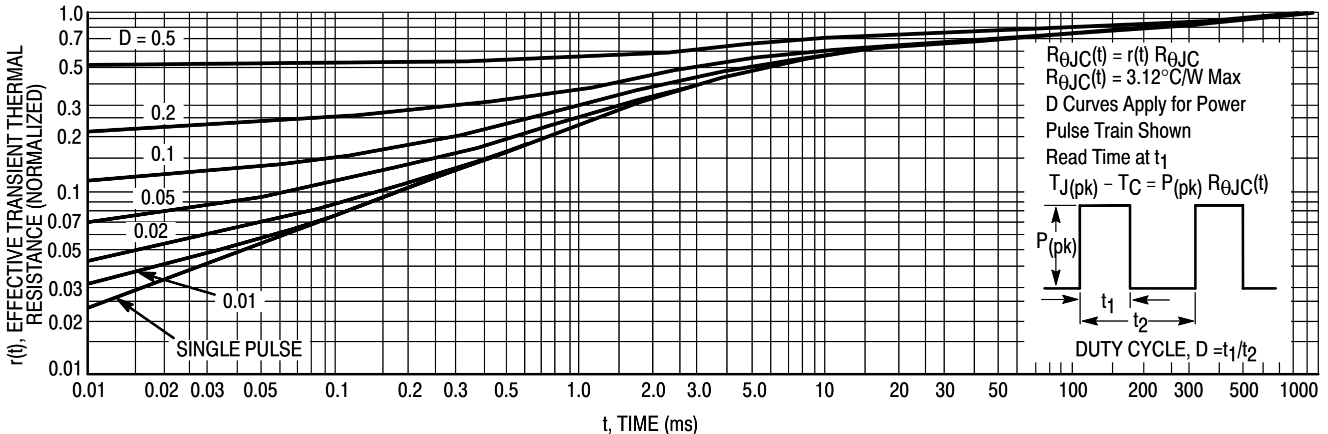



**Figure 9. Thermal Response (MLP1N06CL)**

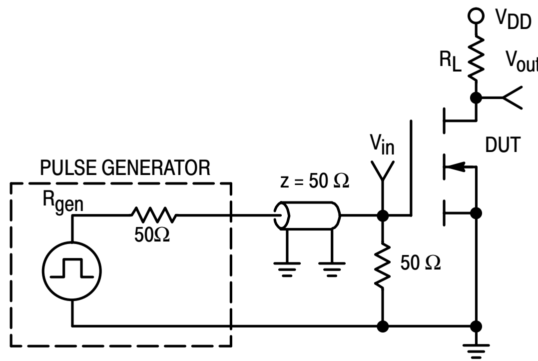
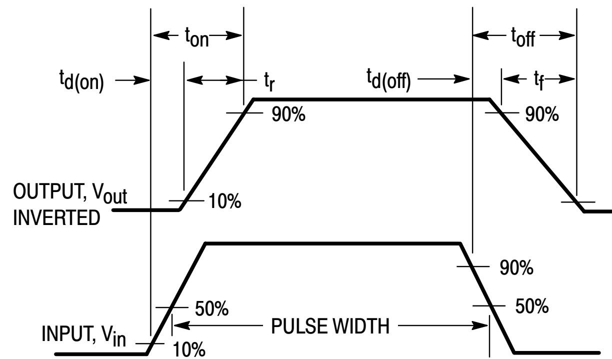



Figure 10. Switching Test Circuit

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**ACTIVE CLAMPING**

SMARTDISCRETES technology can provide on–chip realization of the popular gate–to–source and gate–to–drain Zener diode clamp elements. Until recently, such features have been implemented only with discrete components which consume board space and add system cost. The SMARTDISCRETES technology approach economically melds these features and the power chip with only a slight increase in chip area.

In practice, back–to–back diode elements are formed in a polysilicon region monolithicly integrated with, but electrically isolated from, the main device structure. Each back–to–back diode element provides a temperature compensated voltage element of about 7.2 volts. As the polysilicon region is formed on top of silicon dioxide, the diode elements are free from direct interaction with the conduction regions of the power device, thus eliminating parasitic electrical effects while maintaining excellent thermal coupling.

To achieve high gate–to–drain clamp voltages, several voltage elements are strung together; the MLP1N06CL uses 8 such elements. Customarily, two voltage elements are used to provide a 14.4 volt gate–to–source voltage clamp. For the MLP1N06CL, the integrated gate–to–source voltage elements provide greater than 2.0 kV electrostatic voltage protection.

The avalanche voltage of the gate–to–drain voltage clamp is set less than that of the power MOSFET device. As soon as the drain–to–source voltage exceeds this avalanche voltage, the resulting gate–to–drain Zener current builds a gate voltage across the gate–to–source impedance, turning on the power device which then conducts the current. Since virtually all of the current is carried by the power device, the gate–to–drain voltage clamp element may be small in size. This technique of establishing a temperature compensated drain–to–source sustaining voltage (Figure 7) effectively removes the possibility of drain–to–source avalanche in the power device.

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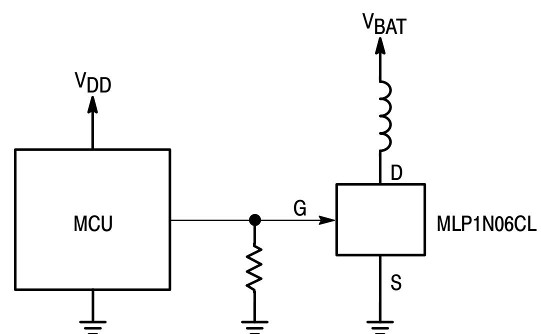
The MLP1N06CL has been designed to allow direct interface to the output of a microcontrol unit to control an isolated load. No additional series gate resistance is required, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition in the event of an MCU failure. The internal clamps allow the device to be used without any external transistent suppressing components.



# MLP2N06CL

**Preferred Device**

# SMARTDISCRETES™ MOSFET 2 Amps, 62 Volts, Logic Level

## N–Channel TO–220

This logic level power MOSFET features current limiting for short circuit protection, integrated Gate–Source clamping for ESD protection and integral Gate–Drain clamping for over–voltage protection and Sensefet technology for low on–resistance. No additional gate series resistance is required when interfacing to the output of a MCU, but a 40 kΩ gate pulldown resistor is recommended to avoid a floating gate condition.

The internal Gate–Source and Gate–Drain clamps allow the device to be applied without use of external transient suppression components. The Gate–Source clamp protects the MOSFET input from electrostatic voltage stress up to 2.0 kV. The Gate–Drain clamp protects the MOSFET drain from the avalanche stress that occurs with inductive loads. Their unique design provides voltage clamping that is essentially independent of operating temperature.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | Clamped | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | Clamped | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±10 | Vdc |
| Drain Current – Continuous @ $T_C$ = 25°C | $I_D$ | Self–limited | Adc |
| Total Power Dissipation @ $T_C$ = 25°C | $P_D$ | 40 | Watts |
| Electrostatic Voltage | ESD | 2.0 | kV |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –50 to 150 | °C |

**THERMAL CHARACTERISTICS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Maximum Junction Temperature | $T_{J(max)}$ | 150 | °C |
| Thermal Resistance – Junction to Case | $R_{\theta JC}$ | 3.12 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 sec. | $T_L$ | 260 | °C |

**DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS**

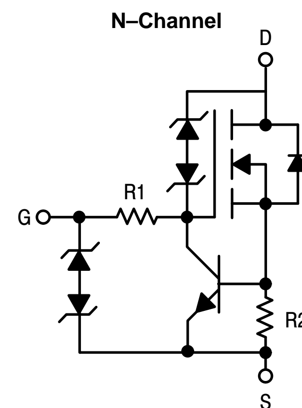
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Single Pulse Drain–to–Source Avalanche Energy (Starting $T_J$ = 25°C, $I_D$ = 2.0 A, L = 40 mH) | $E_{AS}$ | 80 | mJ |

**ON Semiconductor™**

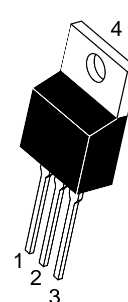
http://onsemi.com

**2 AMPERES**
**62 VOLTS (Clamped)**
**$R_{DS(on)}$ = 400 mΩ**

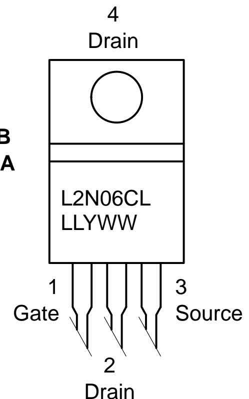
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




| | |
|---|---|
| L2N06CL | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MLP2N06CL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($I_D$ = 20 mAdc, $V_{GS}$ = 0 Vdc) ($I_D$ = 20 mAdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{(BR)DSS}$ | 58<br>58 | 62<br>62 | 66<br>66 | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 40 Vdc, $V_{GS}$ = 0 Vdc) ($V_{DS}$ = 40 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $I_{DSS}$ | –<br>– | 0.6<br>6.0 | 5.0<br>20 | µAdc |
| Gate–Source Leakage Current ($V_G$ = 5.0 Vdc, $V_{DS}$ = 0 Vdc) ($V_G$ = 5.0 Vdc, $V_{DS}$ = 0 Vdc, $T_J$ = 150°C) | $I_{GSS}$ | –<br>– | 0.5<br>1.0 | 5.0<br>20 | µAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($I_D$ = 250 µAdc, $V_{DS}$ = $V_{GS}$) ($I_D$ = 250 µAdc, $V_{DS}$ = $V_{GS}$, $T_J$ = 150°C) | $V_{GS(th)}$ | 1.0<br>0.6 | 1.5<br>1 | 2.0<br>1.6 | Vdc |
| Static Drain Current Limit ($V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 10 Vdc) ($V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 10 Vdc, $T_J$ = 150°C) | $I_{D(lim)}$ | 3.8<br>1.6 | 4.4<br>2.4 | 5.2<br>2.9 | Adc |
| Static Drain–to–Source On–Resistance ($I_D$ = 1.0 Adc, $V_{GS}$ = 5.0 Vdc) ($I_D$ = 1.0 Adc, $V_{GS}$ = 5.0 Vdc, $T_J$ = 150°C) | $R_{DS(on)}$ | –<br>– | 0.3<br>0.53 | 0.4<br>0.7 | Ohms |
| Forward Transconductance ($I_D$ = 1.0 Adc, $V_{DS}$ = 10 Vdc) | $g_{FS}$ | 1.0 | 1.4 | – | mhos |
| Static Source–to–Drain Diode Voltage ($I_S$ = 1.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.1 | 1.5 | Vdc |

**SWITCHING CHARACTERISTICS** (Note 2.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 1.0 Adc, $V_{GS(on)}$ = 5.0 Vdc, $R_{GS}$ = 25 Ohms) | $t_{d(on)}$ | – | 1.0 | 1.5 | µs |
| Rise Time | | $t_r$ | – | 3.0 | 5.0 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 5.0 | 8.0 | |
| Fall Time | | $t_f$ | – | 3.0 | 5.0 | |

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

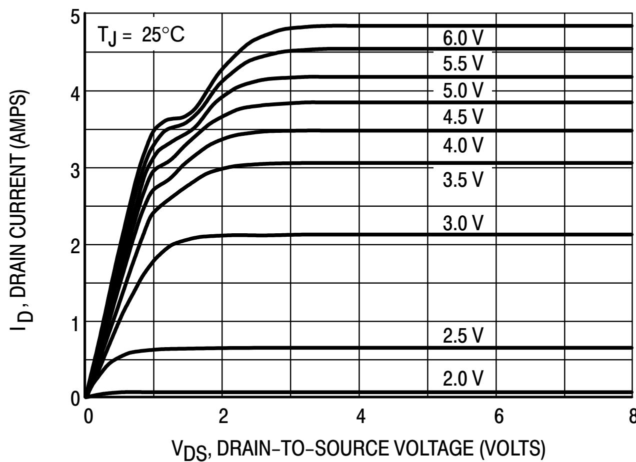


**Figure 1. Output Characteristics**

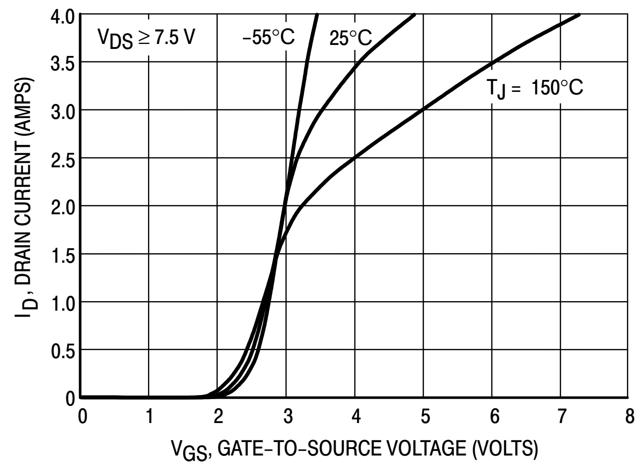


**Figure 2. Transfer Function**

### THE SMARTDISCRETES CONCEPT

From a standard power MOSFET process, several active and passive elements can be obtained that provide on–chip protection to the basic power device. Such elements require only a small increase in silicon area and/or the addition of one masking layer to the process. The resulting device exhibits significant improvements in ruggedness and reliability as well as system cost reduction. The SMARTDISCRETES device functions can now provide an economical alternative to smart power ICs for power applications requiring low on–resistance, high voltage and high current.

These devices are designed for applications that require a rugged power switching device with short circuit protection that can be directly interfaced to a microcontroller unit (MCU). Ideal applications include automotive fuel injector driver, incandescent lamp driver or other applications where a high in–rush current or a shorted load condition could occur.

### OPERATION IN THE CURRENT LIMIT MODE

The amount of time that an unprotected device can withstand the current stress resulting from a shorted load before its maximum junction temperature is exceeded is dependent upon a number of factors that include the amount of heatsinking that is provided, the size or rating of the device, its initial junction temperature, and the supply voltage. Without some form of current limiting, a shorted load can raise a device's junction temperature beyond the maximum rated operating temperature in only a few milliseconds.

Even with no heatsink, the MLP2N06CL can withstand a shorted load powered by an automotive battery (10 to 14 Volts) for almost a second if its initial operating temperature is under 100°C. For longer periods of operation in the current–limited mode, device heatsinking can extend operation from several seconds to indefinitely depending on the amount of heatsinking provided.

### SHORT CIRCUIT PROTECTION AND THE EFFECT OF TEMPERATURE

The on–chip circuitry of the MLP2N06CL offers an integrated means of protecting the MOSFET component from high in–rush current or a shorted load. As shown in the schematic diagram, the current limiting feature is provided by an NPN transistor and integral resistors R1 and R2. R2 senses the current through the MOSFET and forward biases the NPN transistor's base as the current increases. As the NPN turns on, it begins to pull gate drive current through R1, dropping the gate drive voltage across it, and thus lowering the voltage across the gate–to–source of the power MOSFET and limiting the current. The current limit is temperature dependent as shown in Figure 3, and decreases from about 2.3 Amps at 25°C to about 1.3 Amps at 150°C.

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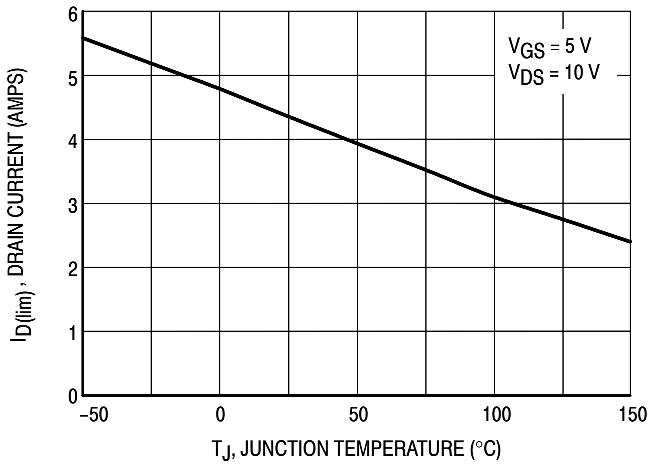


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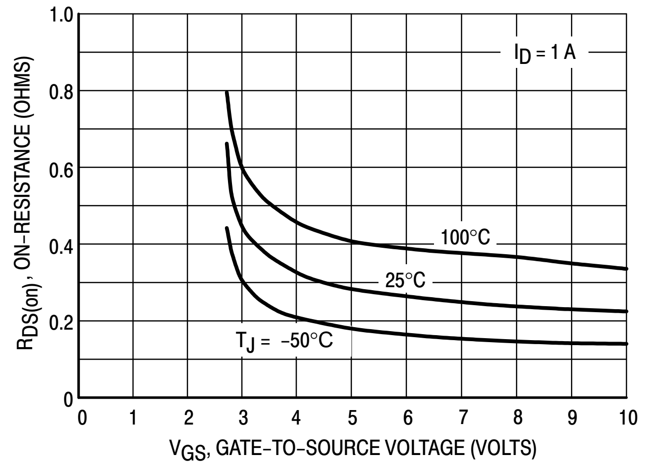
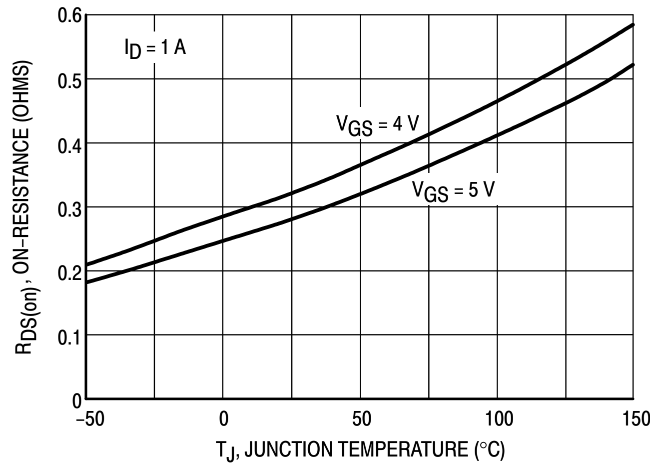



**Figure 4. $R_{DS(on)}$ Variation With Gate−To−Source Voltage**

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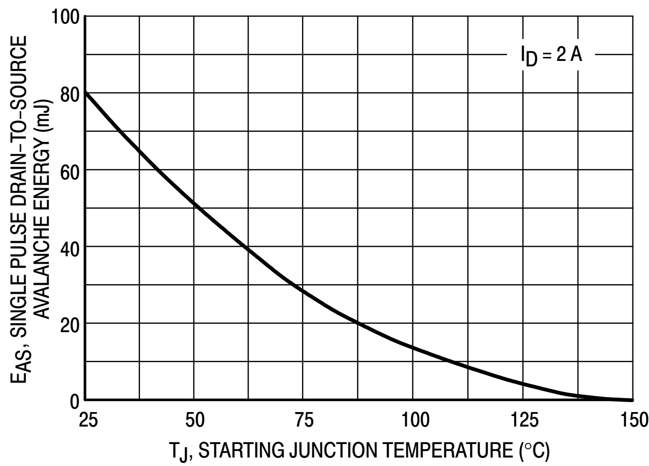
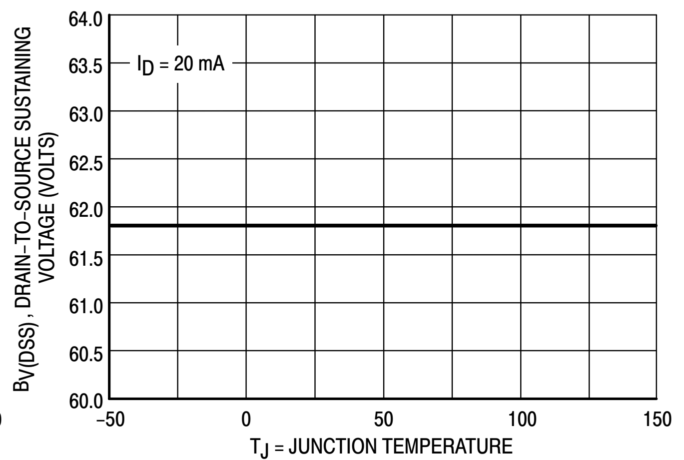



**Figure 6. Maximum Avalanche Energy versus Starting Junction Temperature**

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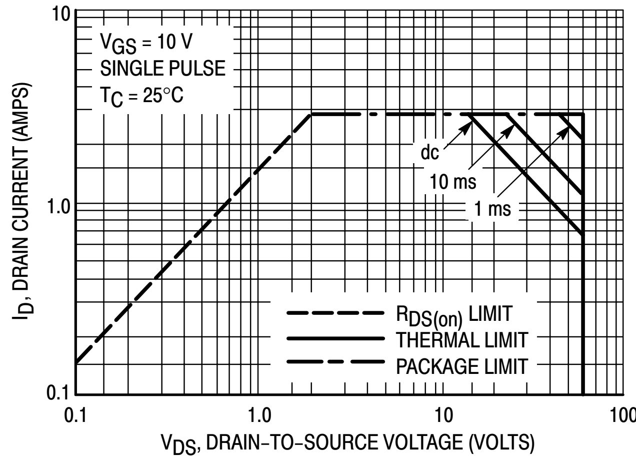


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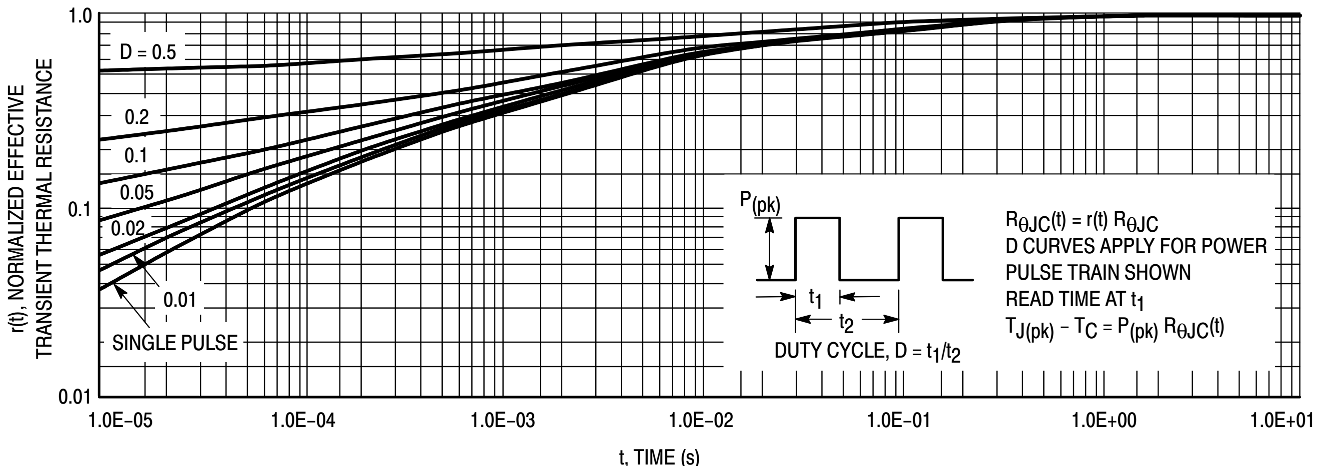


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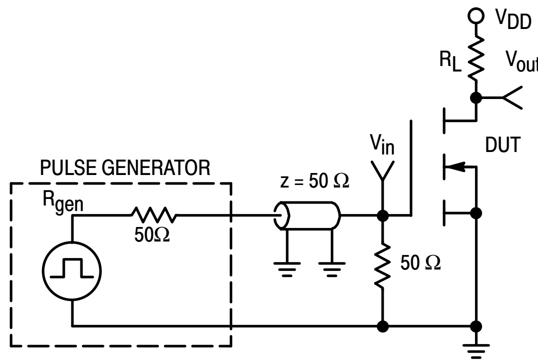


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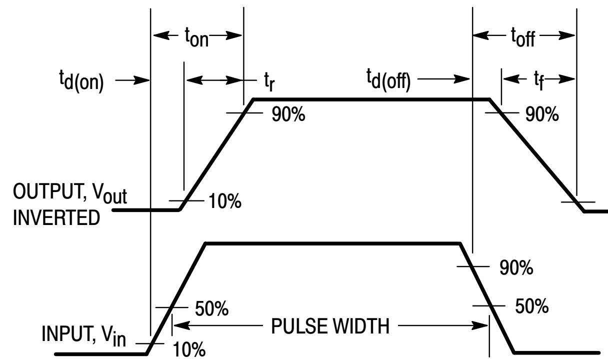


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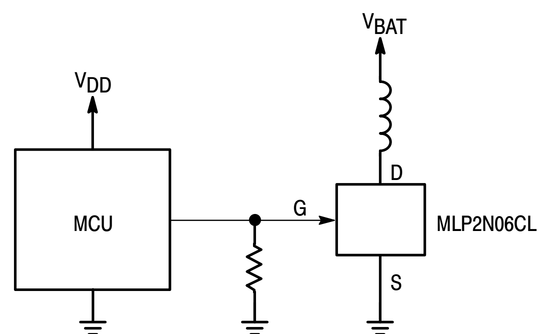

# MMBF0201NLT1

**Preferred Device**

# Power MOSFET 300 mAmps, 20 Volts

## N–Channel SOT–23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

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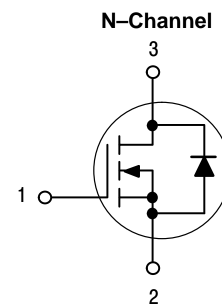
**300 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 1 Ω**

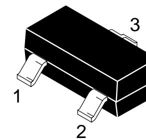
**N–Channel**



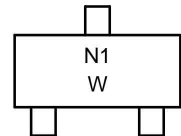

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Pulsed Drain Current ($t_p$ ≤ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>300<br>240<br>750 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C(1) | $P_D$ | 225 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM**

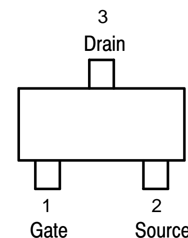



**SOT–23**
**CASE 318**
**STYLE 21**




N1 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMBF0201NLT1 | SOT–23 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 300 mAdc) | | | – | 0.75 | 1.0 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 100 mAdc) | | | – | 1.0 | 1.4 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | $g_{FS}$ | – | 450 | – | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 45 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 25 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 5.0 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 300 mAdc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 2.5 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 15 | – | |
| Fall Time | | $t_f$ | – | 0.8 | – | |
| Gate Charge (See Figure 5) | | $Q_T$ | – | 1400 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.3 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 2.) | | $V_{SD}$ | – | 0.85 | – | V |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

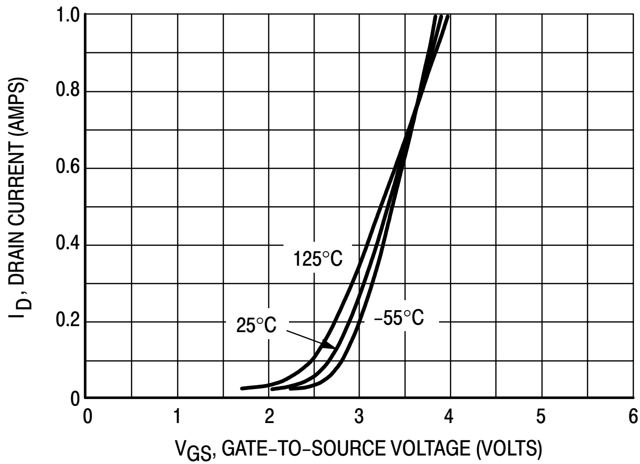



**Figure 1. Transfer Characteristics**

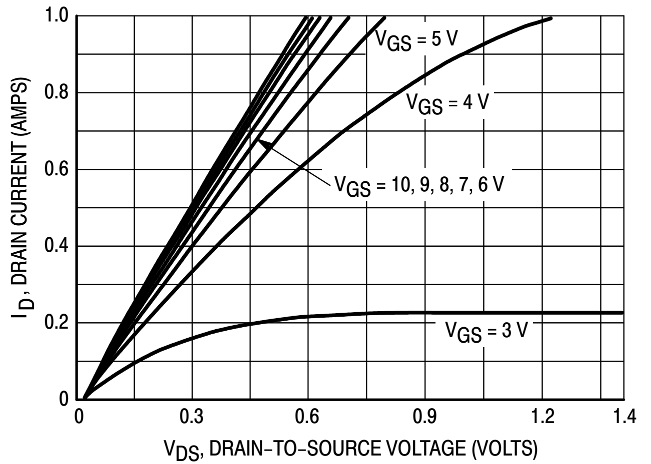



**Figure 2. On–Region Characteristics**

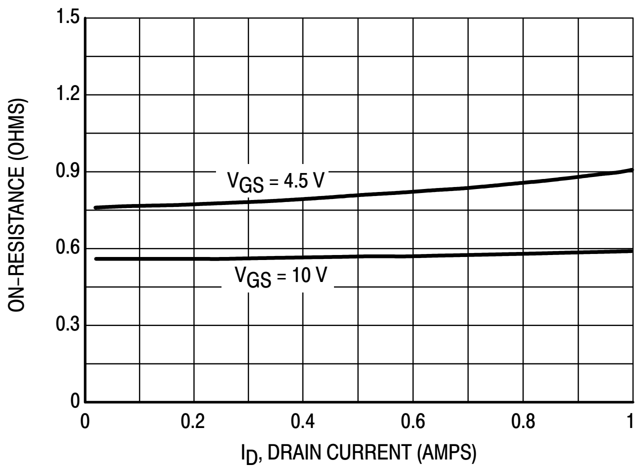



**Figure 3. On–Resistance versus Drain Current**

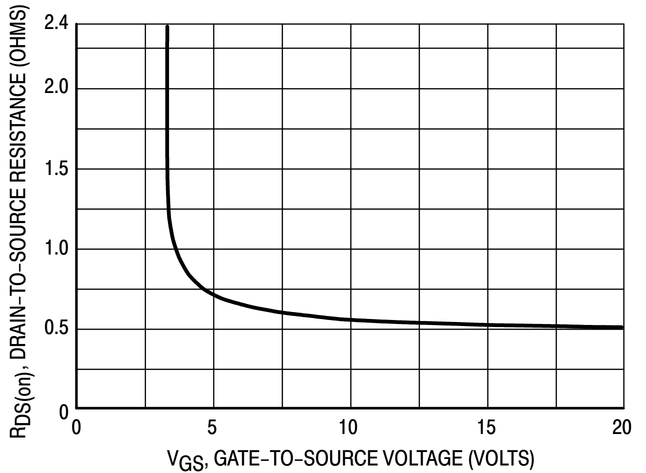



**Figure 4. On–Resistance versus Gate–to–Source Voltage**

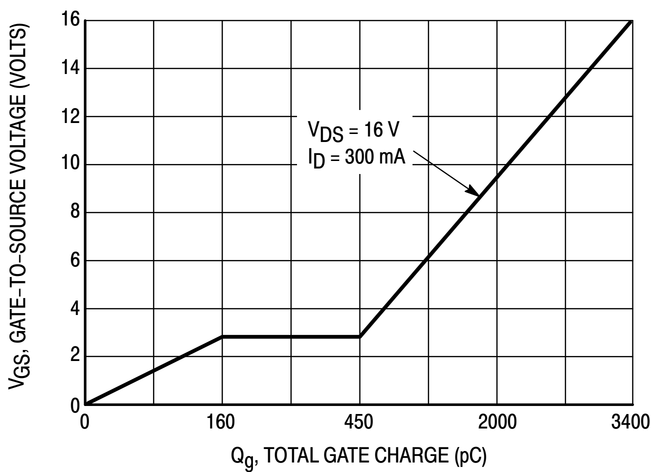



**Figure 5. Gate Charge**

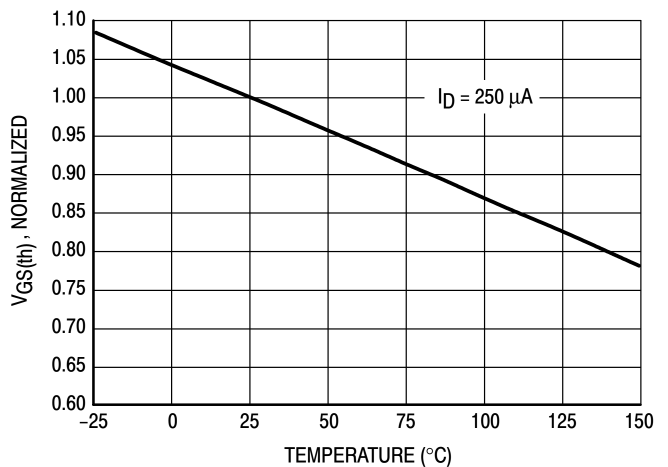



**Figure 6. Threshold Voltage Variance Over Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

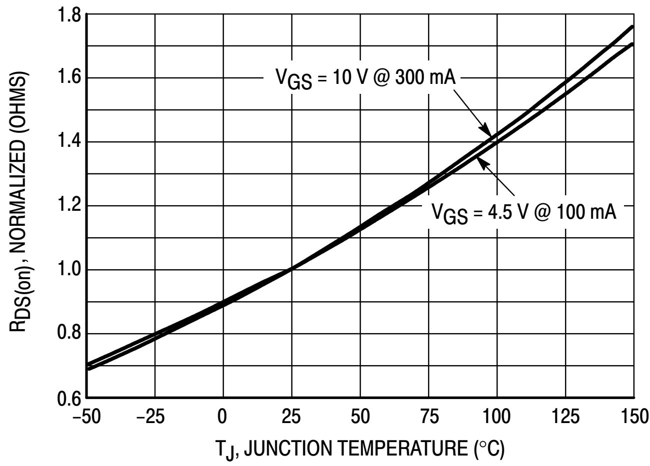



**Figure 7. On−Resistance versus Junction Temperature**

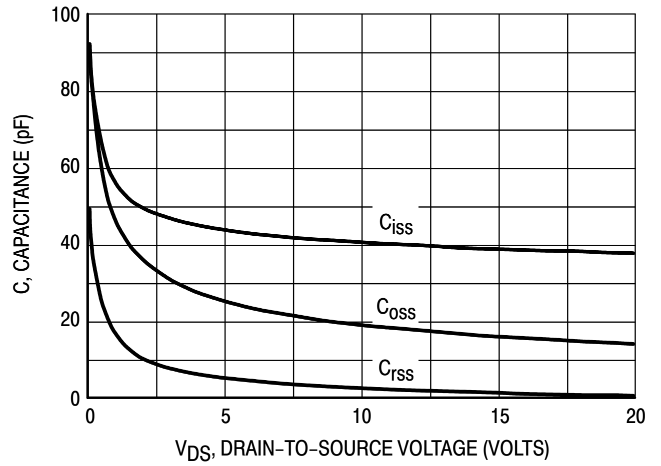



**Figure 8. Capacitance**

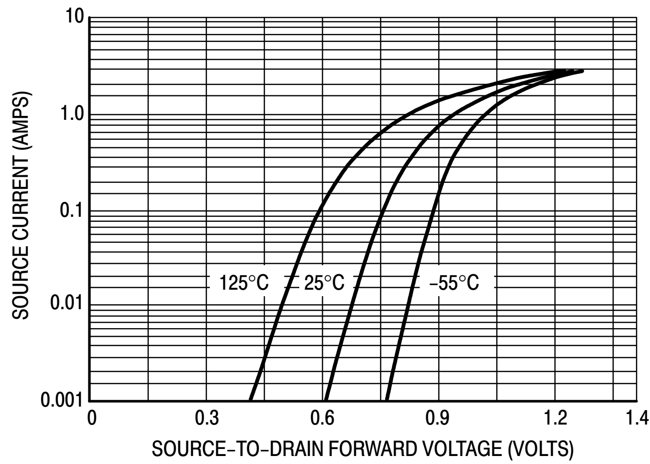
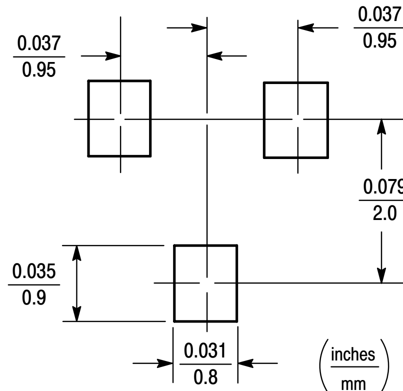



**Figure 9. Source−to−Drain Forward Voltage versus Continuous Current ($I_S$)**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMBF0202PLT1

**Preferred Device**

# Power MOSFET 300 mAmps, 20 Volts

## P–Channel SOT–23

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SOT–23 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Pulsed Drain Current ($t_p$ ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>300<br>240<br>750 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 225 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 625 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

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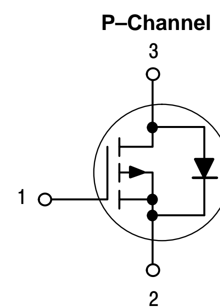
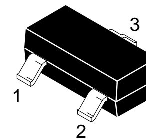
**300 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 1.4 Ω**

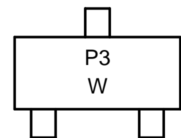
**P–Channel**




**MARKING DIAGRAM**

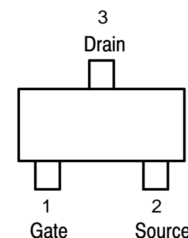



**SOT–23**
**CASE 318**
**STYLE 21**




P3 = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMBF0202PLT1 | SOT–23 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | | – | 0.9 | 1.4 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 50 mAdc) | | | – | 2.0 | 3.5 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | $g_{FS}$ | – | 600 | – | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 50 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 45 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 20 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –15 Vdc, $R_L$ = 75 Ω, $I_D$ = 200 mAdc, $V_{GEN}$ = –10 V, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge (See Figure 5) | ($V_{DS}$ = 16 V, $V_{GS}$ = 10 V, $I_D$ = 200 mA) | $Q_T$ | – | 2700 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.3 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 3.) | | $V_{SD}$ | – | 1.5 | – | V |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

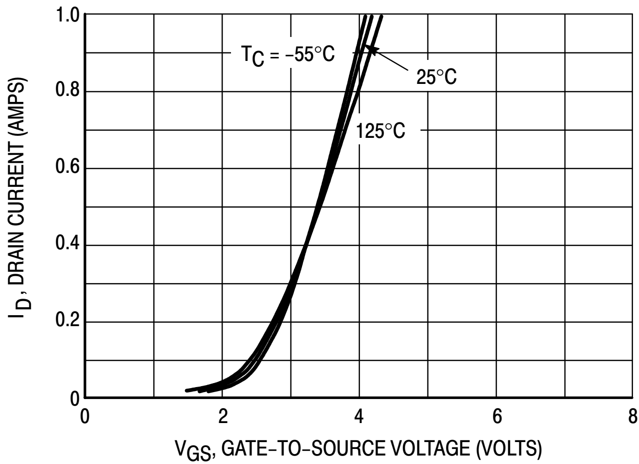



**Figure 1. Transfer Characteristics**

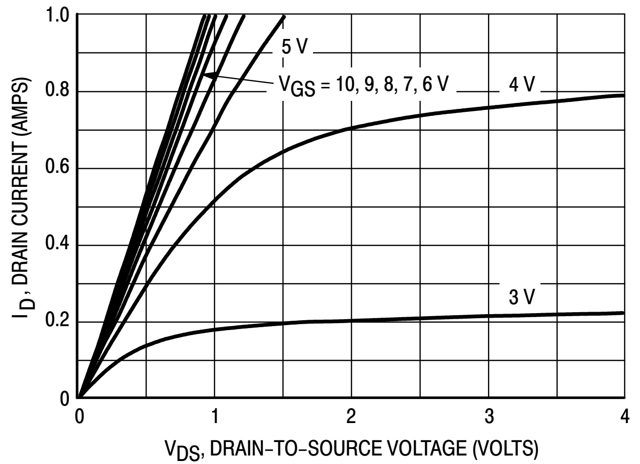



**Figure 2. On–Region Characteristics**

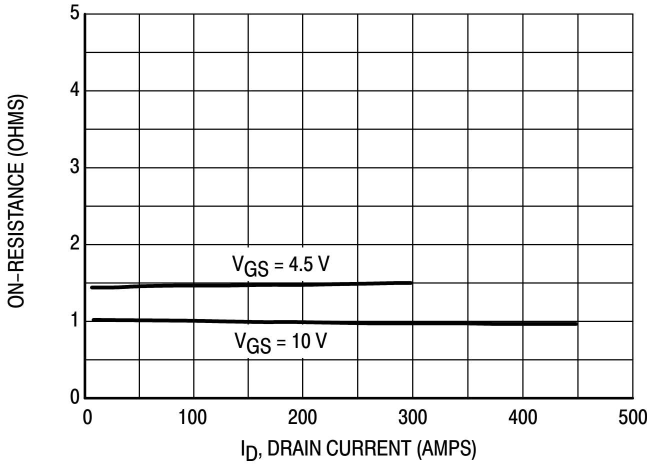



**Figure 3. On–Resistance versus Drain Current**

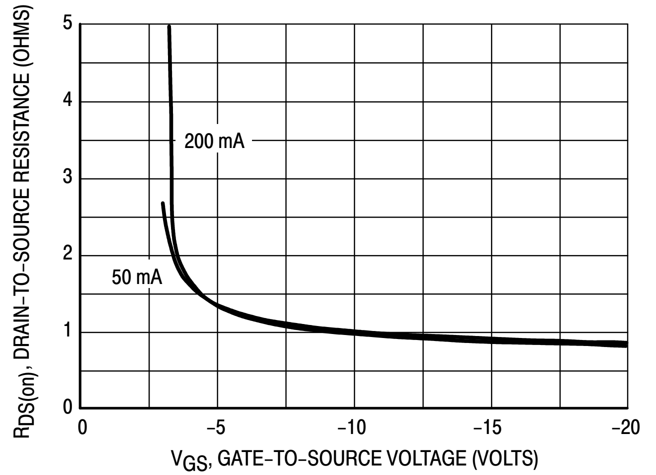



**Figure 4. On–Resistance versus Gate–to–Source Voltage**

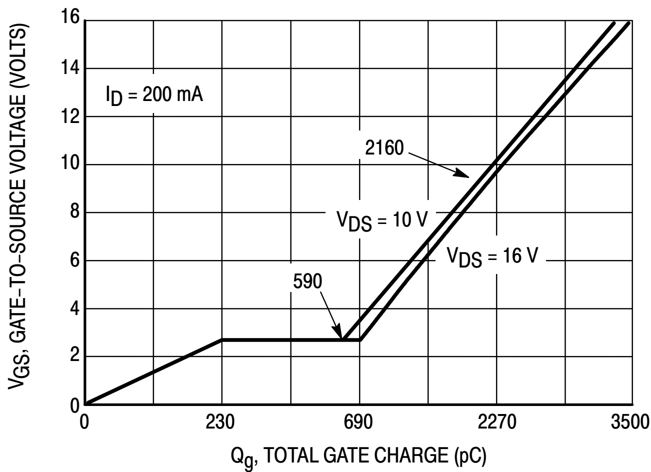



**Figure 5. Gate Charge**

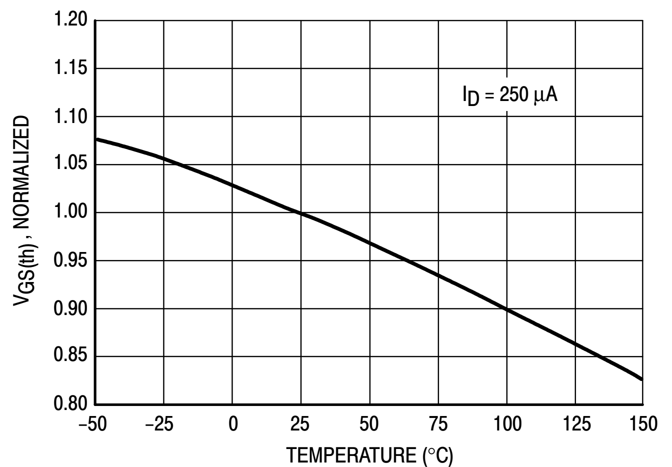



**Figure 6. Threshold Voltage Variance Over Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

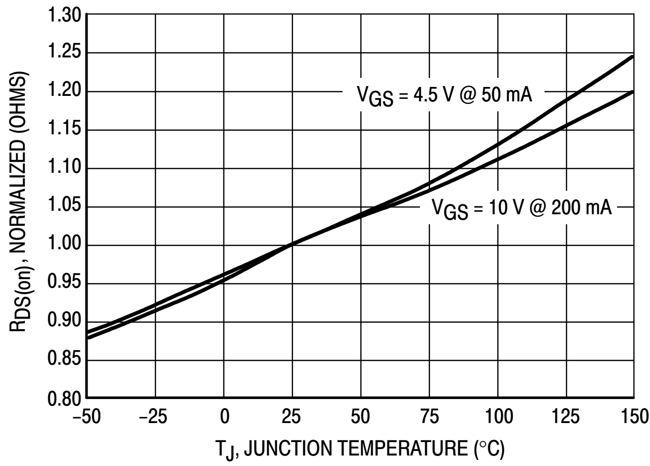



**Figure 7. On–Resistance versus Junction Temperature**

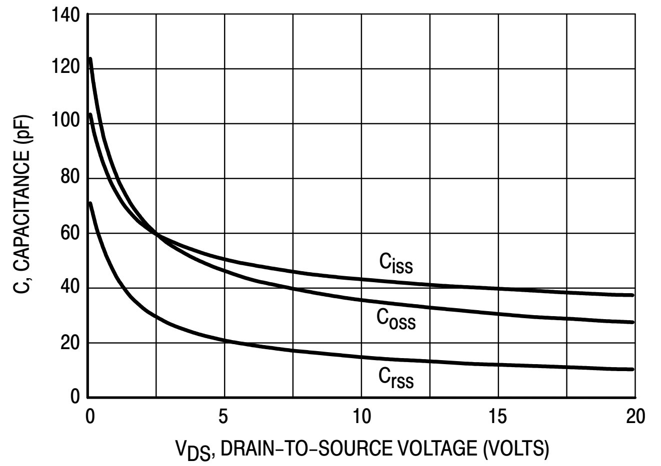



**Figure 8. Capacitance**

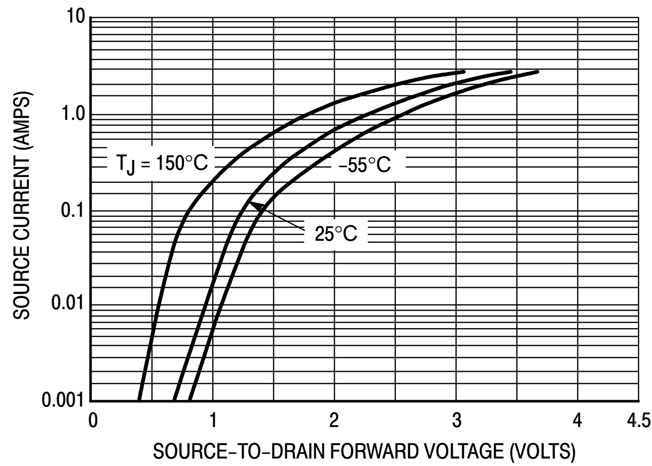
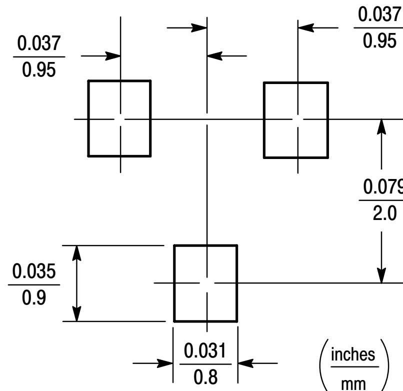



**Figure 9. Source–to–Drain Forward Voltage versus Continuous Current ($I_S$)**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMBF1374T1

Preferred Device

## Small Signal MOSFET 50 mAmps, 30 Volts

### N–Channel SC–70/SOT–323

**ON Semiconductor™**

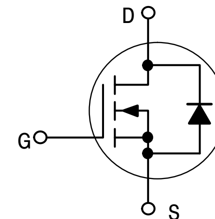
http://onsemi.com

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SC–70/SOT–323 Surface Mount Package Saves Board Space

**50 mAMPS**
**30 VOLTS**
**$R_{DS(on)}$ = 50 Ω**

**N–Channel**

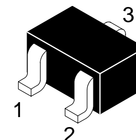



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

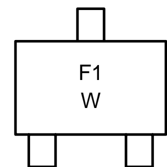
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Pulse | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C | $I_D$ | 50 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) Derate above 25°C | $P_D$ | 100 | mW |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**MARKING DIAGRAM**

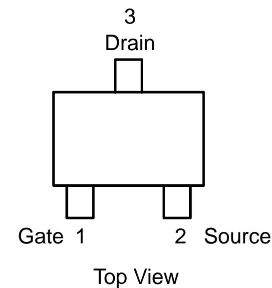



**SC–70/SOT–323**
**CASE 419**
**STYLE 8**




F1 = Device Code
W = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMBF1374T1 | SC–70/ SOT–323 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 1.0 | μAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | – | 2 | 2.8 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 10 mAdc) | | $r_{DS(on)}$ | – | 27 | 50 | Ω |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 50 mAdc) | | $g_{FS}$ | – | 450 | – | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 45 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 25 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 5.0 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 50 mAdc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 2.5 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 15 | – | |
| Fall Time | | $t_f$ | – | 0.8 | – | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

# MMBF170LT1

## Power MOSFET 500 mAmps, 60 Volts

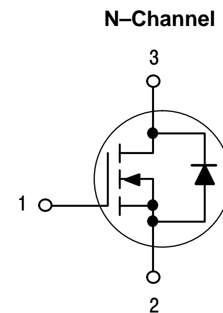
### N–Channel SOT–23

**ON Semiconductor™**

http://onsemi.com

**500 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 5 Ω**

**N–Channel**




**MAXIMUM RATINGS**

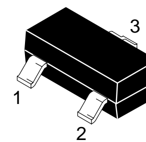
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage | $V_{DGS}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq 50\ \mu s$) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 0.5<br>0.8 | Adc |

**THERMAL CHARACTERISTICS**

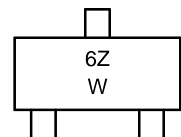
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Total Device Dissipation FR–5 Board<br>(Note 1.) $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 225<br>1.8 | mW<br>mW/°C |
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 556 | °C/W |
| Junction and Storage Temperature | $T_J$, $T_{stg}$ | –55 to +150 | °C |

1. FR–5 = 1.0 × 0.75 × 0.062 in.

**MARKING DIAGRAM**

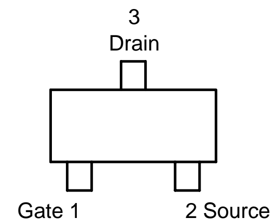



**SOT–23**
**CASE 318**
**STYLE 21**




6Z = Device Code
W = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMBF170LT1 | SOT–23 | 3000 Tape & Reel |
| MMBF170LT3 | SOT–23 | 10,000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 μA) | | $V_{(BR)DSS}$ | 60 | – | Vdc |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | 10 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | | $V_{GS(th)}$ | 0.8 | 3.0 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mA) | | $r_{DS(on)}$ | – | 5.0 | Ω |
| On–State Drain Current ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0) | | $I_{D(off)}$ | – | 0.5 | μA |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 V, f = 1.0 MHz) | | $C_{iss}$ | – | 60 | pF |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 500 mA, $R_{gen}$ = 50 Ω) Figure 1 | $t_{d(on)}$ | – | 10 | ns |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 10 | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

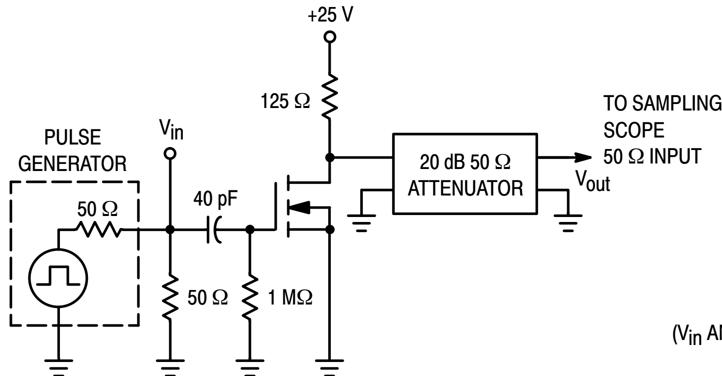



**Figure 1. Switching Test Circuit**

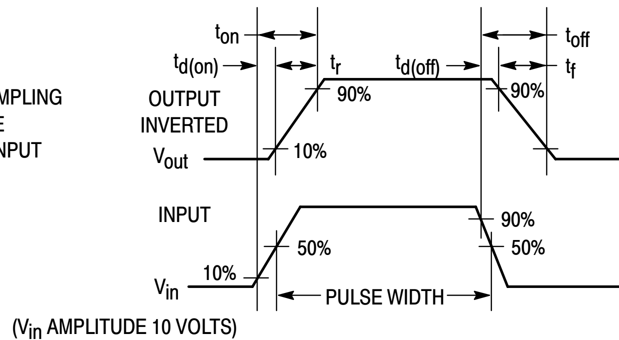



**Figure 2. Switching Waveform**

## TYPICAL ELECTRICAL CHARACTERISTICS

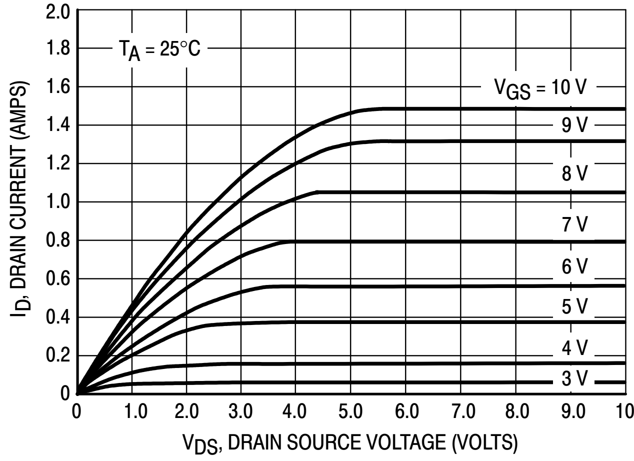



**Figure 3. Ohmic Region**

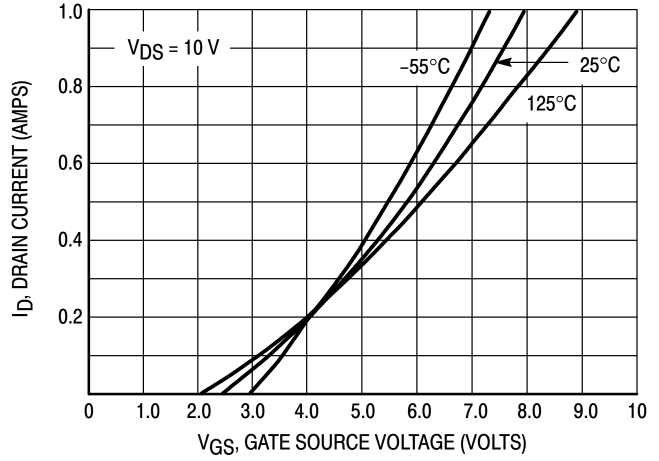



**Figure 4. Transfer Characteristics**

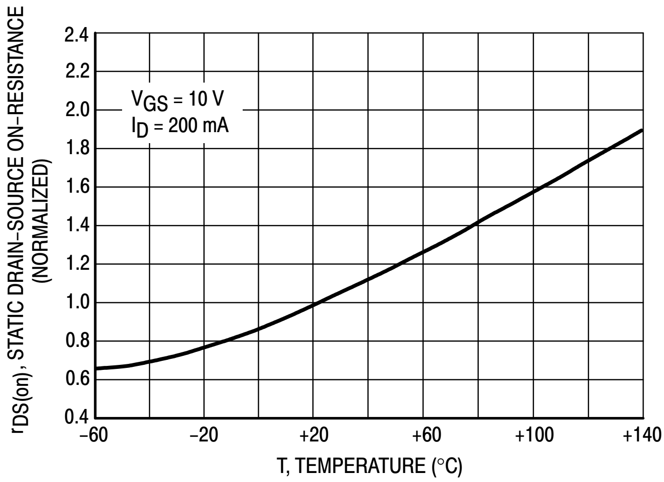



**Figure 5. Temperature versus Static Drain–Source On–Resistance**

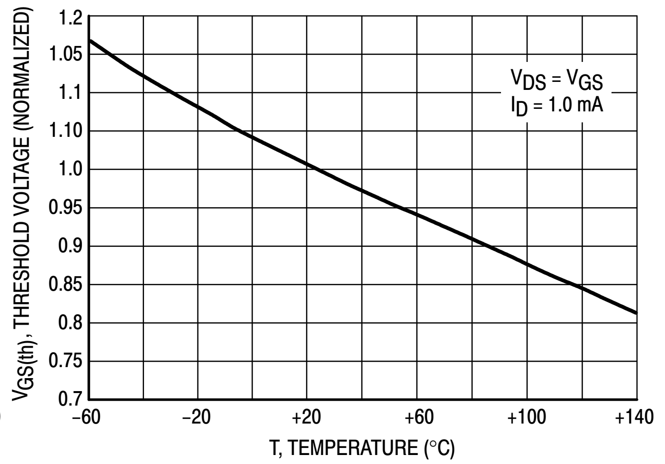
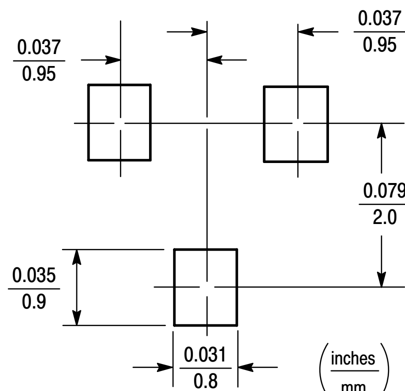



**Figure 6. Temperature versus Gate Threshold Voltage**

# INFORMATION FOR USING THE SOT–23 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–23 POWER DISSIPATION

The power dissipation of the SOT–23 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–23 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 225 milliwatts.

$$P_D = \frac{150°C - 25°C}{556°C/W} = 225 \text{ milliwatts}$$

The 556°C/W for the SOT–23 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 225 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–23 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMBF2201NT1

**Preferred Device**

# Power MOSFET 300 mAmps, 20 Volts

## N–Channel SC–70/SOT–323

**ON Semiconductor™**

http://onsemi.com

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SC–70/SOT–323 Surface Mount Package Saves Board Space

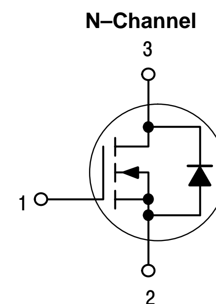
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Pulsed Drain Current ($t_p$ ≤ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>300<br>240<br>750 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Derate above 25°C | $P_D$ | 150<br>1.2 | mW<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 833 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

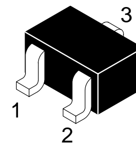
1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**300 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 1 Ω**

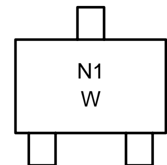
**N–Channel**




**MARKING DIAGRAM**

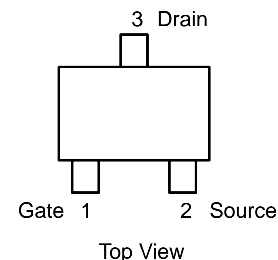



**SC–70/SOT–323**
**CASE 419**
**STYLE 8**




N1 = Device Code
W = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMBF2201NT1 | SC–70/ SOT–323 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 300 mAdc) | | | – | 0.75 | 1.0 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 100 mAdc) | | | – | 1.0 | 1.4 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | $g_{FS}$ | – | 450 | – | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 45 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 25 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 5.0 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 300 mAdc, $R_L$ = 50 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 2.5 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 15 | – | |
| Fall Time | | $t_f$ | – | 0.8 | – | |
| Gate Charge (See Figure 5) | | $Q_T$ | – | 1400 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.3 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 3.) | | $V_{SD}$ | – | 0.85 | – | V |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL CHARACTERISTICS

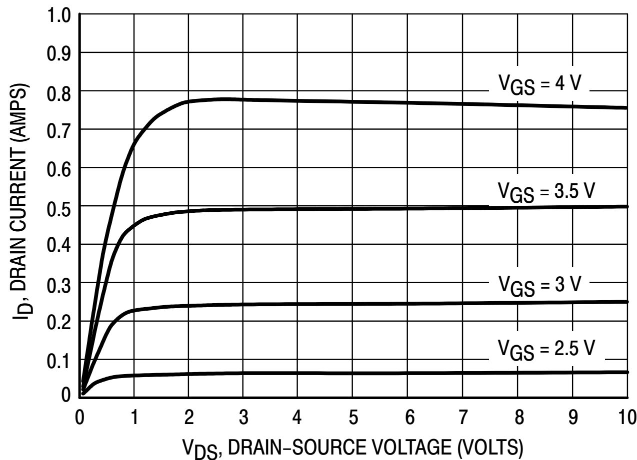



**Figure 1. Typical Drain Characteristics**

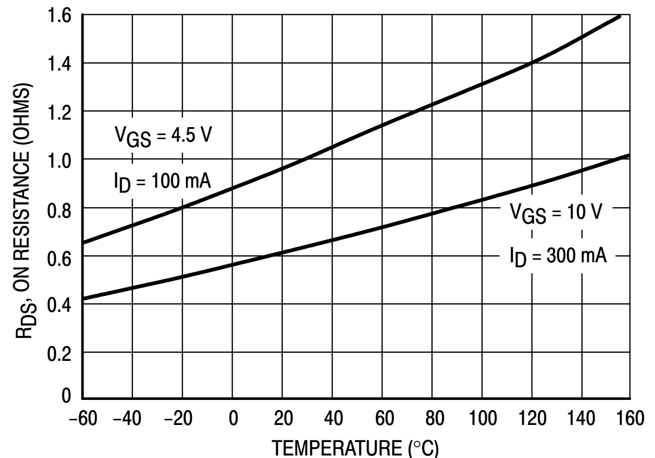



**Figure 2. On Resistance versus Temperature**

## TYPICAL CHARACTERISTICS

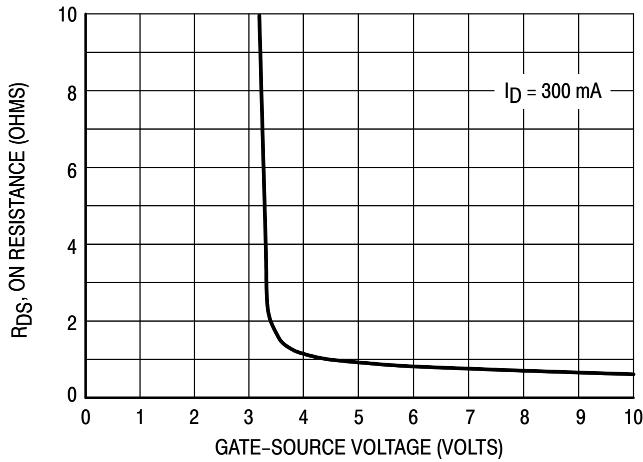



**Figure 3. On Resistance versus Gate–Source Voltage**

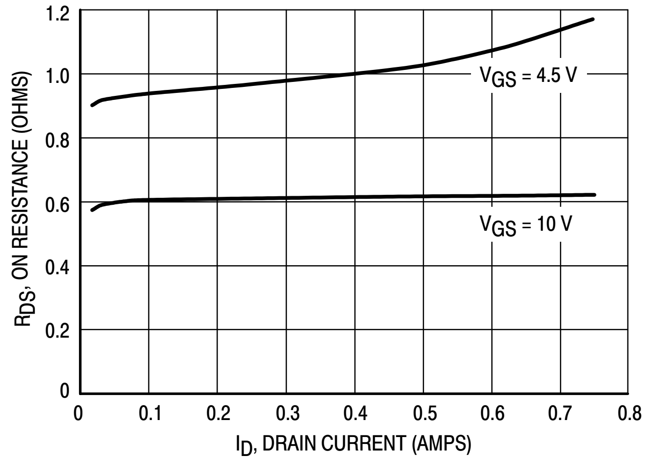



**Figure 4. On Resistance versus Drain Current**

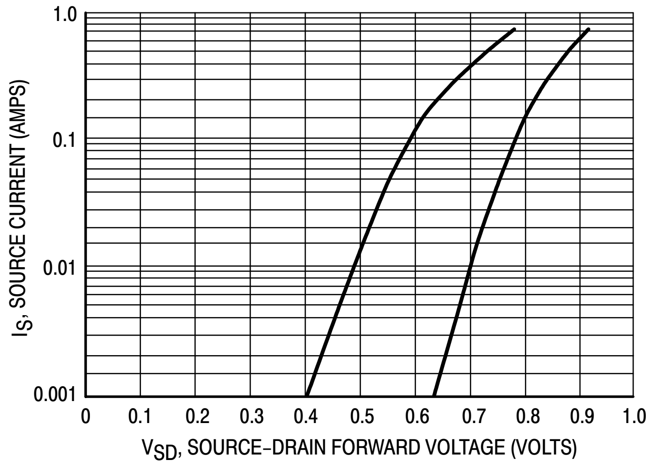



**Figure 5. Source–Drain Forward Voltage**

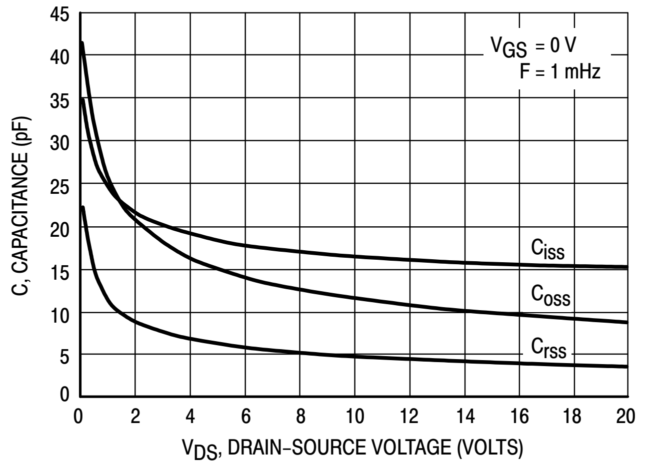



**Figure 6. Capacitance Variation**

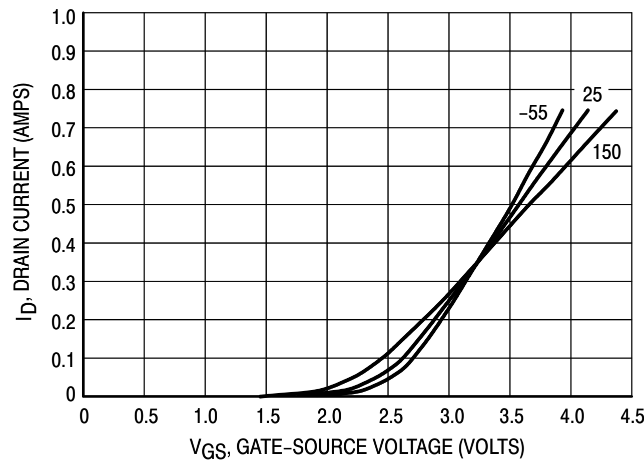
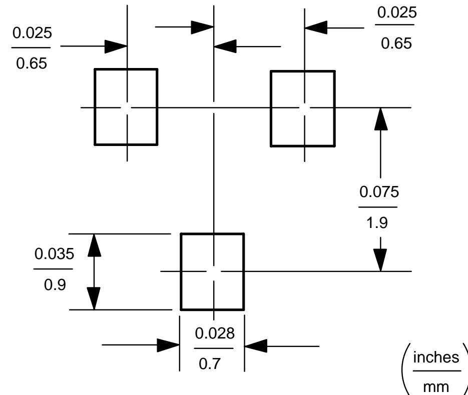



**Figure 7. Transfer Characteristics**

# INFORMATION FOR USING THE SC–70/SOT–323 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SC–70/SOT–323 POWER DISSIPATION

The power dissipation of the SC–70/SOT–323 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SC–70 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SC–70/SOT–323 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SC–70/SOT–323 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMBF2202PT1

Preferred Device

# Power MOSFET
# 300 mAmps, 20 Volts
## P–Channel SC–70/SOT–323

These miniature surface mount MOSFETs low $R_{DS(on)}$ assure minimal power loss and conserve energy, making these devices ideal for use in small power management circuitry. Typical applications are dc–dc converters, power management in portable and battery–powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature SC–70/SOT–323 Surface Mount Package Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Pulsed Drain Current ($t_p \leq 10\ \mu s$) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>300<br>240<br>750 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Derate above 25°C | $P_D$ | 150<br>1.2 | mW<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 833 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, for 10 seconds | $T_L$ | 260 | °C |

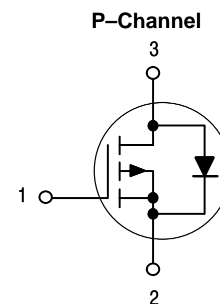
1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**ON Semiconductor™**

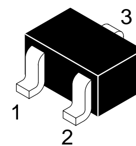
http://onsemi.com

**300 mAMPS**
**20 VOLTS**
**$R_{DS(on)}$ = 2.2 Ω**

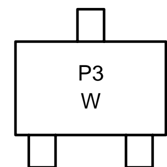
P–Channel




MARKING DIAGRAM

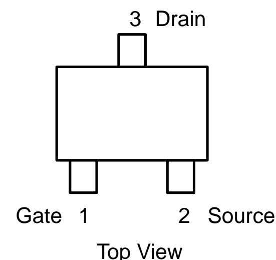



SC–70/SOT–323
CASE 419
STYLE 8




P3 = Device Code
W = Work Week

PIN ASSIGNMENT




Top View

ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| MMBF2202PT1 | SC–70/ SOT–323 | 3000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.4 | Vdc |
| Static Drain–to–Source On–Resistance | | $r_{DS(on)}$ | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | | – | 1.5 | 2.2 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 50 mAdc) | | | – | 2.0 | 3.5 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 200 mAdc) | | $g_{FS}$ | – | 600 | – | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 5.0 V) | $C_{iss}$ | – | 50 | – | pF |
| Output Capacitance | ($V_{DS}$ = 5.0 V) | $C_{oss}$ | – | 45 | – | |
| Transfer Capacitance | ($V_{DG}$ = 5.0 V) | $C_{rss}$ | – | 20 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = –15 Vdc, $R_L$ = 75 Ω, $I_D$ = 200 mAdc, $V_{GEN}$ = –10 V, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 2.5 | – | ns |
| Rise Time | | $t_r$ | – | 1.0 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | – | |
| Fall Time | | $t_f$ | – | 8.0 | – | |
| Gate Charge (See Figure 5) | ($V_{DS}$ = 16 V, $V_{GS}$ = 10 V, $I_D$ = 200 mA) | $Q_T$ | – | 2700 | – | pC |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Continuous Current | | $I_S$ | – | – | 0.3 | A |
| Pulsed Current | | $I_{SM}$ | – | – | 0.75 | |
| Forward Voltage (Note 3.) | | $V_{SD}$ | – | 1.5 | – | V |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL CHARACTERISTICS

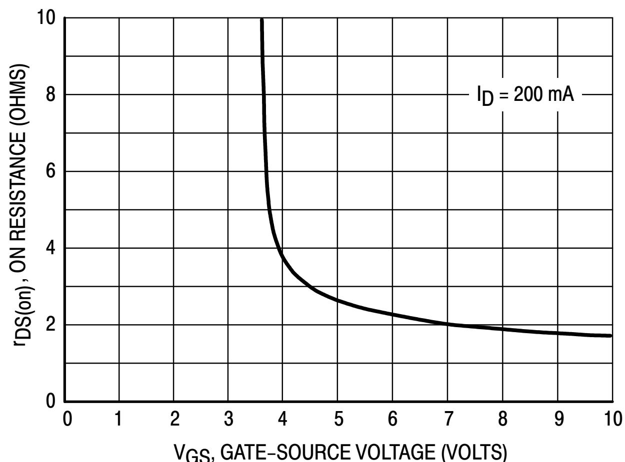



**Figure 1. On Resistance versus Gate–Source Voltage**

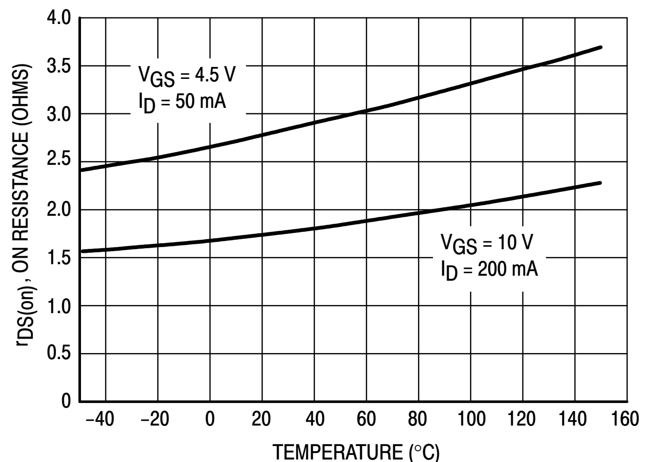



**Figure 2. On Resistance versus Temperature**

## TYPICAL CHARACTERISTICS

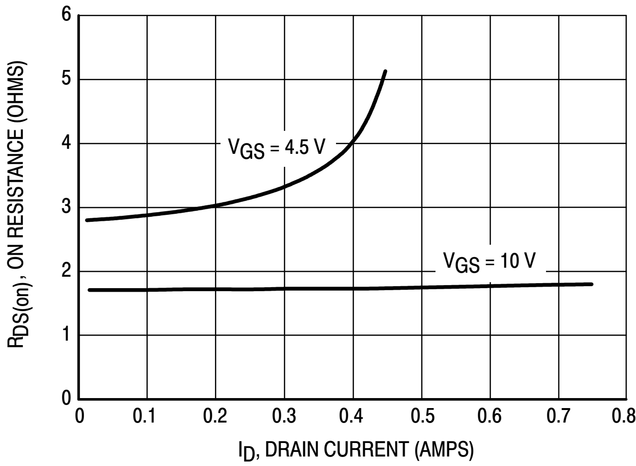



**Figure 3. On Resistance versus Drain Current**

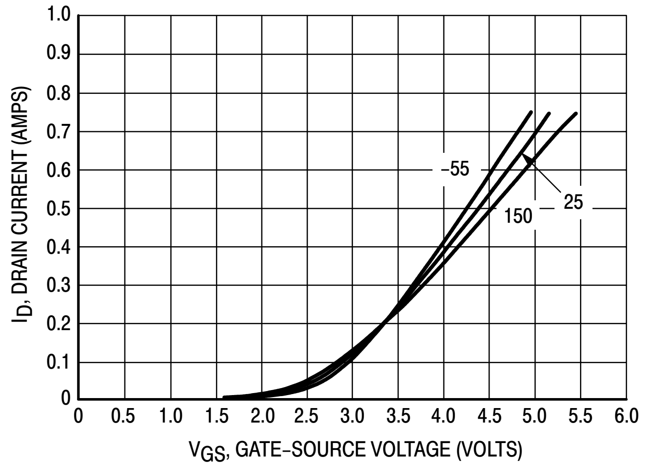



**Figure 4. Transfer Characteristics**

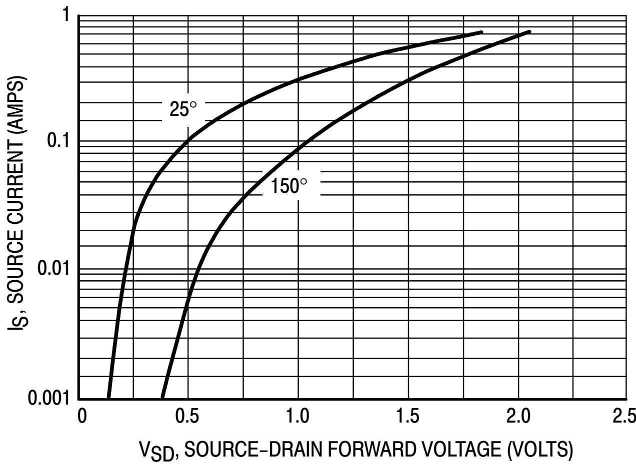



**Figure 5. Source–Drain Forward Voltage**

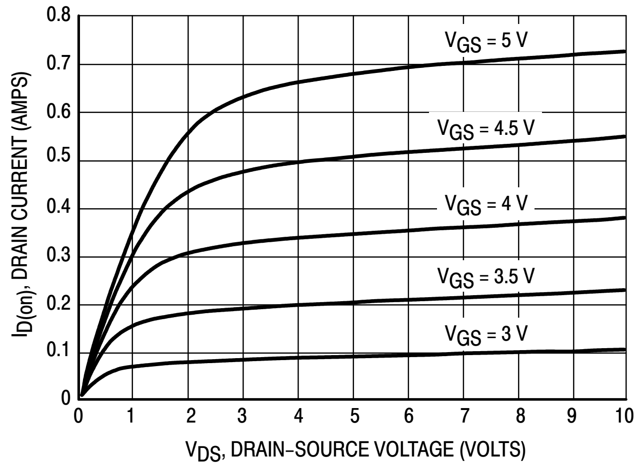



**Figure 6. On Region Characteristics**

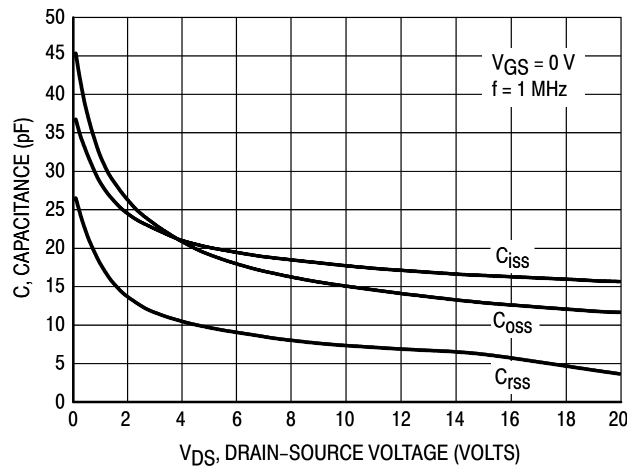
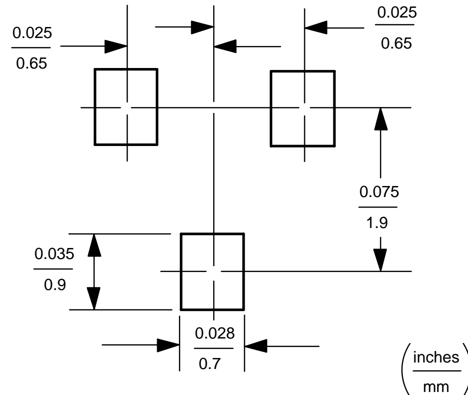



**Figure 7. Capacitance Variation**

# INFORMATION FOR USING THE SC–70/SOT–323 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SC–70/SOT–323 POWER DISSIPATION

The power dissipation of the SC–70/SOT–323 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SC–70/SOT–323 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150°C - 25°C}{833°C/W} = 150 \text{ milliwatts}$$

The 833°C/W for the SC–70/SOT–323 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SC–70/SOT–323 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMDF1300

# Power MOSFET 3 Amps, 25 Volts

## Complementary SO–8, Dual

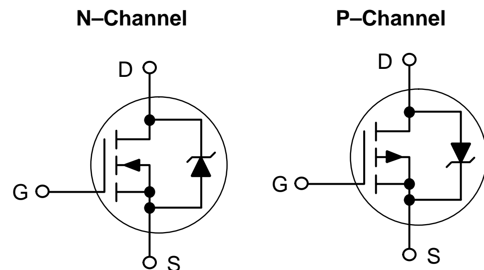
**ON Semiconductor™**

**http://onsemi.com**

**3 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 100 mΩ (N–Channel)**
**$R_{DS(on)}$ = 210 mΩ (P–Channel)**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed, with Soft Recovery

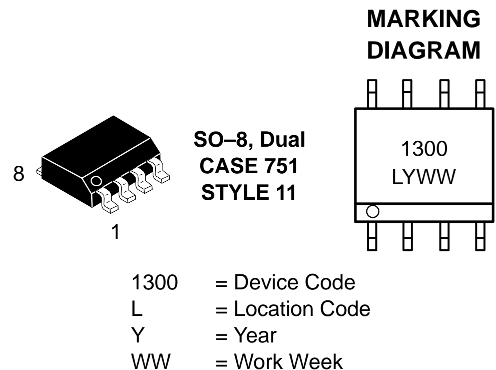



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous<br>N–Channel<br>P–Channel | $I_D$ | <br>3.0<br>2.0 | Adc |
| Drain Current – Pulsed<br>N–Channel<br>P–Channel | $I_{DM}$ | <br>9.0<br>6.0 | Apk |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to +150 | °C |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 1.8 | Watts |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 3.0 Apk, L = 25 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 113 | mJ |
| Thermal Resistance – Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 66.3 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 sec. | $T_L$ | 260 | °C |

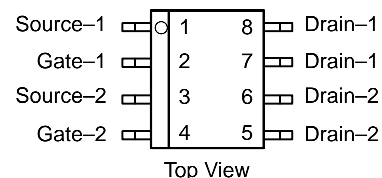
1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

**MARKING DIAGRAM**




1300 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF1300R2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | – | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | (N)<br>(P) | –<br>– | –<br>– | 1.0<br>1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | – | ±100 | nAdc |
| **ON CHARACTERISTICS** (Notes 2. & 3.) | | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | (N)<br>(P) | 1.0<br>1.0 | 1.5<br>2.0 | 2.0<br>3.0 | Vdc |
| Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.09<br>0.16 | 0.10<br>0.21 | Ohms |
| Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.13<br>0.30 | 0.16<br>0.375 | Ohms |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | (N)<br>(P) | 1.0<br>1.0 | –<br>– | –<br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 215<br>200 | 301<br>300 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 111<br>100 | 158<br>160 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 30<br>40 | 60<br>75 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 18<br>14 | 36<br>28 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 98<br>95 | 196<br>180 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 16<br>22 | 32<br>45 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 30<br>40 | 60<br>80 | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 3.3<br>7.0 | 5.0<br>10 | nC |
| | | $Q_1$ | (N)<br>(P) | –<br>– | 1.2<br>1.2 | –<br>– | |
| | | $Q_2$ | (N)<br>(P) | –<br>– | 2.0<br>2.5 | –<br>– | |
| | | $Q_3$ | (N)<br>(P) | –<br>– | 1.9<br>3.5 | –<br>– | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Negative signs for P–Channel device omitted for clarity.
4. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS – continued** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SOURCE–DRAIN DIODE CHARACTERISTICS** (Note 5.) | | | | | | | |
| Forward On–Voltage (Note 6.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | (N)<br>(P) | –<br>– | 1.0<br>1.3 | 1.4<br>1.7 | Vdc |
| Reverse Recovery Time | (N) ($I_D$ = 2.0 Adc, $V_{GS}$ = 0 Vdc dI$_S$/dt = 100 A/µs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 23<br>20 | –<br>– | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 18<br>13 | –<br>– | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 5.0<br>7.0 | –<br>– | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | (N)<br>(P) | –<br>– | 0.02<br>0.02 | –<br>– | µC |

5. Negative signs for P–Channel device omitted for clarity.
6. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

# MMDF1N05E

# Power MOSFET 1 Amp, 50 Volts

## N–Channel SO–8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided
- $I_{DSS}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 50 | Volts |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | Volts |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 2.0<br>10 | Amps |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 V, $V_{GS}$ = 10 V, $I_L$ = 2 Apk) | $E_{AS}$ | 300 | mJ |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 2.0 | Watts |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Temperature for Soldering, Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

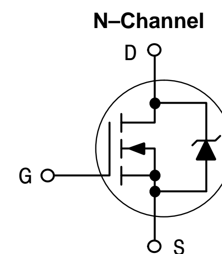
1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**ON Semiconductor™**

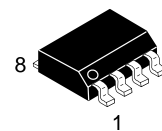
**http://onsemi.com**

**1 AMPERE**
**50 VOLTS**
**$R_{DS(on)}$ = 300 mΩ**

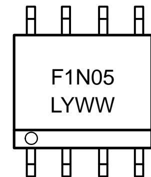
**N–Channel**




**MARKING DIAGRAM**

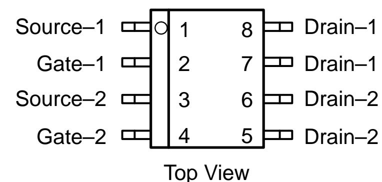



**SO–8, Dual**
**CASE 751**
**STYLE 11**




F1N05 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF1N05ER2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 250 μA) | | $V_{(BR)DSS}$ | 50 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 50 V, $V_{GS}$ = 0) | | $I_{DSS}$ | – | – | 250 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | – | 3.0 | Vdc |
| Drain–to–Source On–Resistance | | | | | | Ohms |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc) | | $R_{DS(on)}$ | – | – | 0.30 | |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 0.6 Adc) | | $R_{DS(on)}$ | – | – | 0.50 | |
| Forward Transconductance ($V_{DS}$ = 15 V, $I_D$ = 1.5 A) | | $g_{FS}$ | – | 1.5 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 330 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 160 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 50 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 V, $I_D$ = 1.5 A, $R_L$ = 10 Ω, $V_G$ = 10 V, $R_G$ = 50 Ω) | $t_{d(on)}$ | – | – | 20 | ns |
| Rise Time | | $t_r$ | – | – | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | – | 40 | |
| Fall Time | | $t_f$ | – | – | 25 | |
| Total Gate Charge | ($V_{DS}$ = 10 V, $I_D$ = 1.5 A, $V_{GS}$ = 10 V) | $Q_g$ | – | 12.5 | – | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.9 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 3.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** ($T_C$ = 25°C) | | | | | | |
| Forward Voltage (Note 2.) | ($I_S$ = 1.5 A, $V_{GS}$ = 0 V) ($dI_S/dt$ = 100 A/μs) | $V_{SD}$ | – | – | 1.6 | V |
| Reverse Recovery Time | | $t_{rr}$ | – | 45 | – | ns |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

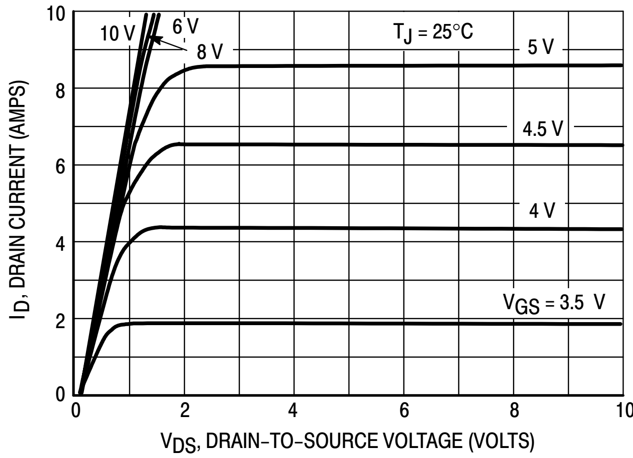



**Figure 1. On–Region Characteristics**

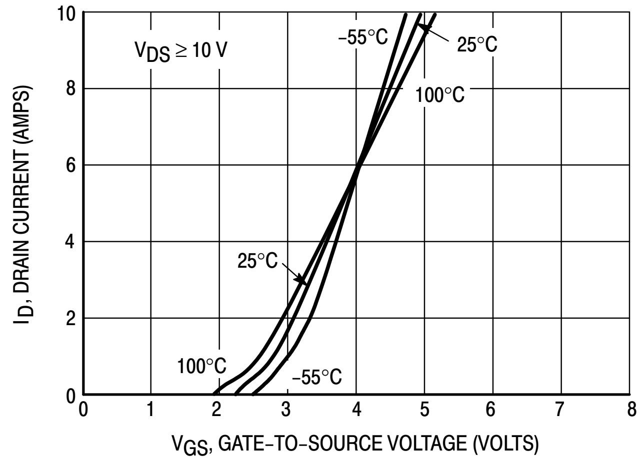



**Figure 2. Transfer Characteristics**

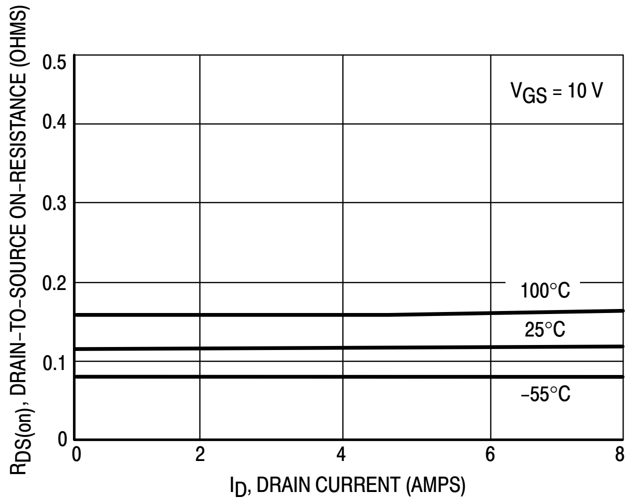



**Figure 3. On–Resistance versus Drain Current**

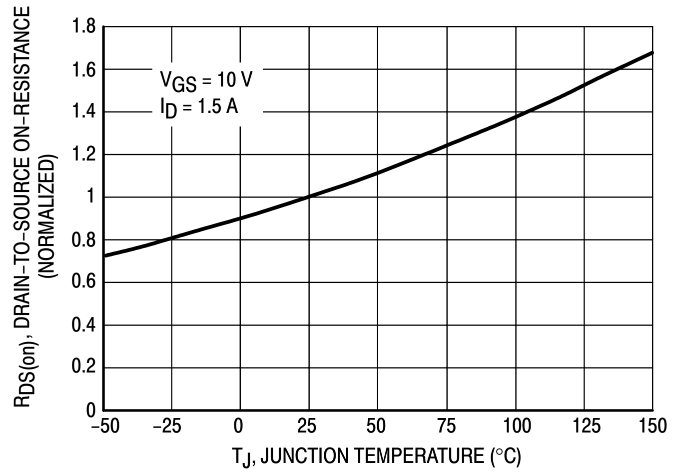



**Figure 4. On–Resistance Variation with Temperature**

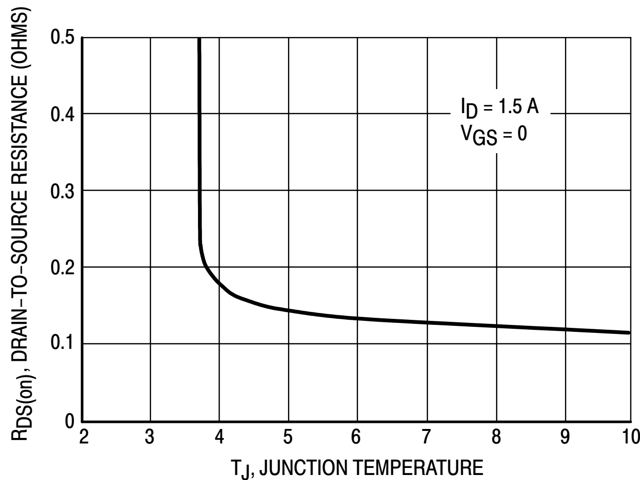



**Figure 5. On Resistance versus Gate–To–Source Voltage**

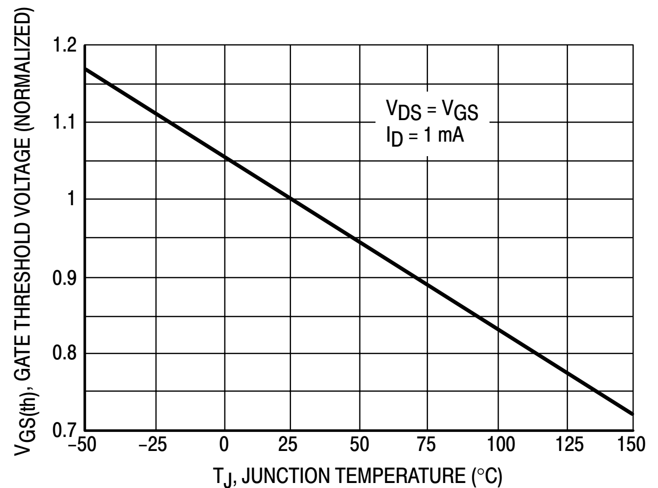



**Figure 6. Gate Threshold Voltage Variation with Temperature**

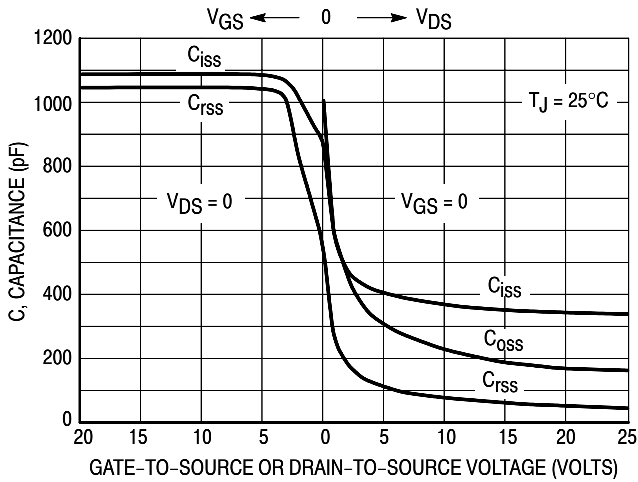



Figure 7. Capacitance Variation

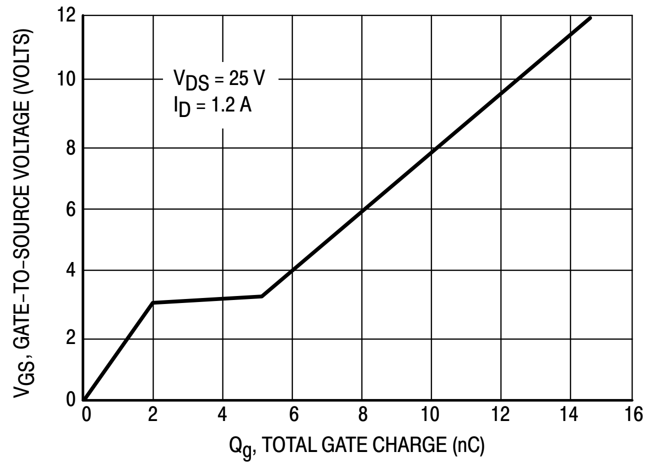



Figure 8. Gate Charge versus Gate–To–Source Voltage

## SAFE OPERATING AREA INFORMATION

### Forward Biased Safe Operating Area

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance – General Data and Its Use” provides detailed instructions.

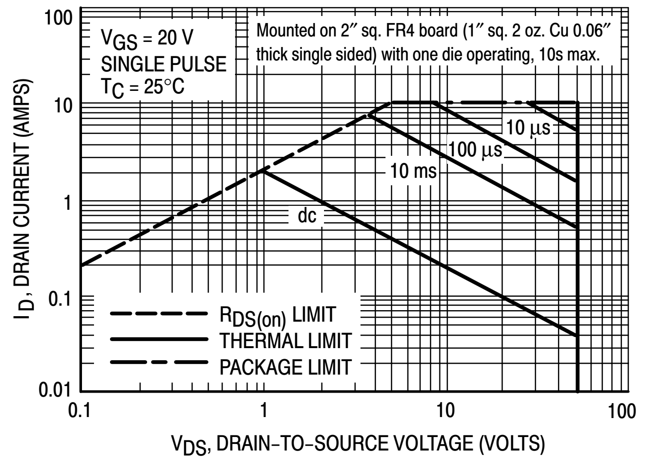



Figure 9. Maximum Rated Forward Biased Safe Operating Area

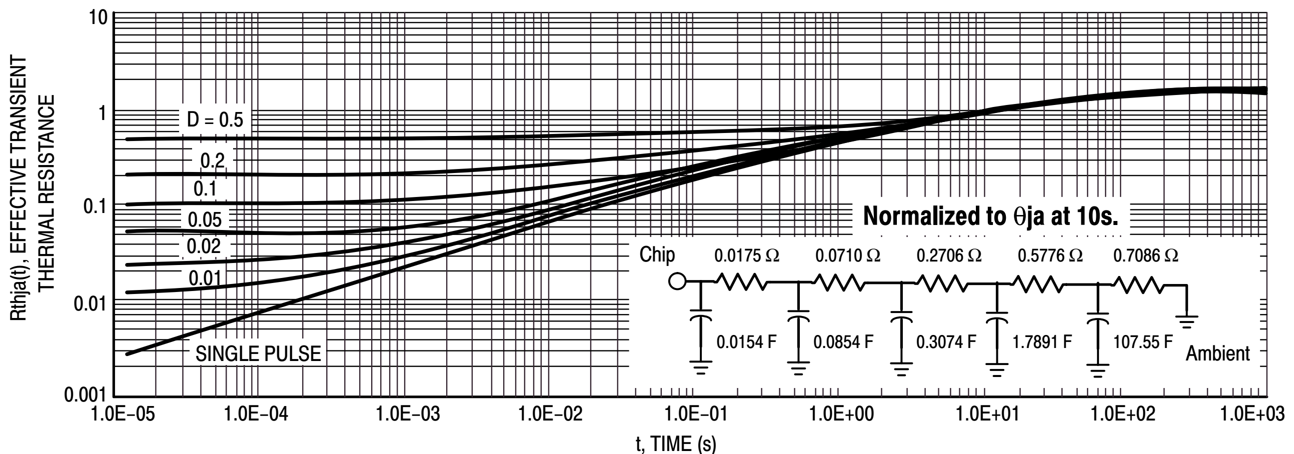
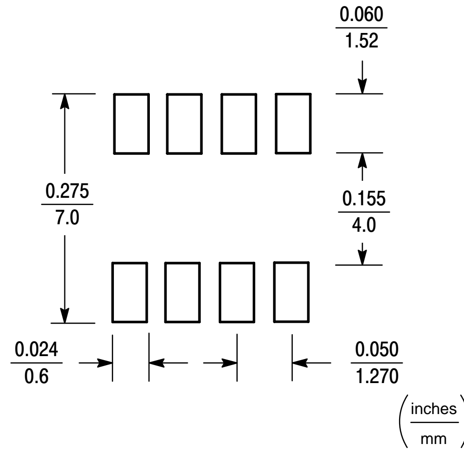



Figure 10. Thermal Response

## INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




### SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

# MMDF2C01HD

**Preferred Device**

# Power MOSFET 2 Amps, 12 Volts

## Complementary SO–8, Dual

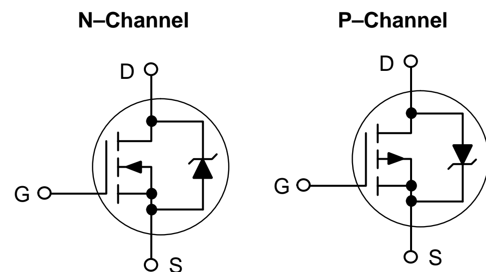
**ON Semiconductor™**

**http://onsemi.com**

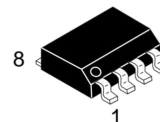
**2 AMPERES**
**12 VOLTS**
**$R_{DS(on)}$ = 45 mΩ (N–Channel)**
**$R_{DS(on)}$ = 180 mΩ (P–Channel)**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

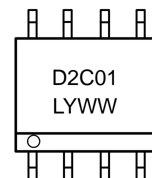
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided




**MARKING DIAGRAM**




**SO–8, Dual**
**CASE 751**
**STYLE 14**



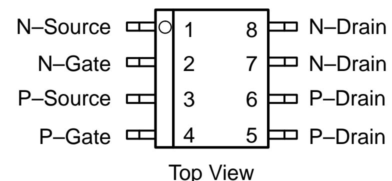

D2C01 = Device Code
L = Location Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage<br>N–Channel<br>P–Channel | $V_{DSS}$ | <br>20<br>12 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current – Continuous N–Channel<br>P–Channel<br>– Pulsed N–Channel<br>P–Channel | $I_D$<br><br>$I_{DM}$ | 5.2<br>3.4<br>48<br>17 | A |
| Operating and Storage Temperature Range | $T_J$ and $T_{stg}$ | –55 to 150 | °C |
| Total Power Dissipation @ $T_A$= 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds. | $T_L$ | 260 | °C |

1. Negative signs for P–Channel device omitted for clarity.
2. Mounted on 2” square FR4 board (1” sq. 2 oz. Cu 0.06” thick single sided) with one die operating, 10 sec. max.

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2C01HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | (N)<br>(P) | 20<br>12 | –<br>– | –<br>– | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = 20 Vdc)<br>($V_{GS}$ = 0 Vdc, $V_{DS}$ = 12 Vdc) | | $I_{DSS}$ | (N)<br>(P) | –<br>– | –<br>– | 1.0<br>1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±8.0 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | (N)<br>(P) | 0.7<br>0.7 | 0.8<br>1.0 | 1.1<br>1.1 | Vdc |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.035<br>0.16 | 0.045<br>0.18 | Ohm |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 2.7 Vdc, $I_D$ = 2.0 Adc)<br>($V_{GS}$ = 2.7 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.043<br>0.2 | 0.055<br>0.22 | Ohm |
| Forward Transconductance<br>($V_{DS}$ = 2.5 Adc, $I_D$ = 2.0 Adc)<br>($V_{DS}$ = 2.5 Adc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | (N)<br>(P) | 3.0<br>3.0 | 6.0<br>4.75 | –<br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 425<br>530 | 595<br>740 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 270<br>410 | 378<br>570 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 115<br>177 | 230<br>250 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 13<br>21 | 26<br>45 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 60<br>156 | 120<br>315 | |
| Turn–Off Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 20<br>38 | 40<br>75 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 29<br>68 | 58<br>135 | |
| Turn–On Delay Time | ($V_{DS}$ = 6.0 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 10<br>16 | 20<br>35 | |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 42<br>44 | 84<br>90 | |
| Turn–Off Delay Time | ($V_{DS}$ = 6.0 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 24<br>68 | 48<br>135 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 28<br>54 | 56<br>110 | |

3. Negative signs for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS – continued** ($T_A$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS – continued** (Note 8.) | | | | | | | |
| Total Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 4.5 Vdc)<br>($V_{DS}$ = 6.0 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 9.2<br>9.3 | 13<br>13 | nC |
| Gate–Source Charge | | $Q_1$ | (N)<br>(P) | –<br>– | 1.3<br>0.8 | –<br>– | |
| Gate–Drain Charge | | $Q_2$ | (N)<br>(P) | –<br>– | 3.5<br>4.0 | –<br>– | |
| | | $Q_3$ | (N)<br>(P) | –<br>– | 3.0<br>3.0 | –<br>– | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** ($T_C$ = 25°C) | | | | | | | |
| Forward Voltage (Note 7.) | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | (N)<br>(P) | –<br>– | 0.95<br>1.69 | 1.1<br>2.0 | Vdc |
| Reverse Recovery Time | ($I_F$ = $I_S$, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 38<br>48 | –<br>– | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 17<br>23 | –<br>– | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 22<br>25 | –<br>– | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | (N)<br>(P) | –<br>– | 0.028<br>0.05 | –<br>– | µC |

6. Negative signs for P–Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
8. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

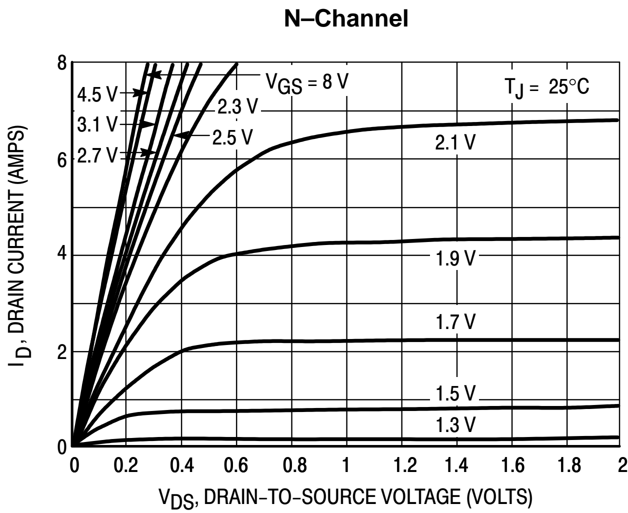



**Figure 1. On–Region Characteristics**

**P–Channel**

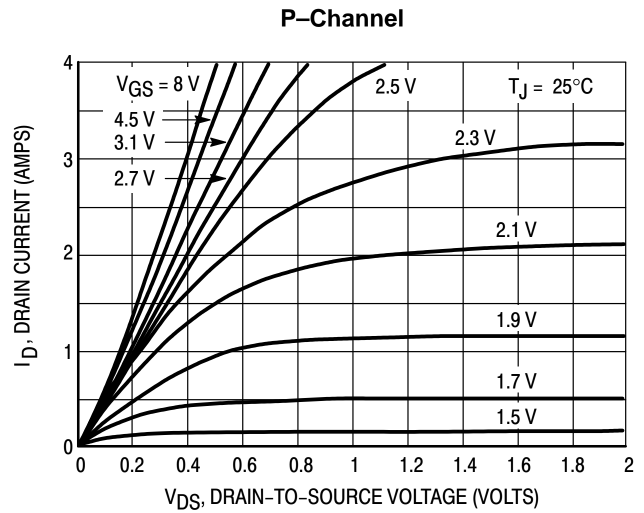



**Figure 1. On–Region Characteristics**

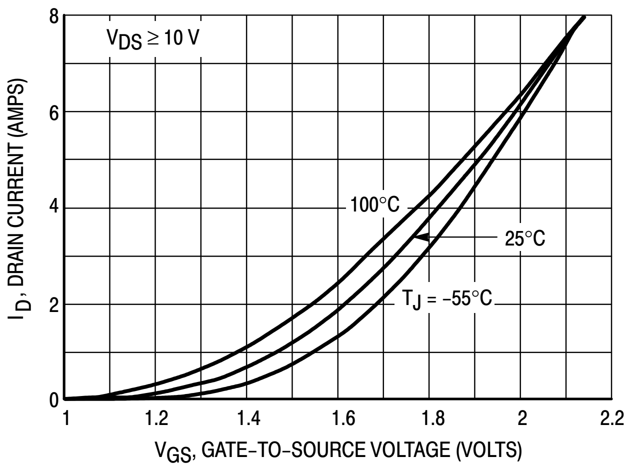



**Figure 2. Transfer Characteristics**

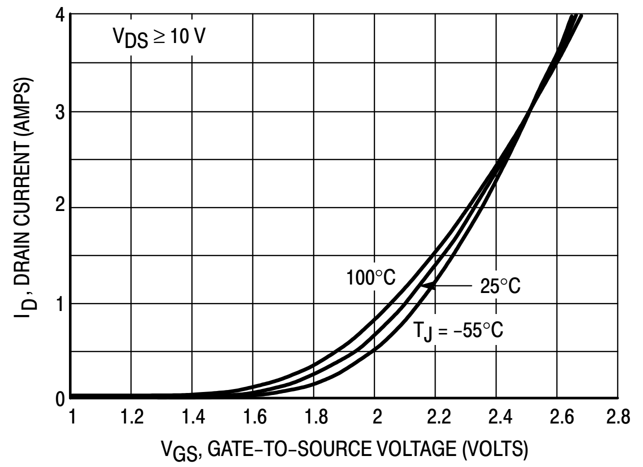



**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

**P–Channel**

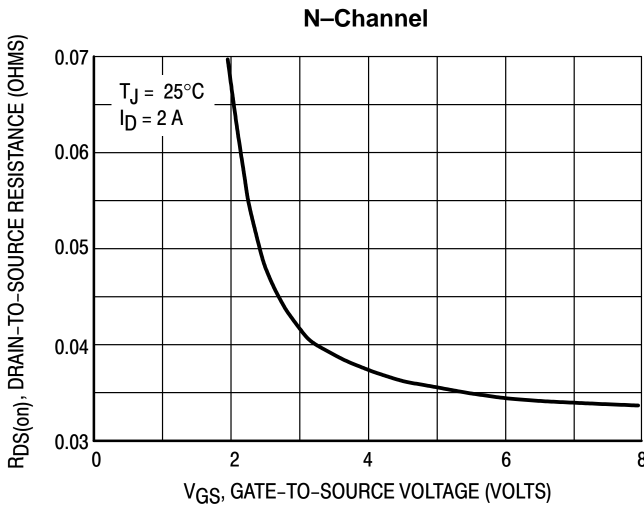



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

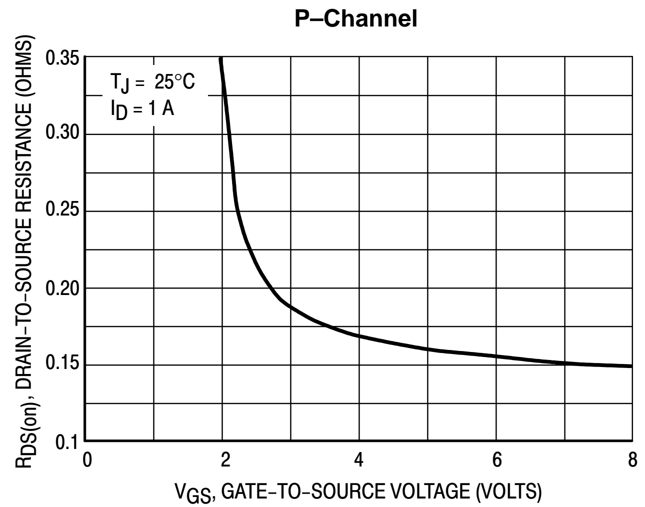



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

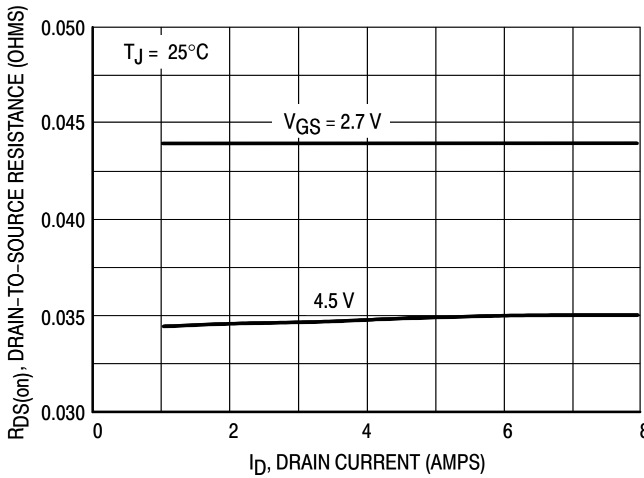



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

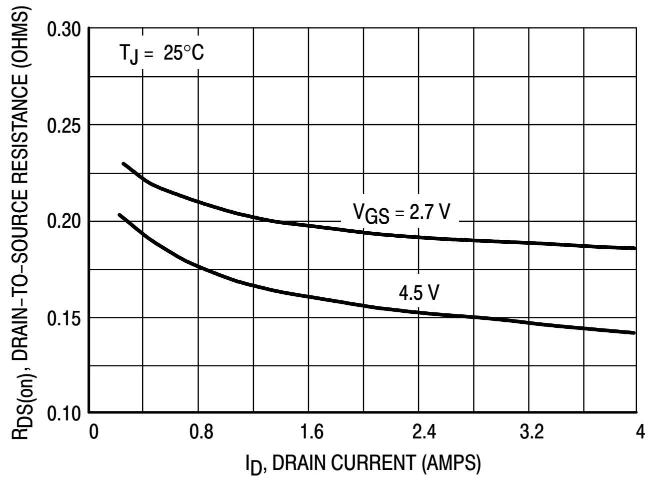



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

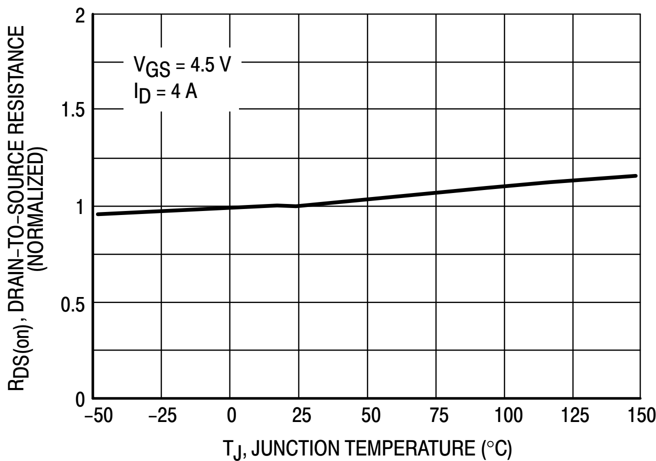



**Figure 5. On–Resistance Variation with Temperature**

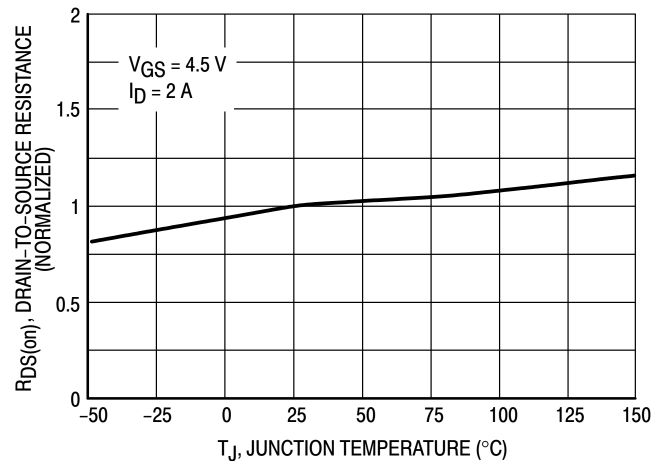



**Figure 5. On–Resistance Variation with Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

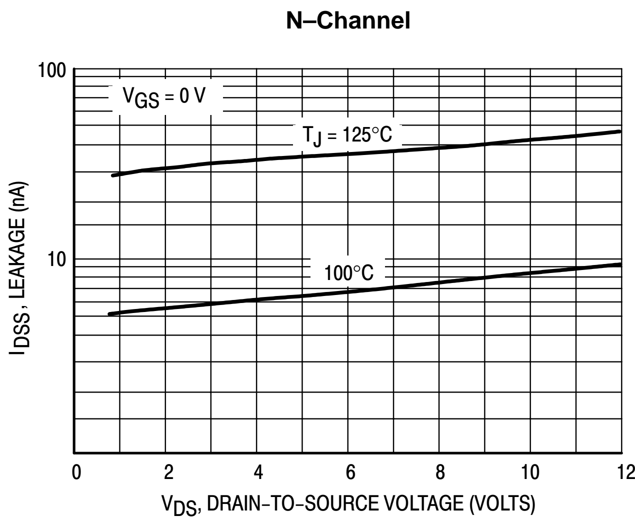



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

**P–Channel**

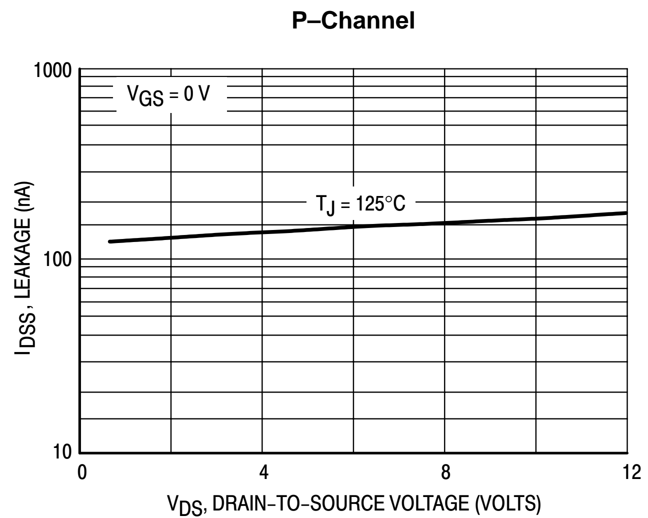



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

**N–Channel** **P–Channel**

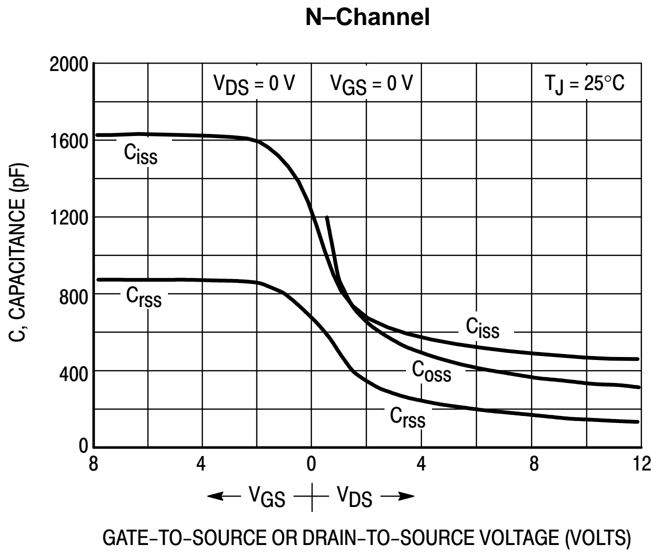



**Figure 7. Capacitance Variation**

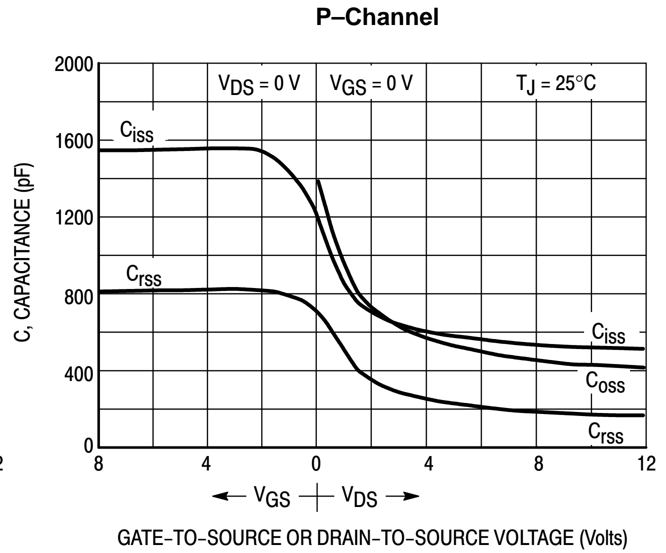



**Figure 7. Capacitance Variation**

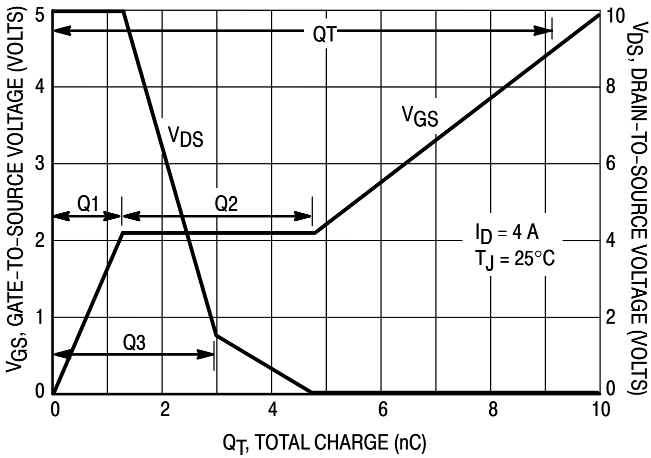



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

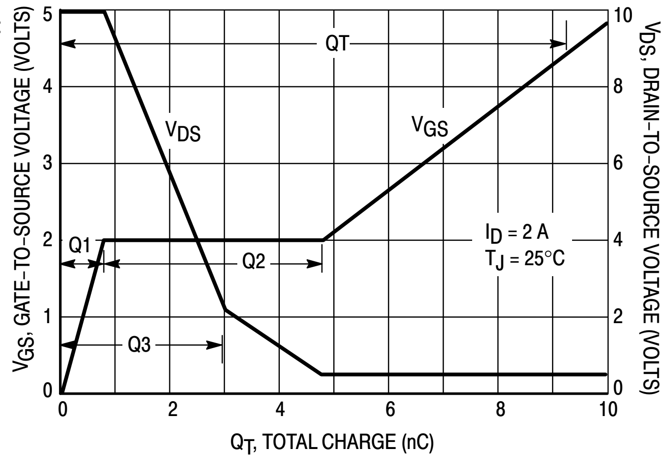



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

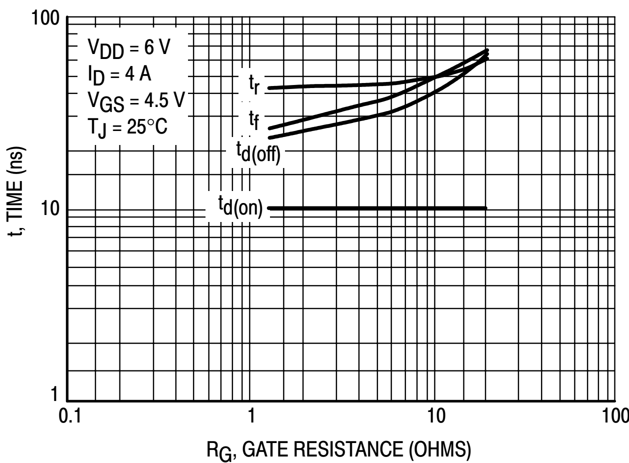



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

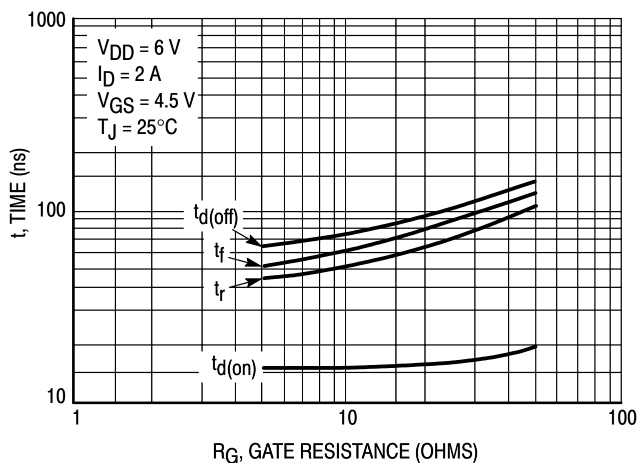



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

**N–Channel**

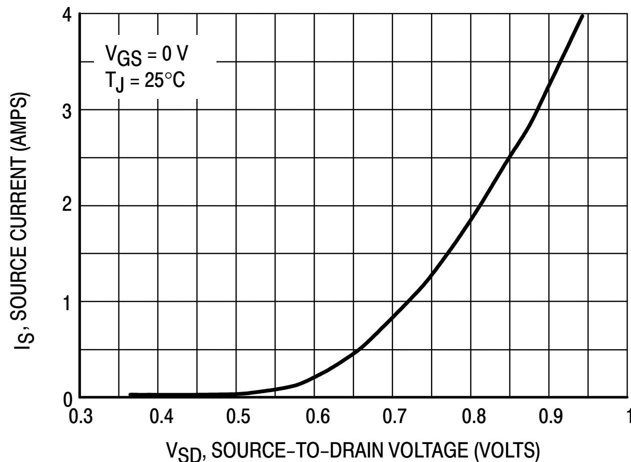



**Figure 10. Diode Forward Voltage versus Current**

**P–Channel**

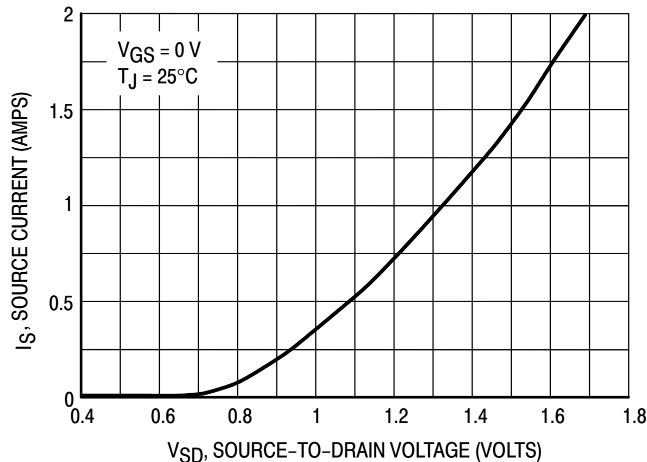



**Figure 10. Diode Forward Voltage versus Current**

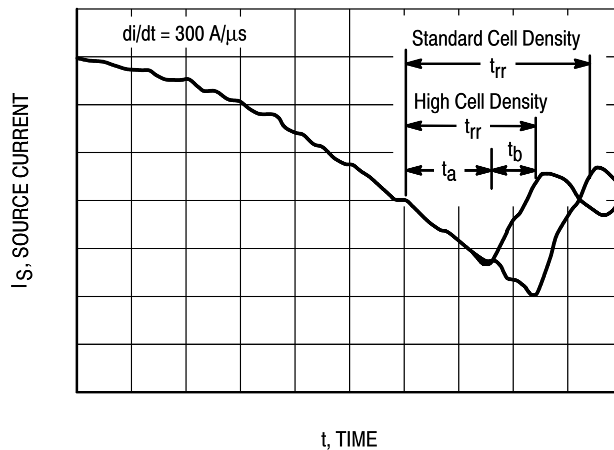



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

**N–Channel**

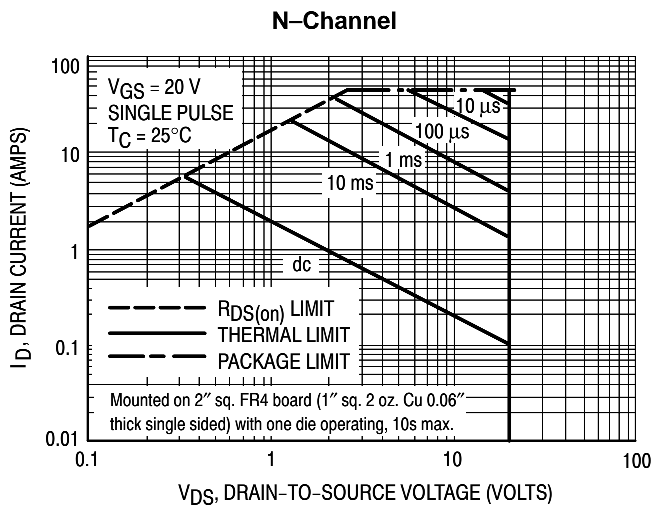



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

**P–Channel**

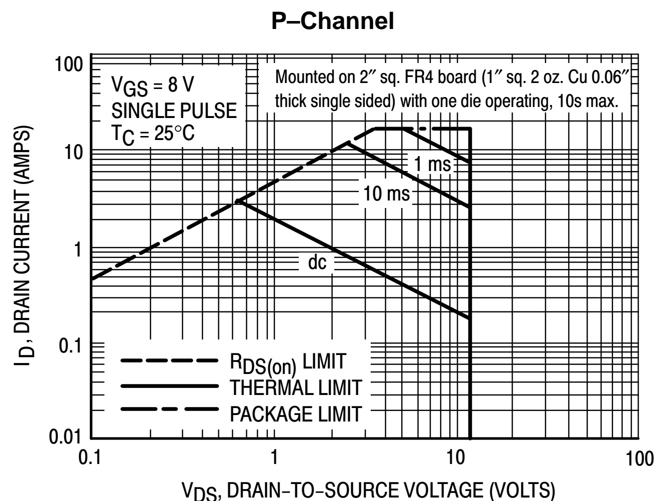



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

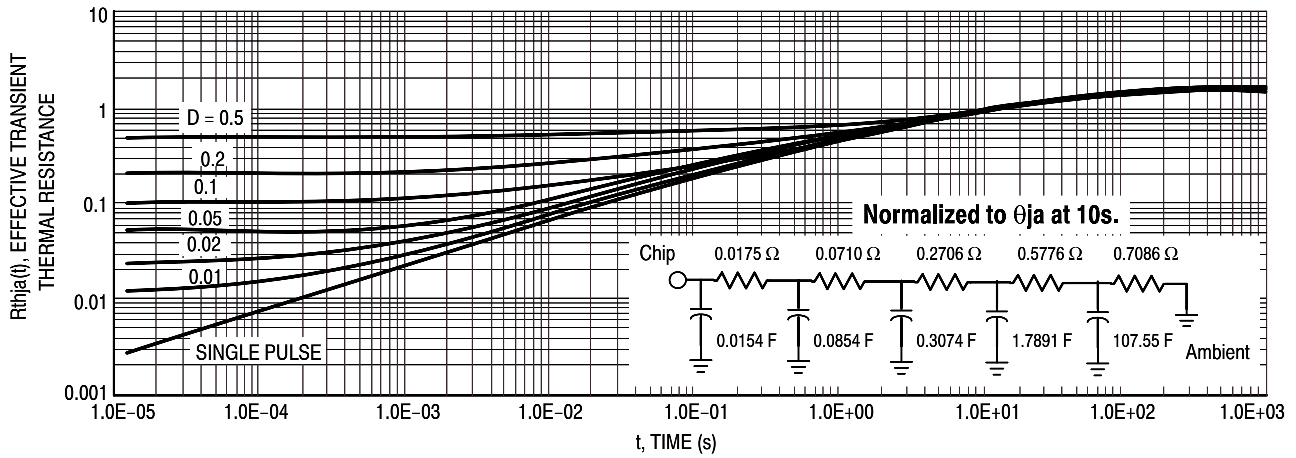



**Figure 13. Thermal Response**

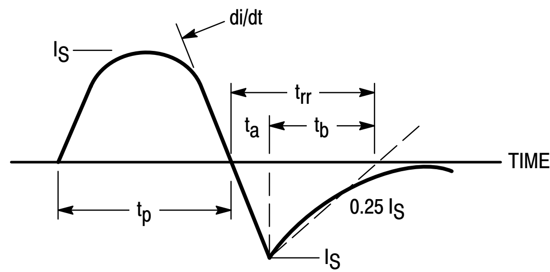
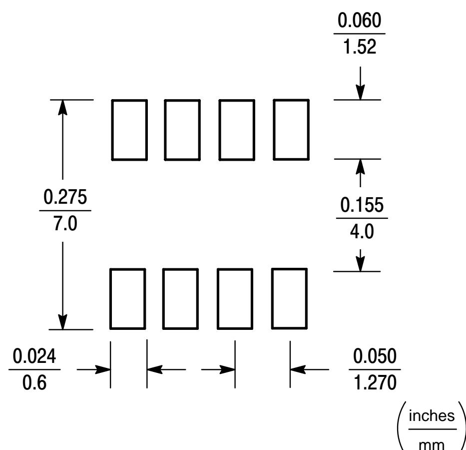



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

### TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

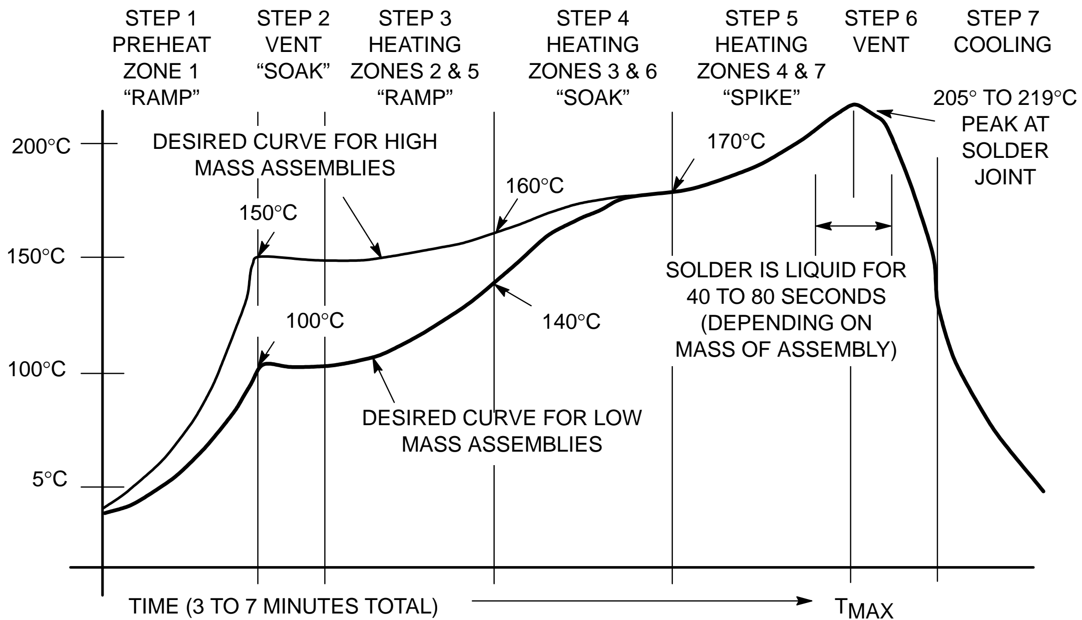



**Figure 15. Typical Solder Heating Profile**

# MMDF2C02E

*Advance Information*

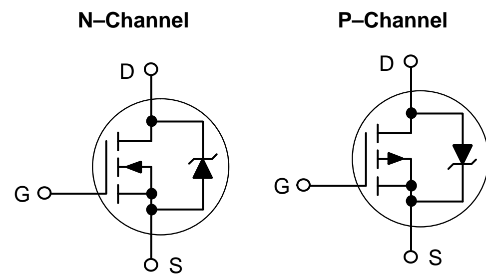
# Power MOSFET 2.5 Amps, 25 Volts

## Complementary SO–8, Dual

**ON Semiconductor**™

**http://onsemi.com**

**2.5 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 100 mΩ (N–Channel)**
**$R_{DS(on)}$ = 250 mΩ (P–Channel)**




These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

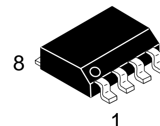
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous N–Channel<br>P–Channel<br>– Pulsed N–Channel<br>P–Channel | $I_D$<br><br>$I_{DM}$ | 3.6<br>2.5<br>18<br>13 | Adc |
| Operating and Storage Temperature Range | $T_J$ and $T_{stg}$ | – 55 to 150 | °C |
| Total Power Dissipation @ $T_A$= 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 20 V, $V_{GS}$ = 10 V, Peak $I_L$ = 9.0 A, L = 6.0 mH, $R_G$ = 25 Ω) N–Channel<br>($V_{DD}$ = 20 V, $V_{GS}$ = 10 V, Peak $I_L$ = 7.0 A, L = 10 mH, $R_G$ = 25 Ω) P–Channel | $E_{AS}$ | <br>245<br>245 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds. | $T_L$ | 260 | °C |

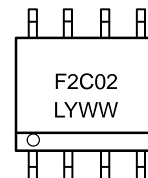
1. Negative signs for P–Channel device omitted for clarity.
2. Mounted on 2” square FR4 board (1” sq. 2 oz. Cu 0.06” thick single sided) with one die operating, 10 sec. max.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MARKING DIAGRAM**

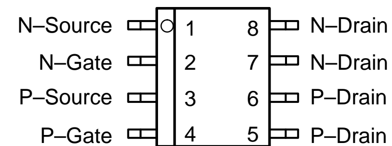



**SO–8, Dual**
**CASE 751**
**STYLE 14**




F2C02 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2C02ER2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | – | 25 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | (N)<br>(P) | –<br>– | –<br>– | 1.0<br>1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | – | 1.0 | 2.0 | 3.0 | Vdc |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.2 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | –<br>– | 0.100<br>0.250 | Ohm |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | –<br>– | 0.200<br>0.400 | Ohm |
| On–State Drain Current ($V_{DS}$ = 5.0 Vdc, $V_{GS}$ = 4.5 Vdc) | | $I_{D(on)}$ | (N)<br>(P) | 2.0<br>2.0 | –<br>– | –<br>– | Adc |
| Forward Transconductance<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc)<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | (N)<br>(P) | 1.0<br>1.0 | 2.6<br>2.8 | –<br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 380<br>340 | 532<br>475 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 235<br>220 | 329<br>300 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 55<br>75 | 110<br>150 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω)<br>($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 25 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 10<br>20 | 30<br>40 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 35<br>40 | 70<br>80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 19<br>53 | 38<br>106 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 25<br>41 | 50<br>82 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω)<br>($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 7.0<br>13 | 21<br>26 | |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 17<br>29 | 30<br>58 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 27<br>30 | 48<br>60 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 18<br>28 | 30<br>56 | |

3. Negative signs for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS – continued** ($T_A$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS – continued** (Note 8.) | | | | | | | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 10.6<br>10 | 30<br>15 | nC |
| Gate–Source Charge | | $Q_1$ | (N)<br>(P) | –<br>– | 1.3<br>1.0 | –<br>– | |
| Gate–Drain Charge | | $Q_2$ | (N)<br>(P) | –<br>– | 2.9<br>3.5 | –<br>– | |
| | | $Q_3$ | (N)<br>(P) | –<br>– | 2.7<br>3.0 | –<br>– | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** ($T_C$ = 25°C) | | | | | | | |
| Forward Voltage (Note 7.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | (N)<br>(P) | –<br>– | 1.0<br>1.5 | 1.4<br>2.0 | Vdc |
| Reverse Recovery Time<br>see Figure 7 | ($I_F$ = $I_S$, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 34<br>32 | 66<br>64 | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 17<br>19 | –<br>– | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 17<br>12 | –<br>– | |
| | | $Q_{RR}$ | (N)<br>(P) | –<br>– | 0.025<br>0.035 | –<br>– | µC |

6. Negative signs for P–Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
8. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

**P–Channel**

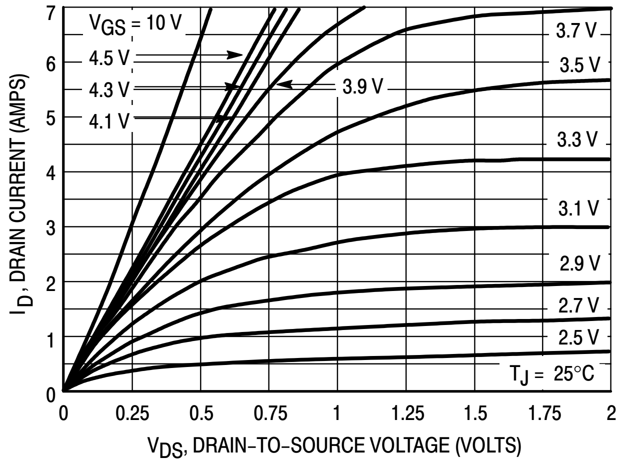



**Figure 1. On–Region Characteristics**

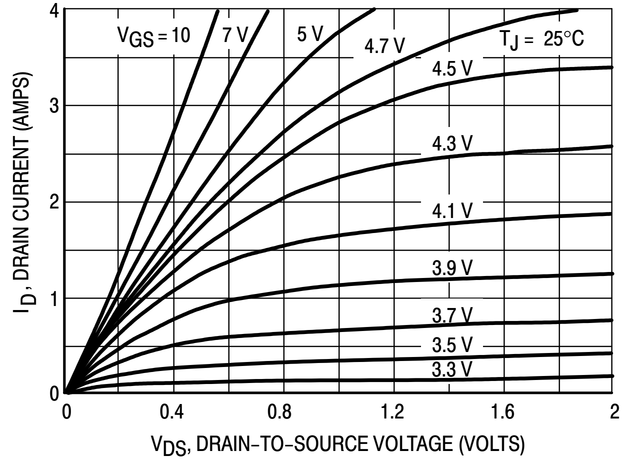



**Figure 1. On–Region Characteristics**

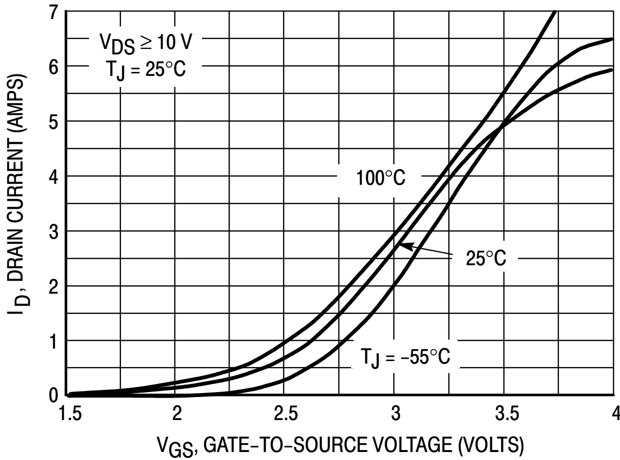



**Figure 2. Transfer Characteristics**

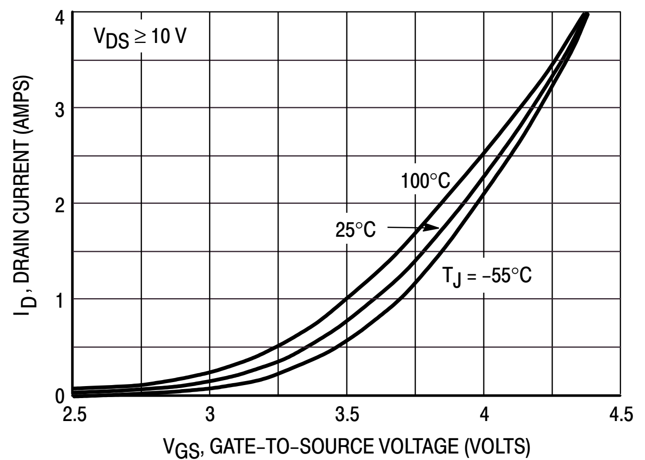



**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel** | **P–Channel**

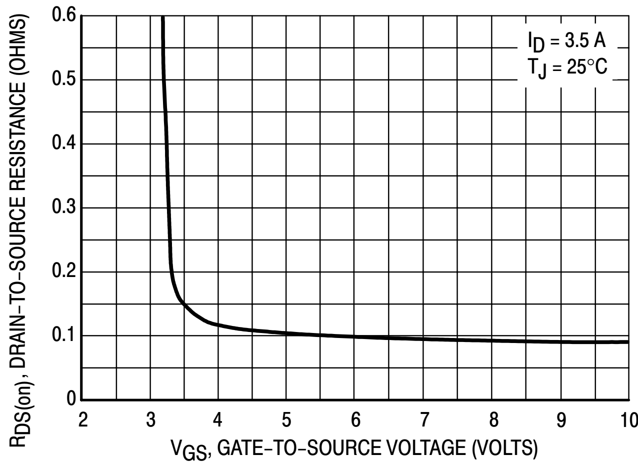



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

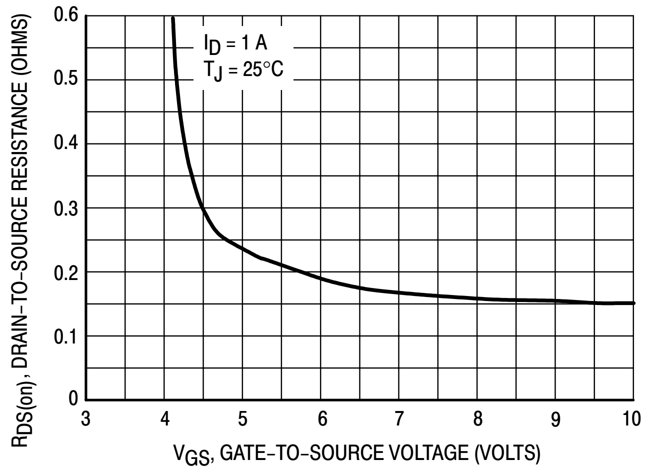



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

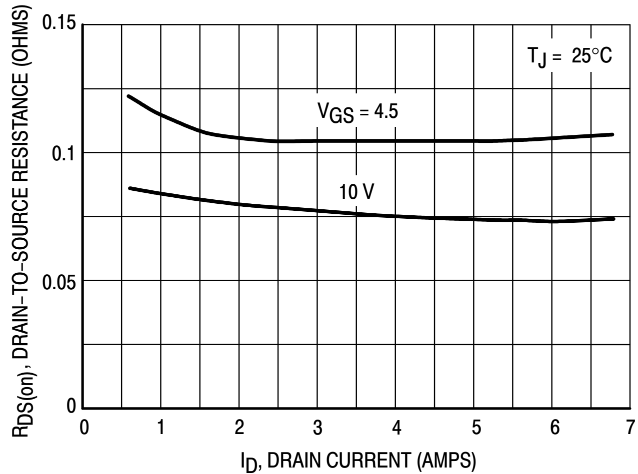



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

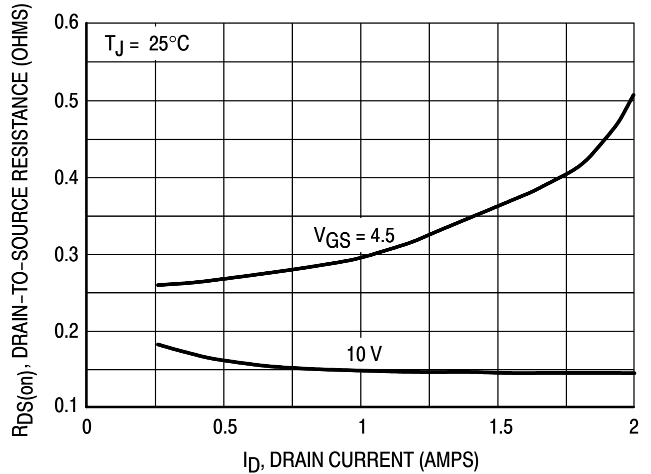



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

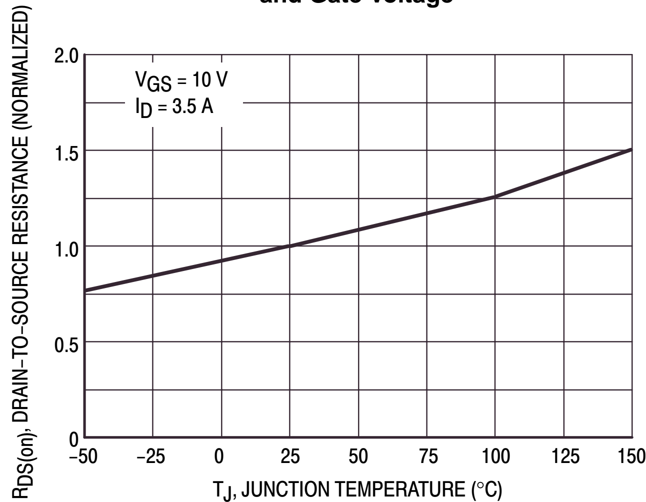



**Figure 5. On–Resistance Variation with Temperature**

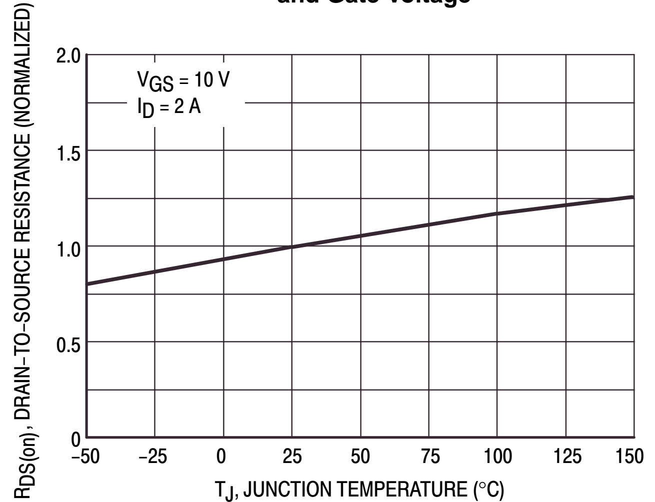



**Figure 5. On–Resistance Variation with Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

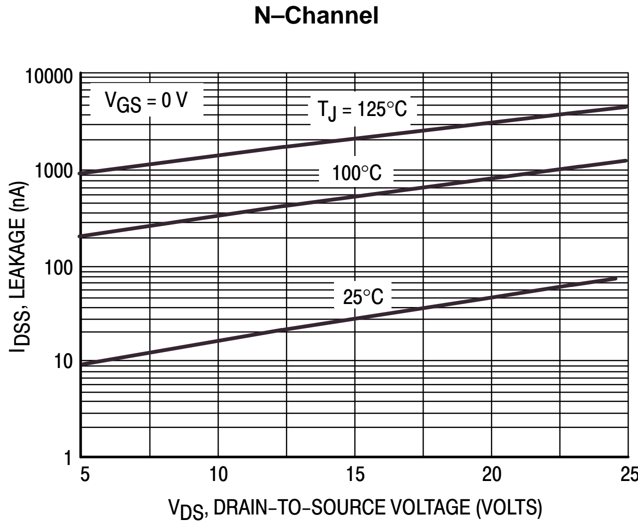



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

**P–Channel**

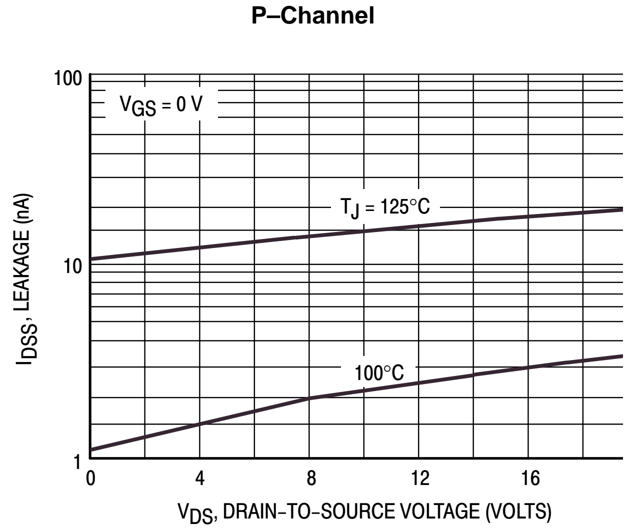



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

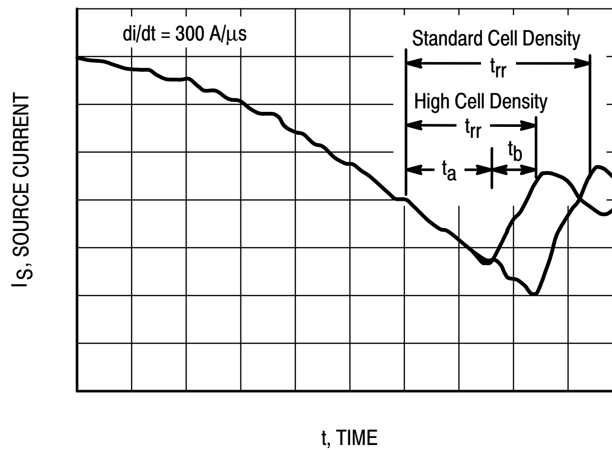



**Figure 7. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

**N–Channel**

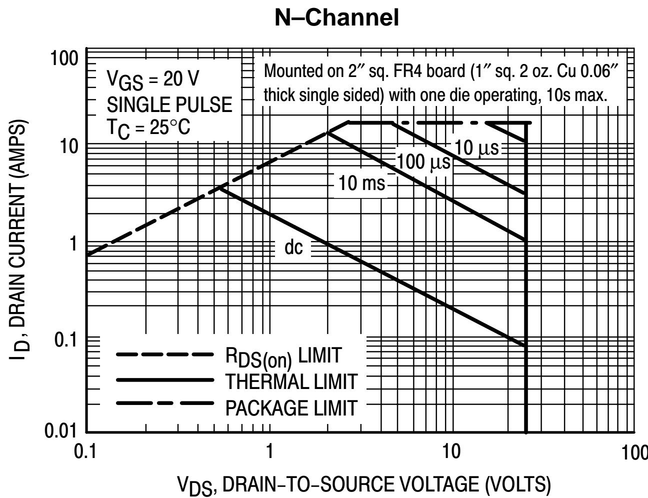



**Figure 8. Maximum Rated Forward Biased Safe Operating Area**

**P–Channel**

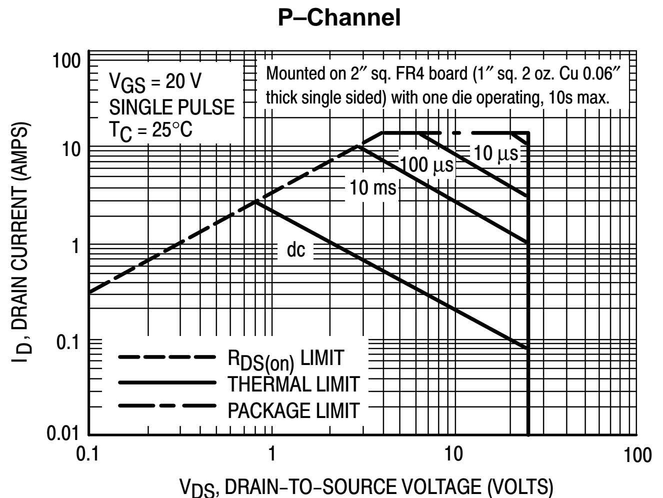



**Figure 8. Maximum Rated Forward Biased Safe Operating Area**

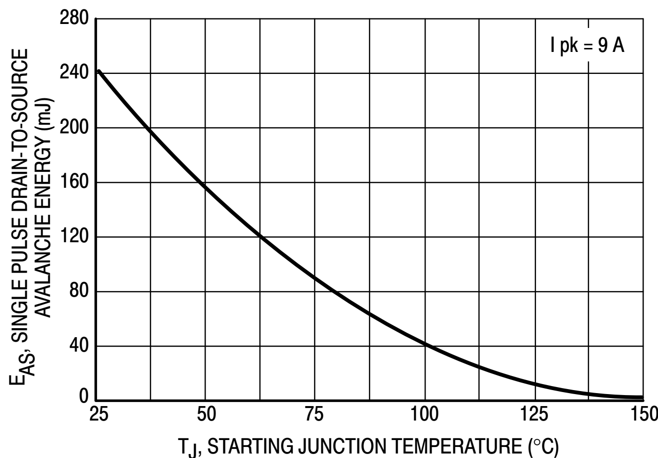



**Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature**

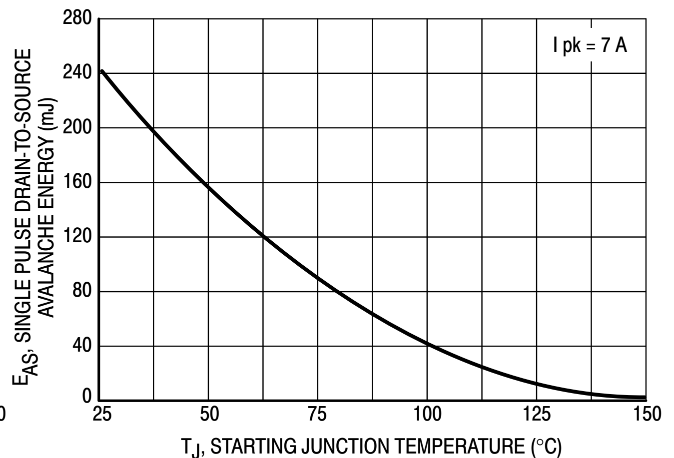



**Figure 9. Maximum Avalanche Energy versus Starting Junction Temperature**

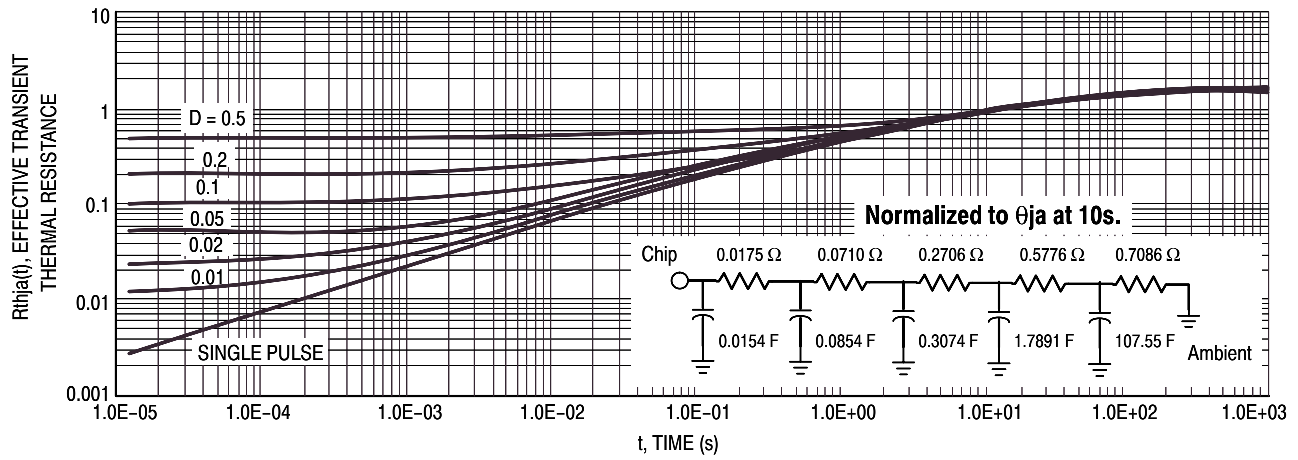



**Figure 10. Thermal Response**

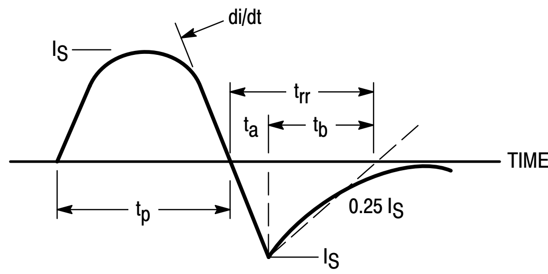
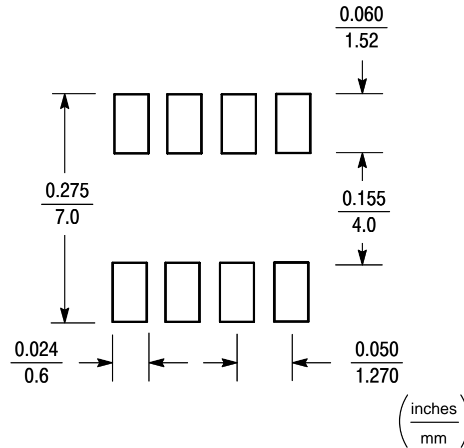



**Figure 11. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

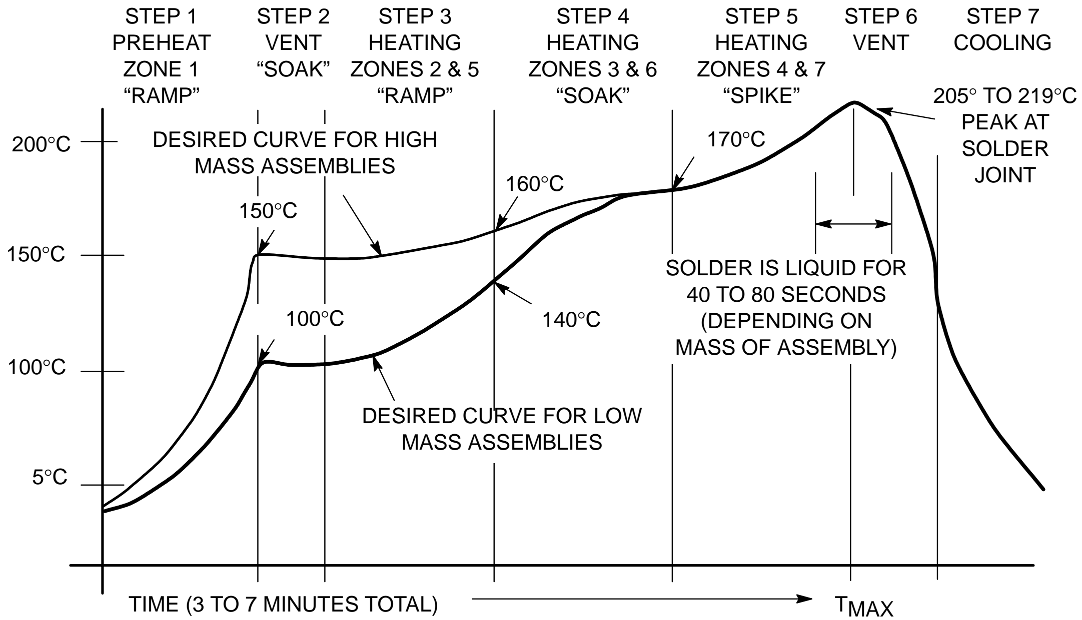



**Figure 12. Typical Solder Heating Profile**

# MMDF2C02HD

**Preferred Device**

# Power MOSFET 2 Amps, 20 Volts

## Complementary SO–8, Dual

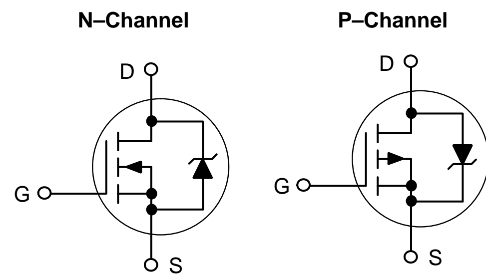
**ON Semiconductor™**

**http://onsemi.com**

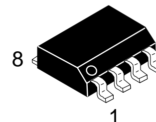
**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ (N–Channel)**
**$R_{DS(on)}$ = 160 mΩ (P–Channel)**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

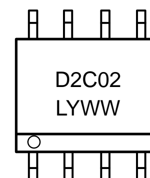
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided




**MARKING DIAGRAM**

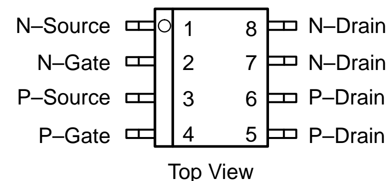



**SO–8, Dual**
**CASE 751**
**STYLE 14**




D2C02 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | 20 | Vdc |
| Drain Current – Continuous N–Channel<br>P–Channel<br>– Pulsed N–Channel<br>P–Channel | $I_D$<br><br>$I_{DM}$ | 3.8<br>3.3<br>19<br>20 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Total Power Dissipation @ $T_A$= 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 20 V, $V_{GS}$ = 5.0 V, Peak $I_L$ = 9.0 A, L = 10 mH, $R_G$ = 25 Ω) N–Channel<br>($V_{DD}$ = 20 V, $V_{GS}$ = 5.0 V, Peak $I_L$ = 6.0 A, L = 18 mH, $R_G$ = 25 Ω) P–Channel | $E_{AS}$ | <br>405<br>324 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds. | $T_L$ | 260 | °C |

1. Negative signs for P–Channel device omitted for clarity.
2. Mounted on 2” square FR4 board (1” sq. 2 oz. Cu 0.06” thick single sided) with one die operating, 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2C02HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | – | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | (N)<br>(P) | –<br>– | –<br>– | 1.0<br>1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | – | 1.0 | 1.5 | 2.0 | Vdc |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.5 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.074<br>0.152 | 0.100<br>0.180 | Ohm |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.058<br>0.118 | 0.090<br>0.160 | Ohm |
| Forward Transconductance<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc)<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | (N)<br>(P) | 2.0<br>2.0 | 3.88<br>3.0 | –<br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 455<br>420 | 630<br>588 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 184<br>290 | 250<br>406 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 45<br>116 | 90<br>232 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω)<br>($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 11<br>19 | 22<br>38 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 58<br>66 | 116<br>132 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 17<br>25 | 35<br>50 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 20<br>37 | 40<br>74 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω)<br>($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 7.0<br>11 | 21<br>22 | |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 32<br>21 | 64<br>42 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 27<br>45 | 54<br>90 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 21<br>36 | 42<br>72 | |

3. Negative signs for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS – continued** ($T_A$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS – continued** (Note 8.) | | | | | | | |
| Total Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc)<br>($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 12.5<br>15 | 18<br>20 | nC |
| Gate–Source Charge | | $Q_1$ | (N)<br>(P) | –<br>– | 1.3<br>1.2 | –<br>– | |
| Gate–Drain Charge | | $Q_2$ | (N)<br>(P) | –<br>– | 2.8<br>5.0 | –<br>– | |
| | | $Q_3$ | (N)<br>(P) | –<br>– | 2.4<br>4.0 | –<br>– | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** ($T_C$ = 25°C) | | | | | | | |
| Forward Voltage (Note 7.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | (N)<br>(P) | –<br>– | 0.79<br>1.5 | 1.3<br>2.1 | Vdc |
| Reverse Recovery Time | ($I_S$ = 3.0 Adc, $V_{AS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs)<br>($I_S$ = 2.0 Adc, $V_{AS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 23<br>38 | –<br>– | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 18<br>17 | –<br>– | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 5.0<br>21 | –<br>– | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | (N)<br>(P) | –<br>– | 0.025<br>0.034 | –<br>– | µC |

6. Negative signs for P–Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
8. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

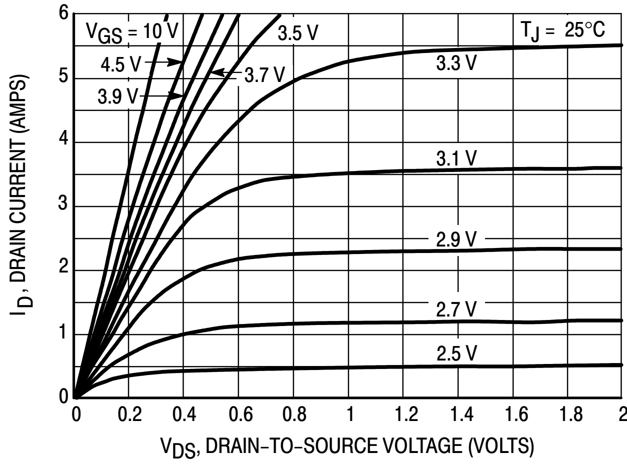



**Figure 1. On–Region Characteristics**

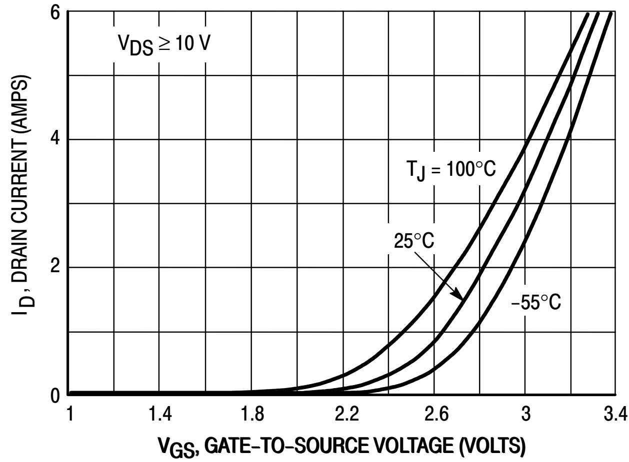



**Figure 2. Transfer Characteristics**

**P–Channel**

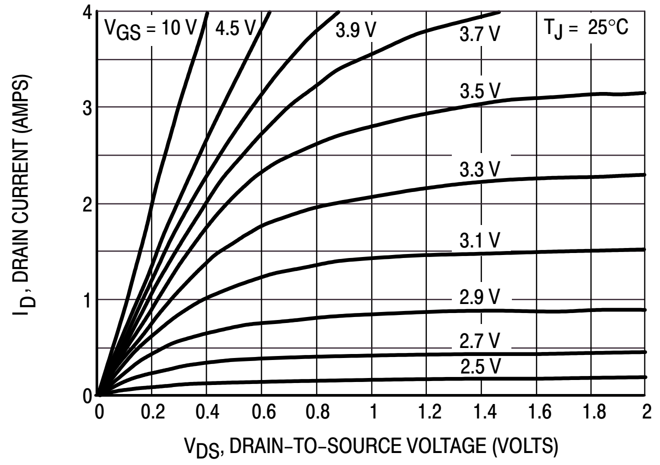



**Figure 1. On–Region Characteristics**

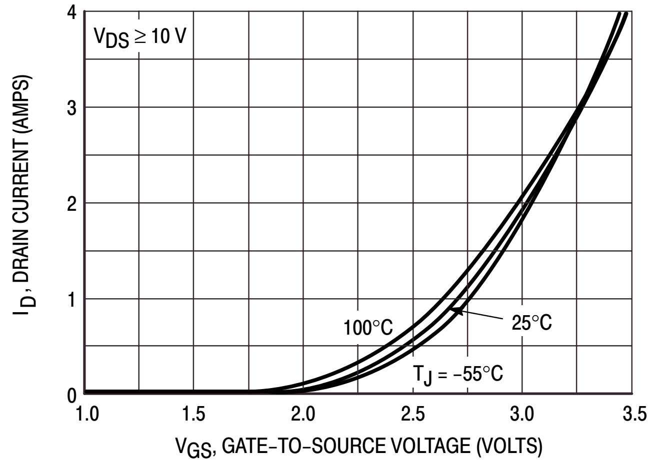



**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel** **P–Channel**

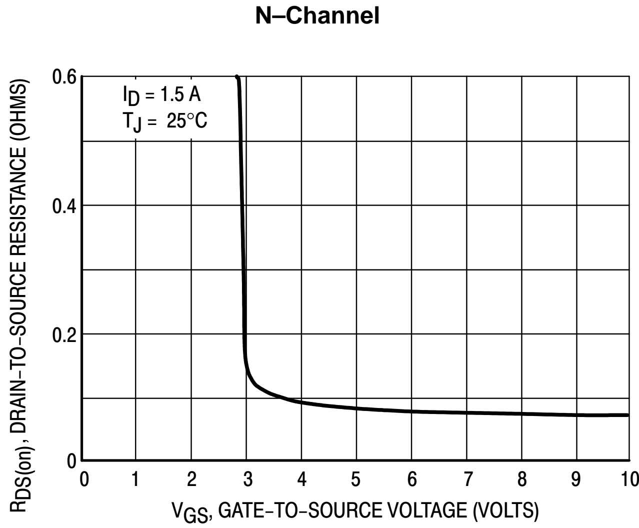



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

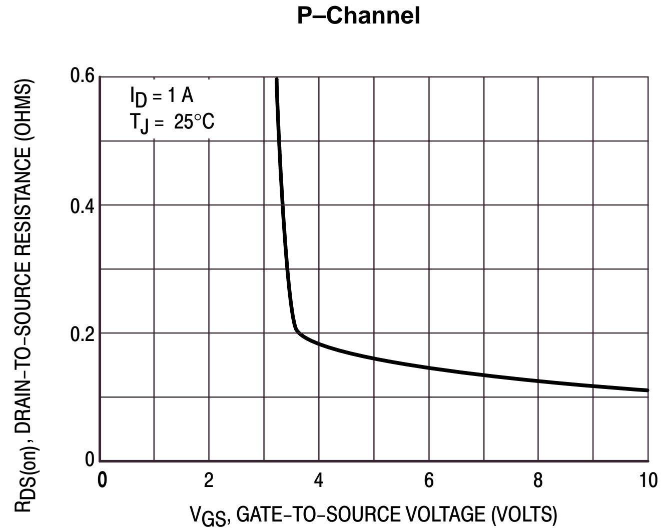



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

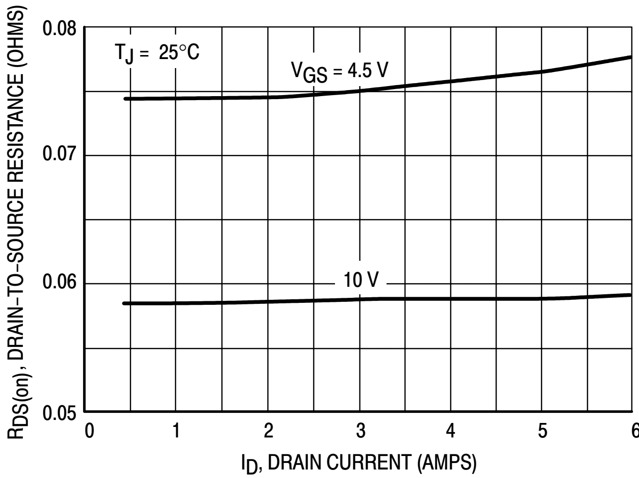



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

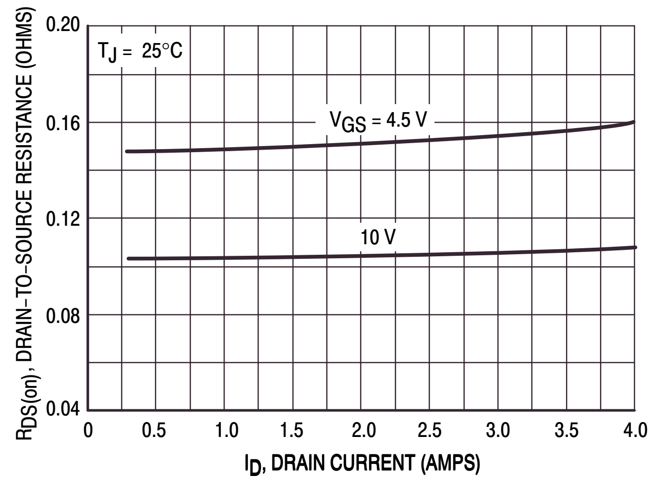



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

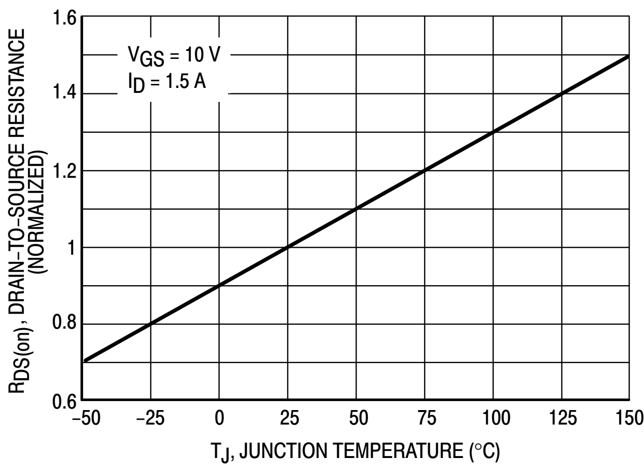



**Figure 5. On–Resistance Variation with Temperature**

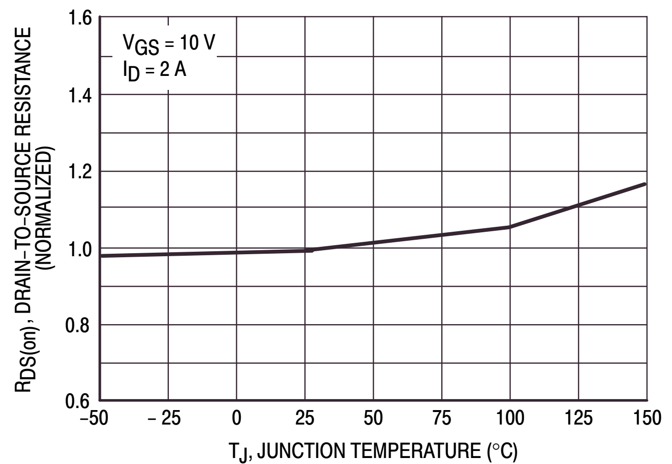



**Figure 5. On–Resistance Variation with Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

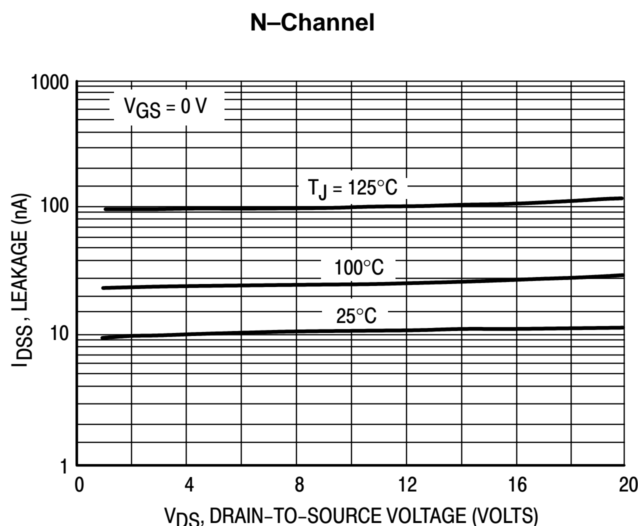



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

**P–Channel**

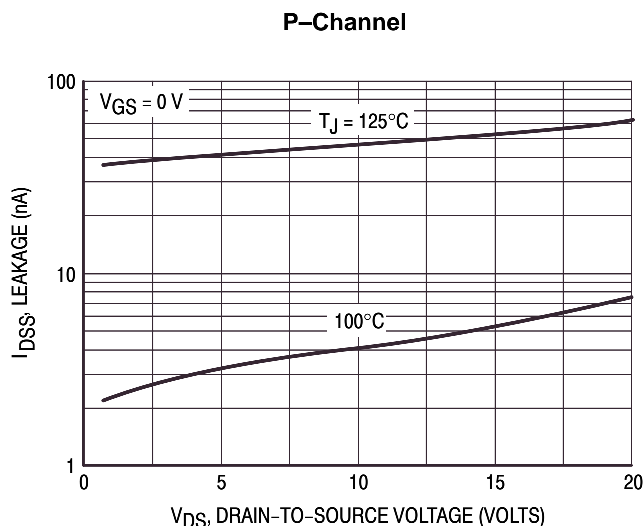



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

**N–Channel** **P–Channel**

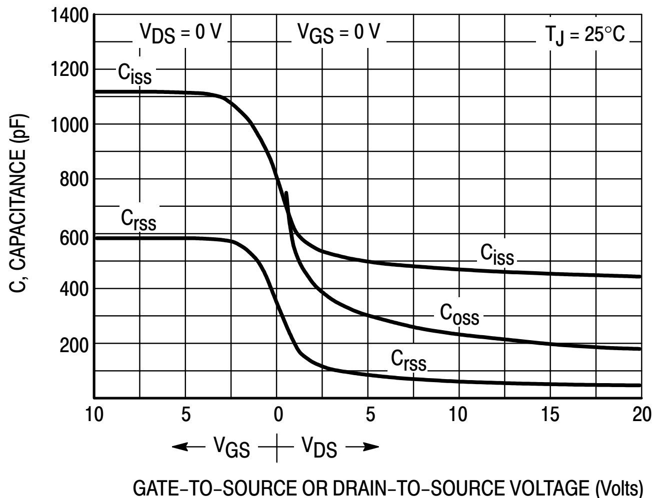



**Figure 7. Capacitance Variation**

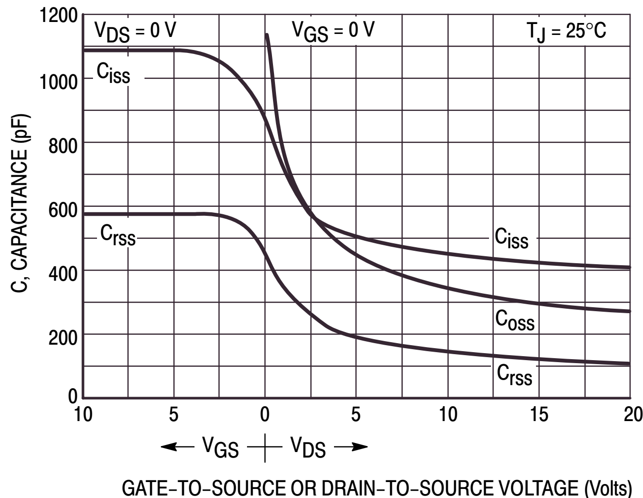



**Figure 7. Capacitance Variation**

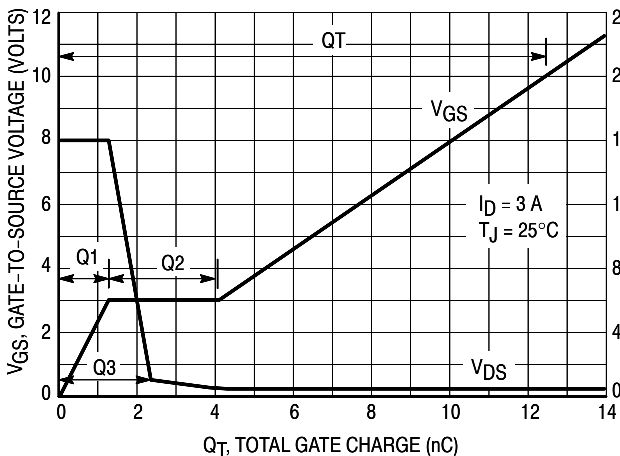



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

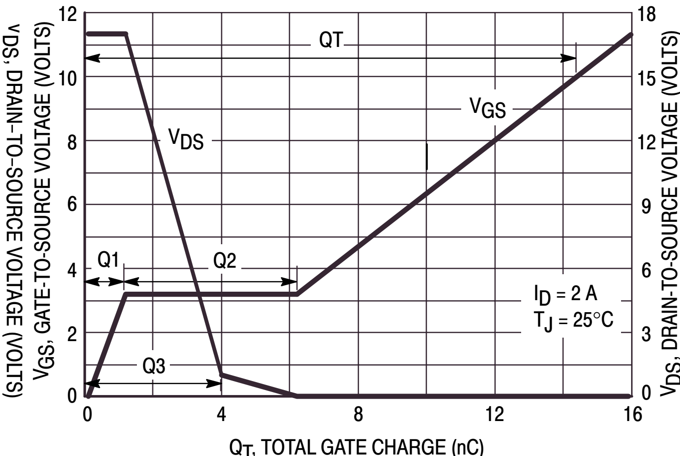



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

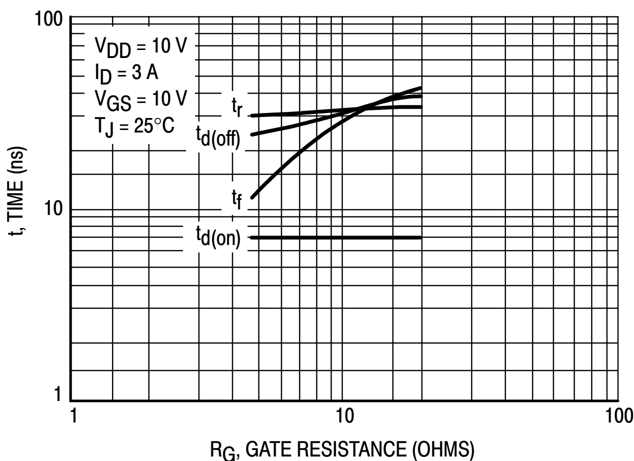



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

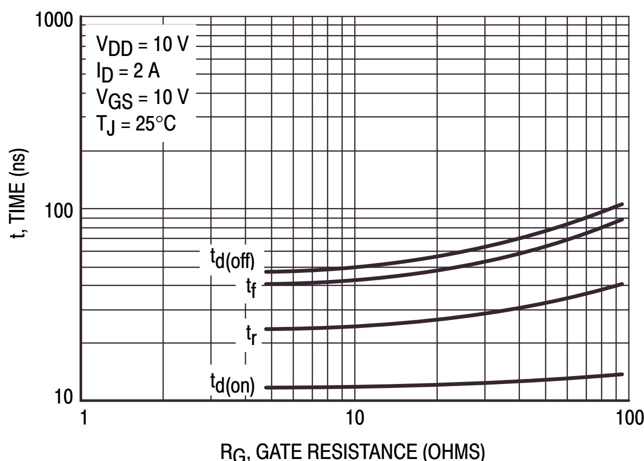



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

**N–Channel**

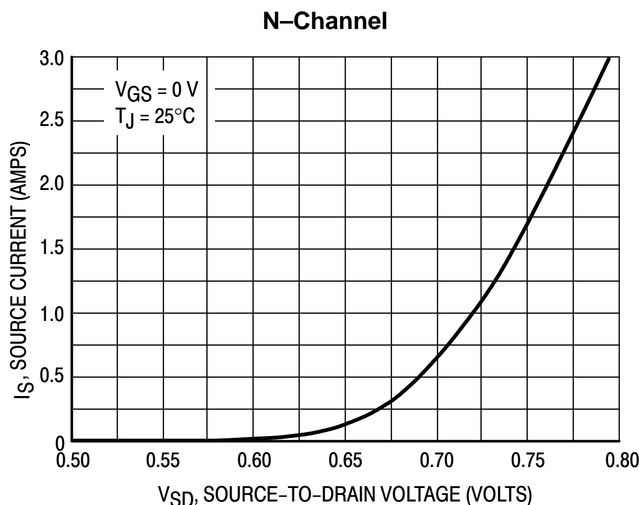



**Figure 10. Diode Forward Voltage versus Current**

**P–Channel**

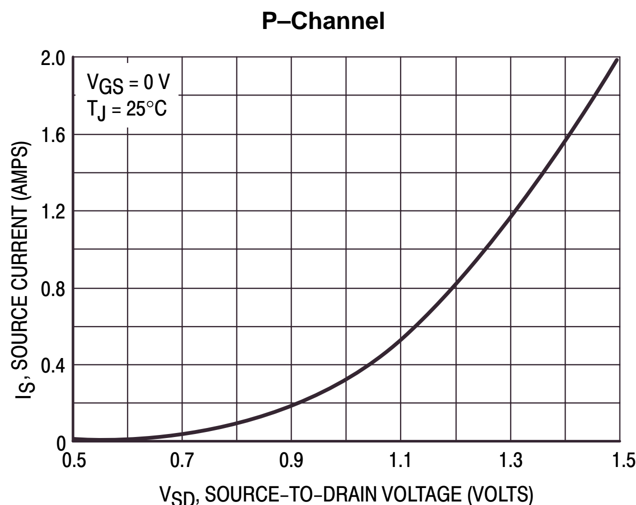



**Figure 10. Diode Forward Voltage versus Current**

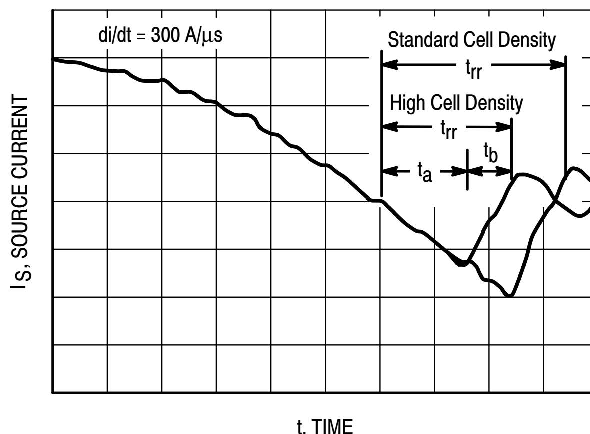



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

**N–Channel**

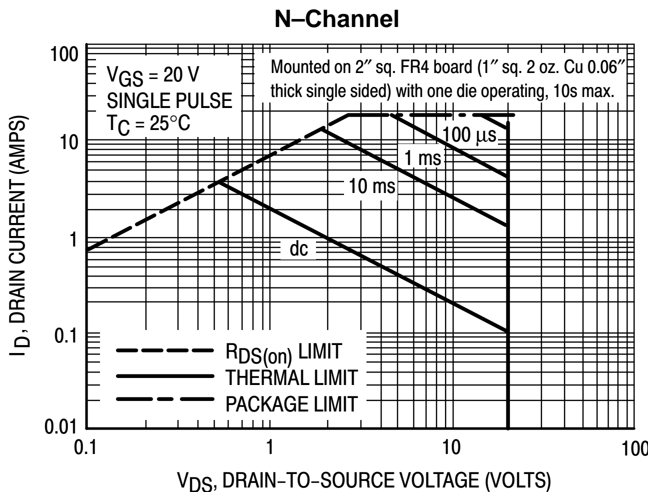



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

**P–Channel**

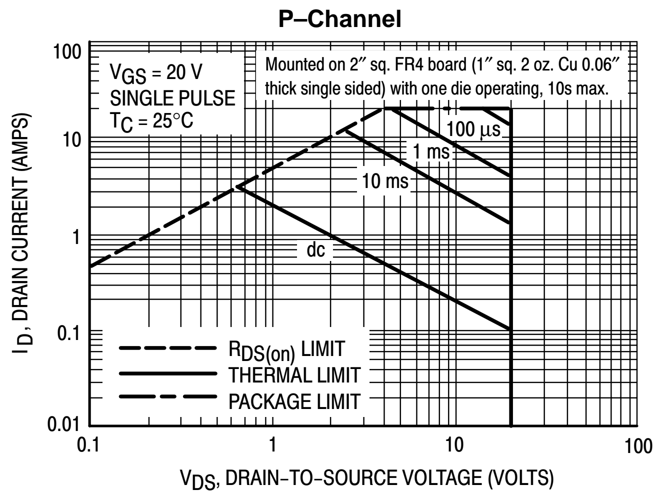



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

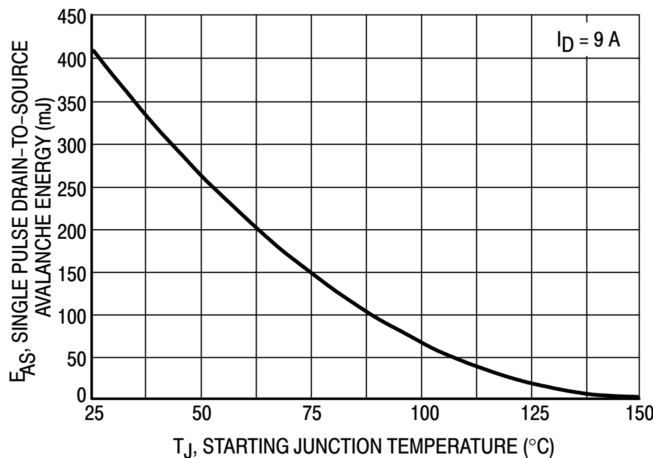



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

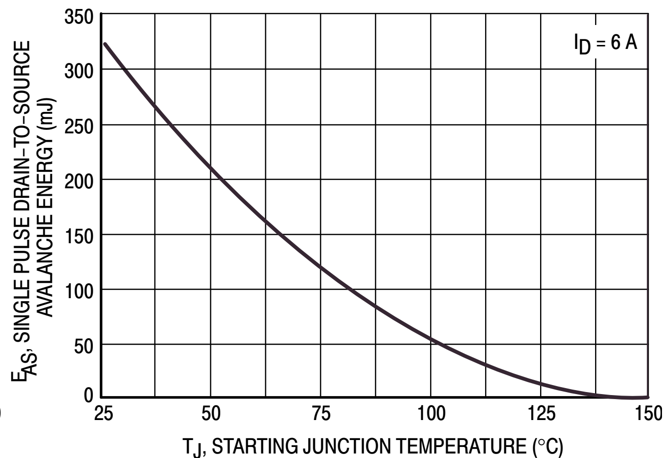



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

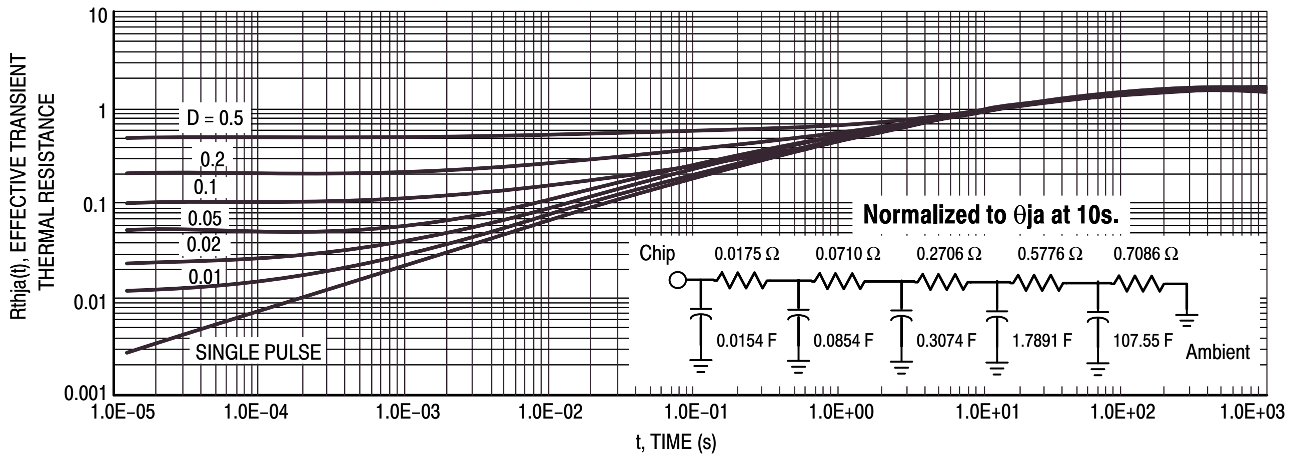



**Figure 14. Thermal Response**

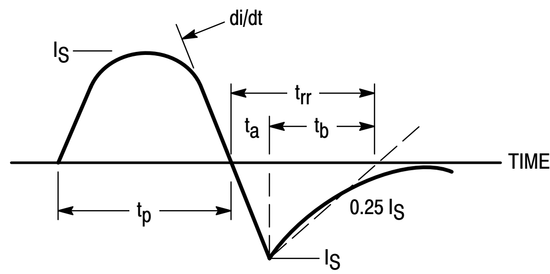
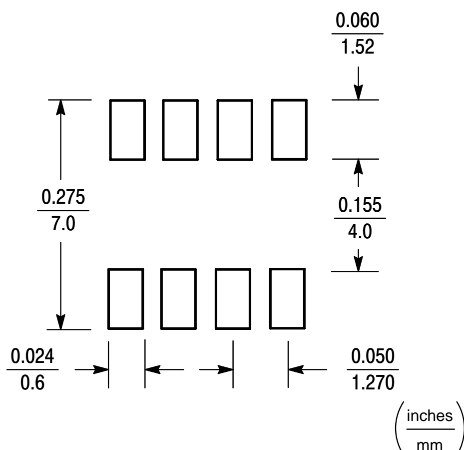



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

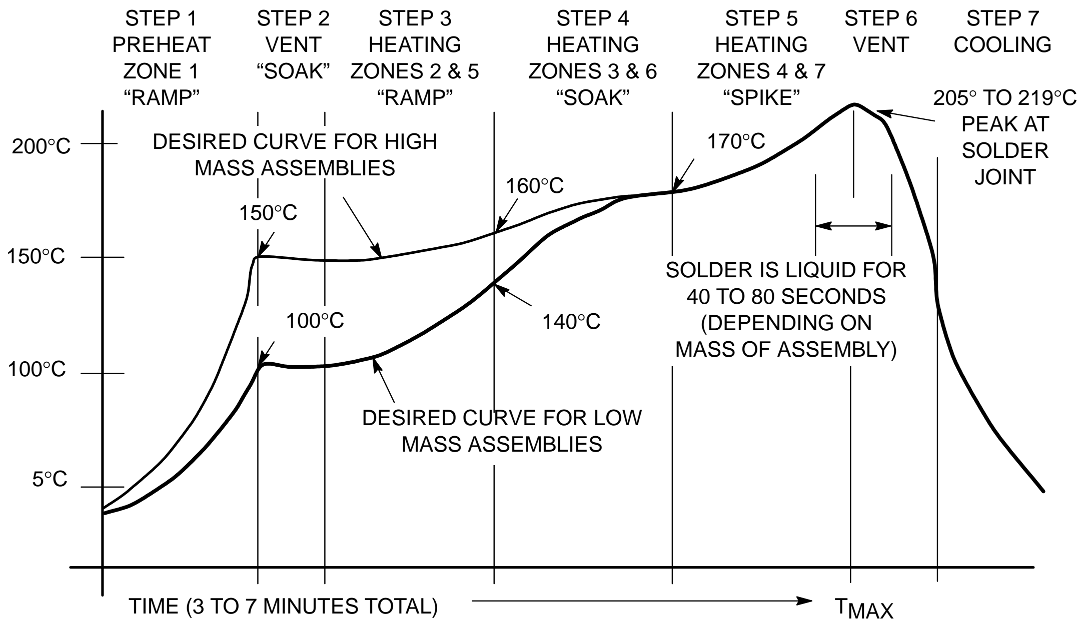



**Figure 16. Typical Solder Heating Profile**

# MMDF2C03HD

Preferred Device

# Power MOSFET 2 Amps, 30 Volts

## Complementary SO–8, Dual

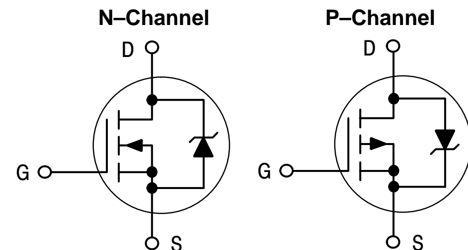
**ON Semiconductor™**

http://onsemi.com

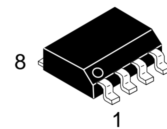
**2 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 70 mΩ (N-Channel)**
**$R_{DS(on)}$ = 200 mΩ (P-Channel)**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain-to-source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc-dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

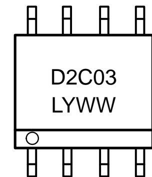
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO-8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO-8 Package Provided




**MARKING DIAGRAM**

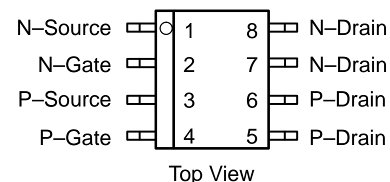



SO–8, Dual
CASE 751
STYLE 14




D2C03 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous N–Channel<br>P–Channel<br>– Pulsed N–Channel<br>P–Channel | $I_D$<br><br>$I_{DM}$ | 4.1<br>3.0<br>21<br>15 | A |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Total Power Dissipation @ $T_A$= 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 V, $V_{GS}$ = 5.0 V, Peak $I_L$ = 9.0 Apk, L = 8.0 mH, $R_G$ = 25 Ω) N–Channel<br>($V_{DD}$ = 30 V, $V_{GS}$ = 5.0 V, Peak $I_L$ = 6.0 Apk, L = 18 mH, $R_G$ = 25 Ω) P–Channel | $E_{AS}$ | <br>324<br><br>324 | mJ |
| Maximum Lead Temperature for Soldering, 0.0625″ from case. Time in Solder Bath is 10 seconds. | $T_L$ | 260 | °C |

1. Negative signs for P–Channel device omitted for clarity.
2. Mounted on 2” square FR4 board (1” sq. 2 oz. Cu 0.06” thick single sided) with one die operating, 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2C03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | – | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | (N)<br>(P) | –<br>– | –<br>– | 1.0<br>1.0 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | (N)<br>(P) | 1.0<br>1.0 | 1.7<br>1.5 | 3.0<br>2.0 | Vdc |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.06<br>0.17 | 0.070<br>0.200 | Ohm |
| Drain–to–Source On–Resistance<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.5 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | (N)<br>(P) | –<br>– | 0.065<br>0.225 | 0.075<br>0.300 | Ohm |
| Forward Transconductance<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc)<br>($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | (N)<br>(P) | 2.0<br>2.0 | 3.6<br>3.4 | –<br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | (N)<br>(P) | –<br>– | 450<br>397 | 630<br>550 | pF |
| Output Capacitance | | $C_{oss}$ | (N)<br>(P) | –<br>– | 160<br>189 | 225<br>250 | |
| Transfer Capacitance | | $C_{rss}$ | (N)<br>(P) | –<br>– | 35<br>64 | 70<br>126 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω)<br>($V_{DD}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 12<br>16 | 24<br>32 | ns |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 65<br>18 | 130<br>36 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 16<br>63 | 32<br>126 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 19<br>194 | 38<br>390 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω)<br>($V_{DD}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | (N)<br>(P) | –<br>– | 8.0<br>9.0 | 16<br>18 | |
| Rise Time | | $t_r$ | (N)<br>(P) | –<br>– | 15<br>10 | 30<br>20 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | (N)<br>(P) | –<br>– | 30<br>81 | 60<br>162 | |
| Fall Time | | $t_f$ | (N)<br>(P) | –<br>– | 23<br>192 | 46<br>384 | |

3. Negative signs for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

**ELECTRICAL CHARACTERISTICS – continued** ($T_A$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | | Symbol | Polarity | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS – continued** (Note 8.) | | | | | | | |
| Total Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc)<br>($V_{DS}$ = 24 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | (N)<br>(P) | –<br>– | 11.5<br>14.2 | 16<br>19 | nC |
| Gate–Source Charge | | $Q_1$ | (N)<br>(P) | –<br>– | 1.5<br>1.1 | –<br>– | |
| Gate–Drain Charge | | $Q_2$ | (N)<br>(P) | –<br>– | 3.5<br>4.5 | –<br>– | |
| | | $Q_3$ | (N)<br>(P) | –<br>– | 2.8<br>3.5 | –<br>– | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** ($T_C$ = 25°C) | | | | | | | |
| Forward Voltage (Note 7.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | (N)<br>(P) | –<br>– | 0.82<br>1.82 | 1.2<br>2.0 | Vdc |
| Reverse Recovery Time | ($I_F$ = $I_S$, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | (N)<br>(P) | –<br>– | 24<br>42 | –<br>– | ns |
| | | $t_a$ | (N)<br>(P) | –<br>– | 17<br>16 | –<br>– | |
| | | $t_b$ | (N)<br>(P) | –<br>– | 7.0<br>26 | –<br>– | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | (N)<br>(P) | –<br>– | 0.025<br>0.043 | –<br>– | µC |

6. Negative signs for P–Channel device omitted for clarity.
7. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
8. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel** | **P–Channel**

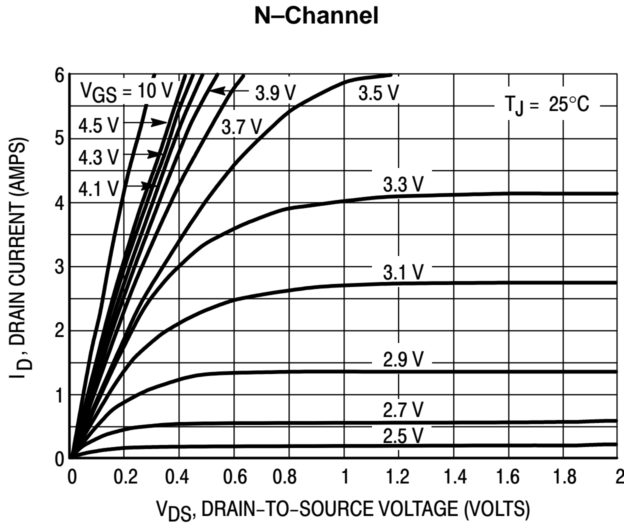



**Figure 1. On–Region Characteristics**

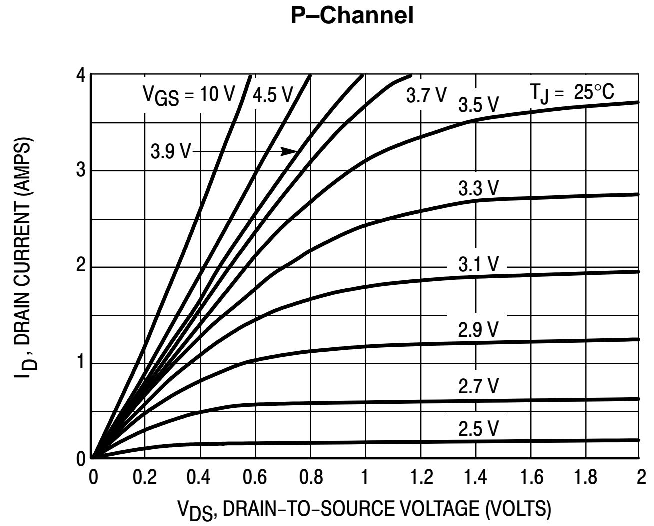



**Figure 1. On–Region Characteristics**

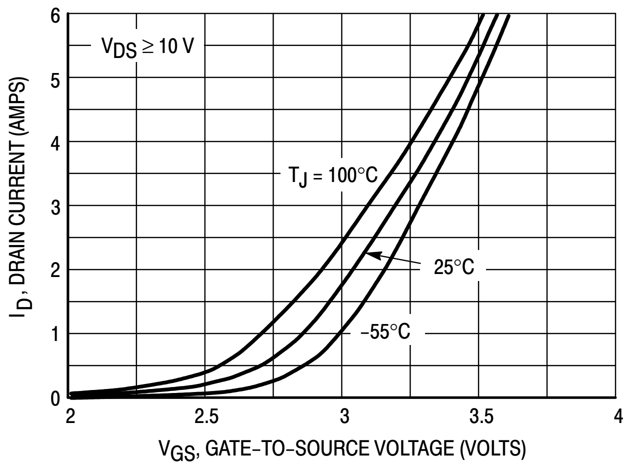



**Figure 2. Transfer Characteristics**

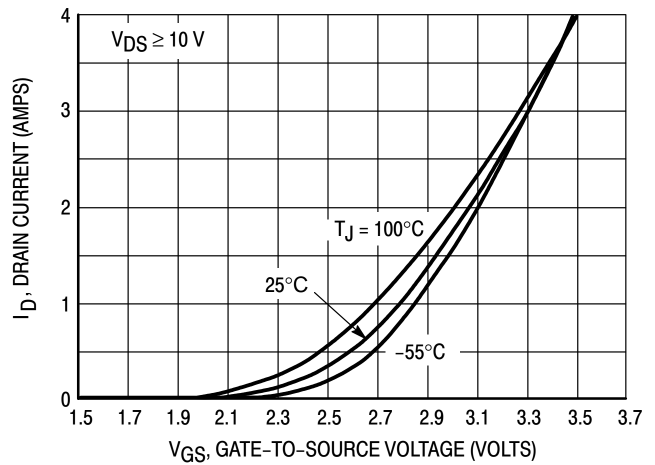



**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

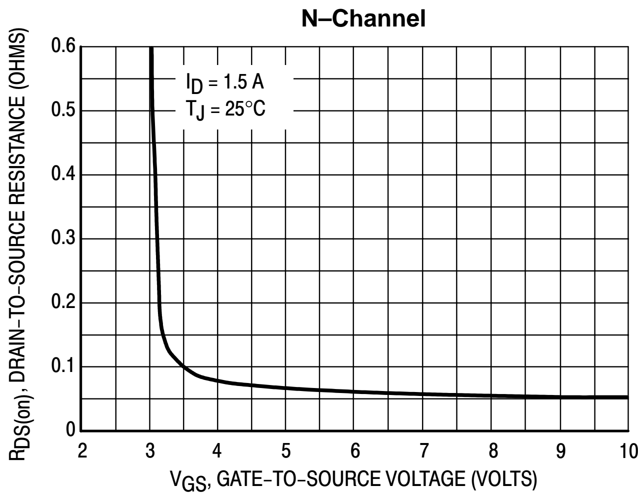



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

**P–Channel**

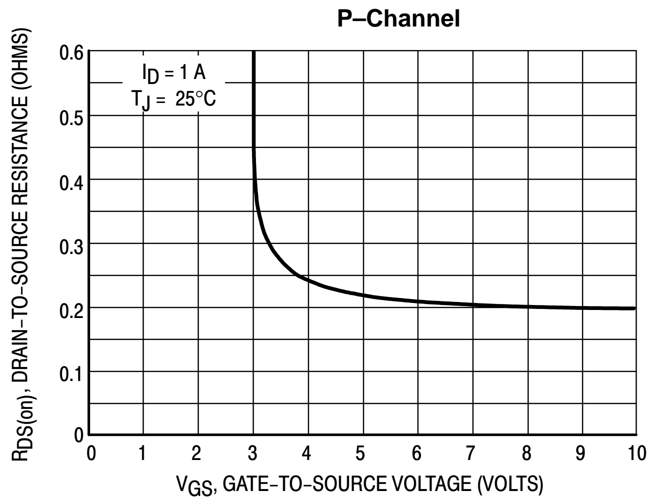



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

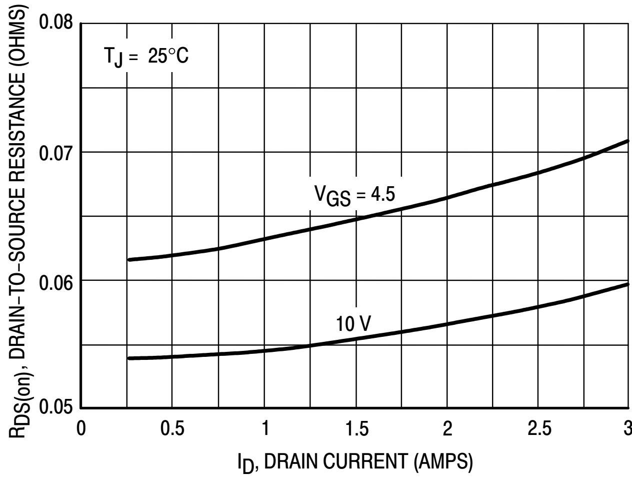



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

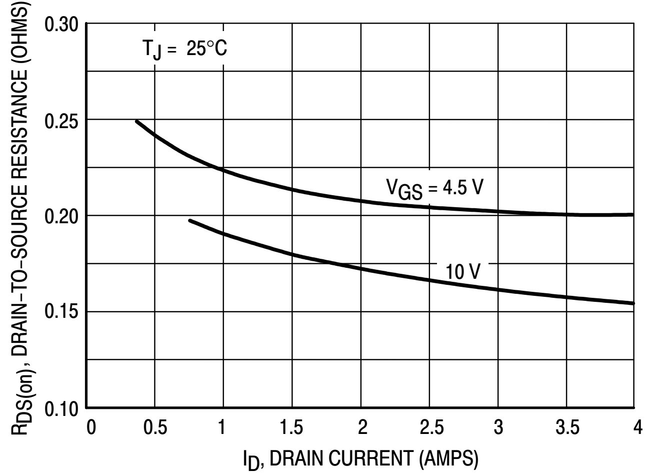



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

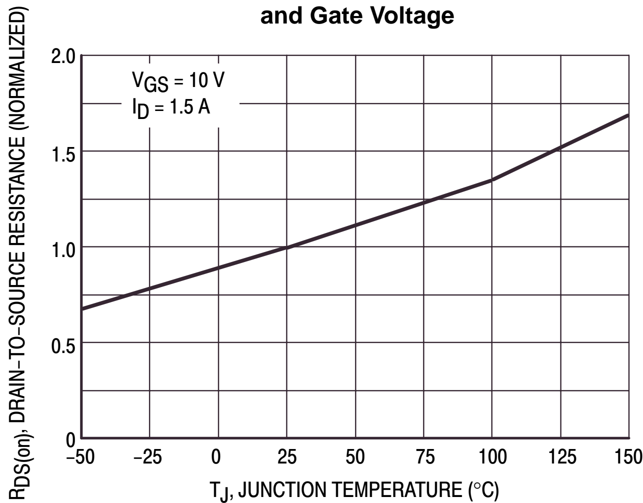



**Figure 5. On–Resistance Variation with Temperature**

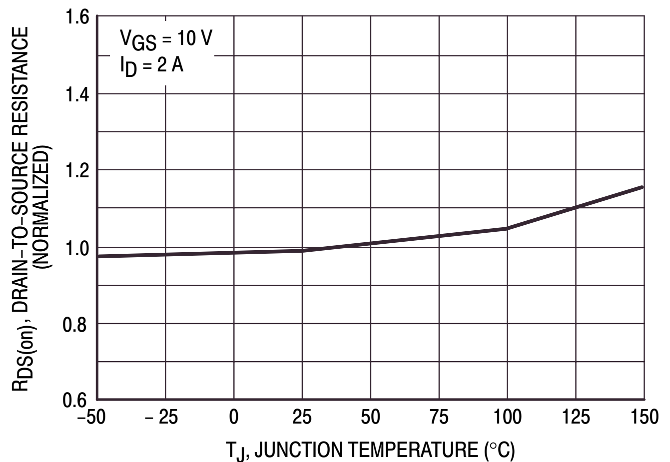



**Figure 5. On–Resistance Variation with Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

**N–Channel**

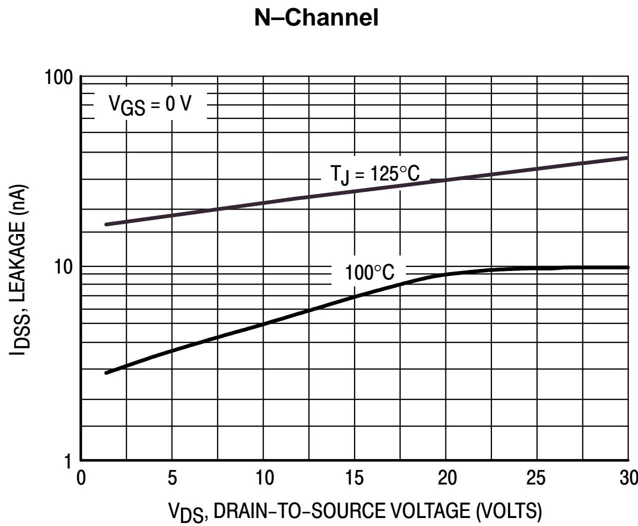



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

**P–Channel**

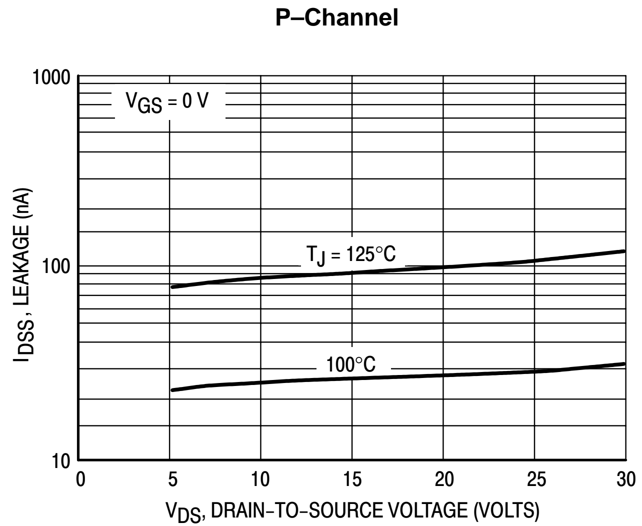



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

**N–Channel** **P–Channel**

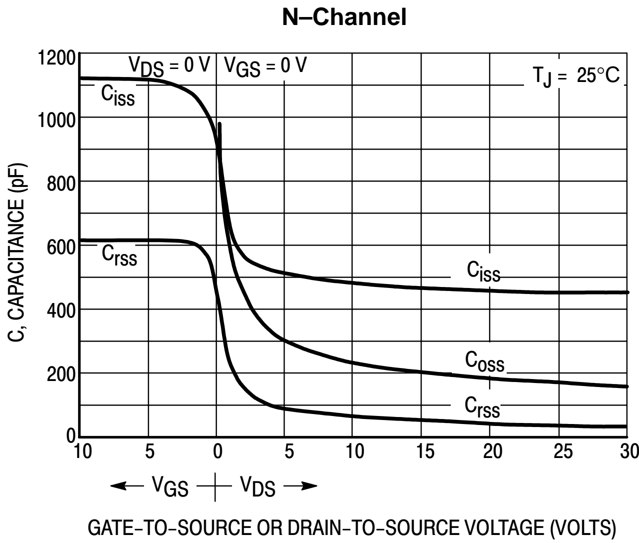



**Figure 7. Capacitance Variation**

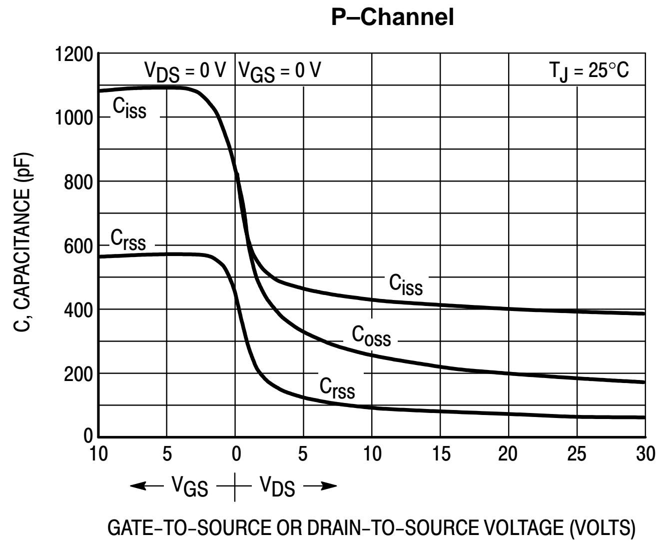



**Figure 7. Capacitance Variation**

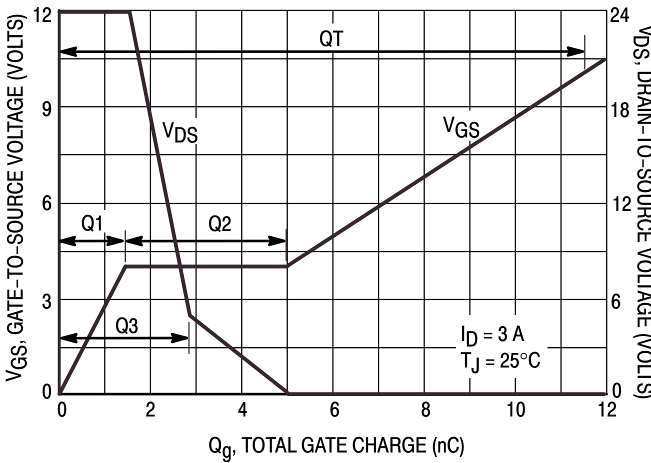



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

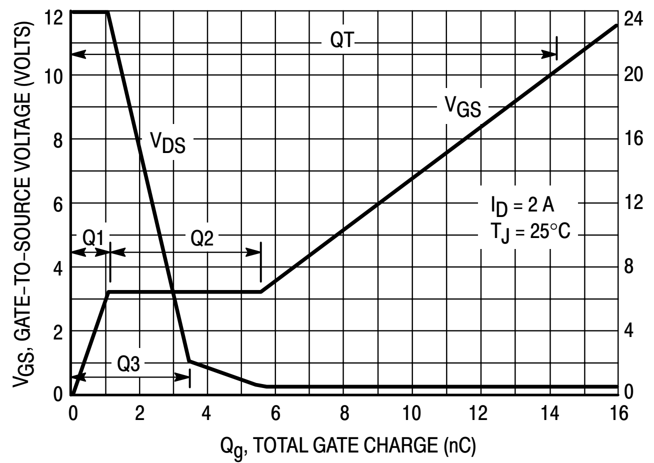



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

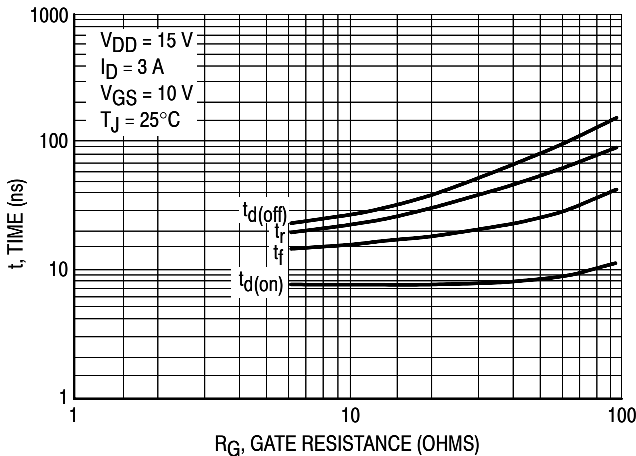



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

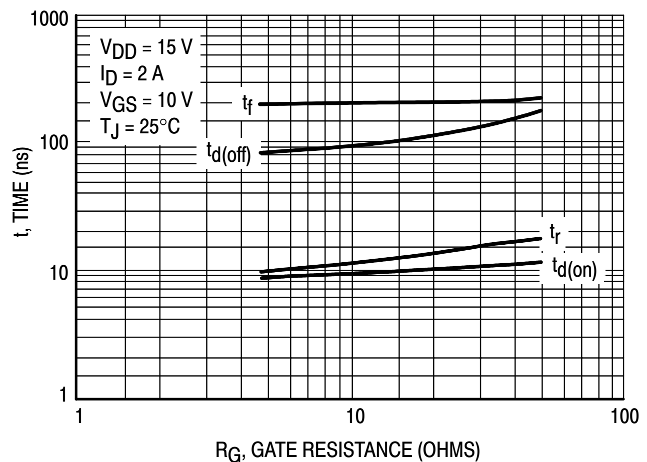



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

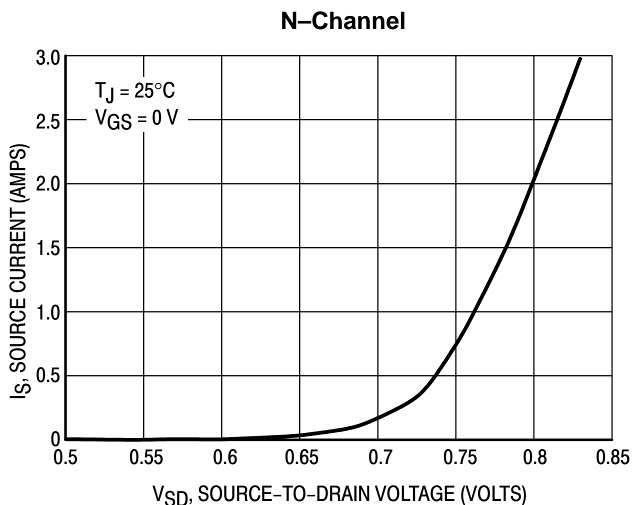



**Figure 10. Diode Forward Voltage versus Current**

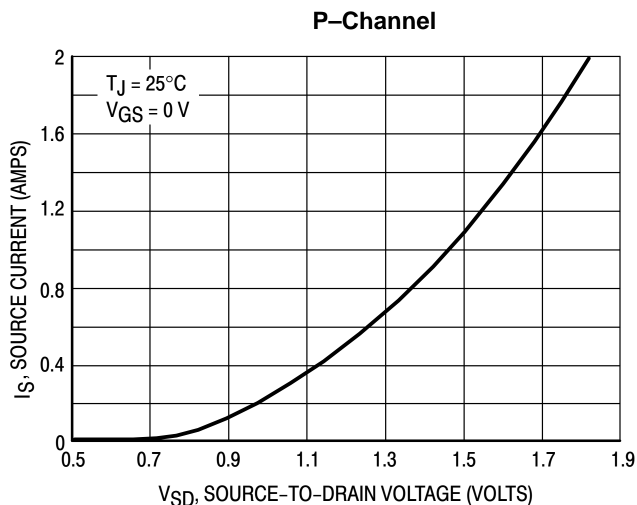



**Figure 10. Diode Forward Voltage versus Current**

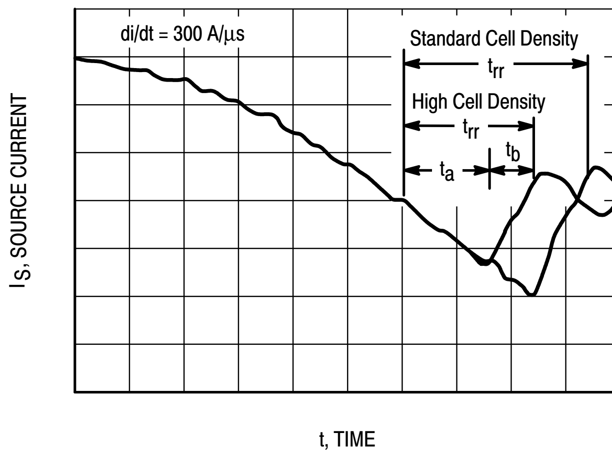



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

**N–Channel**

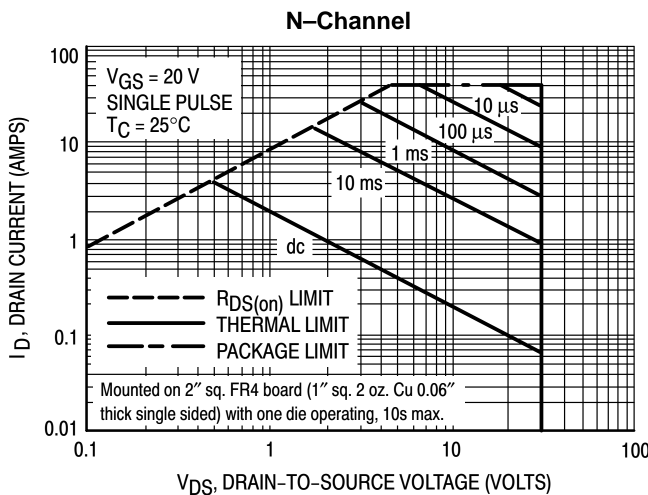



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

**N–Channel**

**P–Channel**

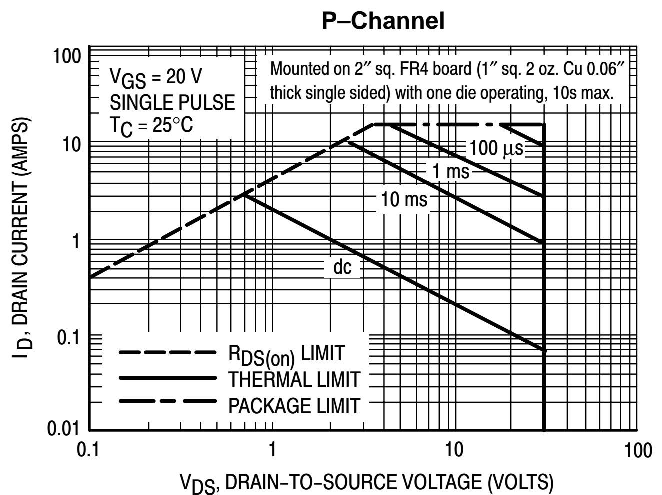



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

**P–Channel**

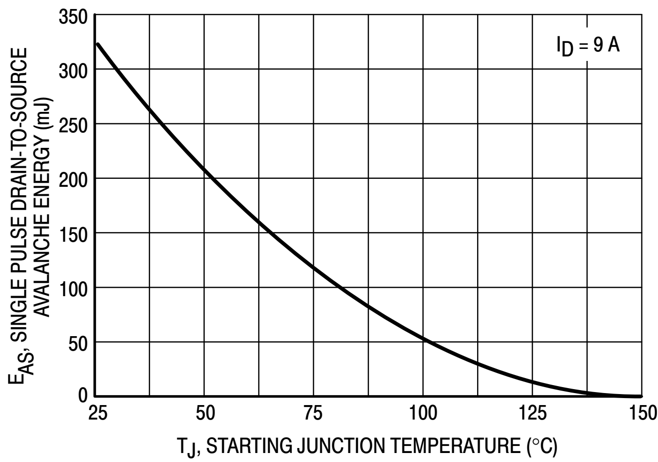



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

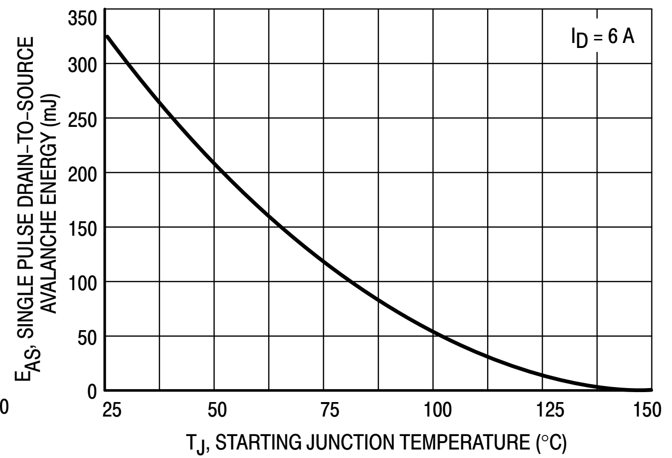



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

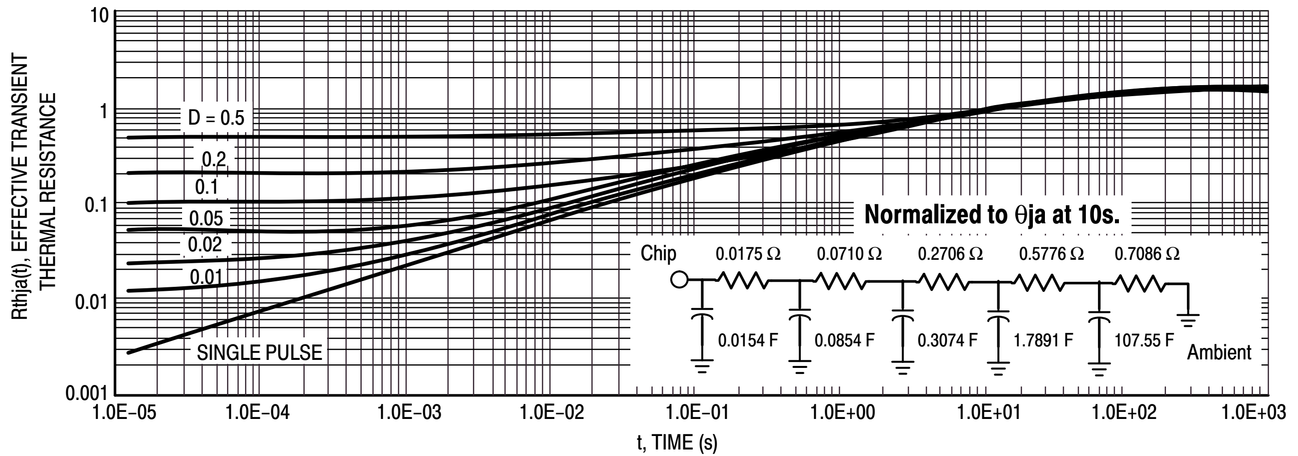



**Figure 14. Thermal Response**

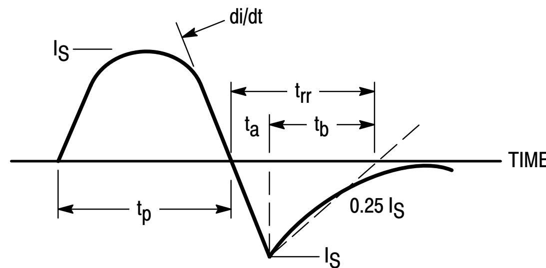
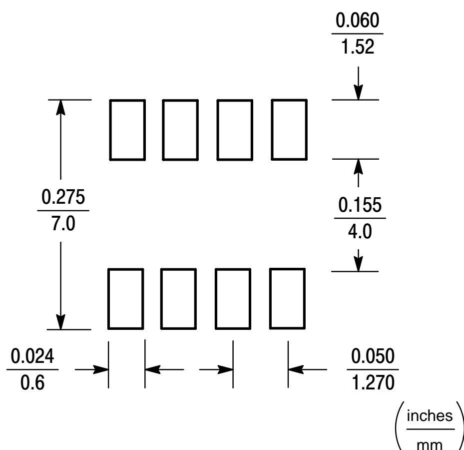



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

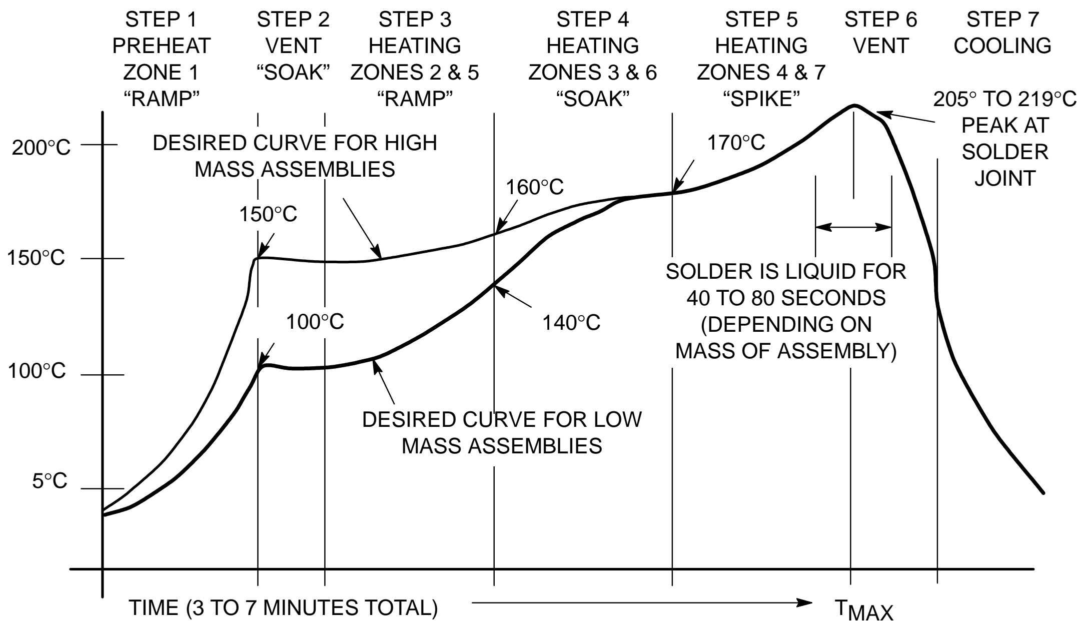



**Figure 16. Typical Solder Heating Profile**

# MMDF2N02E

## Power MOSFET 2 Amps, 25 Volts

### N–Channel SO–8, Dual

ON Semiconductor™

http://onsemi.com

**2 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 100 mΩ**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

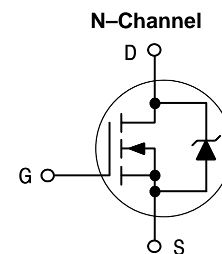
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- $I_{DSS}$ Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

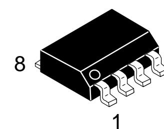
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.6<br>2.5<br>18 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 9.0 Apk, L = 6.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 245 | mJ |
| Thermal Resistance, Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

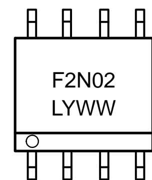
N–Channel



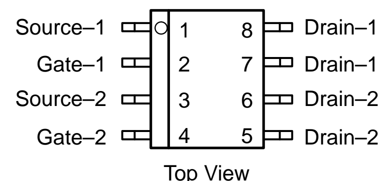

SO–8, Dual
CASE 751
STYLE 11

**MARKING DIAGRAM**




F2N02 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2N02ER2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 25 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc | | $V_{GS(th)}$ | 1.0 | 2.0 | 3.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.2 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | –<br>– | 0.083<br>0.110 | 0.100<br>0.200 | Ohm |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 1.0 | 2.6 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 380 | 532 | pF |
| Output Capacitance | | $C_{oss}$ | – | 235 | 329 | |
| Transfer Capacitance | | $C_{rss}$ | – | 55 | 110 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 7.0 | 21 | ns |
| Rise Time | | $t_r$ | – | 17 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27 | 48 | |
| Fall Time | | $t_f$ | – | 18 | 30 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 10 | 30 | |
| Rise Time | | $t_r$ | – | 35 | 70 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 19 | 38 | |
| Fall Time | | $t_f$ | – | 25 | 50 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 10.6 | 30 | nC |
| | | $Q_1$ | – | 1.3 | – | |
| | | $Q_2$ | – | 2.9 | – | |
| | | $Q_3$ | – | 2.7 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.0 | 1.4 | Vdc |
| Reverse Recovery Time See Figure 11 | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 34 | 66 | ns |
| | | $t_a$ | – | 17 | – | |
| | | $t_b$ | – | 17 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

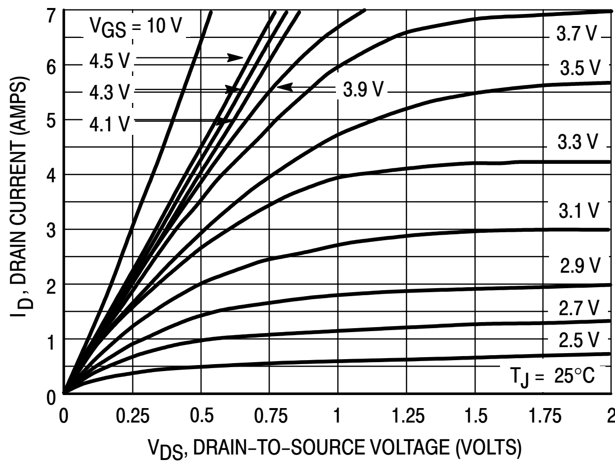


**Figure 1. On–Region Characteristics**

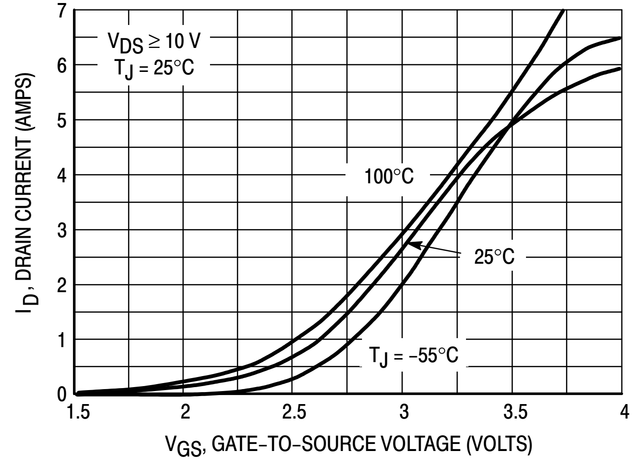


**Figure 2. Transfer Characteristics**

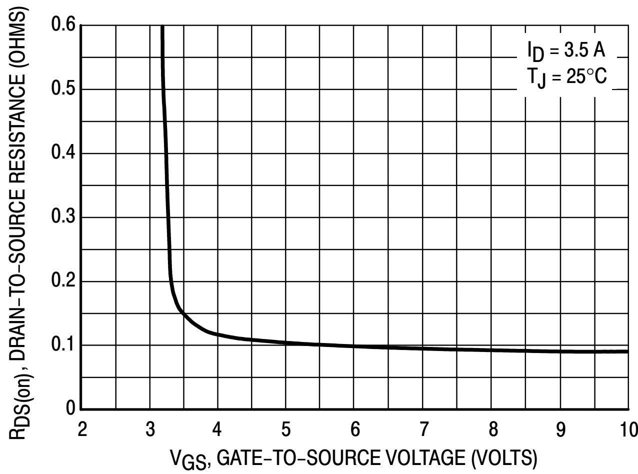


**Figure 3. On–Resistance versus Gate–to–Source Voltage**

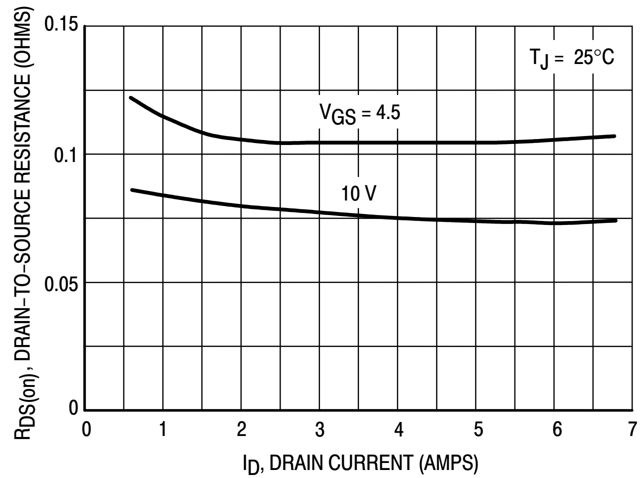


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

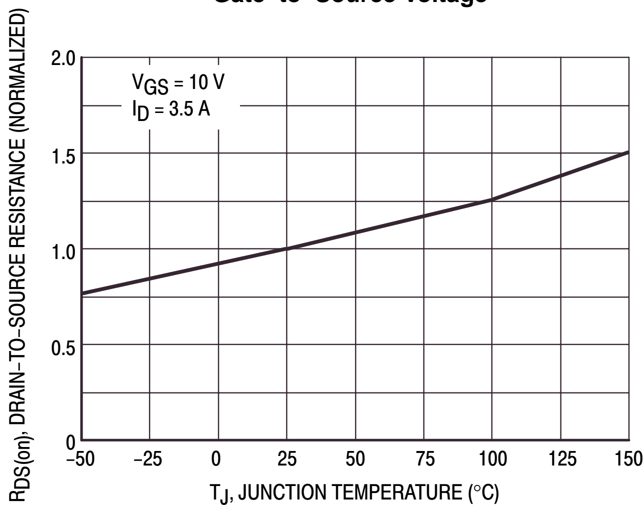


**Figure 5. On–Resistance Variation with Temperature**

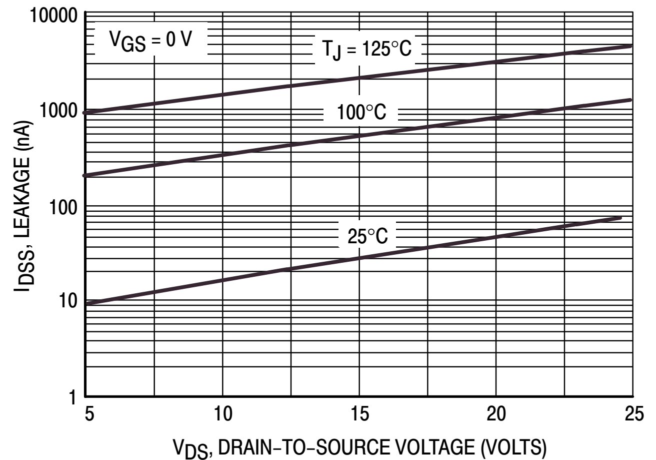


**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \mathrm{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \mathrm{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

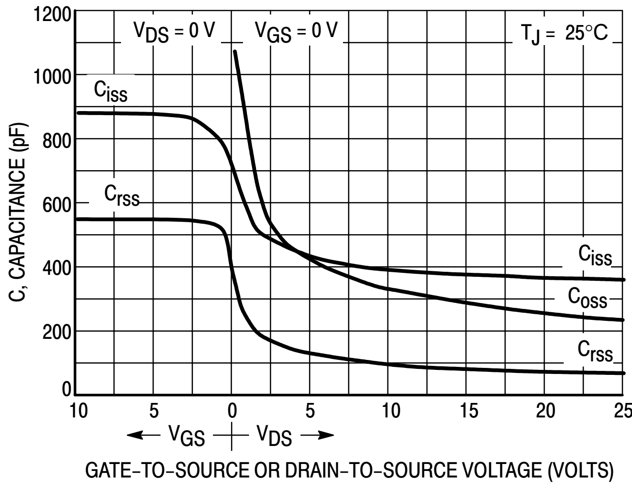


**Figure 7. Capacitance Variation**

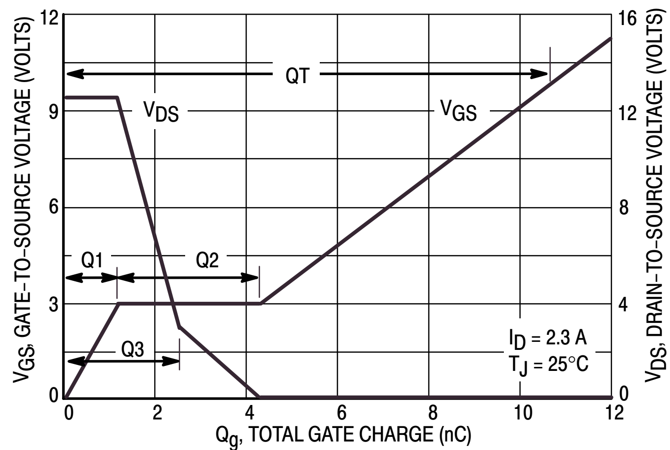


**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

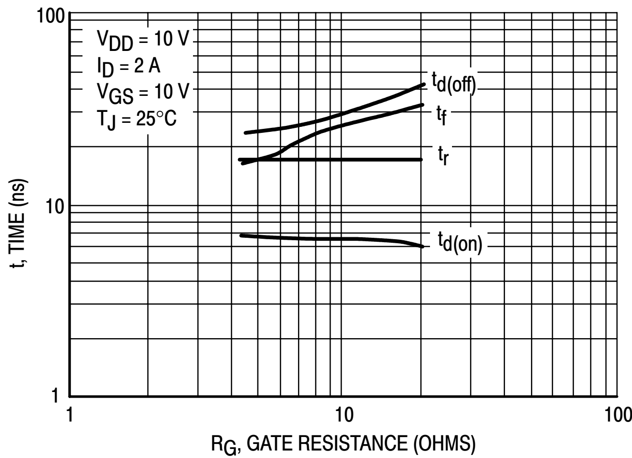


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

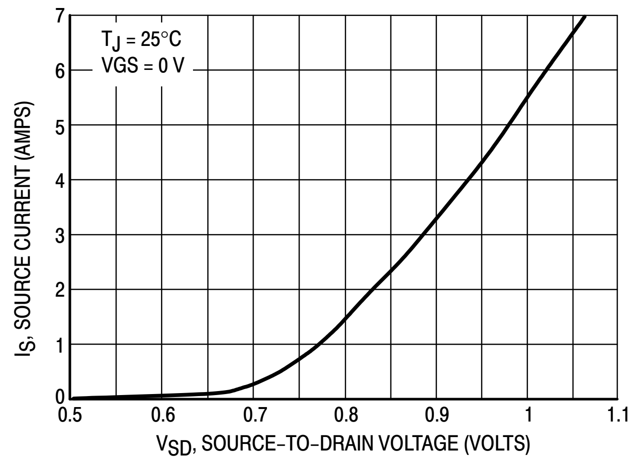


**Figure 10. Diode Forward Voltage versus Current**

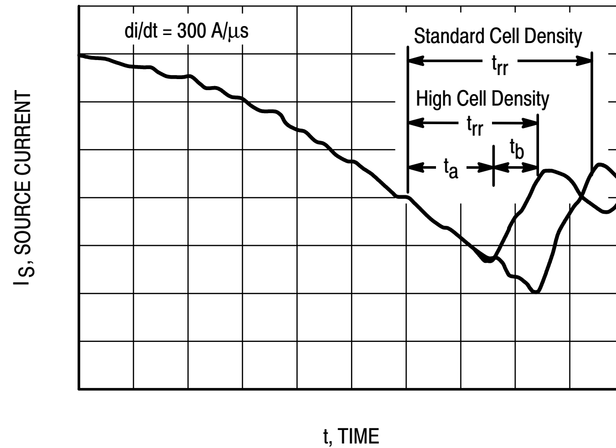


**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

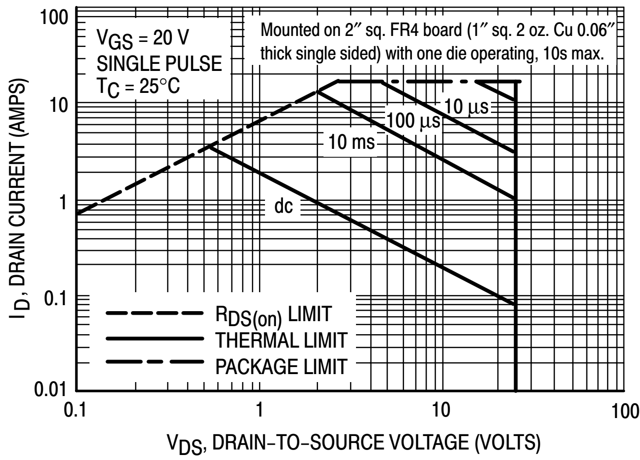


**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

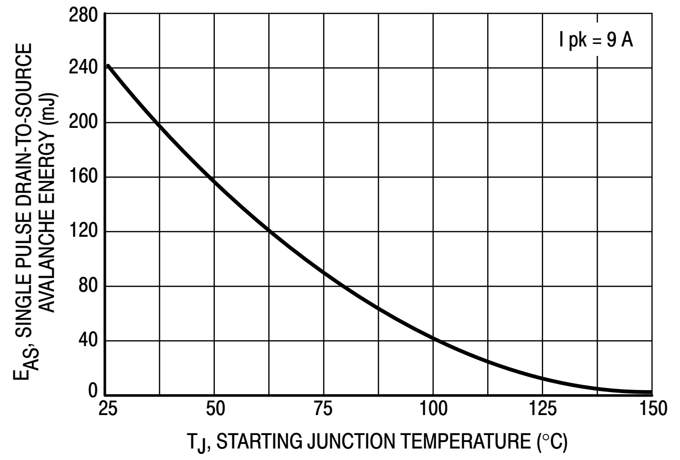


**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

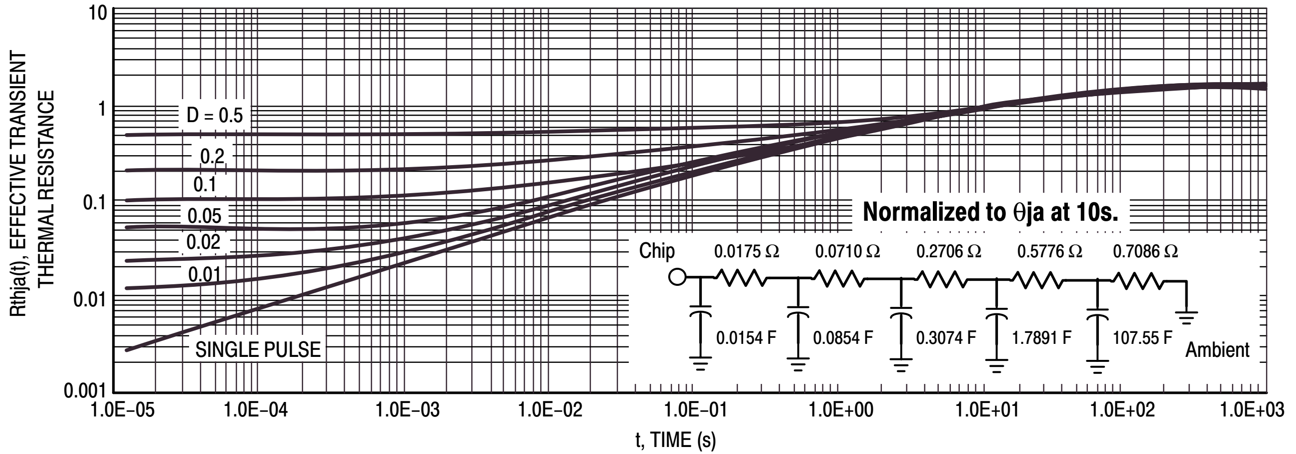


**Figure 14. Thermal Response**

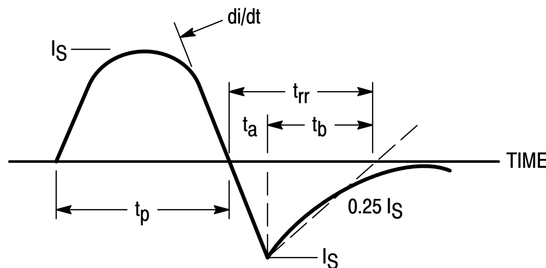


**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

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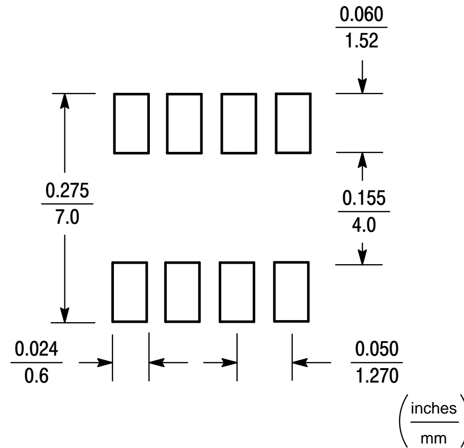
Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

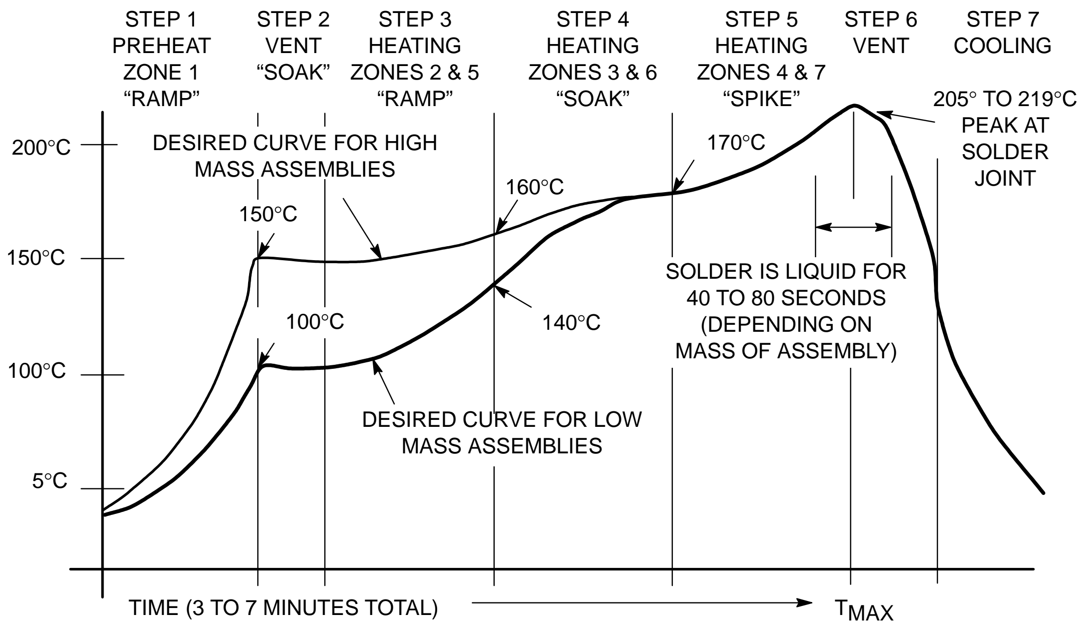



**Figure 16. Typical Solder Heating Profile**

# MMDF2N05ZR2

**Preferred Device**

# Power MOSFET 2 Amps, 50 Volts

## N–Channel SO–8, Dual

**ON Semiconductor™**

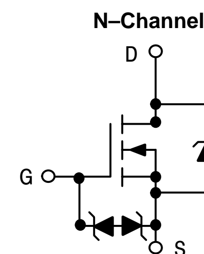
**http://onsemi.com**

EZFETs™ are an advanced series of power MOSFETs which contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

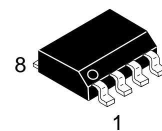
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**2 AMPERES**
**50 VOLTS**
**$R_{DS(on)}$ = 300 mΩ**

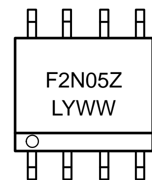
**N–Channel**




**MARKING DIAGRAM**




**SO–8, Dual**
**CASE 751**
**STYLE 11**



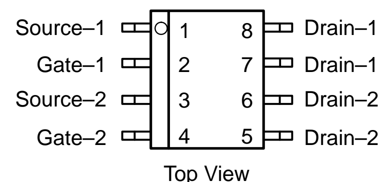

F2N05Z = Device Code
L = Location Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 50 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 50 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 15 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 2.0<br>1.7<br>8.0 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction to Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Temperature for Soldering Purposes | $T_L$ | 260 | °C |

1. When mounted on G10/FR–4 glass epoxy board using minimum recommended footprint.

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2N05ZR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

© Semiconductor Components Industries, LLC, 2000

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>50<br>– | <br>56<br>55 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 55°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>2.0<br>25 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | 0.14 | 0.5 | |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>–5.0 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 0.6 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>200<br>350 | <br>300<br>500 | mΩ |
| Forward Transconductance<br>($V_{DS}$ = 15 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | <br>– | <br>2.0 | <br>– | mMhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 104 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 58 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 16 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 0.6 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 25 Ω) | $t_{d(on)}$ | – | 24 | 48 | ns |
| Rise Time | | $t_r$ | – | 46 | 92 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 130 | 260 | |
| Fall Time | | $t_f$ | – | 71 | 142 | |
| Gate Charge<br>(see figure 8) | ($V_{DS}$ = 25 Vdc, $I_D$ = 1.3 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 3.3 | 4.6 | nC |
| | | $Q_1$ | – | 0.7 | – | |
| | | $Q_2$ | – | 1.3 | – | |
| | | $Q_3$ | – | 1.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.82 | 1.4 | Vdc |
| Reverse Recovery Time | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 66 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 43 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.08 | – | µC |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

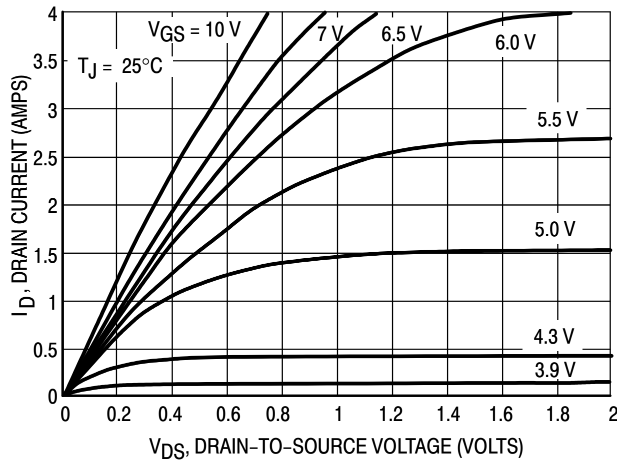



**Figure 1. On−Region Characteristics**

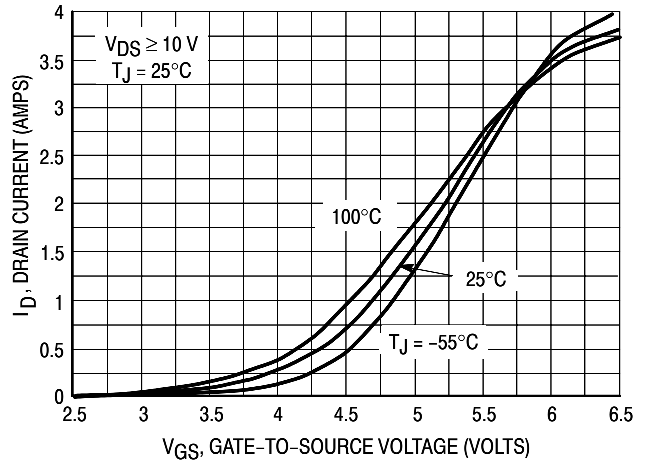



**Figure 2. Transfer Characteristics**

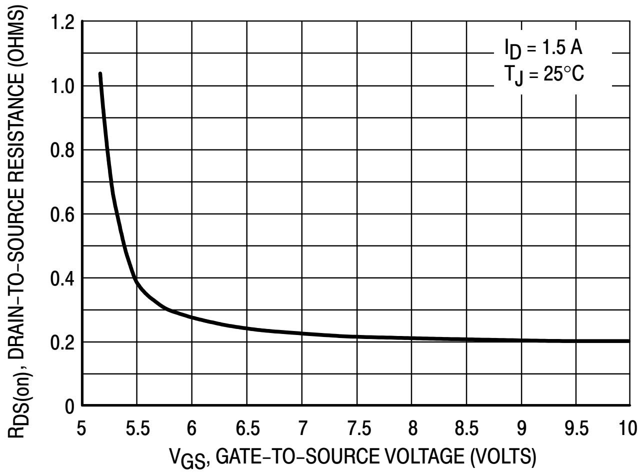



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

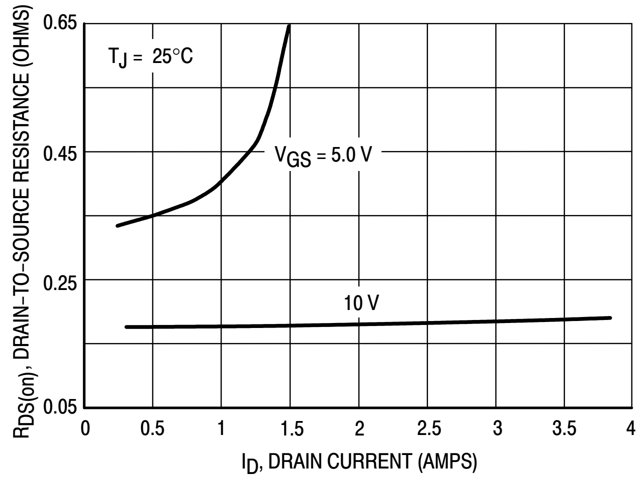



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

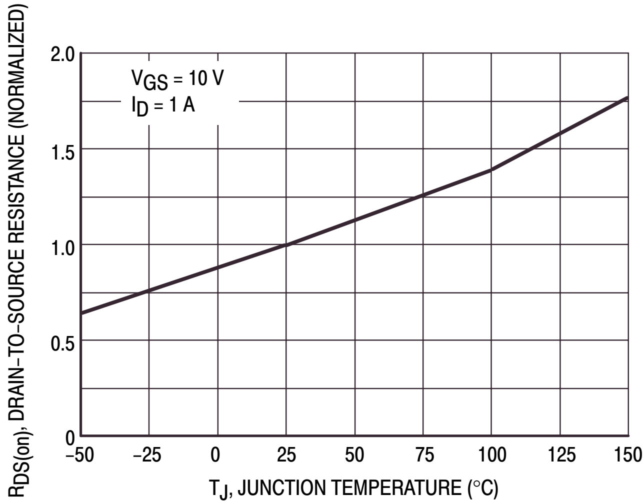



**Figure 5. On−Resistance Variation with Temperature**

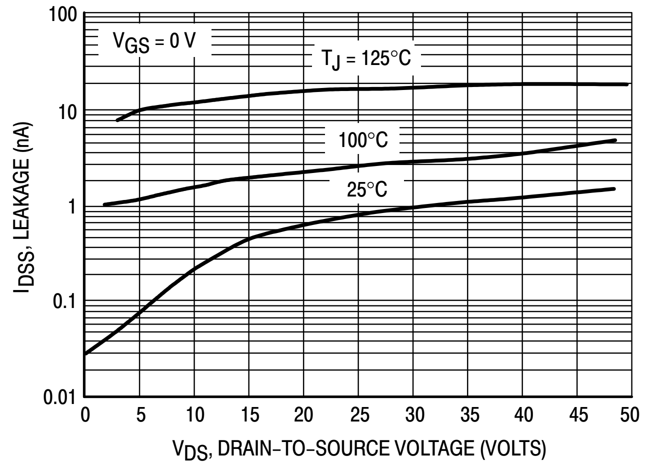



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

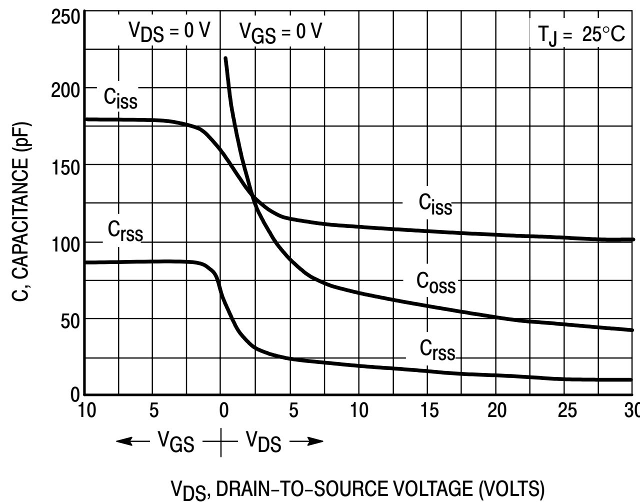



**Figure 7. Capacitance Variation**

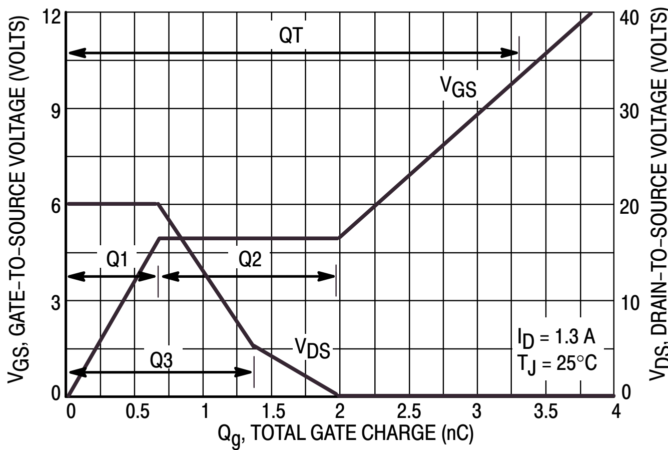



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

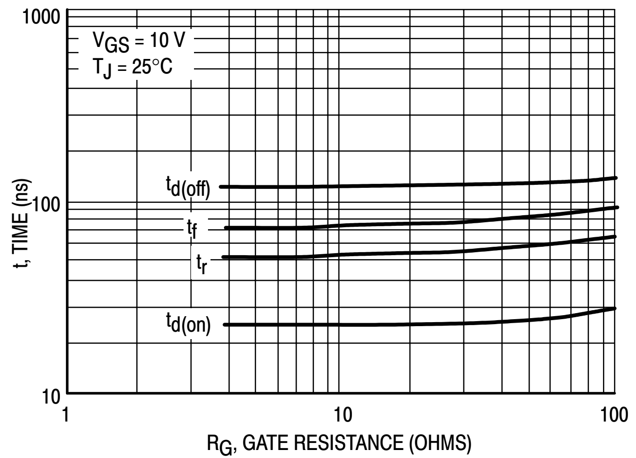



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

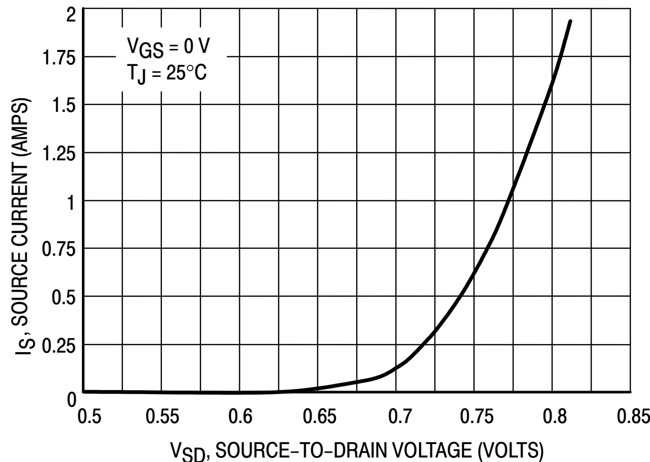



**Figure 10. Diode Forward Voltage versus Current**

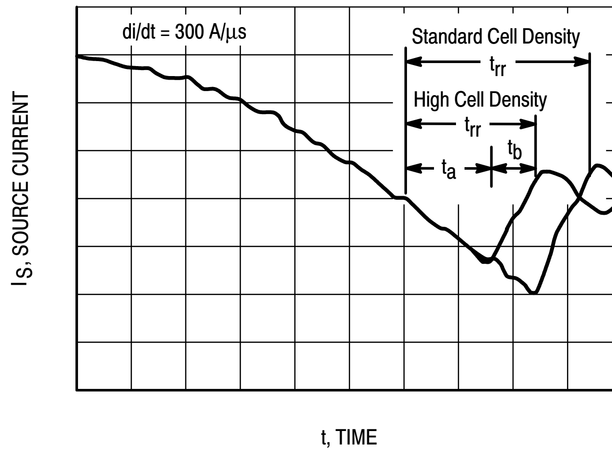



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

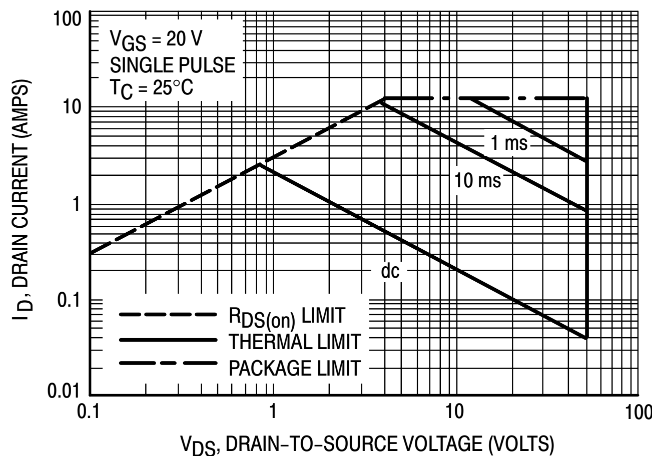



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

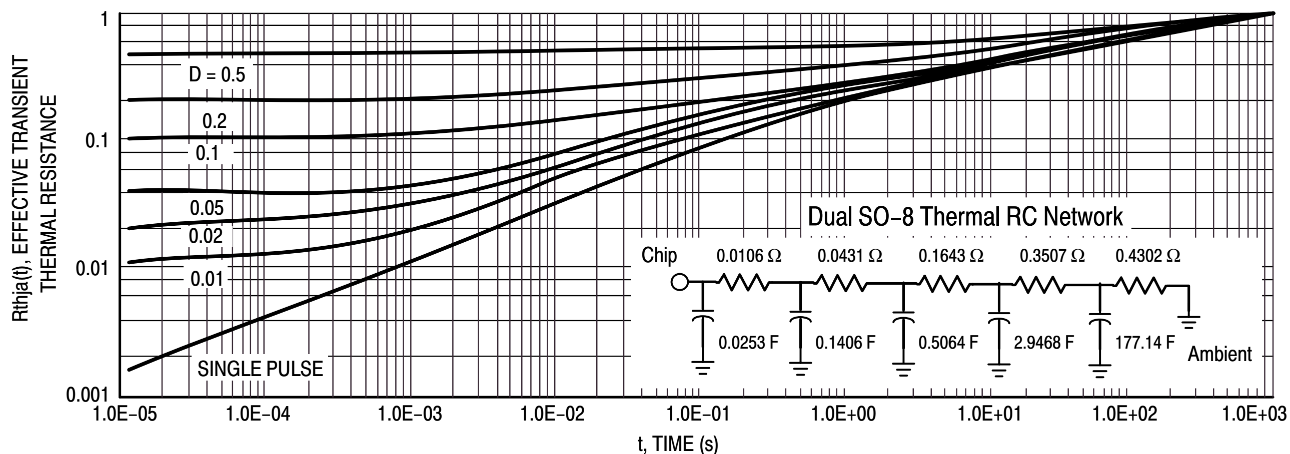



**Figure 13. Thermal Response**

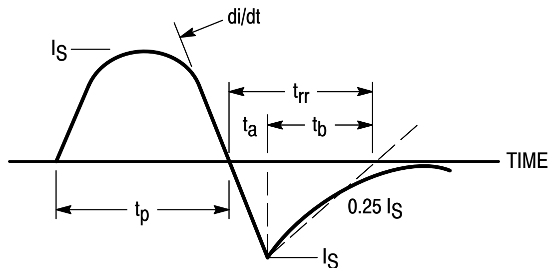
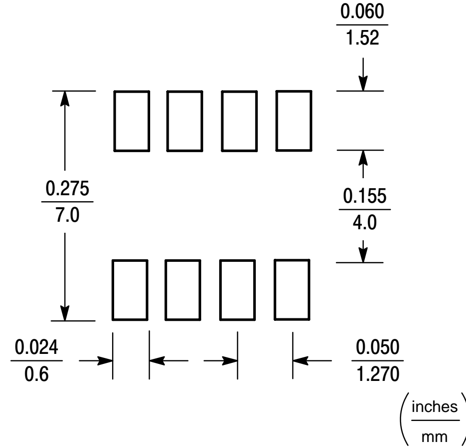



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

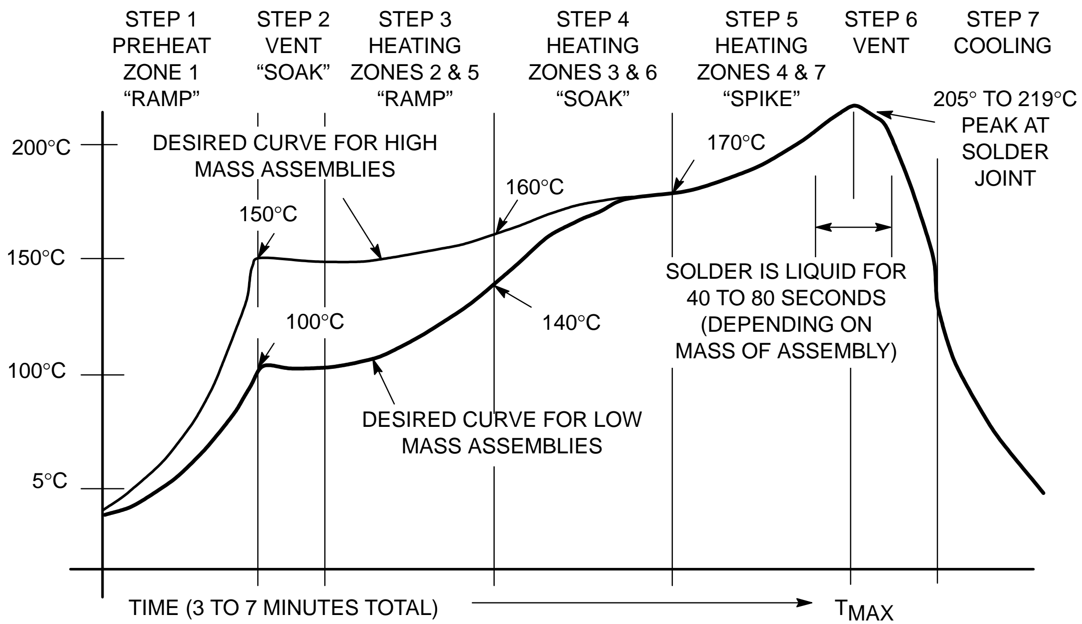



**Figure 15. Typical Solder Heating Profile**

# MMDF2P01HD

**Preferred Device**

# Power MOSFET 2 Amps, 12 Volts

## P–Channel SO–8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

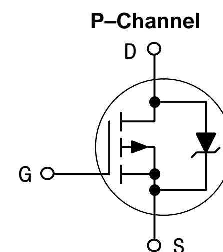
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**ON Semiconductor™**

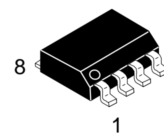
**http://onsemi.com**

**2 AMPERES**
**12 VOLTS**
**$R_{DS(on)}$ = 180 mΩ**

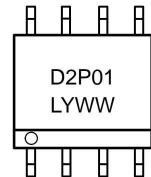
**P–Channel**




**MARKING DIAGRAM**

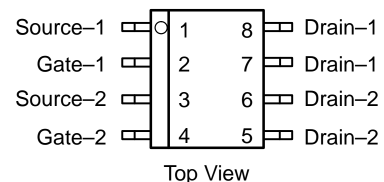



**SO–8, Dual**
**CASE 751**
**STYLE 11**




D2P01 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 12 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 12 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.4<br>2.1<br>17 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | | – 55 to 150 | °C |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2P01HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 12 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 17 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.7 | 1.0 | 1.1 | Vdc |
| Temperature Coefficient (Negative) | | | – | 3.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | – | 0.16 | 0.180 | Ohm |
| (VGS = 2.7 Vdc, $I_D$ = 1.0 Adc) | | | – | 0.2 | 0.220 | |
| Forward Transconductance ($V_{DS}$ = 2.5 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 3.0 | 4.75 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 530 | 740 | pF |
| Output Capacitance | | $C_{oss}$ | – | 410 | 570 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 177 | 250 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 21 | 45 | ns |
| Rise Time | | $t_r$ | – | 156 | 315 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 38 | 75 | |
| Fall Time | | $t_f$ | – | 68 | 135 | |
| Turn–On Delay Time | ($V_{DS}$ = 6.0 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | 35 | |
| Rise Time | | $t_r$ | – | 44 | 90 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 68 | 135 | |
| Fall Time | | $t_f$ | – | 54 | 110 | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 9.3 | 13 | nC |
| | | $Q_1$ | – | 0.8 | – | |
| | | $Q_2$ | – | 4.0 | – | |
| | | $Q_3$ | – | 3.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.69 | 2.0 | Vdc |
| | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 1.2 | – | |
| Reverse Recovery Time | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 48 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 25 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.05 | – | μC |

3. Negative sign for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

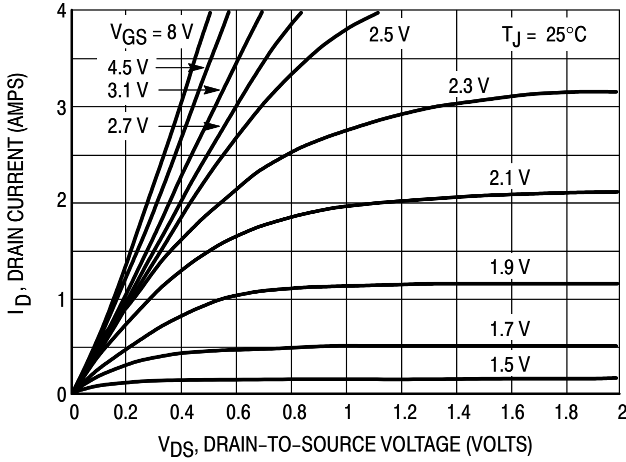



**Figure 1. On–Region Characteristics**

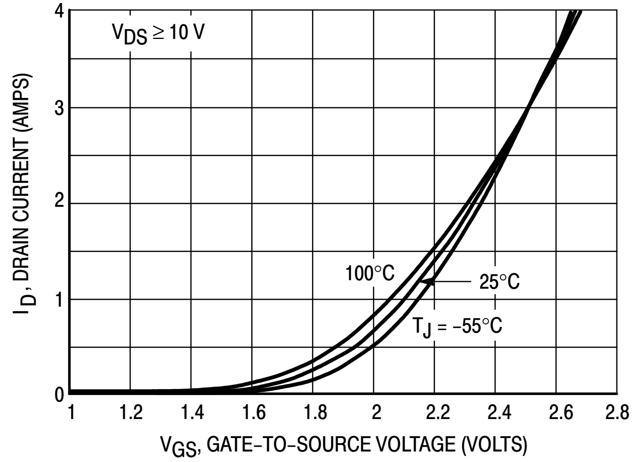



**Figure 2. Transfer Characteristics**

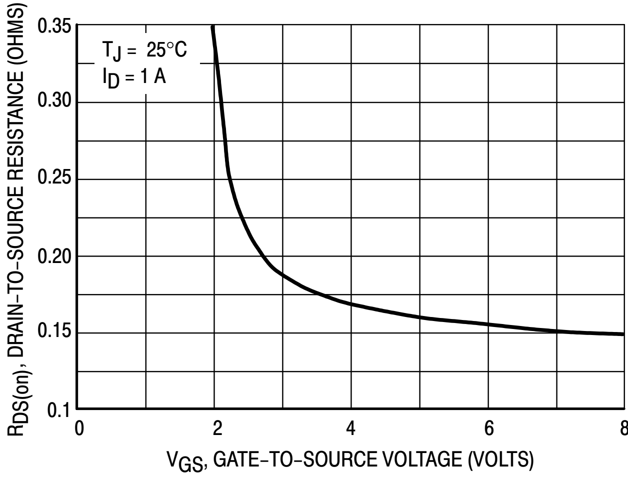



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

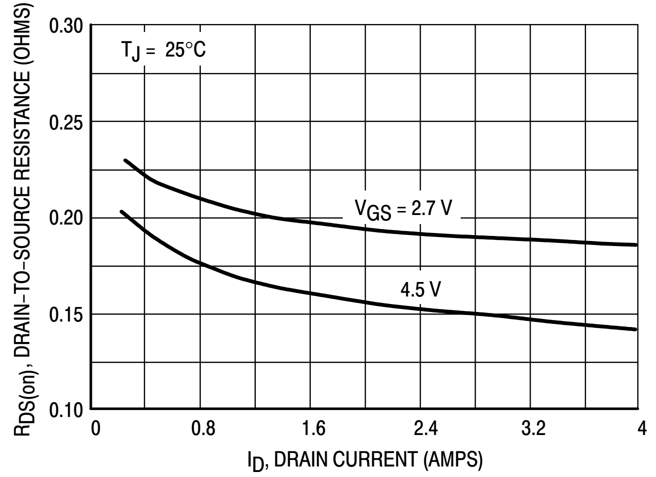



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

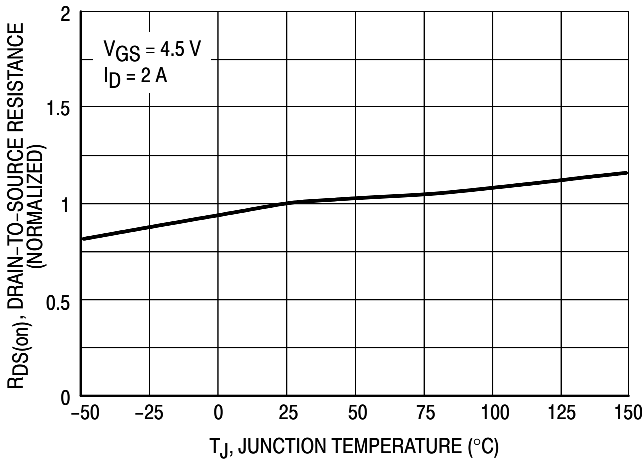



**Figure 5. On–Resistance Variation with Temperature**

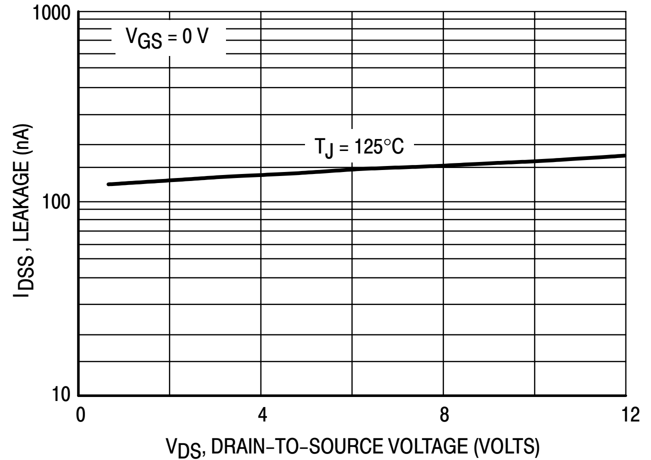



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

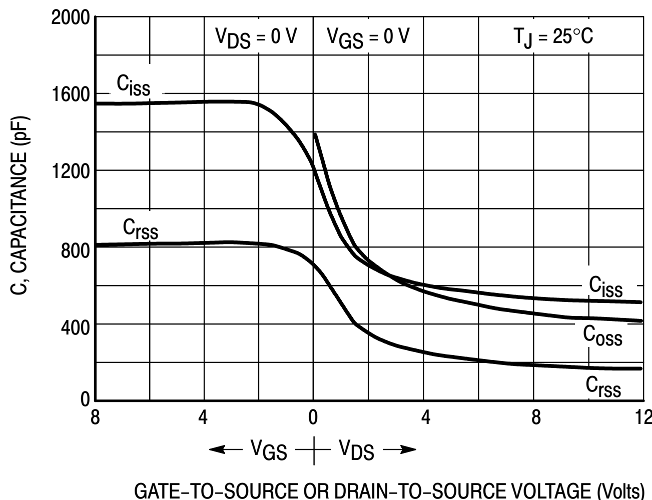



**Figure 7. Capacitance Variation**

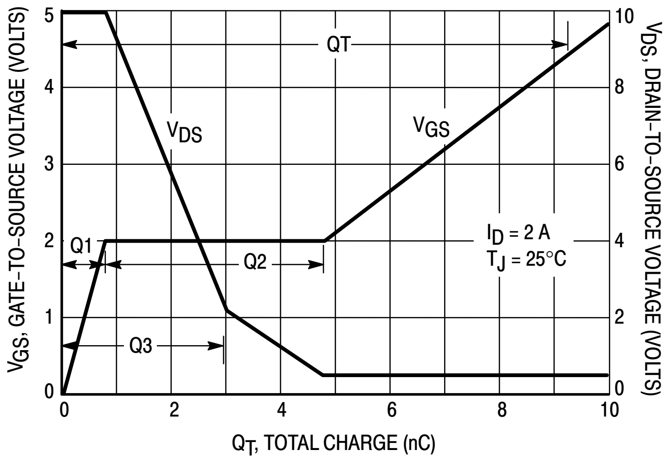



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

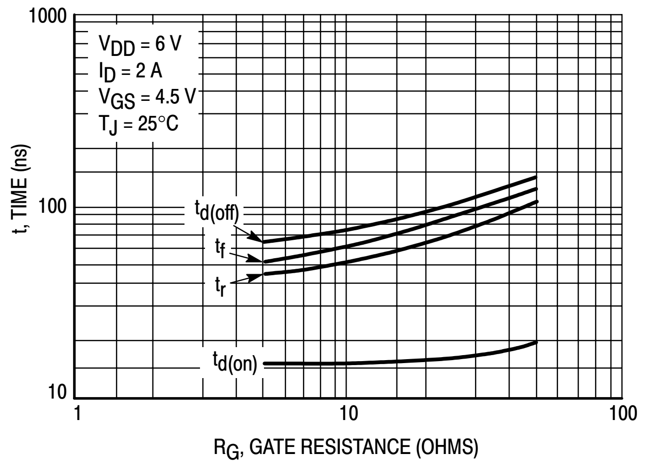



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

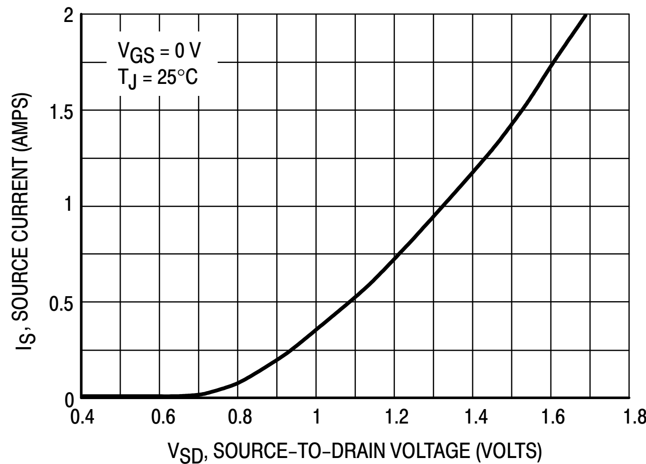



**Figure 10. Diode Forward Voltage versus Current**

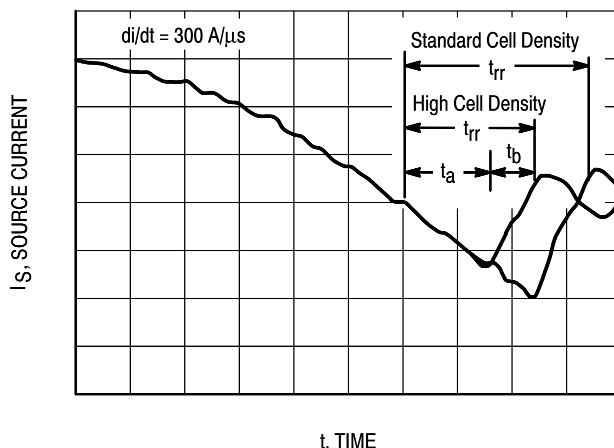



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

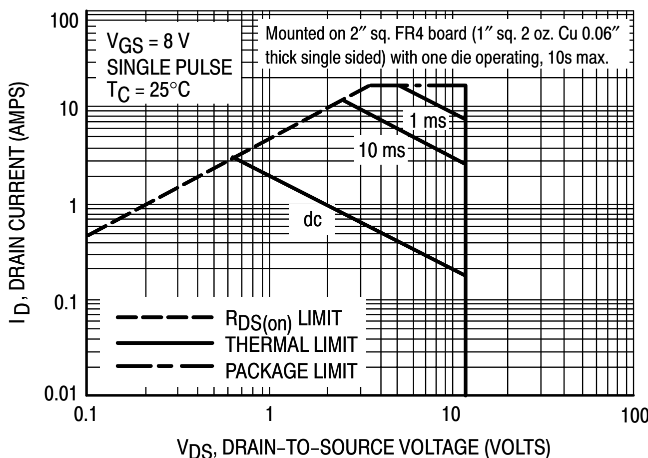



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

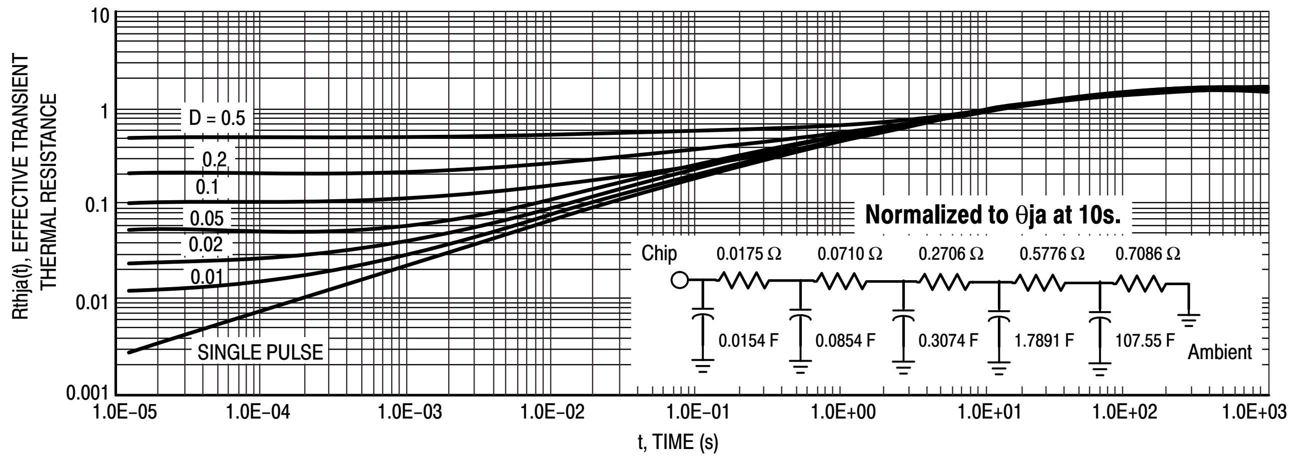



**Figure 13. Thermal Response**

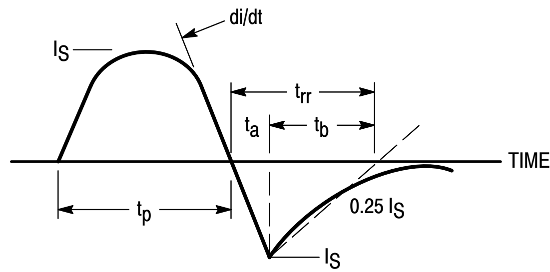
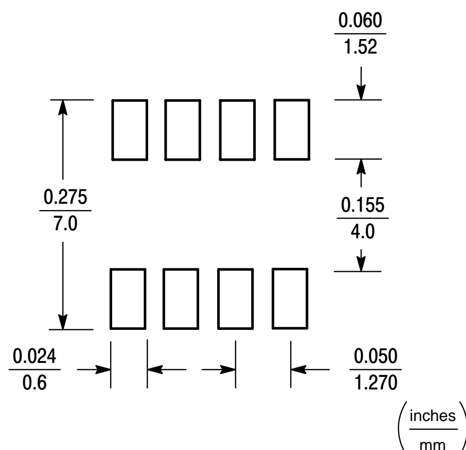



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

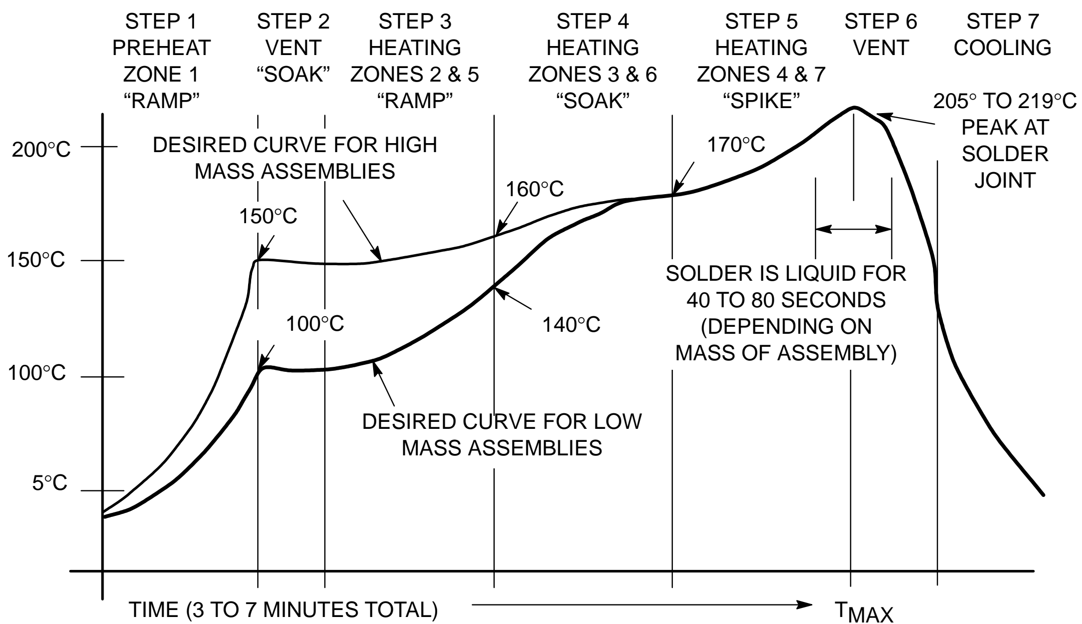



**Figure 15. Typical Solder Heating Profile**

# MMDF2P02E

**ON Semiconductor™**

**http://onsemi.com**

## Power MOSFET 2 Amps, 25 Volts

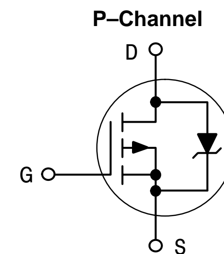
### P–Channel SO–8, Dual

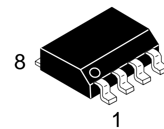
These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperatures
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

**2 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 250 mΩ**

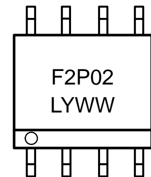
**P–Channel**



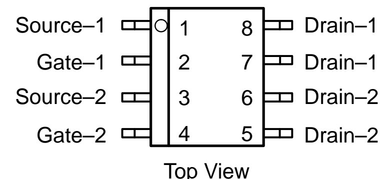

**SO–8, Dual**
**CASE 751**
**STYLE 11**

**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 2.5<br>1.7<br>13 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Derate above 25°C | $P_D$ | 2.0<br>16 | W<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 7.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 245 | mJ |
| Thermal Resistance, Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2P02ER2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 25<br>– | –<br>2.2 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 2.0<br>3.8 | 3.0<br>– | Vdc |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | –<br>– | 0.19<br>0.3 | 0.25<br>0.4 | Ohm |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 1.0 | 2.8 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 340 | 475 | pF |
| Output Capacitance | | $C_{oss}$ | – | 220 | 300 | |
| Transfer Capacitance | | $C_{rss}$ | – | 75 | 150 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | 40 | ns |
| Rise Time | | $t_r$ | – | 40 | 80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 53 | 106 | |
| Fall Time | | $t_f$ | – | 41 | 82 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 13 | 26 | |
| Rise Time | | $t_r$ | – | 29 | 58 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 60 | |
| Fall Time | | $t_f$ | – | 28 | 56 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 10 | 15 | nC |
| | | $Q_1$ | – | 1.0 | – | |
| | | $Q_2$ | – | 3.5 | – | |
| | | $Q_3$ | – | 3.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.5 | 2.0 | Vdc |
| Reverse Recovery Time<br>See Figure 11 | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 32 | 64 | ns |
| | | $t_a$ | – | 19 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.035 | – | μC |

3. Negative sign for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

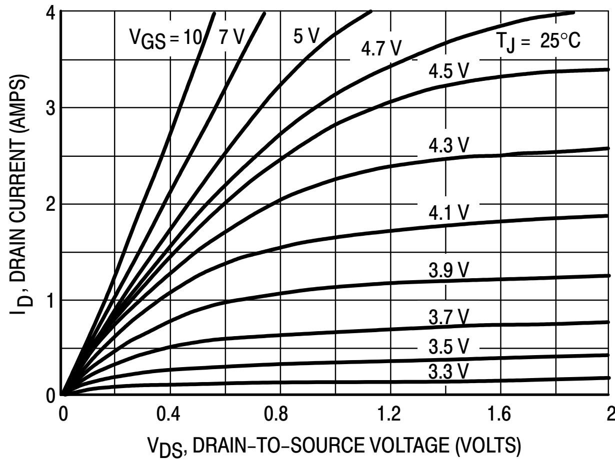



**Figure 1. On–Region Characteristics**

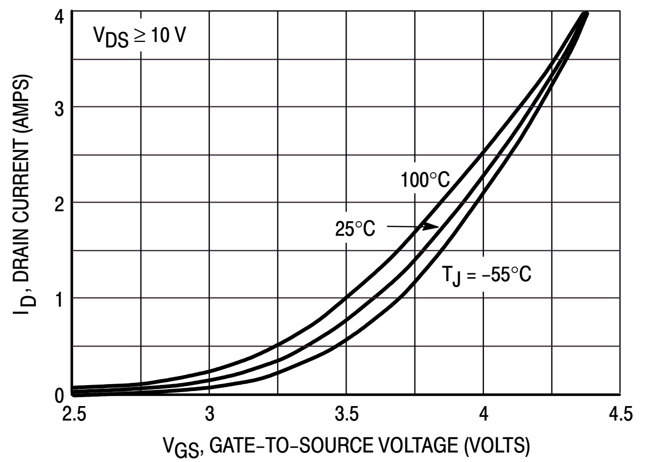



**Figure 2. Transfer Characteristics**

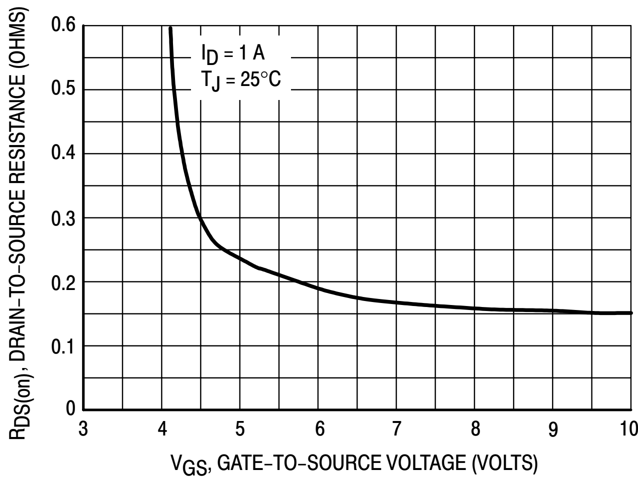



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

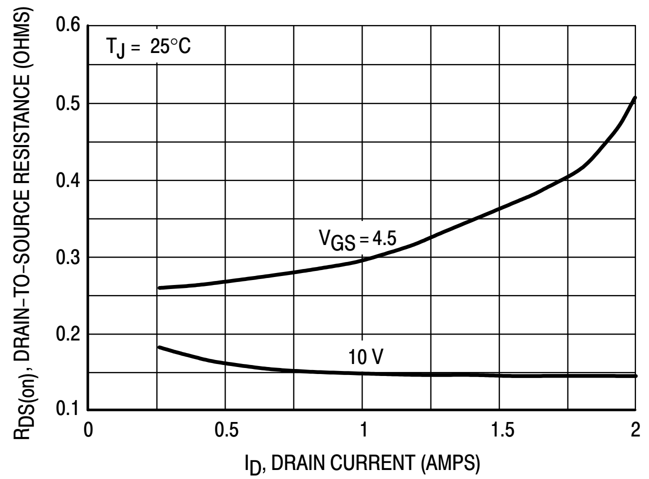



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

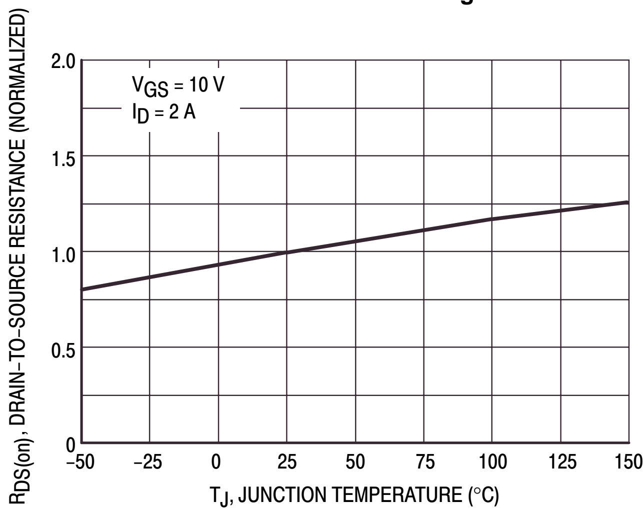



**Figure 5. On–Resistance Variation with Temperature**

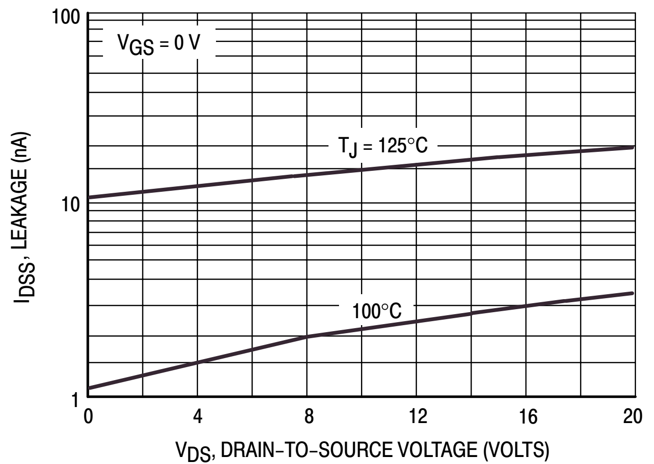



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

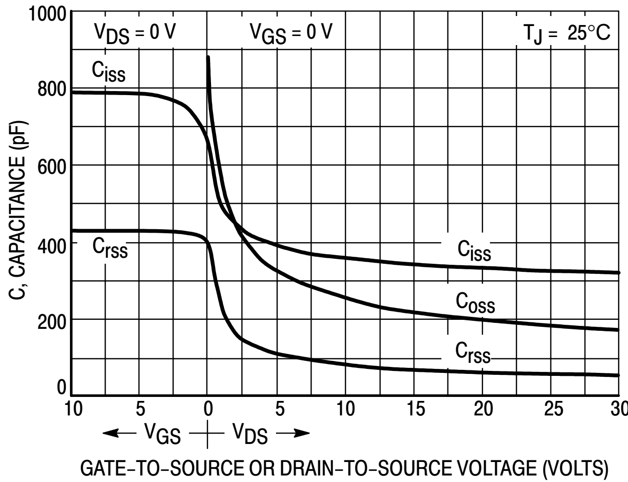



**Figure 7. Capacitance Variation**

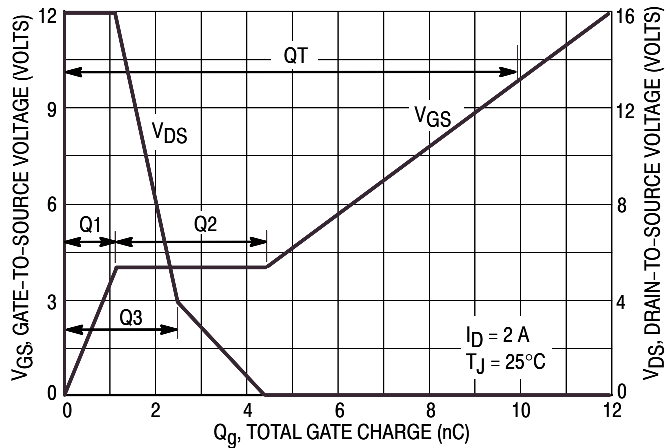



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

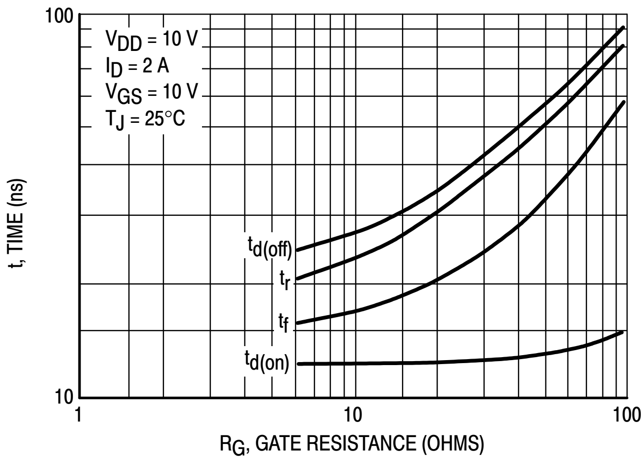



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

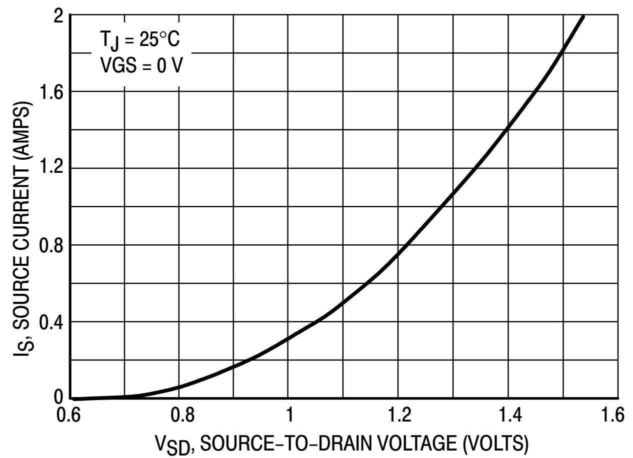



**Figure 10. Diode Forward Voltage versus Current**

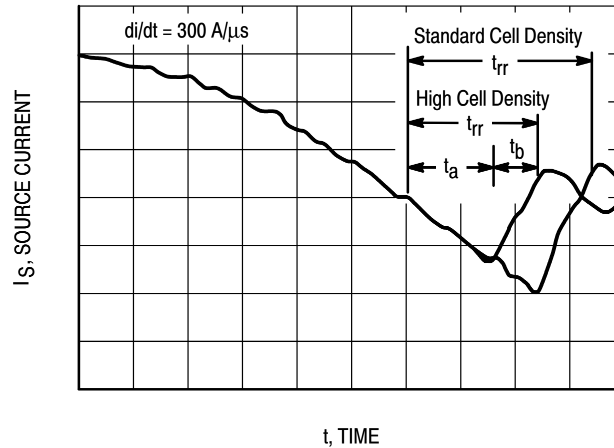



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

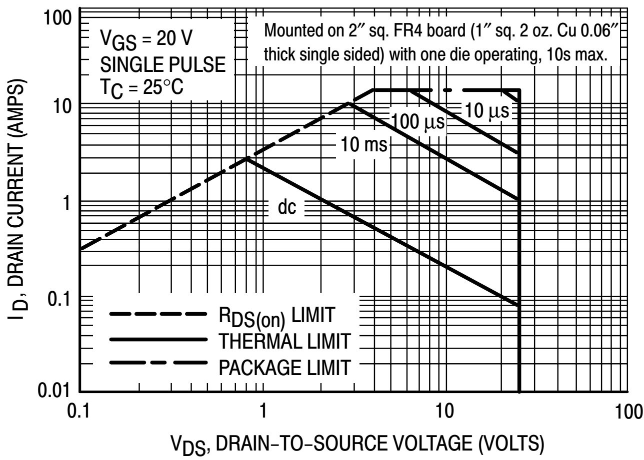



Figure 12. Maximum Rated Forward Biased Safe Operating Area

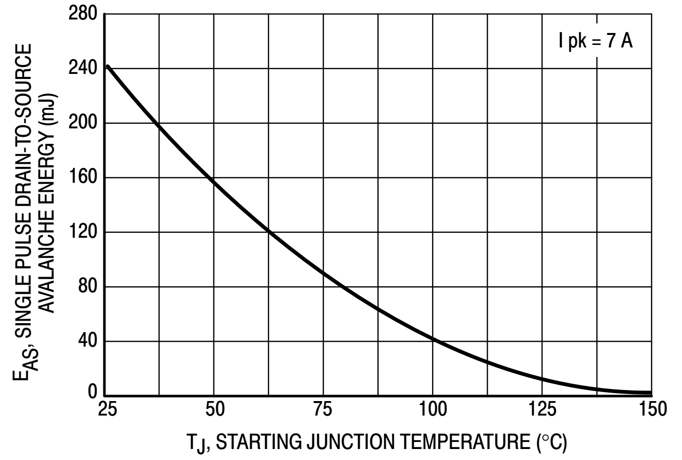



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

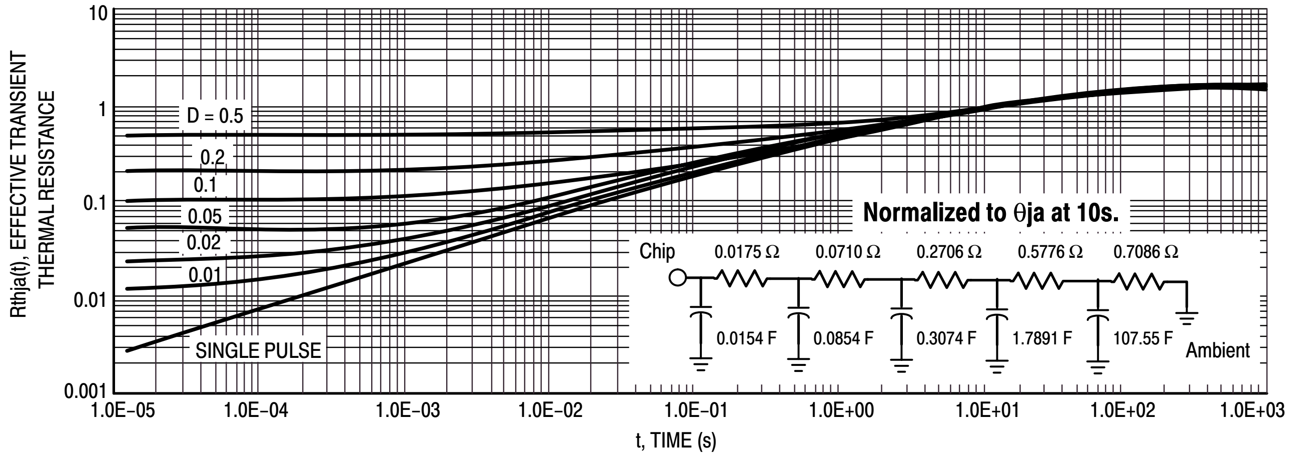



Figure 14. Thermal Response

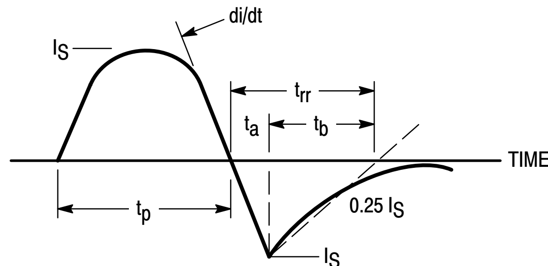
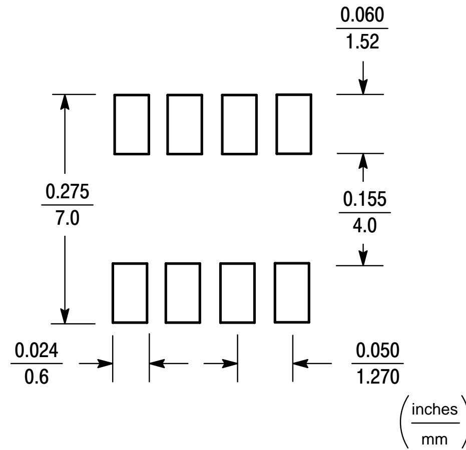



Figure 15. Diode Reverse Recovery Waveform

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. These can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

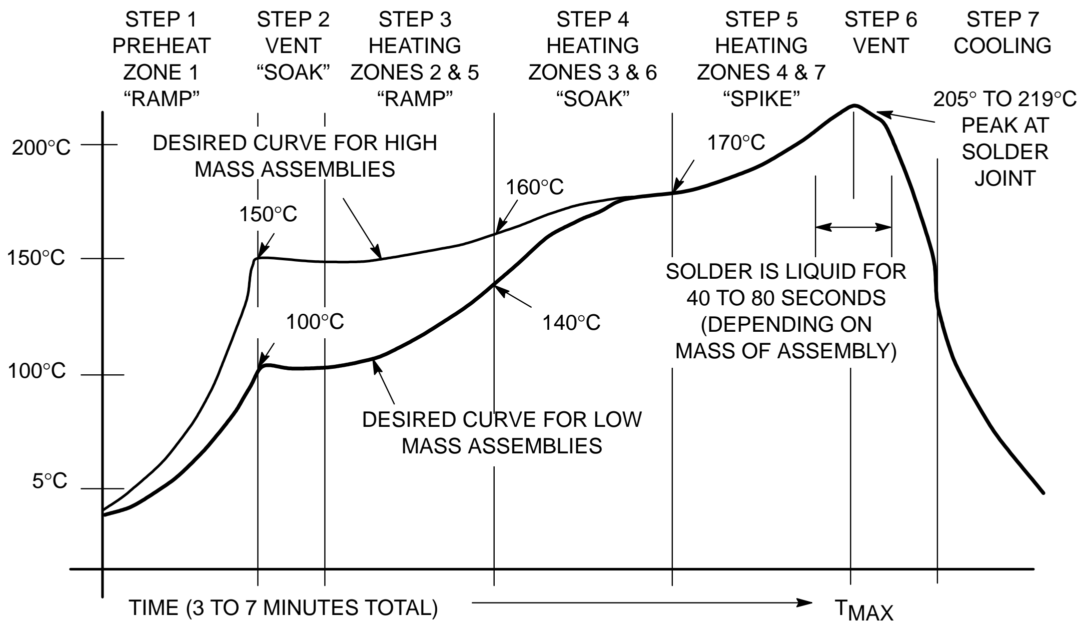



**Figure 16. Typical Solder Heating Profile**

# MMDF2P02HD

**Preferred Device**

# Power MOSFET 2 Amps, 20 Volts

## P–Channel SO–8, Dual

**ON Semiconductor™**

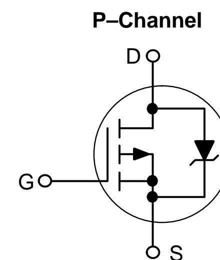
**http://onsemi.com**

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 160 mΩ**

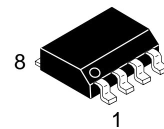
These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

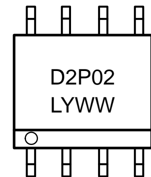
**P–Channel**




**MARKING DIAGRAM**

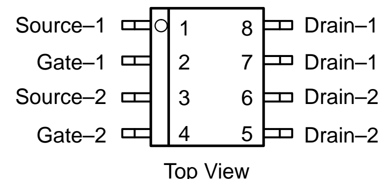



**SO–8, Dual**
**CASE 751**
**STYLE 11**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.3<br>2.1<br>20 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 6.0 Apk, L = 18 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 324 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2P02HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 25 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | µAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | – | 0.118 | 0.160 | Ohm |
| (VGS = 4.5 Vdc, $I_D$ = 1.0 Adc) | | | – | 0.152 | 0.180 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 2.0 | 3.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 420 | 588 | pF |
| Output Capacitance | | $C_{oss}$ | – | 290 | 406 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 116 | 232 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 19 | 38 | ns |
| Rise Time | | $t_r$ | – | 66 | 132 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 25 | 50 | |
| Fall Time | | $t_f$ | – | 37 | 74 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 11 | 22 | |
| Rise Time | | $t_r$ | – | 21 | 42 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 90 | |
| Fall Time | | $t_f$ | – | 36 | 72 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 15 | 20 | nC |
| | | $Q_1$ | – | 1.2 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 4.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.5 | 2.1 | Vdc |
| | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 1.24 | – | |
| Reverse Recovery Time | ($V_{DD}$ = 15 V, $I_S$ = 2.0 A, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 17 | – | |
| | | $t_b$ | – | 21 | – | |
| | | $Q_{RR}$ | – | 0.034 | – | µC |

3. Negative sign for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.max.
5. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

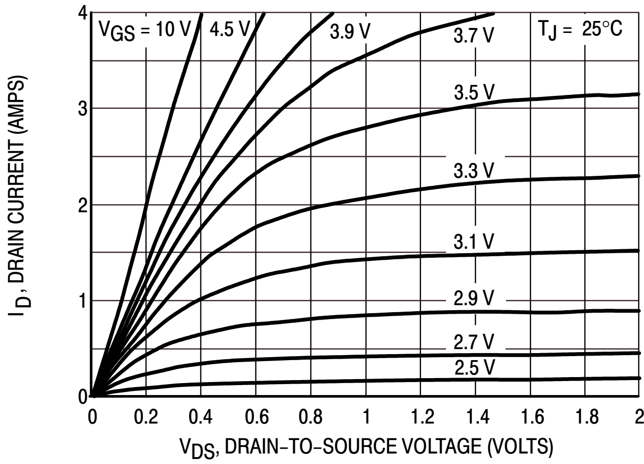



**Figure 1. On–Region Characteristics**

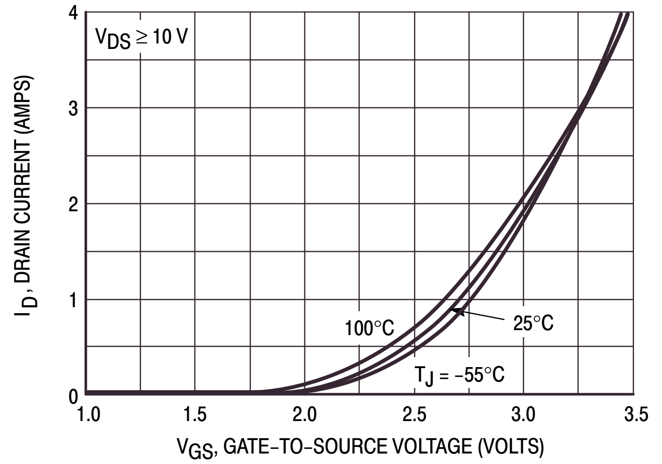



**Figure 2. Transfer Characteristics**

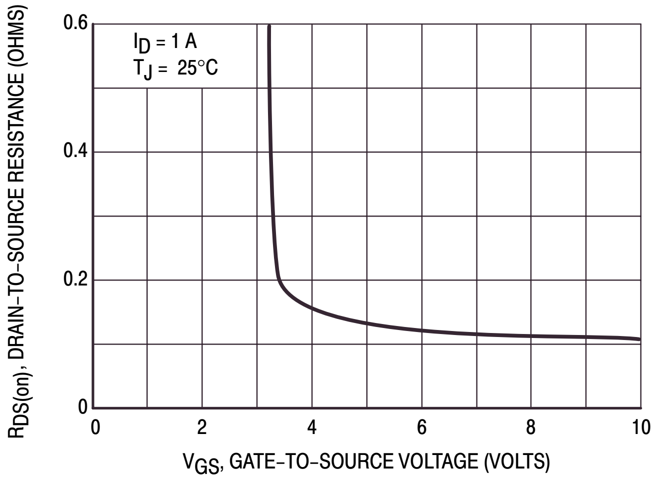



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

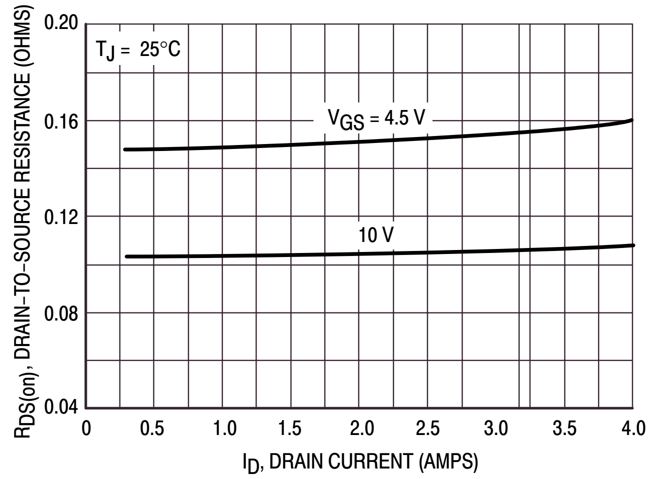



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

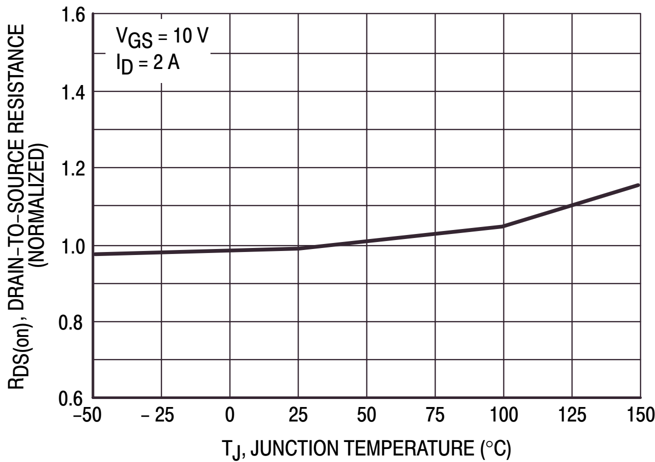



**Figure 5. On–Resistance Variation with Temperature**

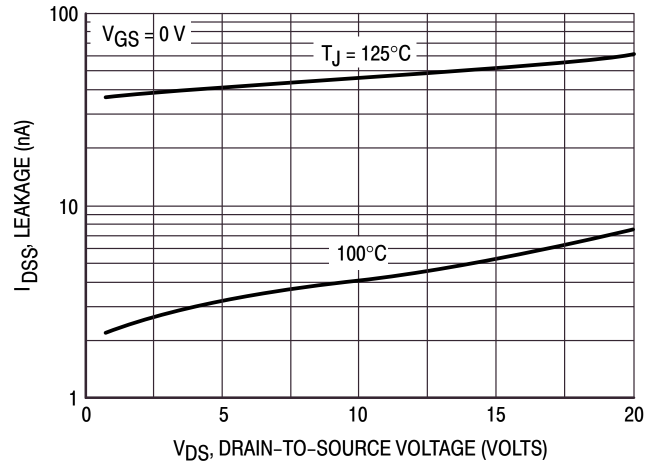



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \text{In} \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \text{In} \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

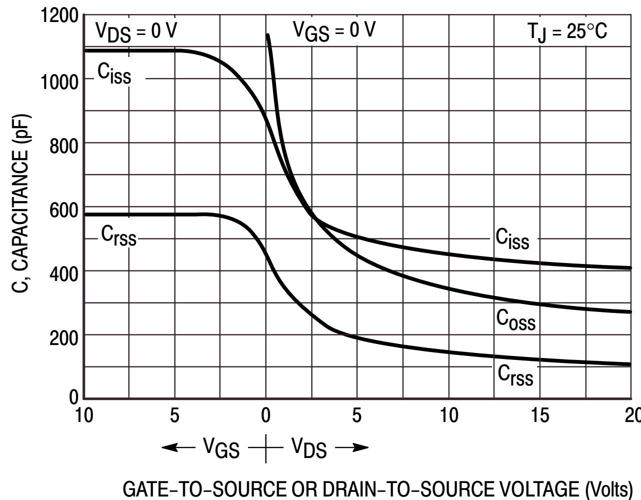



**Figure 7. Capacitance Variation**

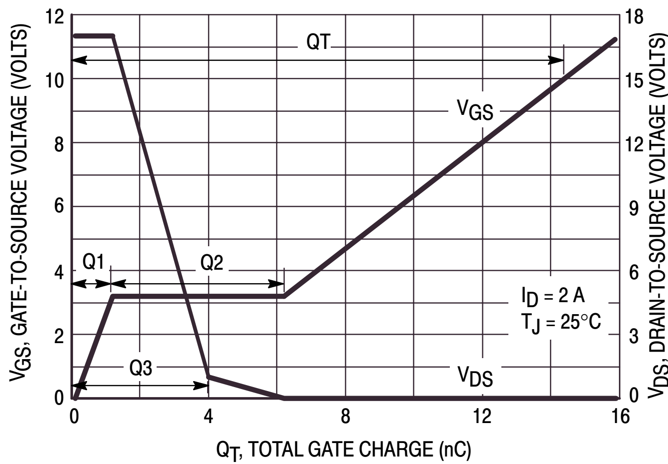



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

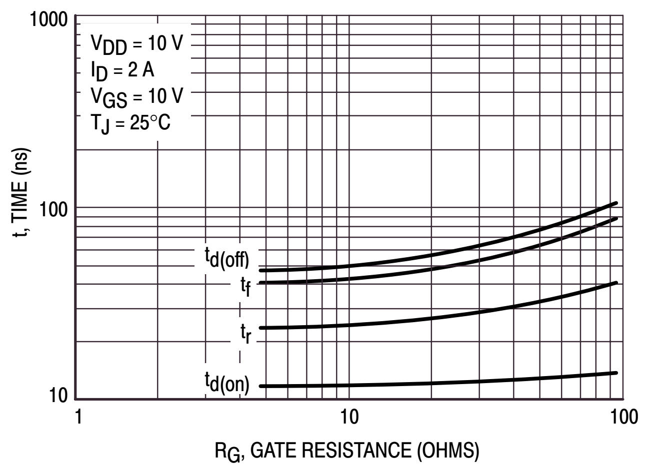



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

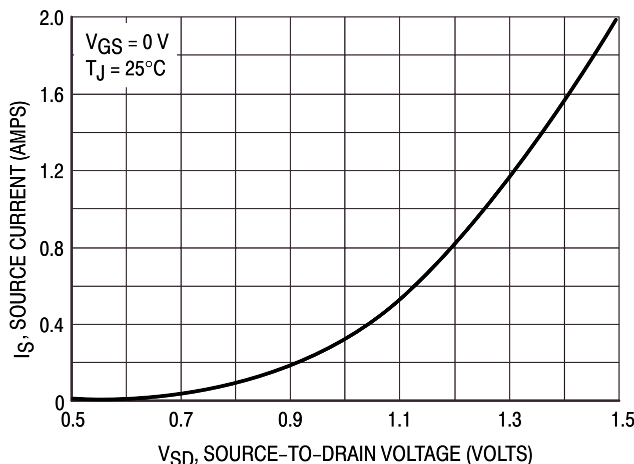



**Figure 10. Diode Forward Voltage versus Current**

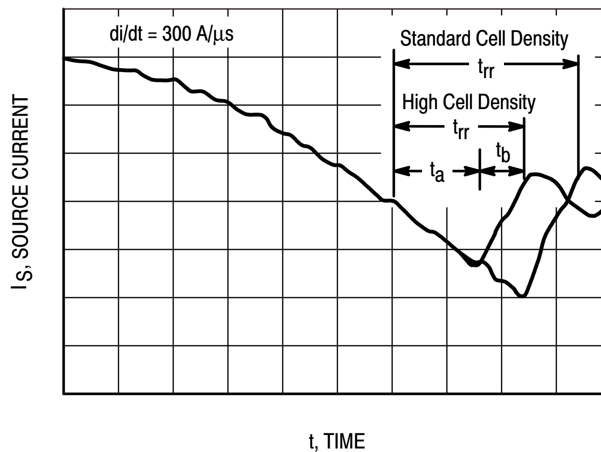



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

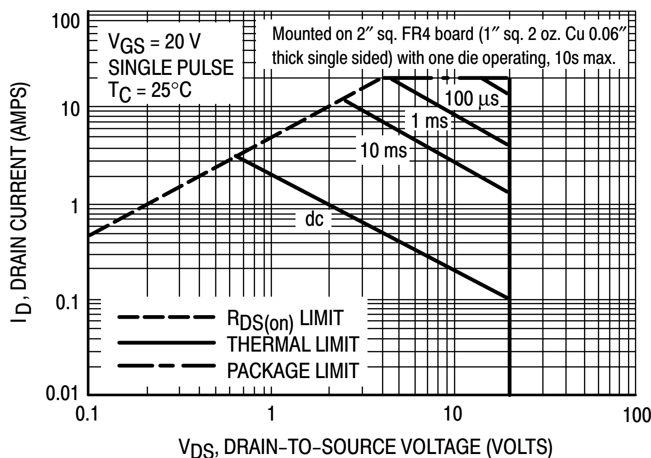



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

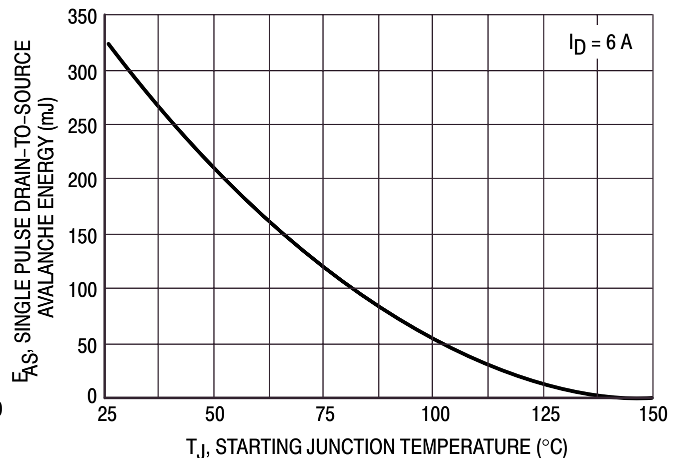



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

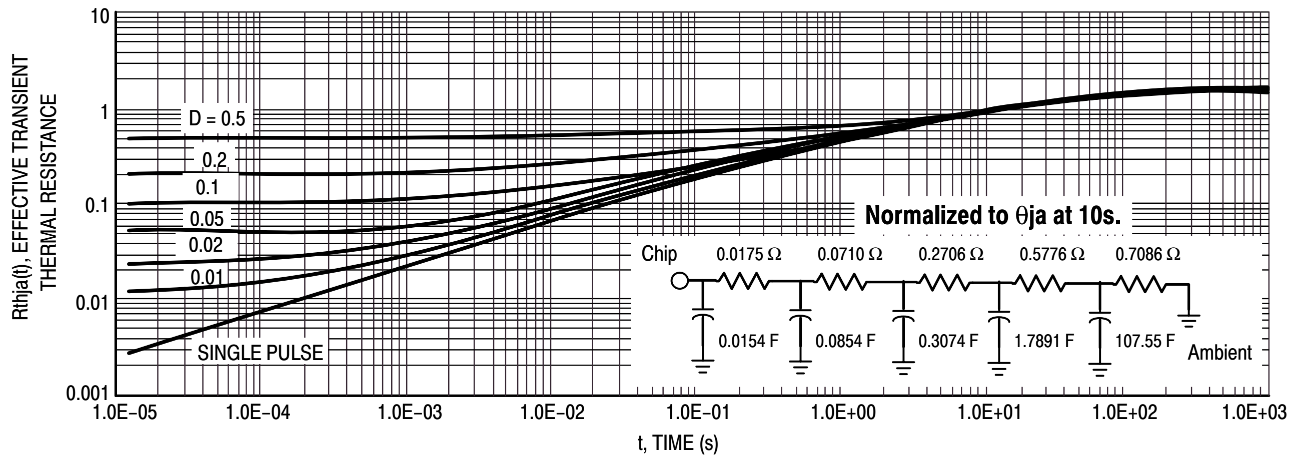



**Figure 14. Thermal Response**

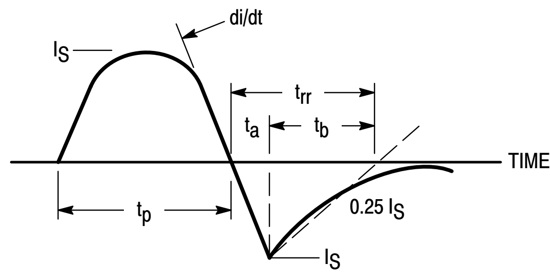
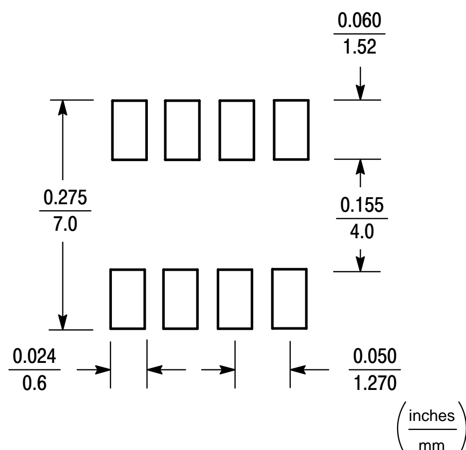



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

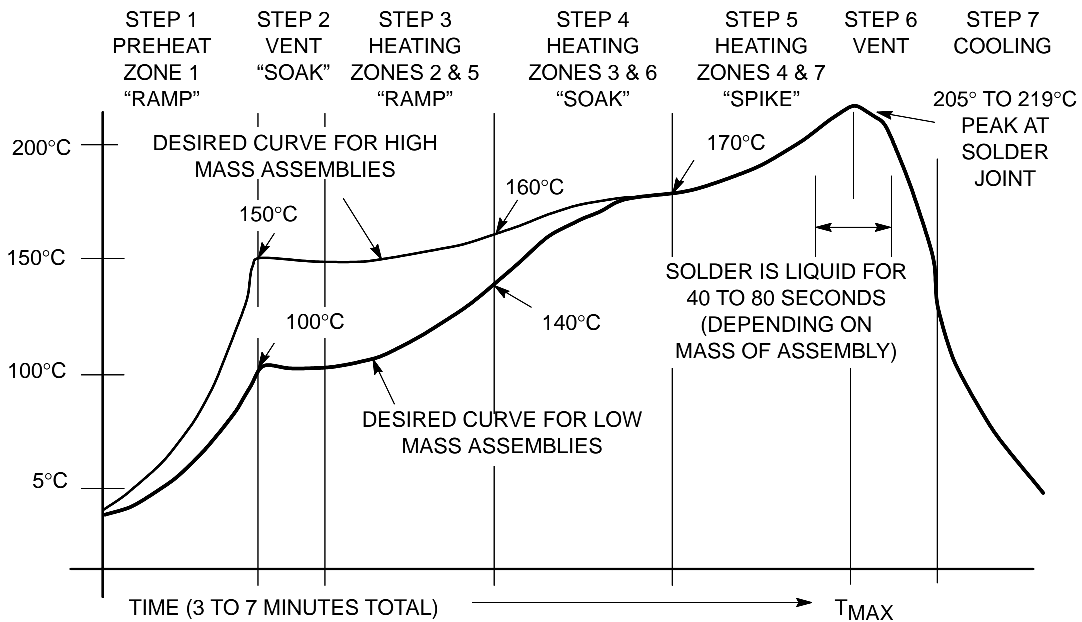



**Figure 16. Typical Solder Heating Profile**

# MMDF2P03HD

**Preferred Device**

# Power MOSFET 2 Amps, 30 Volts

## P–Channel SO–8, Dual

**ON Semiconductor™**

**http://onsemi.com**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

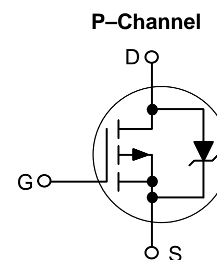
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.0<br>1.9<br>15 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 6.0 Apk, L = 18 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 324 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{θJA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

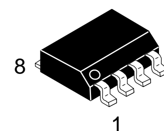
1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**2 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 200 mΩ**

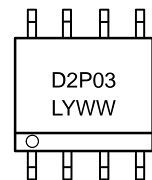
**P–Channel**




**MARKING DIAGRAM**

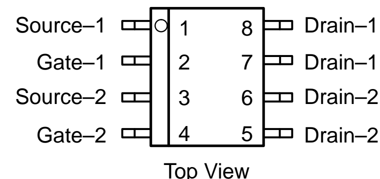



**SO–8, Dual**
**CASE 751**
**STYLE 11**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF2P03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 1.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>27 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>0.170<br>0.225 | <br>0.200<br>0.300 | Ohm |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 2.0 | 3.4 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 397 | 550 | pF |
| Output Capacitance | | $C_{oss}$ | – | 189 | 250 | |
| Transfer Capacitance | | $C_{rss}$ | – | 64 | 126 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16.25 | 33 | ns |
| Rise Time | | $t_r$ | – | 17.5 | 35 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 62.5 | 125 | |
| Fall Time | | $t_f$ | – | 194 | 390 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 9.0 | 18 | |
| Rise Time | | $t_r$ | – | 10 | 20 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 81 | 162 | |
| Fall Time | | $t_f$ | – | 192 | 384 | |
| Gate Charge<br>See Figure 8 | ($V_{DS}$ = 24 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 14.2 | 19 | nC |
| | | $Q_1$ | – | 1.1 | – | |
| | | $Q_2$ | – | 4.5 | – | |
| | | $Q_3$ | – | 3.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 3.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.82<br>1.36 | 2.0<br>– | Vdc |
| Reverse Recovery Time<br>See Figure 15 | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 42.3 | – | ns |
| | | $t_a$ | – | 15.6 | – | |
| | | $t_b$ | – | 26.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.044 | – | μC |

1. Negative sign for P–Channel device omitted for clarity.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

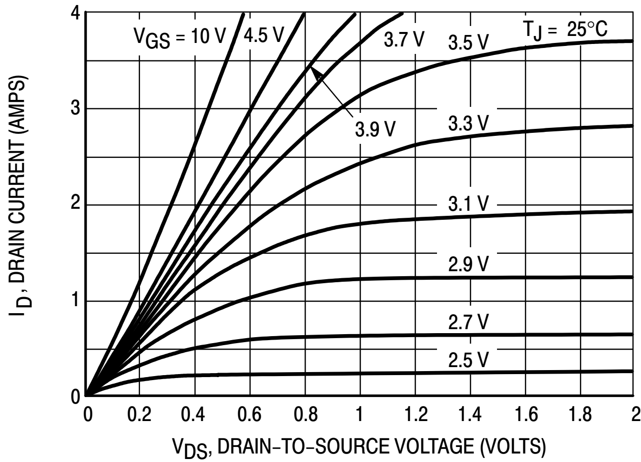



**Figure 1. On–Region Characteristics**

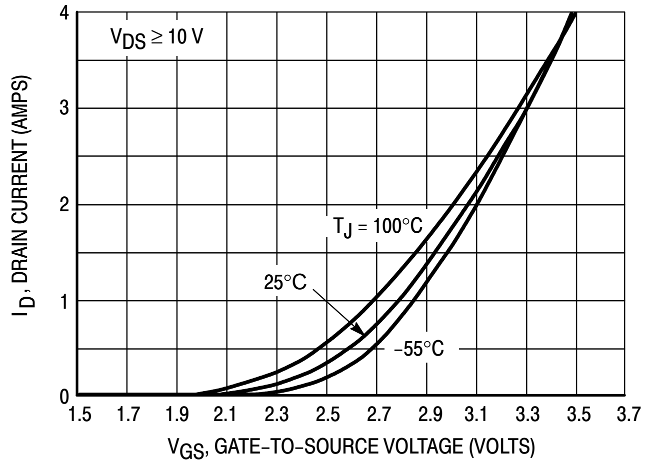



**Figure 2. Transfer Characteristics**

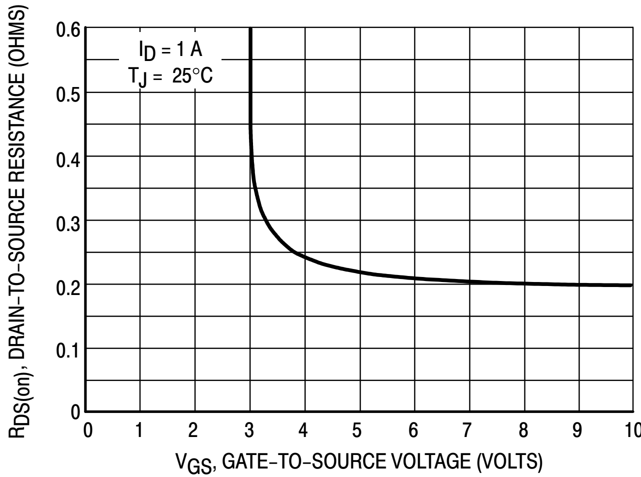



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

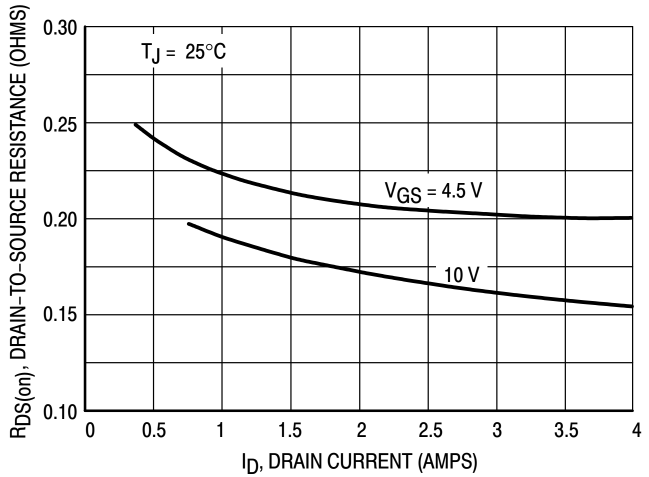



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

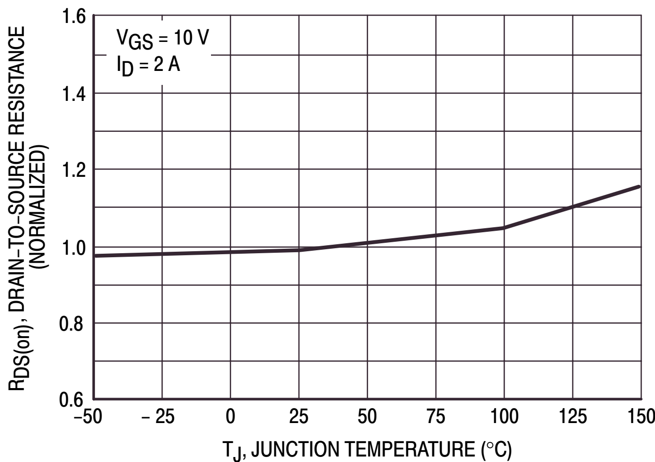



**Figure 5. On–Resistance Variation with Temperature**

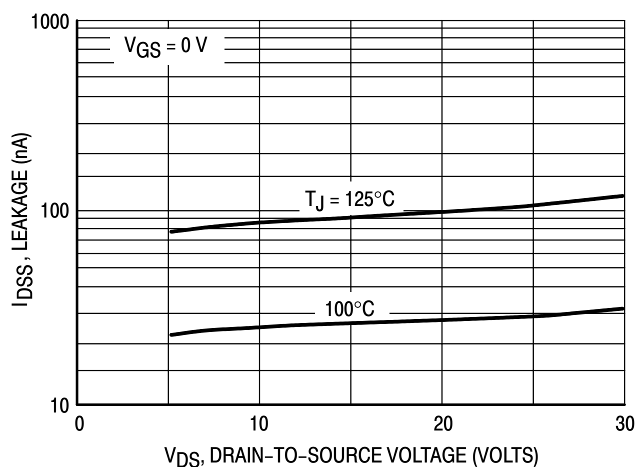



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

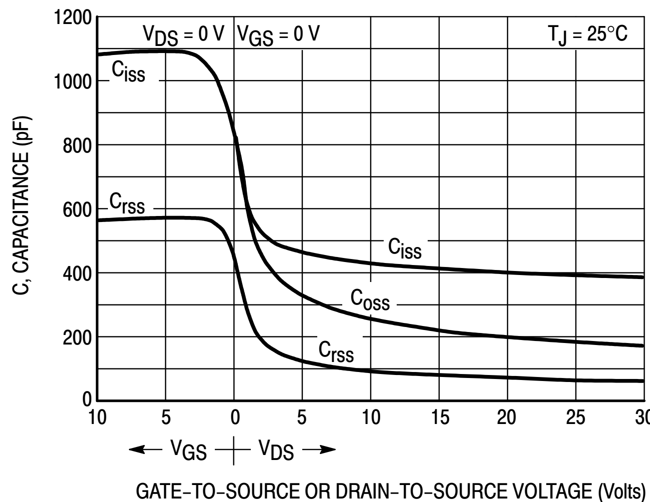



**Figure 7. Capacitance Variation**

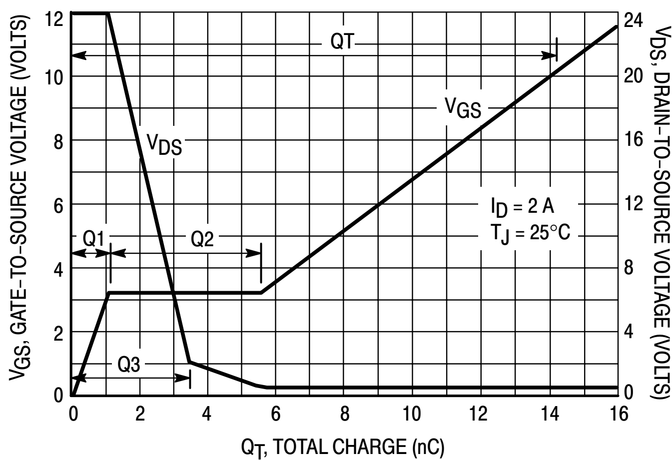



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

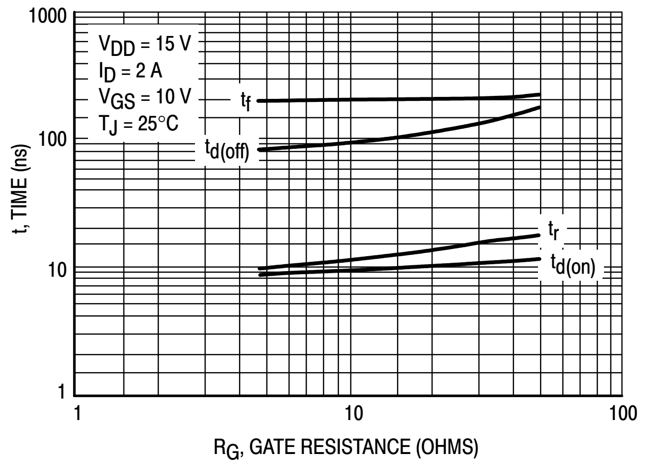



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

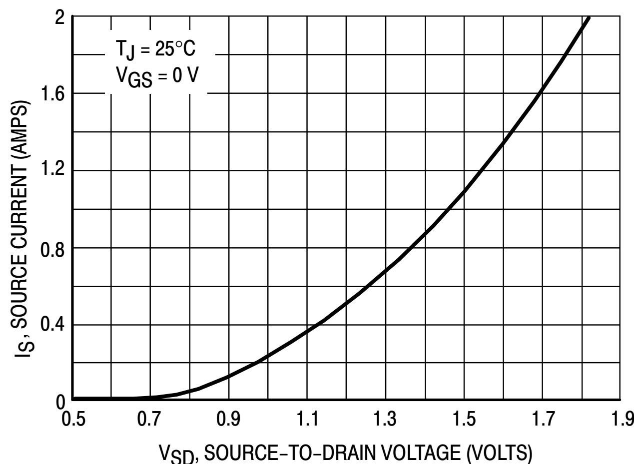



**Figure 10. Diode Forward Voltage versus Current**

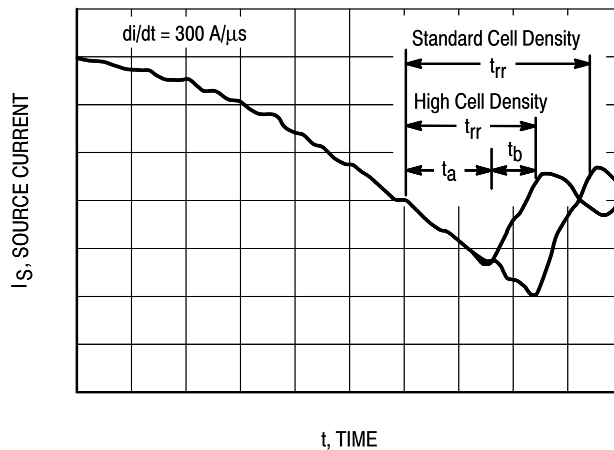



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

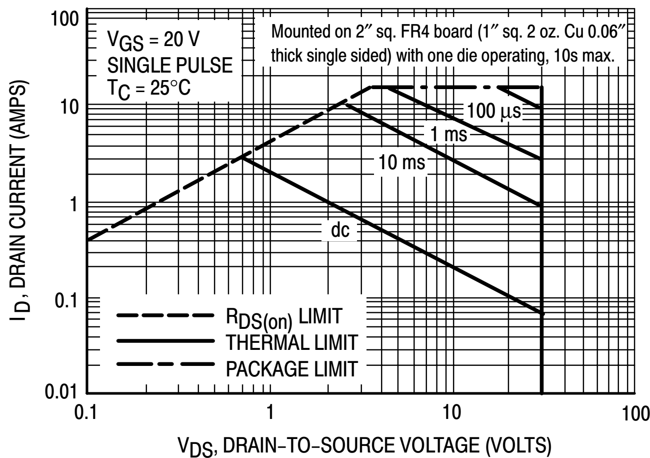



Figure 12. Maximum Rated Forward Biased Safe Operating Area

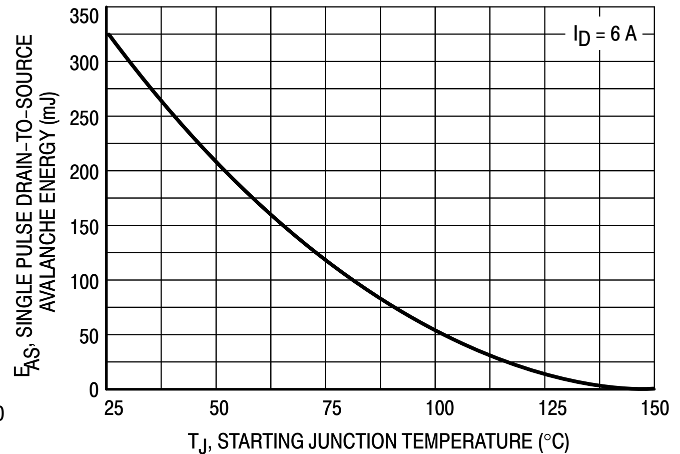



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

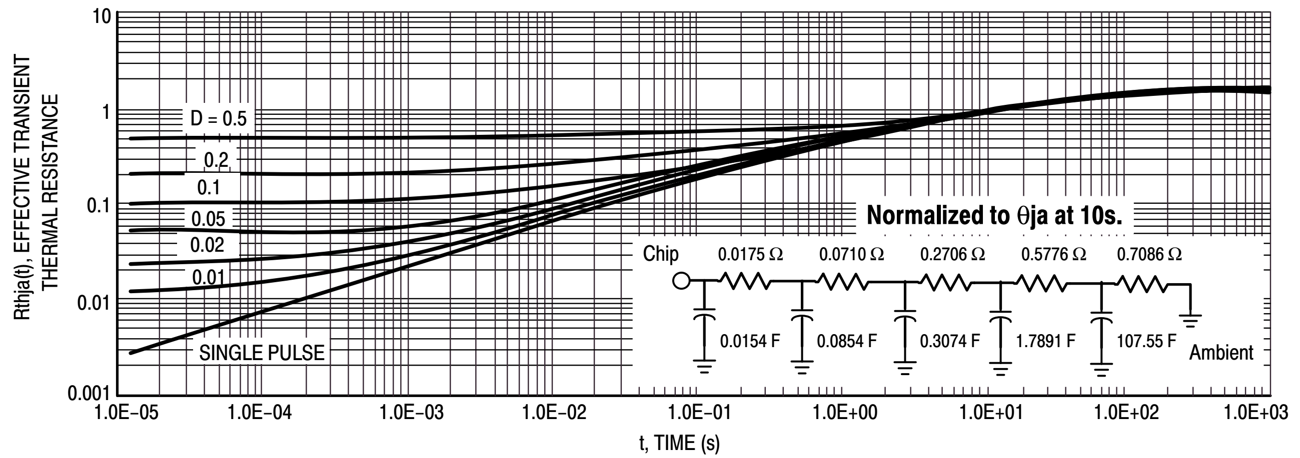



**Figure 14. Thermal Response**

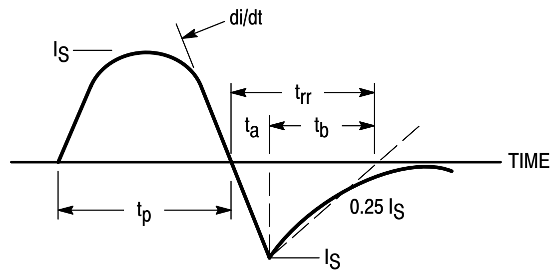
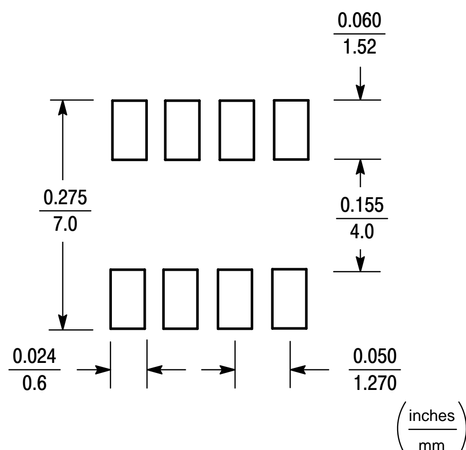



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

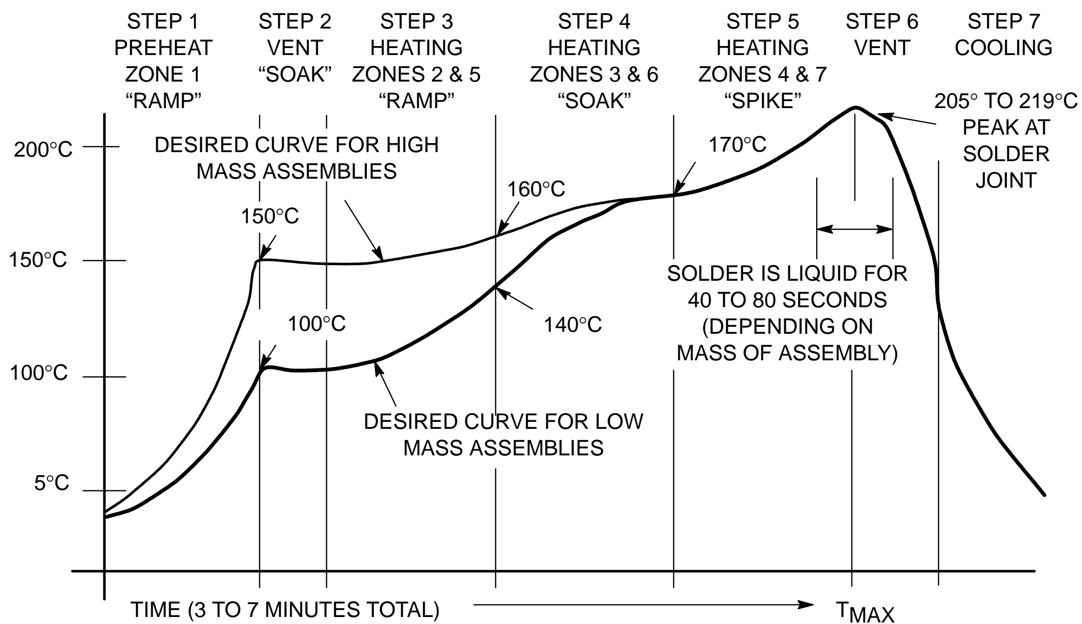



**Figure 16. Typical Solder Heating Profile**

# MMDF3N02HD

**Preferred Device**

# Power MOSFET 3 Amps, 20 Volts

## N–Channel SO–8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.8<br>2.6<br>19 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 9.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 405 | mJ |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

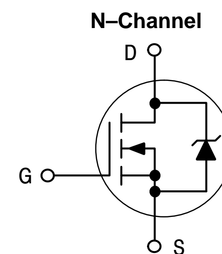
1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**ON Semiconductor™**

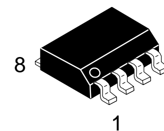
**http://onsemi.com**

**3 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 90 mΩ**

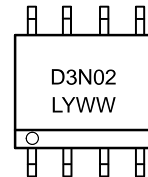
**N–Channel**




**MARKING DIAGRAM**

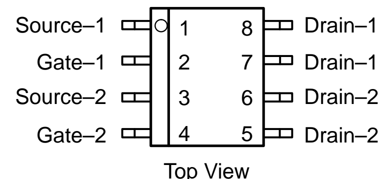



**SO–8, Dual**
**CASE 751**
**STYLE 11**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF3N02HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 29 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc) | | $R_{DS(on)}$ | – | 0.058 | 0.090 | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.5 Adc) | | | – | 0.074 | 0.100 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | 2.0 | 3.88 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 455 | 630 | pF |
| Output Capacitance | | $C_{oss}$ | – | 184 | 250 | |
| Transfer Capacitance | | $C_{rss}$ | – | 45 | 90 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 11 | 22 | ns |
| Rise Time | | $t_r$ | – | 58 | 116 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 35 | |
| Fall Time | | $t_f$ | – | 20 | 40 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 7.0 | 21 | |
| Rise Time | | $t_r$ | – | 32 | 64 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27 | 54 | |
| Fall Time | | $t_f$ | – | 21 | 42 | |
| Gate Charge See Figure 8 | ($V_{DS}$ = 16 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 12.5 | 18 | nC |
| | | $Q_1$ | – | 1.3 | – | |
| | | $Q_2$ | – | 2.8 | – | |
| | | $Q_3$ | – | 2.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.79 | 1.3 | Vdc |
| | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.72 | – | |
| Reverse Recovery Time See Figure 15 | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 23 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 5.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.025 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

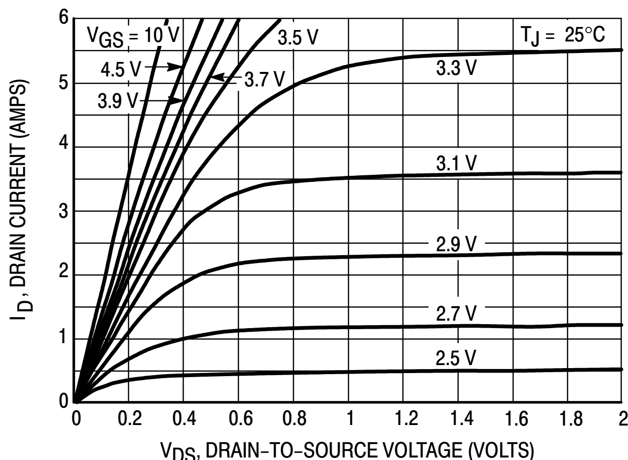



**Figure 1. On–Region Characteristics**

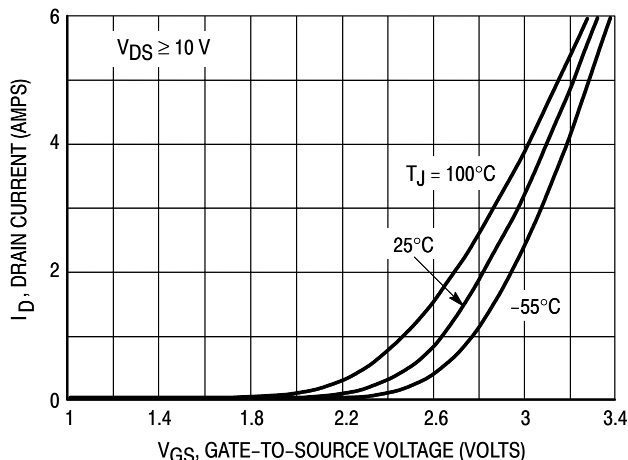



**Figure 2. Transfer Characteristics**

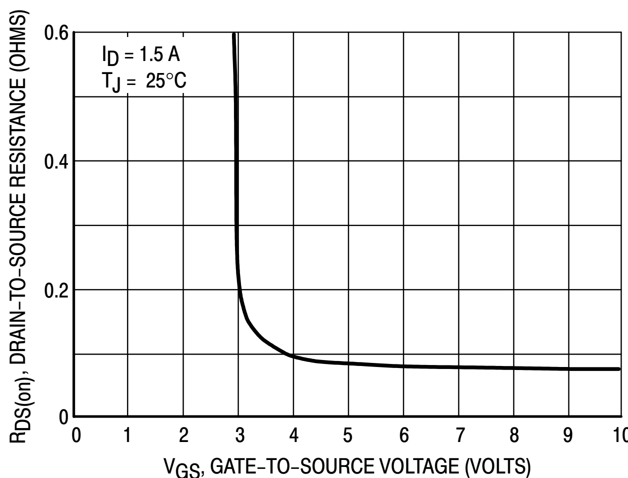



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

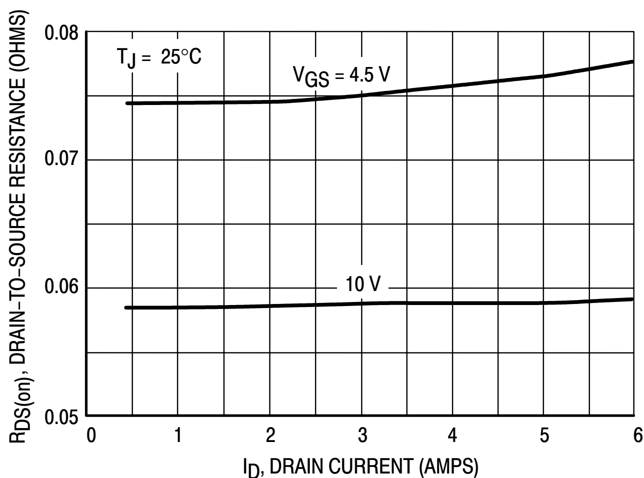



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

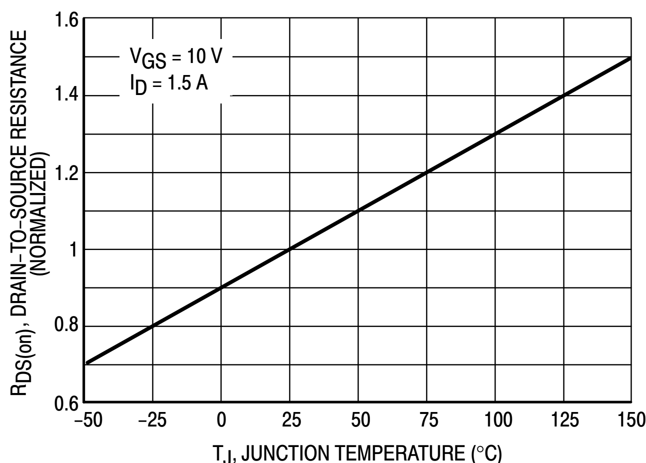



**Figure 5. On–Resistance Variation with Temperature**

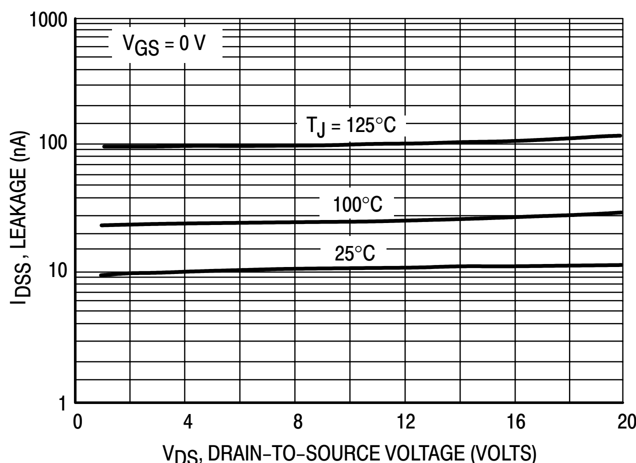



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \mathrm{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \mathrm{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

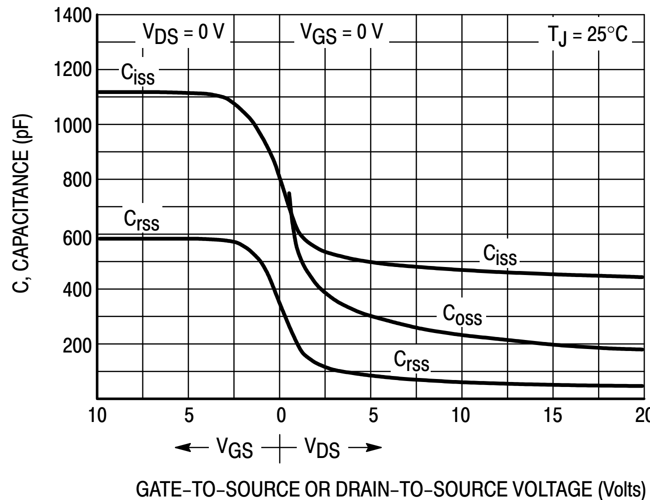



**Figure 7. Capacitance Variation**

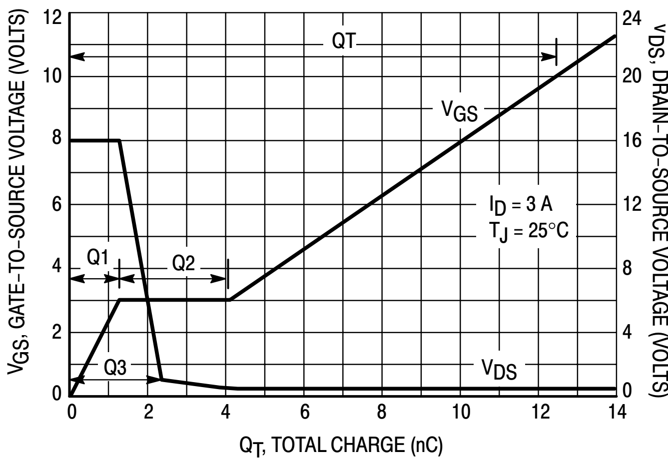



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

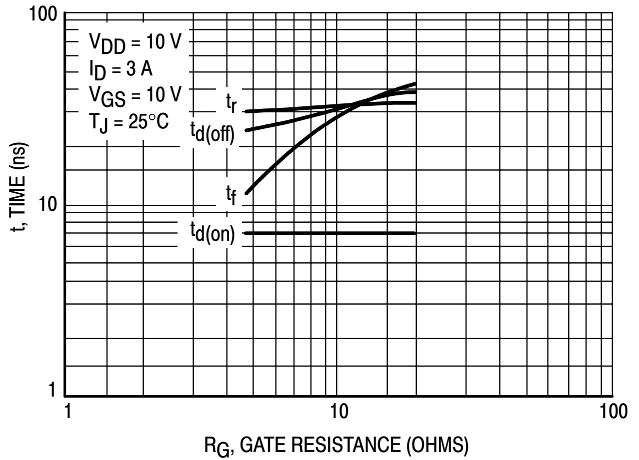



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

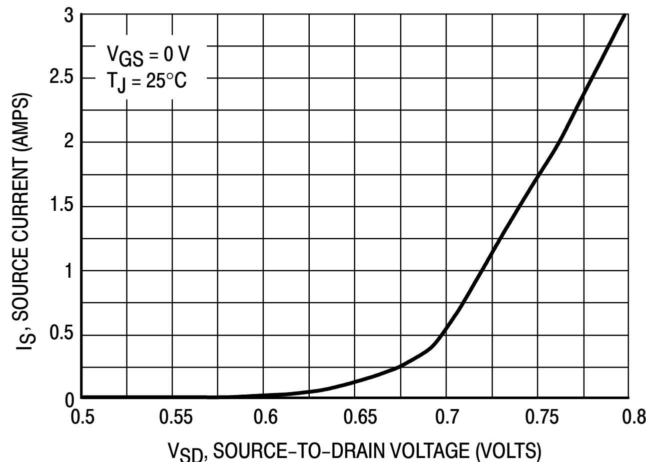



**Figure 10. Diode Forward Voltage versus Current**

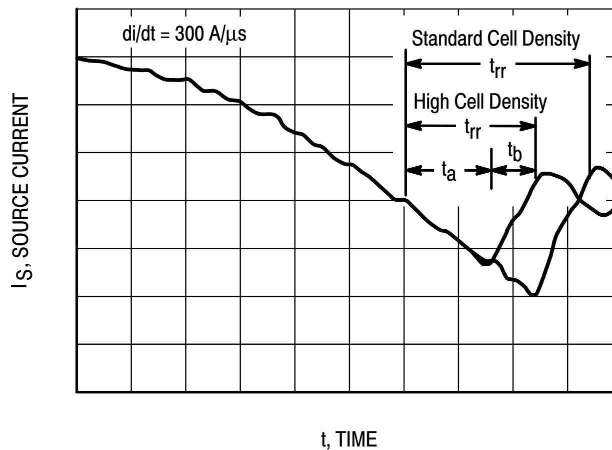



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

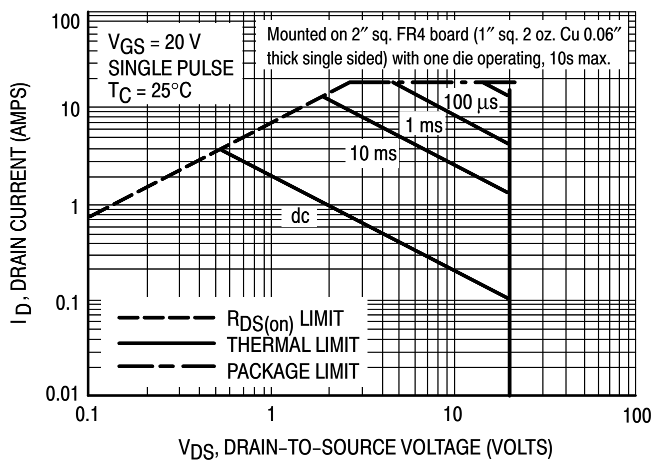



Figure 12. Maximum Rated Forward Biased Safe Operating Area

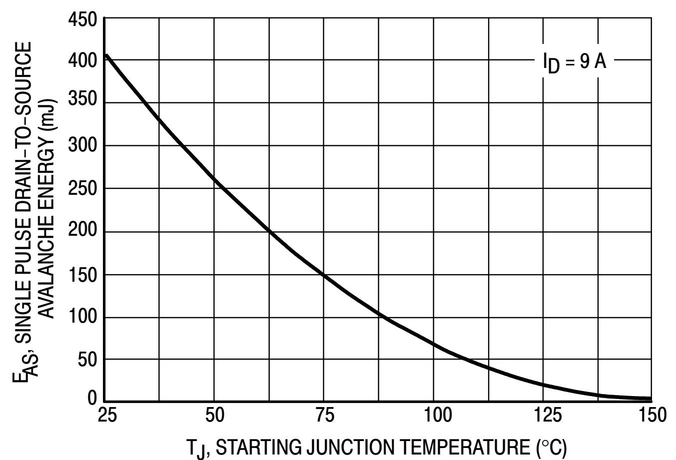



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

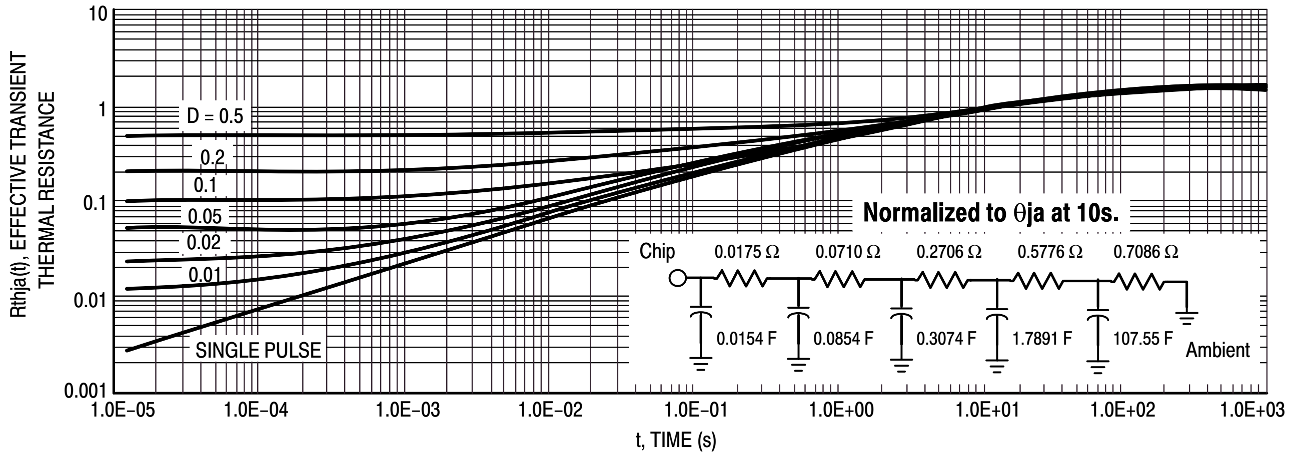



**Figure 14. Thermal Response**

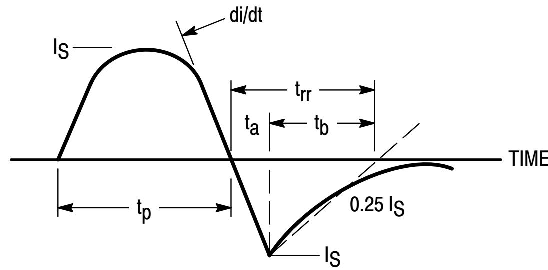
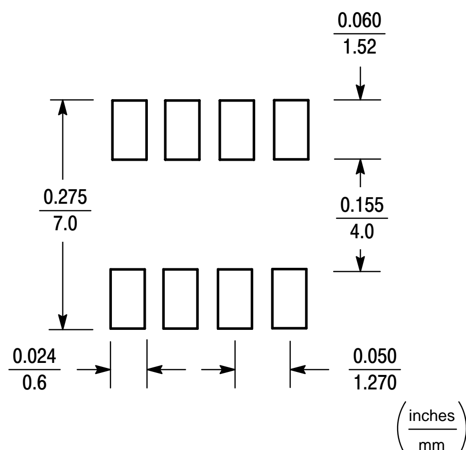



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

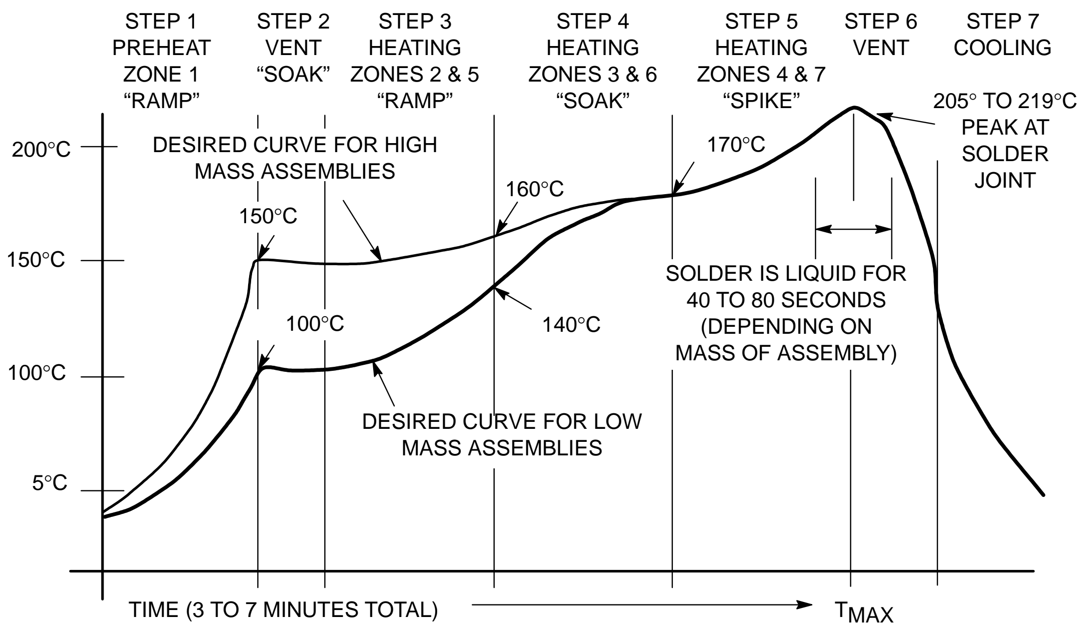



**Figure 16. Typical Solder Heating Profile**

# MMDF3N03HD

**Preferred Device**

# Power MOSFET 3 Amps, 30 Volts

## N–Channel SO–8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq 10\ \mu s$) | $I_D$<br>$I_D$<br>$I_{DM}$ | 4.1<br>3.0<br>40 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 9.0 Apk, L = 8.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 324 | mJ |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

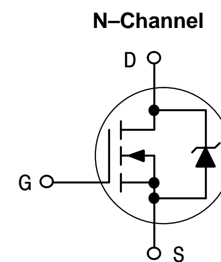
1. When mounted on 2″ square FR–4 board (1″ square 2 oz. Cu 0.06″ thick single sided) with one die operating, 10s max.

**ON Semiconductor™**

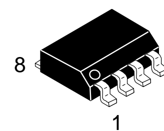
**http://onsemi.com**

**3 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 70 mΩ**

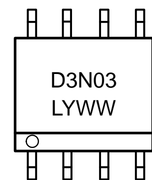
**N–Channel**




**MARKING DIAGRAM**

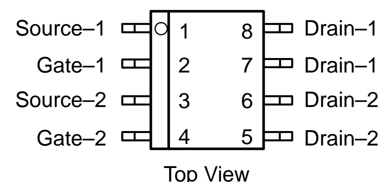



**SO–8, Dual**
**CASE 751**
**STYLE 11**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF3N03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 34.5 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 3.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | | | | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc) | | $R_{DS(on)}$ | – | 0.06 | 0.07 | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.5 Adc) | | | – | 0.065 | 0.075 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | 2.0 | 3.6 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 450 | 630 | pF |
| Output Capacitance | | $C_{oss}$ | – | 160 | 225 | |
| Transfer Capacitance | | $C_{rss}$ | – | 35 | 70 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 24 | ns |
| Rise Time | | $t_r$ | – | 65 | 130 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | 32 | |
| Fall Time | | $t_f$ | – | 19 | 38 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 8 | 16 | ns |
| Rise Time | | $t_r$ | – | 15 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 60 | |
| Fall Time | | $t_f$ | – | 23 | 46 | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 11.5 | 16 | nC |
| | | $Q_1$ | – | 1.5 | – | |
| | | $Q_2$ | – | 3.5 | – | |
| | | $Q_3$ | – | 2.8 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.82 | 1.2 | Vdc |
| | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.7 | – | |
| Reverse Recovery Time See Figure 12 | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 24 | – | ns |
| | | $t_a$ | – | 17 | – | |
| | | $t_b$ | – | 7 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.025 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

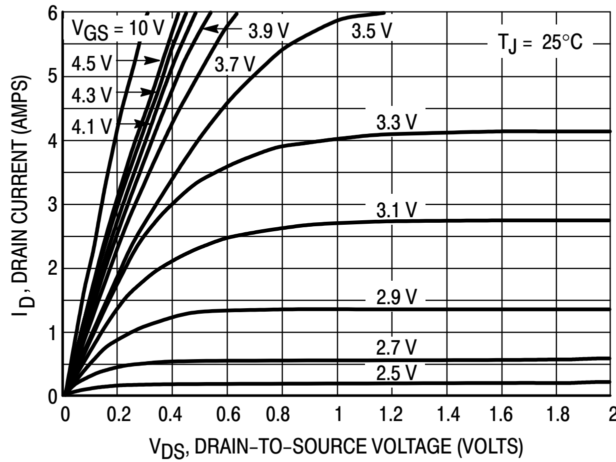



**Figure 1. On–Region Characteristics**

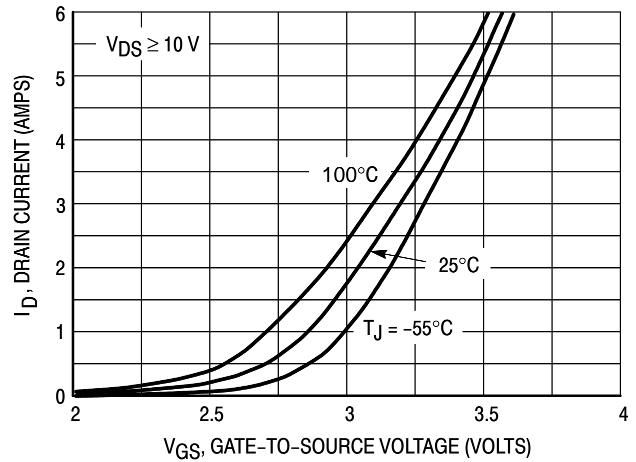



**Figure 2. Transfer Characteristics**

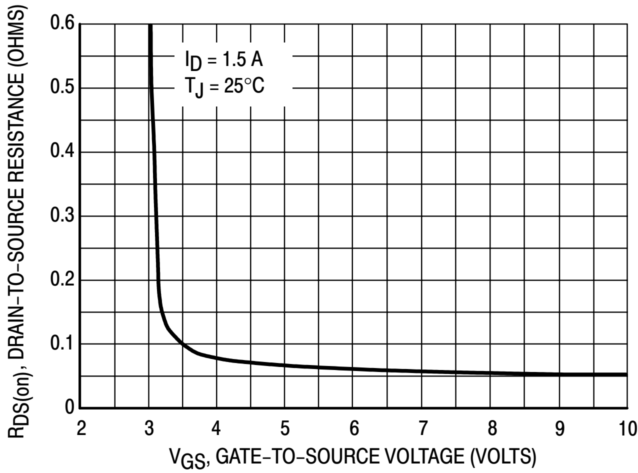



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

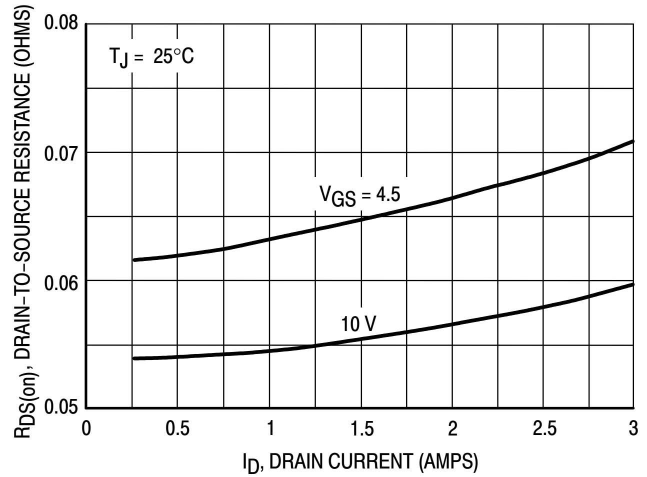



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

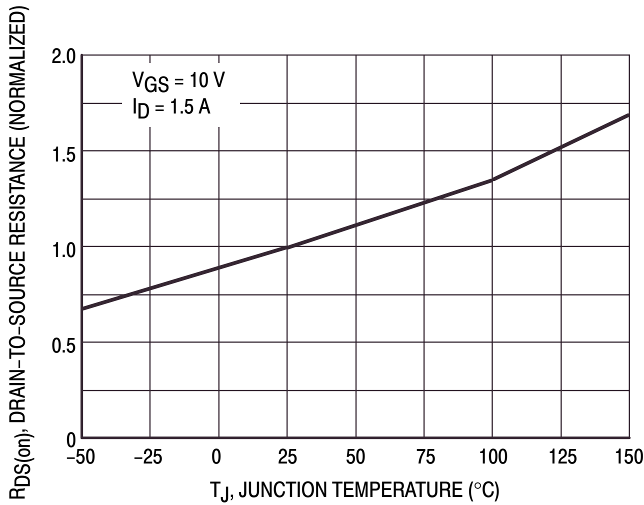



**Figure 5. On–Resistance Variation with Temperature**

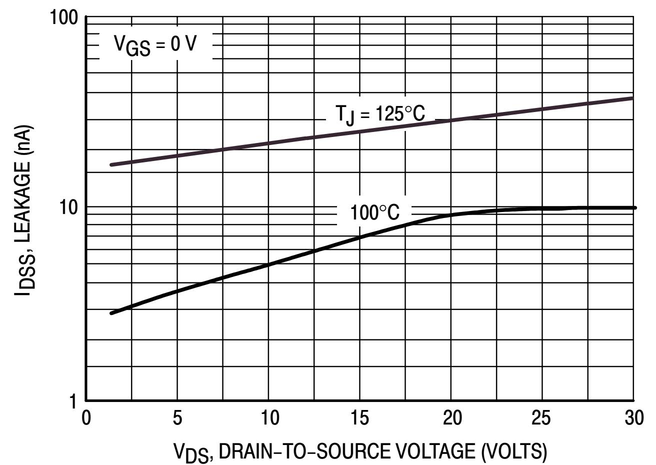



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

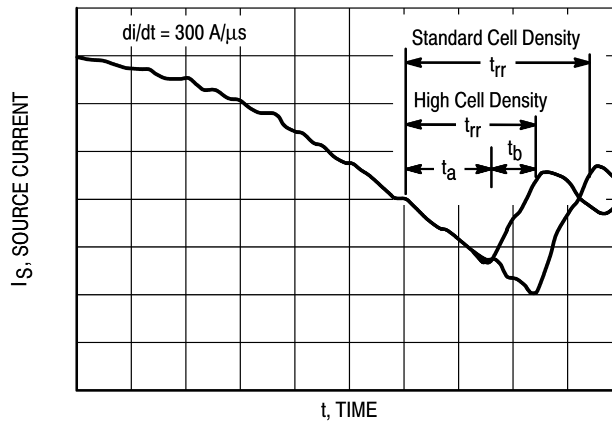



**Figure 7. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

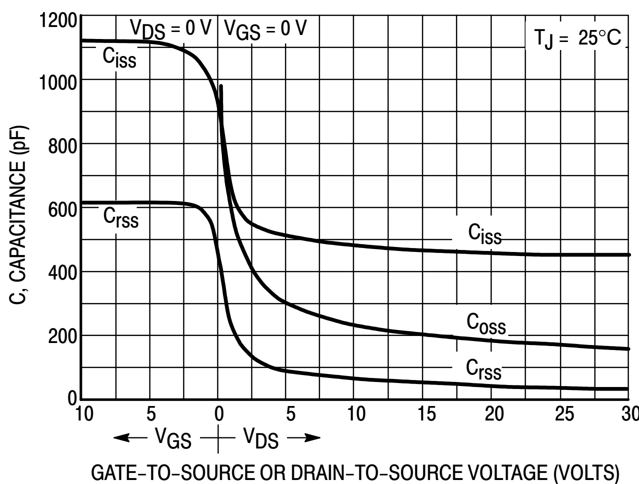



**Figure 8. Capacitance Variation**

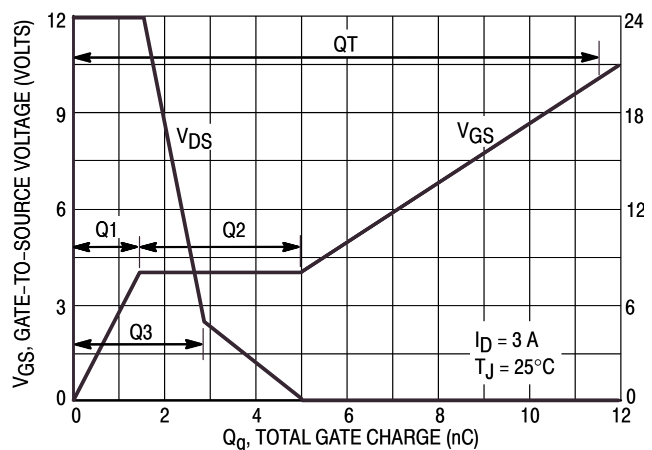



**Figure 9. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

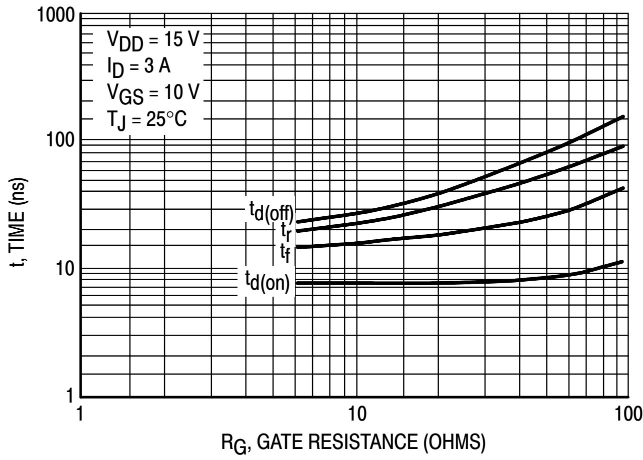



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

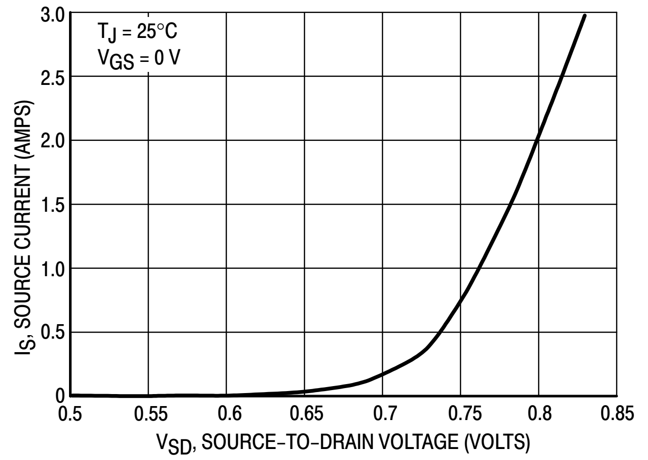



**Figure 11. Diode Forward Voltage versus Current**

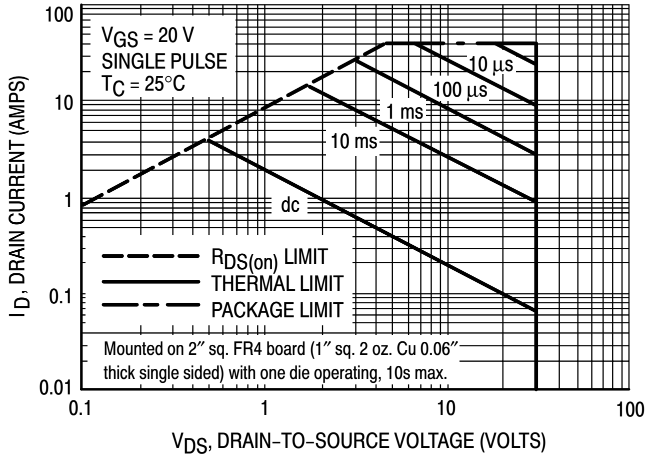



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

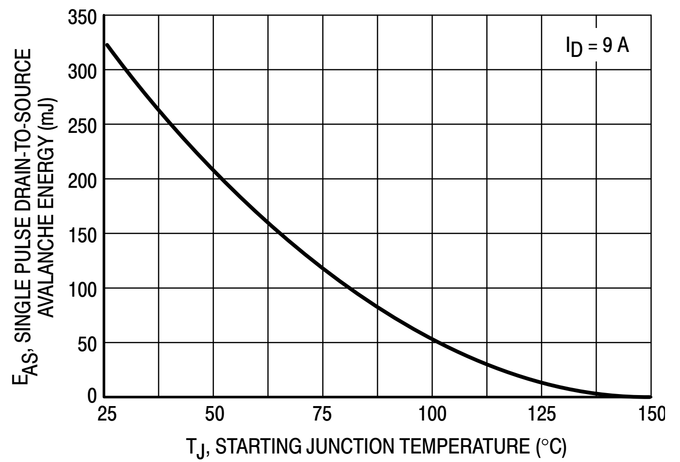



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

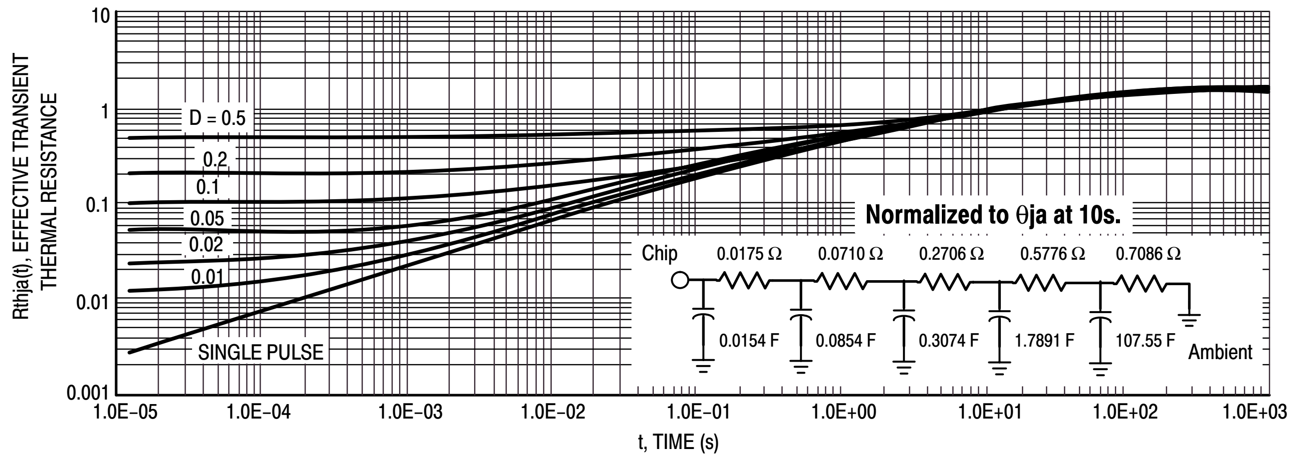



**Figure 14. Thermal Response**

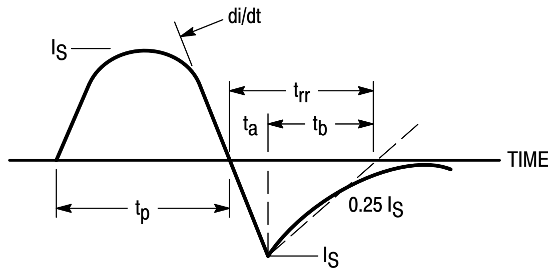
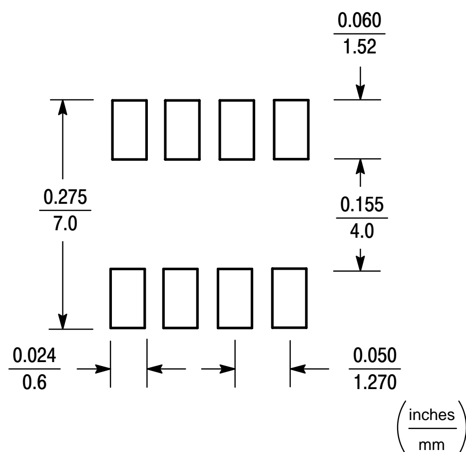



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

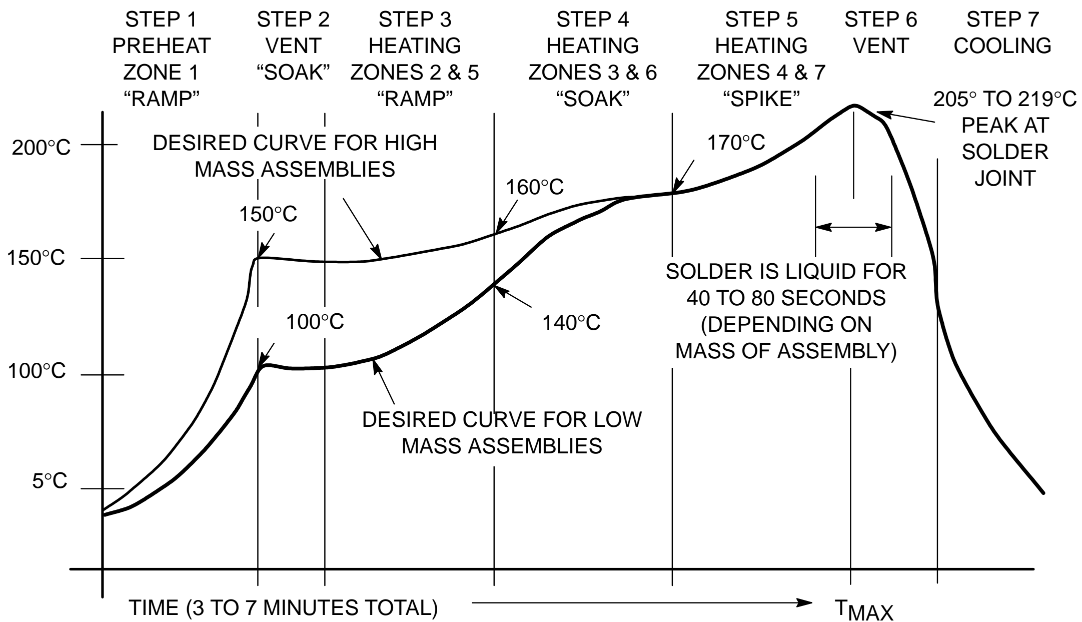



**Figure 16. Typical Solder Heating Profile**

# MMDF3N04HD

**Preferred Device**

# Power MOSFET 3 Amps, 40 Volts

## N–Channel SO–8, Dual

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

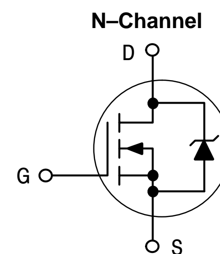
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided
- Avalanche Energy Specified

**ON Semiconductor™**

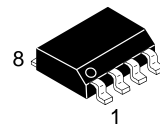
**http://onsemi.com**

**3 AMPERES**
**40 VOLTS**
**$R_{DS(on)}$ = 80 mΩ**

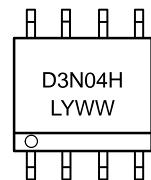
**N–Channel**




**MARKING DIAGRAM**

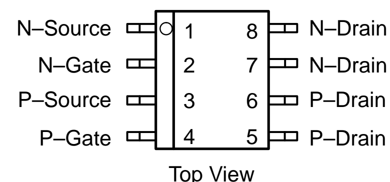



**SO–8, Dual**
**CASE 751**
**STYLE 14**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF3N04HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 40 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 40 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C (Note 1.)<br>– Continuous @ $T_A$ = 70°C (Note 1.)<br>– Pulsed Drain Current (Note 3.) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.4<br>3.0<br>40 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Linear Derating Factor (1) | $P_D$ | 2.0<br>16 | Watts<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Linear Derating Factor (2) | $P_D$ | 1.39<br>11.11 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 9.0 Apk, L = 4.0 mH, $V_{DS}$ = 40 Vdc) | $E_{AS}$ | 162 | mJ |

**THERMAL RESISTANCE**

| Rating | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Thermal Resistance – Junction to Ambient, PCB Mount (Note 1.)<br>– Junction to Ambient, PCB Mount (Note 2.) | $R_{\theta JA}$<br>$R_{\theta JA}$ | –<br>– | 62.5<br>90 | °C/W |

1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ 10 Seconds)
2. When mounted on minimum recommended FR–4 or G–10 board ($V_{GS}$ = 10 V, @ Steady State)
3. Repetitive rating; pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>40<br>– | <br>–<br>4.3 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 40 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 40 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>0.015<br>0.15 | <br>2.5<br>10 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | 0.013 | 500 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>2.0<br>4.9 | <br>3.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.4 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.7 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>55<br>79 | <br>80<br>100 | mΩ |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.7 Adc) (Note 4.) | | $g_{FS}$ | 2.0 | 4.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 32 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 450 | 900 | pF |
| Output Capacitance | | $C_{oss}$ | – | 130 | 230 | |
| Transfer Capacitance | | $C_{rss}$ | – | 32 | 96 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 20 Vdc, $I_D$ = 3.4 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6 Ω) (Note 4.) | $t_{d(on)}$ | – | 9.0 | 18 | ns |
| Rise Time | | $t_r$ | – | 15 | 30 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 28 | 56 | |
| Fall Time | | $t_f$ | – | 19 | 38 | |
| Turn–On Delay Time | ($V_{DD}$ = 20 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 4.) | $t_{d(on)}$ | – | 13 | 26 | ns |
| Rise Time | | $t_r$ | – | 77 | 144 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 34 | |
| Fall Time | | $t_f$ | – | 20 | 40 | |
| Gate Charge | ($V_{DS}$ = 40 Vdc, $I_D$ = 3.4 Adc, $V_{GS}$ = 10 Vdc) (Note 4.) | $Q_T$ | – | 13.9 | 28 | nC |
| | | $Q_1$ | – | 2.1 | – | |
| | | $Q_2$ | – | 3.7 | – | |
| | | $Q_3$ | – | 5.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 3.4 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 3.4 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.87<br>0.8 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 3.4 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) (Note 4.) | $t_{rr}$ | – | 27 | – | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 7.0 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.03 | – | µC |

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.
6. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

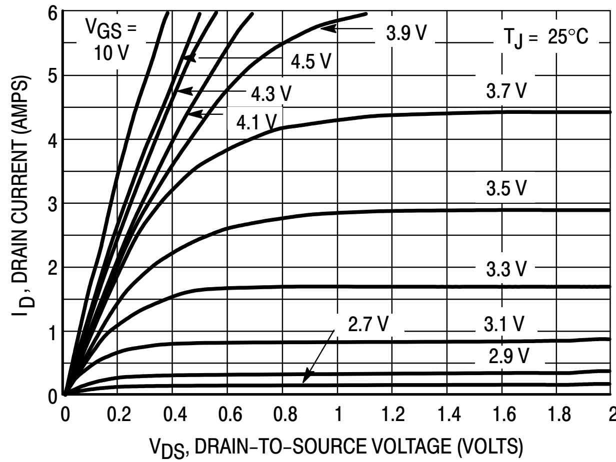



**Figure 1. On–Region Characteristics**

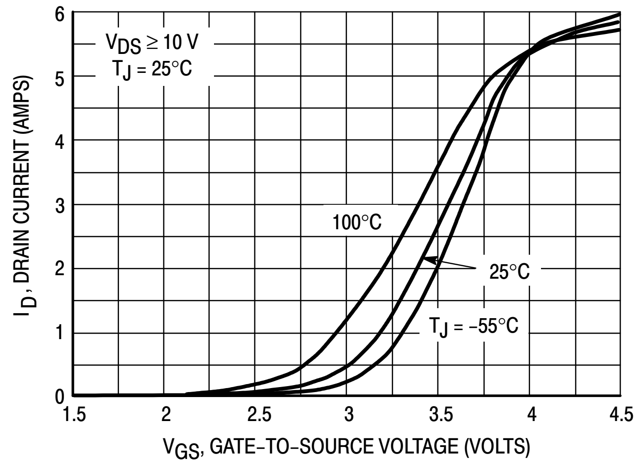



**Figure 2. Transfer Characteristics**

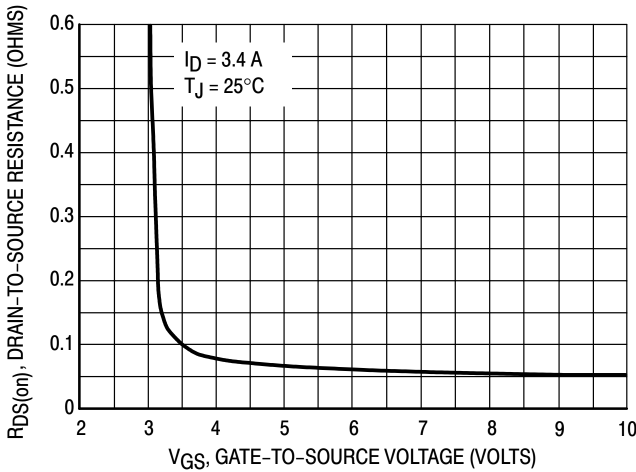



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

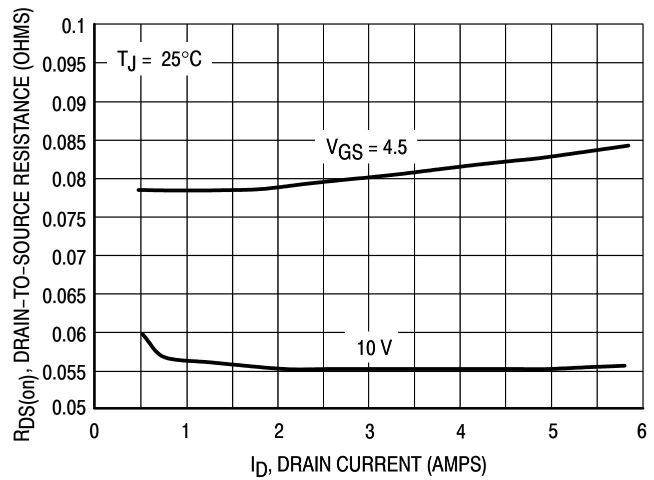



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

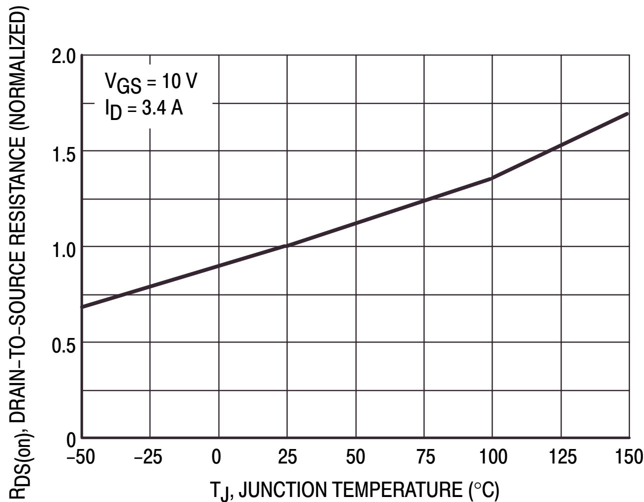



**Figure 5. On–Resistance Variation with Temperature**

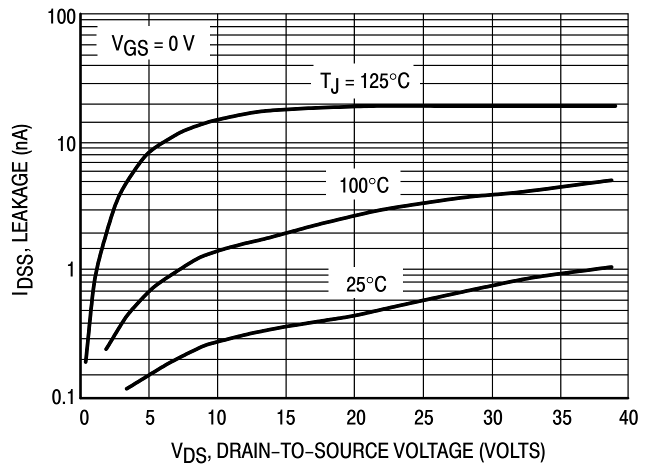



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{In} [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \text{In} (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

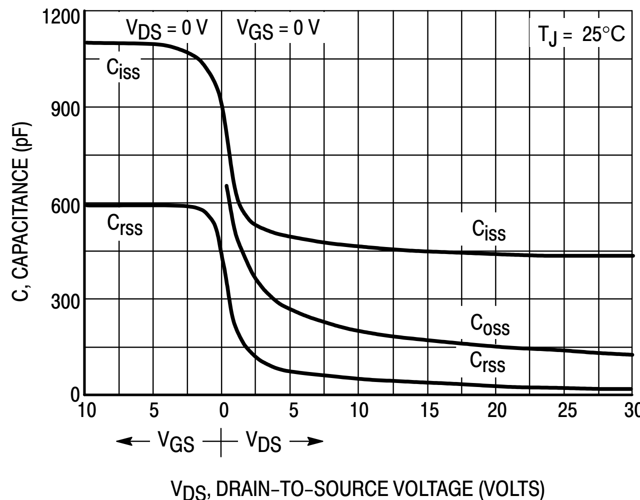



**Figure 7. Capacitance Variation**

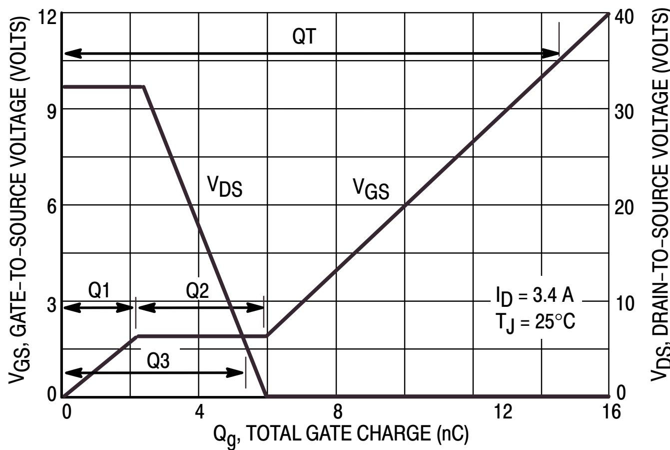



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

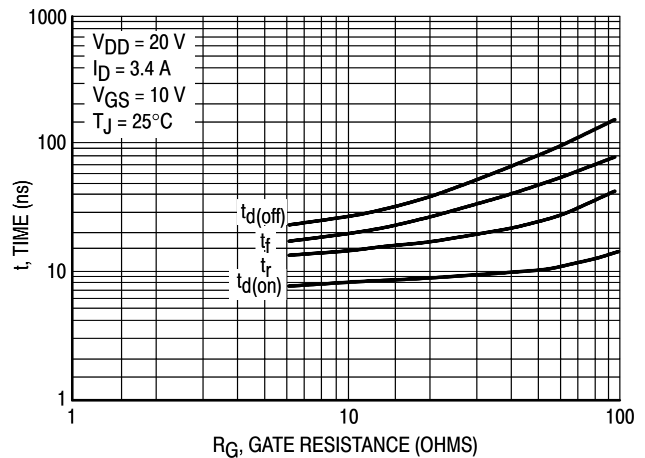



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

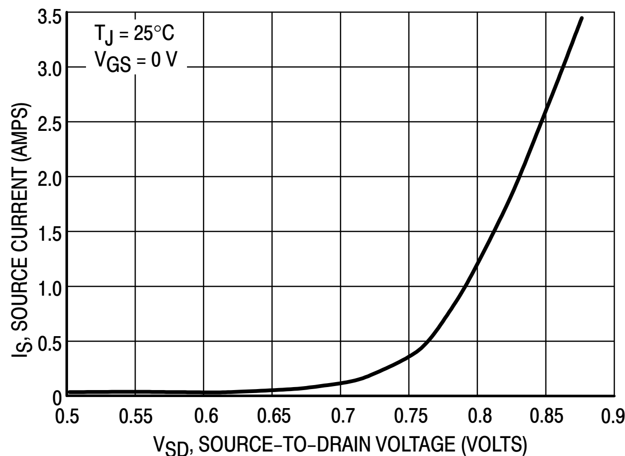



**Figure 10. Diode Forward Voltage versus Current**

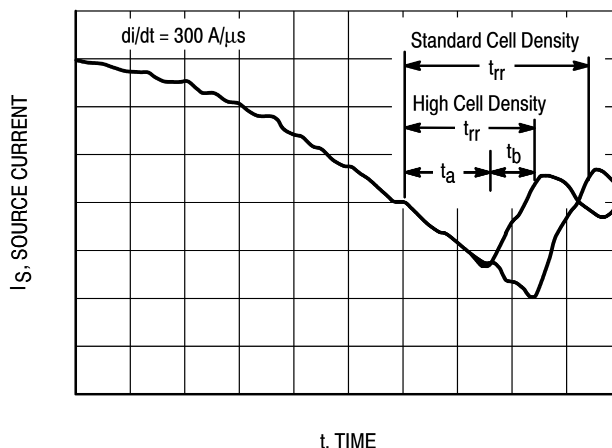



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

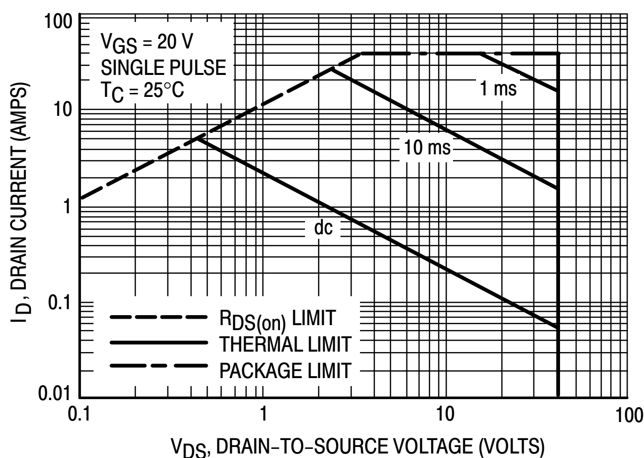



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

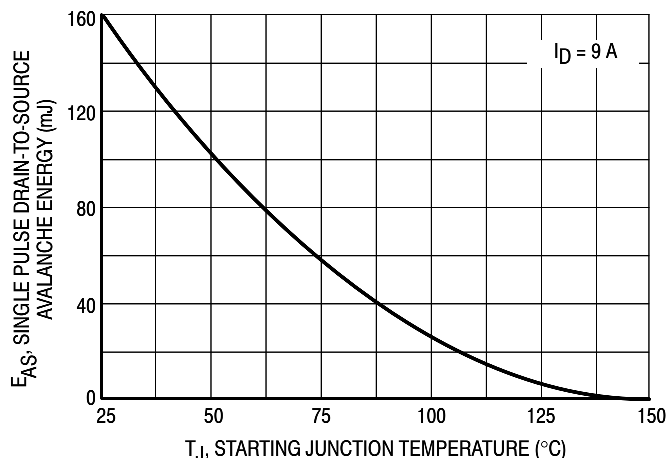



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

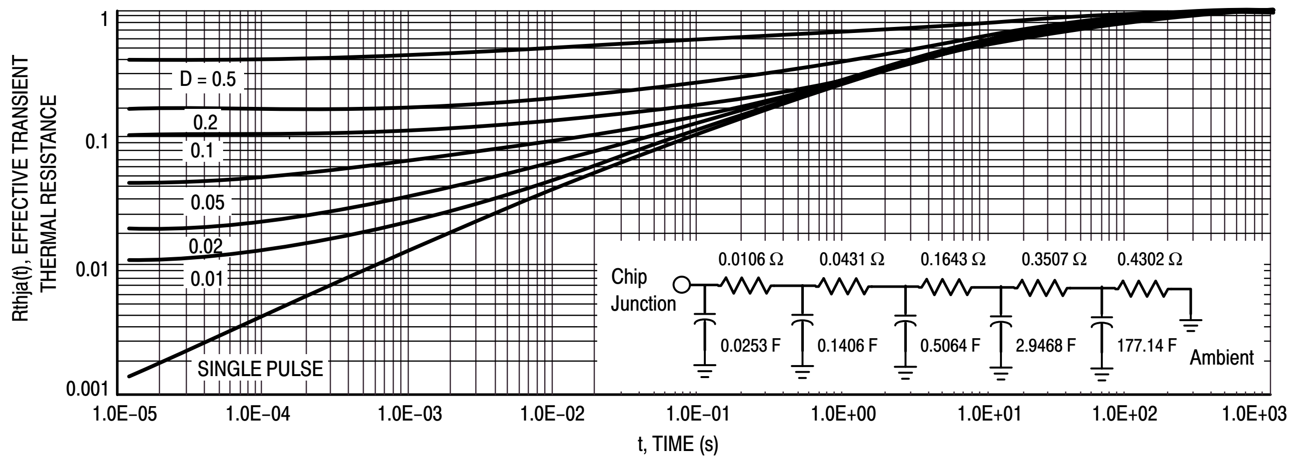



**Figure 14. Thermal Response**

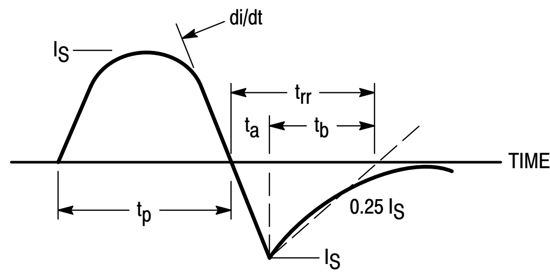
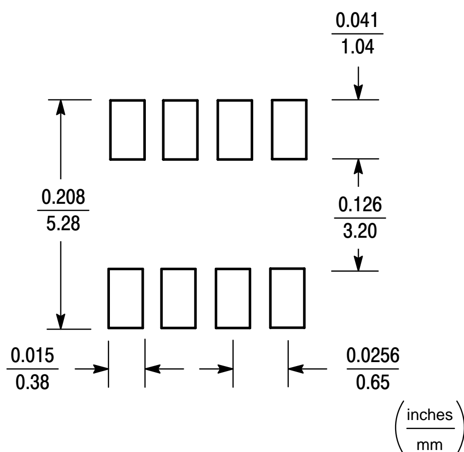



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

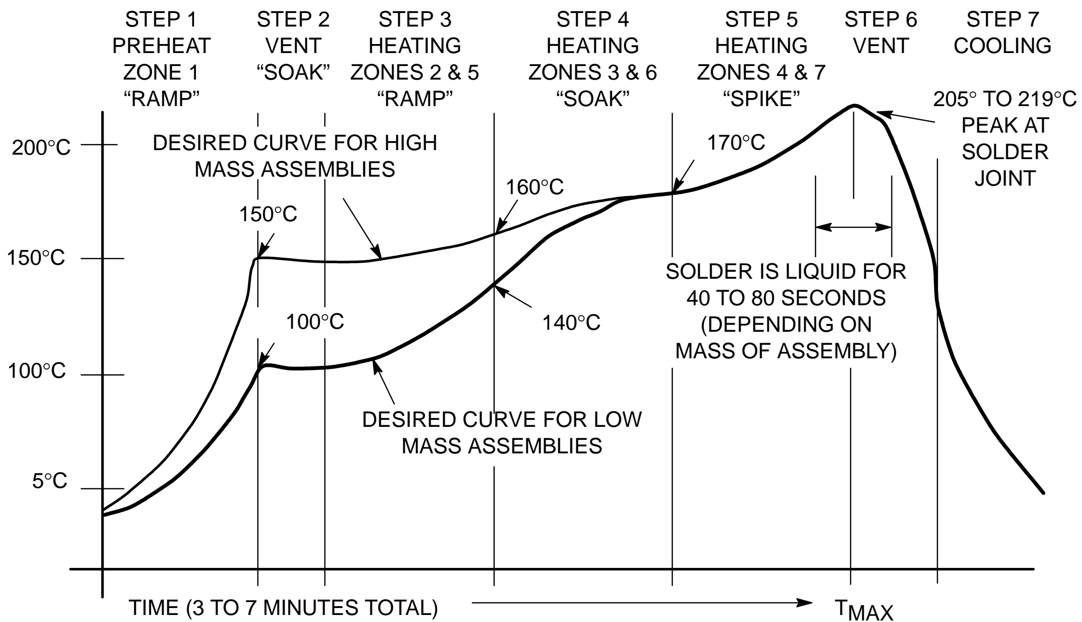



**Figure 16. Typical Solder Heating Profile**

# MMDF3N06HD

**Preferred Device**

*Advance Information*

# Power MOSFET 3 Amps, 60 Volts

## N–Channel SO–8, Dual

**ON Semiconductor™**

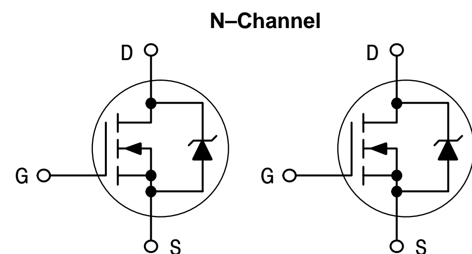
**http://onsemi.com**

**3 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 100 mΩ**

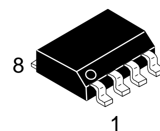
These miniature surface mount MOSFETs feature low $R_{DS(on)}$ and true logic level performance. Dual MOSFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

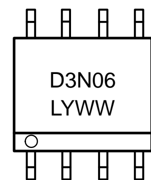
**N–Channel**




**MARKING DIAGRAM**




**SO–8, Dual**
**CASE 751**
**STYLE 11**



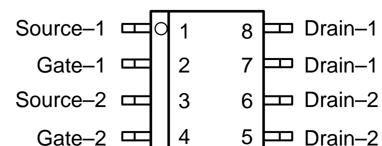

L = Location Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C | $I_D$<br>$I_{DM}$ | 3.3<br>16.5 | Adc<br>Apk |
| Source Current – Continuous @ $T_A$ = 25°C | $I_S$ | 1.7 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 60 Vdc, $V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 32 Vdc, $I_L$ = 15 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 105 | mJ |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF3N06HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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November, 2000 – Rev. 1

Publication Order Number:
MMDF3N06HD/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | 0.001<br>0.05 | 1.0<br>25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | 12 | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | | $V_{GS(th)}$ | 1.0 | – | – | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.3 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | –<br>– | 67.5<br>82.5 | 100<br>200 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | – | 7.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 442 | 618 | pF |
| Output Capacitance | | $C_{oss}$ | – | 97.6 | 137 | |
| Transfer Capacitance | | $C_{rss}$ | – | 24.4 | 34.2 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 3.3 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 30 Ω) | $t_{d(on)}$ | – | 10.6 | 22.1 | ns |
| Rise Time | | $t_r$ | – | 15.9 | 31.8 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 23.8 | 47.6 | |
| Fall Time | | $t_f$ | – | 14.7 | 29.4 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.0 | 14 | ns |
| Rise Time | | $t_r$ | – | 4.8 | 9.6 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32.4 | 64.8 | |
| Fall Time | | $t_f$ | – | 14.2 | 28.4 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 30 Vdc, $I_D$ = 3.3 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 14.5 | 29 | nC |
| | | $Q_1$ | – | 1.8 | – | |
| | | $Q_2$ | – | 3.5 | – | |
| | | $Q_3$ | – | 3.75 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.78<br>0.65 | 1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 27.9 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 4.9 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.038 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

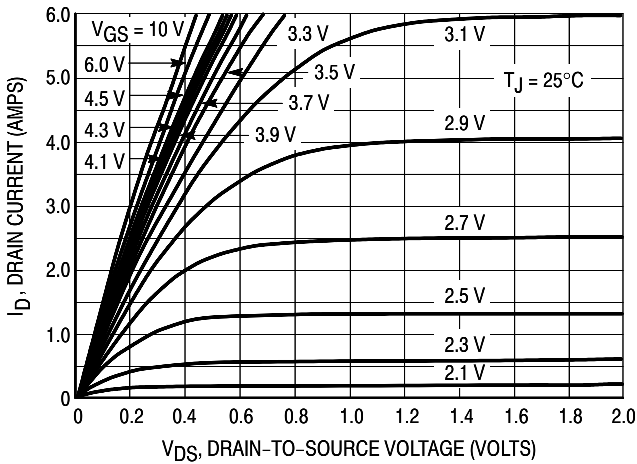



**Figure 1. On−Region Characteristics**

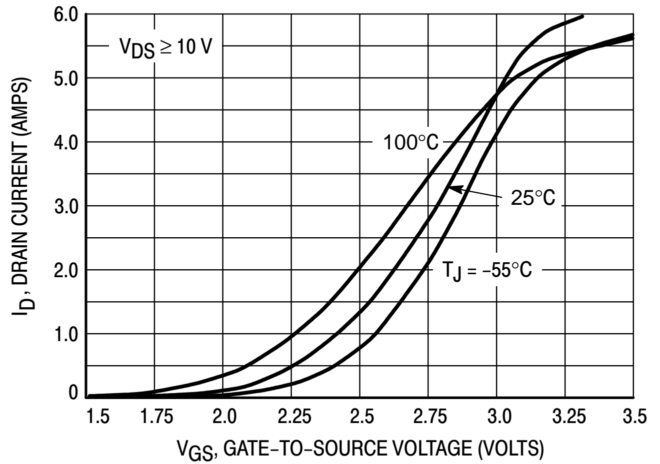



**Figure 2. Transfer Characteristics**

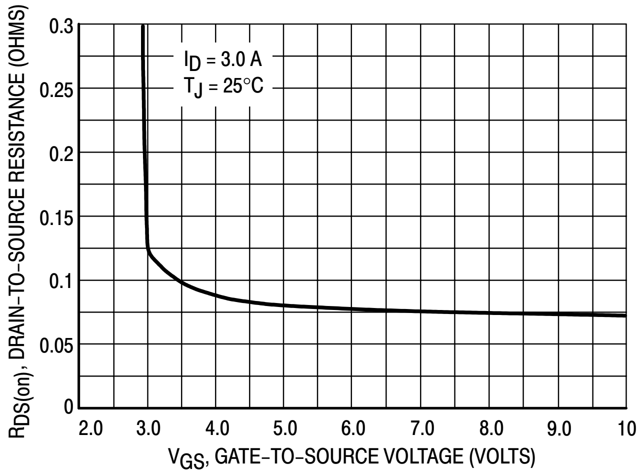



**Figure 3. On−Resistance versus Gate−to−Source Voltage**

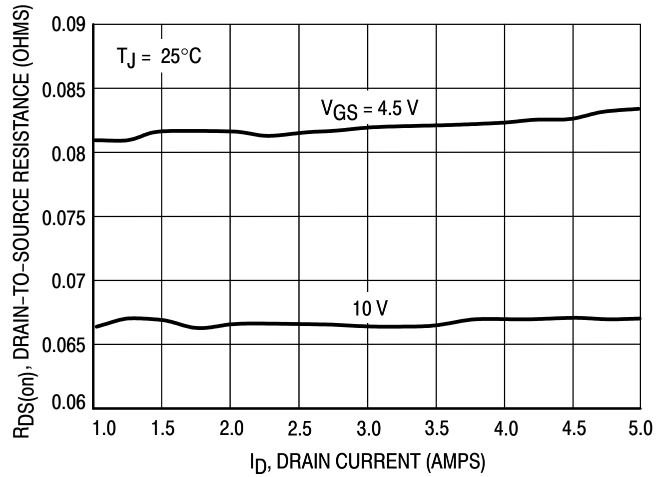



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

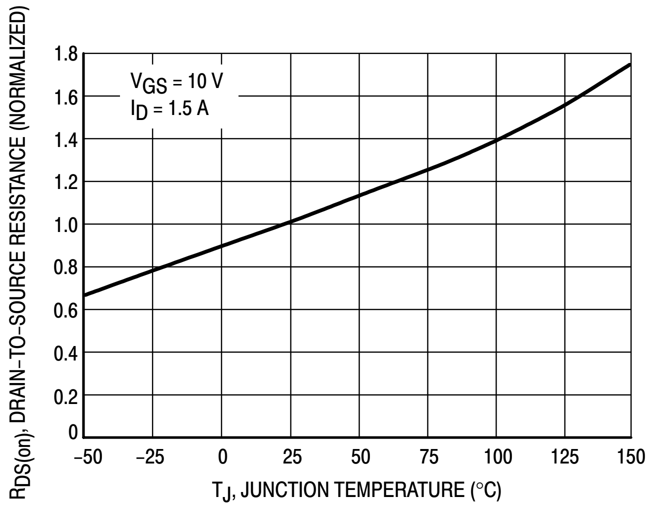



**Figure 5. On−Resistance Variation with Temperature**

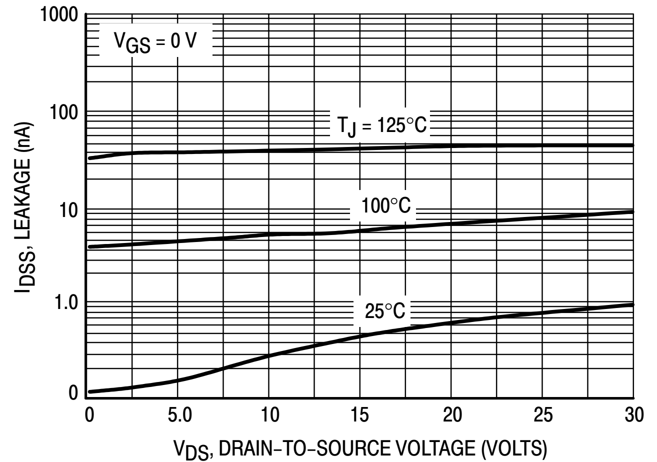



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

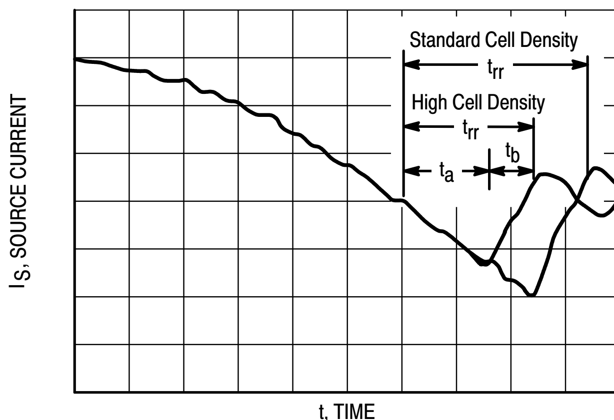



**Figure 7. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 9). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

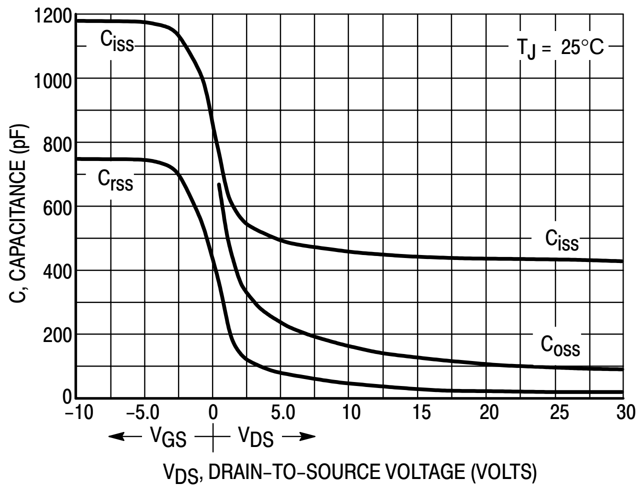



**Figure 8. Capacitance Variation**

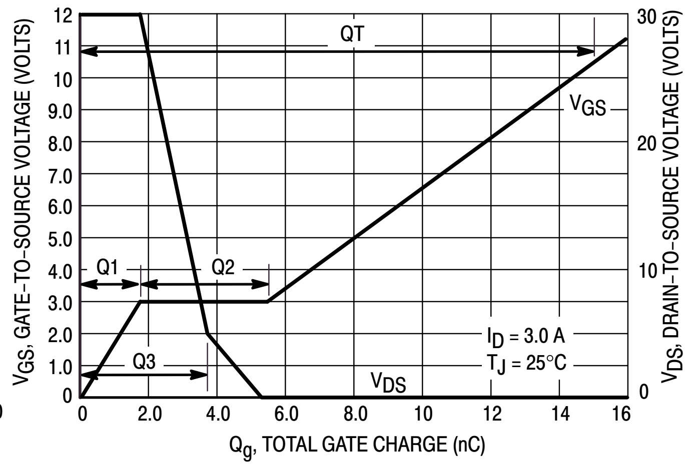



**Figure 9. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

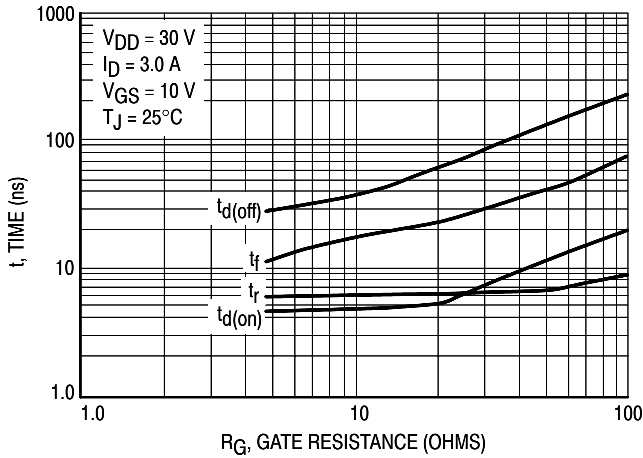



**Figure 10. Resistive Switching Time Variation versus Gate Resistance**

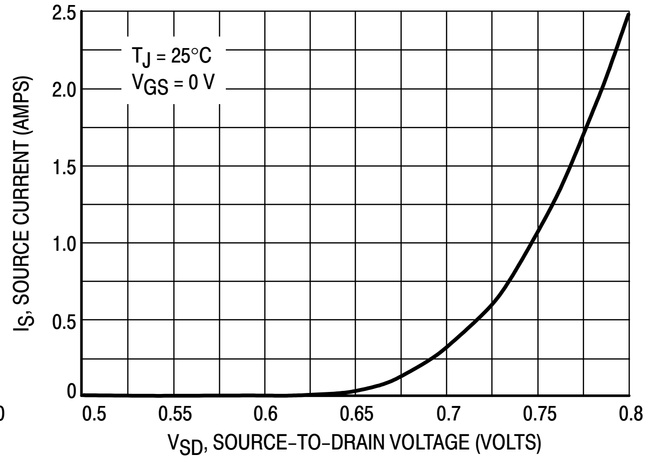



**Figure 11. Diode Forward Voltage versus Current**

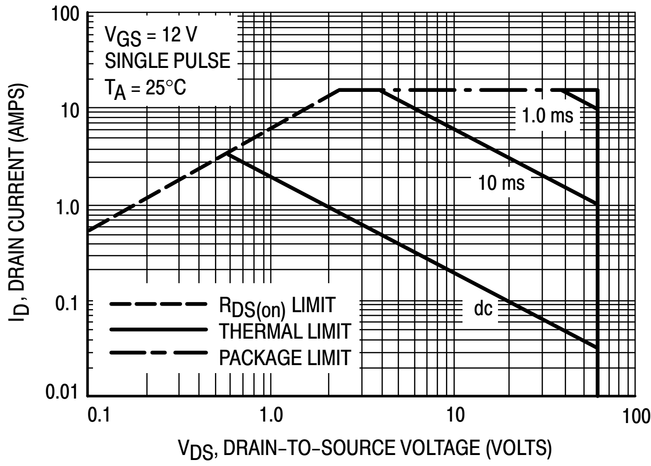



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

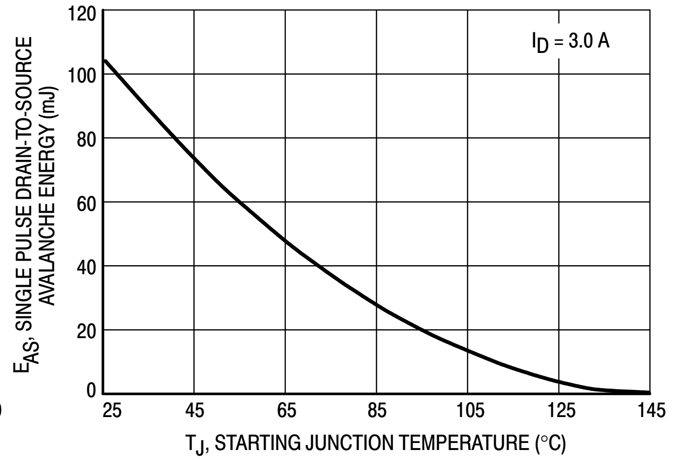



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

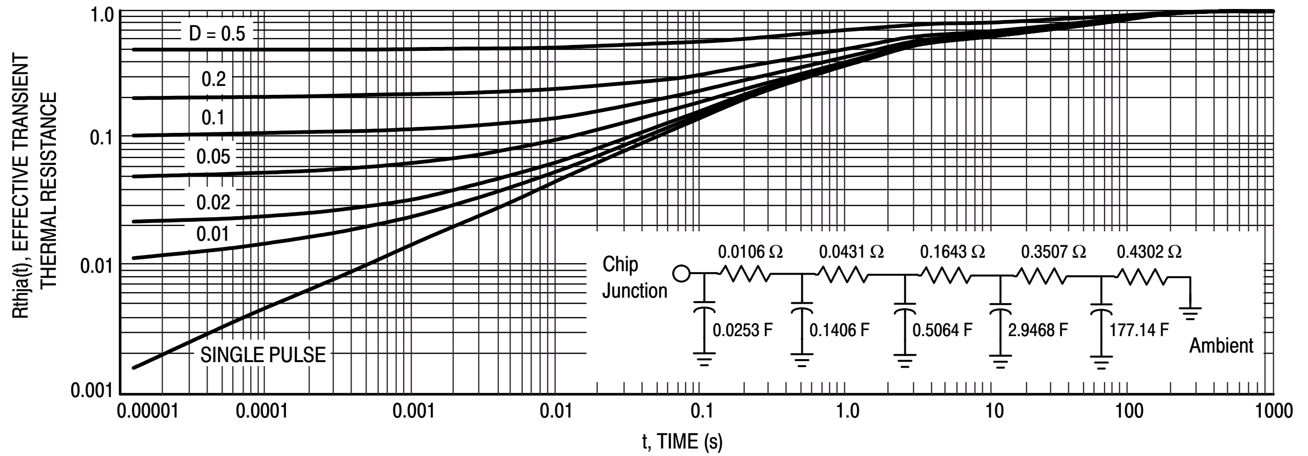



**Figure 14. Thermal Response**

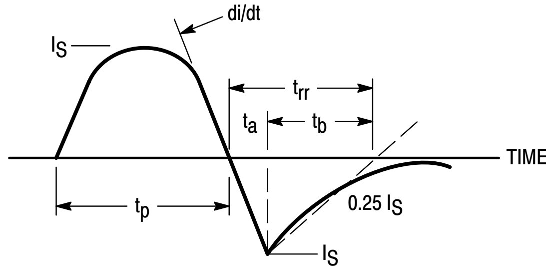
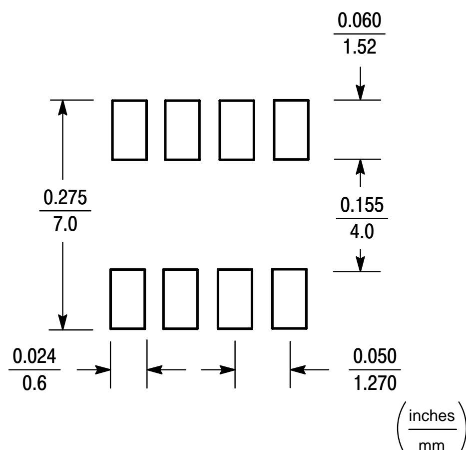



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

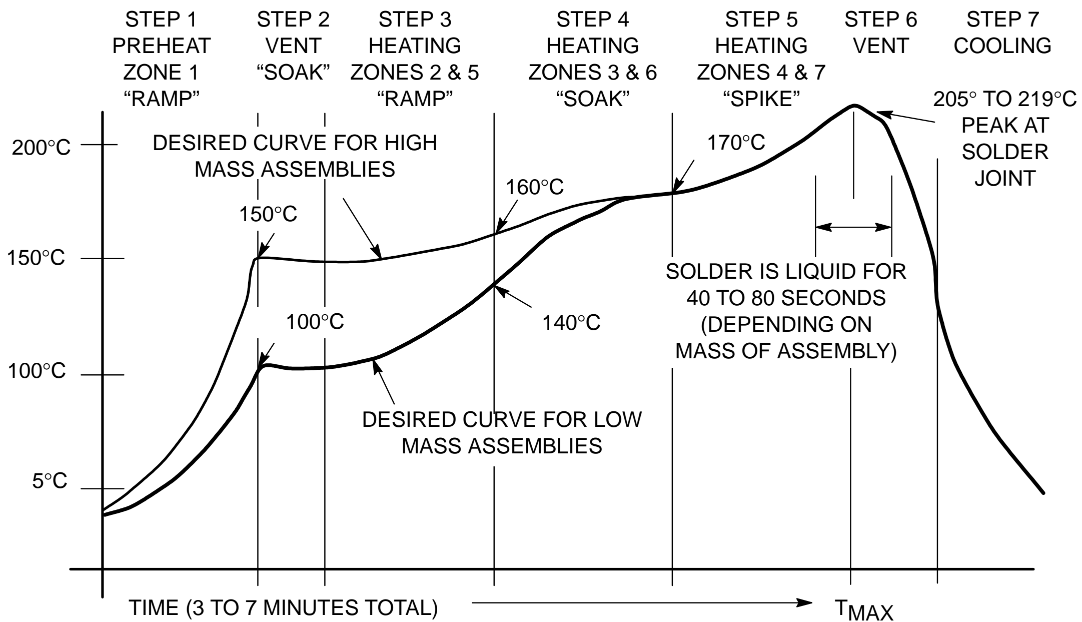



**Figure 16. Typical Solder Heating Profile**

# MMDF3N06VL

*Product Preview*

## Power MOSFET 3 Amps, 60 Volts

### N–Channel SO–8, Dual

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET™ Predecessors
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Mounting Information for SO–8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage, ($R_{GS}$ = 1 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 15 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 3.3<br>0.7<br>10 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 3.3 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 54 | mJ |
| Thermal Resistance, Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 0.0625″ from case for 10 seconds | $T_L$ | 260 | °C |

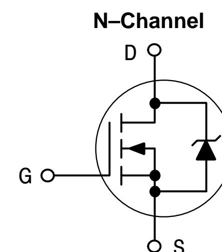
1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**ON Semiconductor™**

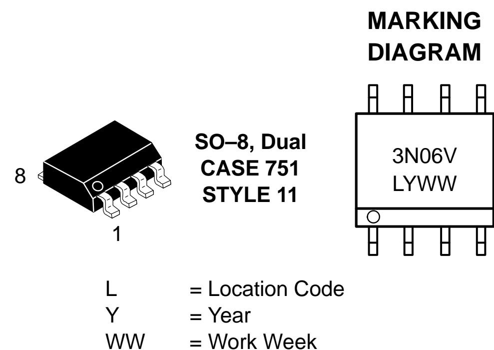
http://onsemi.com

**3 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 130 mΩ**

**N–Channel**

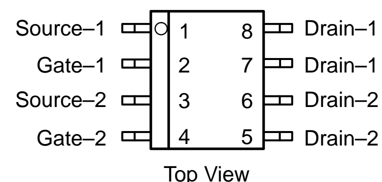



**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF3N06VLR2 | SO–8 | 2500 Tape & Reel |

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 66 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 3.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 3.3 Adc) | | $R_{DS(on)}$ | – | 0.12 | 0.13 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5.0 Vdc, $I_D$ = 3.3 Adc) | | $V_{DS(on)}$ | – | – | 0.5 | Vdc |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 1.65 Adc, $T_J$ = 150°C) | | | – | – | 0.4 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 1.65 Adc) | | $g_{FS}$ | 1.0 | 3.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 340 | 480 | pF |
| Output Capacitance | | $C_{oss}$ | – | 110 | 150 | |
| Transfer Capacitance | | $C_{rss}$ | – | 27 | 50 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 3.3 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 30 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | 60 | |
| Fall Time | | $t_f$ | – | 28 | 60 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 3.3 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 9.0 | 20 | nC |
| | | $Q_1$ | – | 1.5 | – | |
| | | $Q_2$ | – | 4.3 | – | |
| | | $Q_3$ | – | 3.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 3.3 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.84 | 1.2 | Vdc |
| | ($I_S$ = 3.3 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 0.67 | – | |
| Reverse Recovery Time | ($I_S$ = 3.3 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 58 | – | ns |
| | | $t_a$ | – | 38 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.11 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

# MMDF4N01HD

**Preferred Device**

# Power MOSFET 4 Amps, 20 Volts

## N–Channel SO–8, Dual

**ON Semiconductor™**

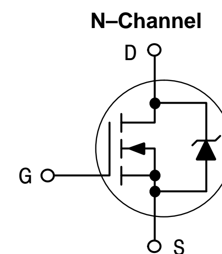
**http://onsemi.com**

**4 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 45 mΩ**

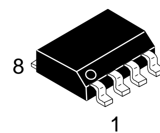
These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

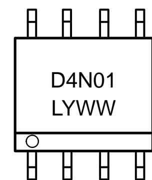
**N–Channel**




**MARKING DIAGRAM**




**SO–8, Dual**
**CASE 751**
**STYLE 11**



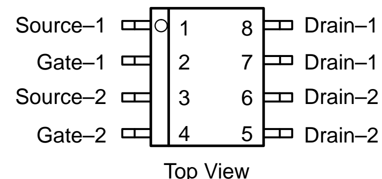

L = Location Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5.2<br>4.1<br>48 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided) with one die operating, 10 sec. max.

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF4N01HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 20<br>– | –<br>2.0 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 0.6<br>– | 0.8<br>2.8 | 1.1<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 4.0 Adc)<br>(VGS = 2.7 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | –<br>– | 0.035<br>0.043 | 0.045<br>0.055 | Ohm |
| Forward Transconductance ($V_{DS}$ = 2.5 Vdc, $I_D$ = 2.0 Adc) | | $g_{FS}$ | 3.0 | 6.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 425 | 595 | pF |
| Output Capacitance | | $C_{oss}$ | – | 270 | 378 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 115 | 230 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 13 | 26 | ns |
| Rise Time | | $t_r$ | – | 60 | 120 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 20 | 40 | |
| Fall Time | | $t_f$ | – | 29 | 58 | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 10 | 20 | |
| Rise Time | | $t_r$ | – | 42 | 84 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 24 | 48 | |
| Fall Time | | $t_f$ | – | 28 | 56 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 10 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 9.2 | 13 | nC |
| | | $Q_1$ | – | 1.3 | – | |
| | | $Q_2$ | – | 3.5 | – | |
| | | $Q_3$ | – | 3.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.95<br>0.78 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 17 | – | |
| | | $t_b$ | – | 22 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.028 | – | µC |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

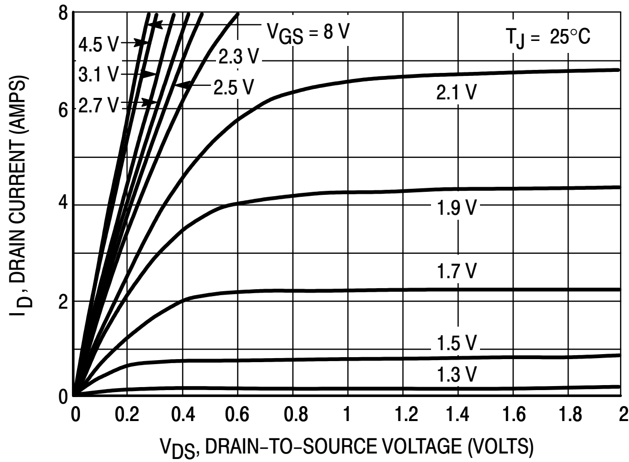



**Figure 1. On–Region Characteristics**

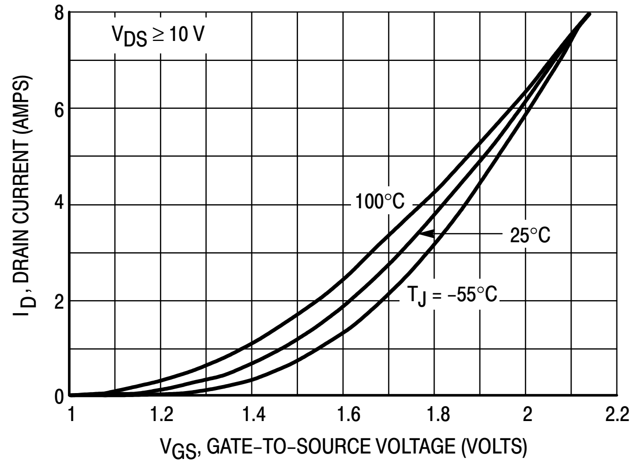



**Figure 2. Transfer Characteristics**

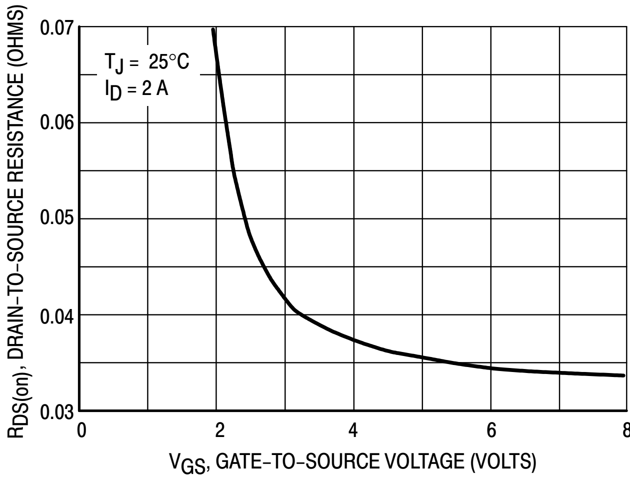



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

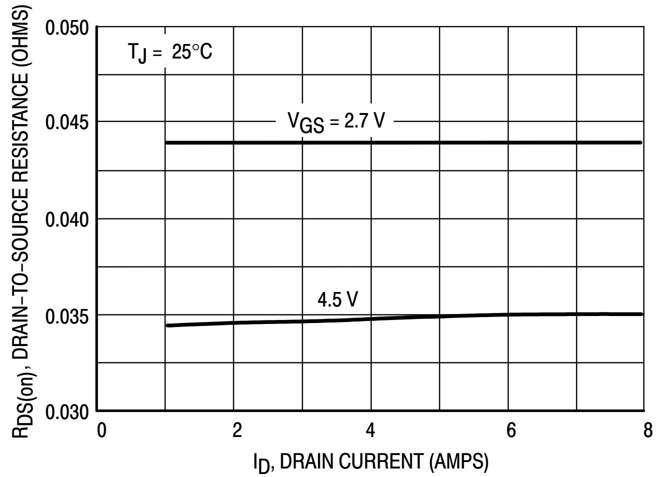



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

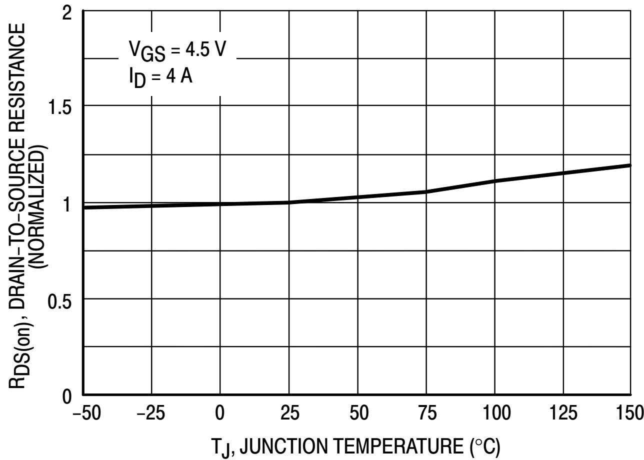



**Figure 5. On–Resistance Variation with Temperature**

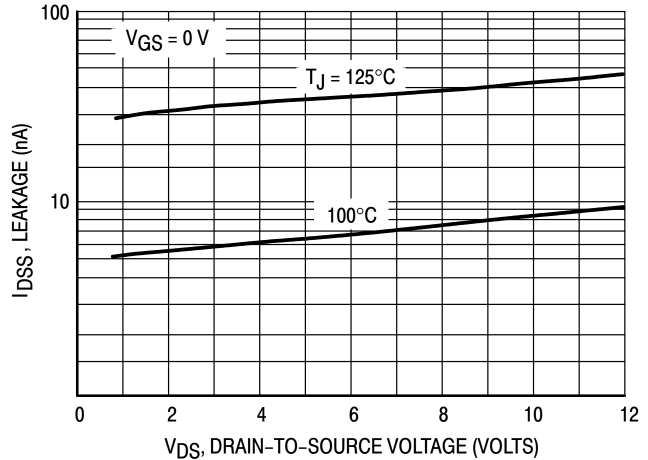



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \mathrm{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \mathrm{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

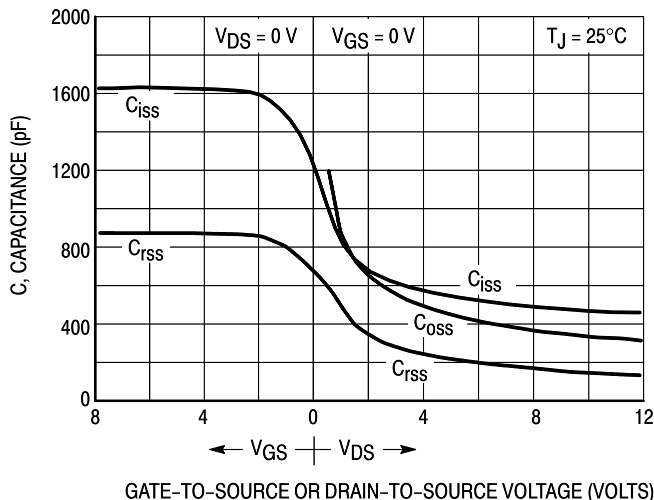



**Figure 7. Capacitance Variation**

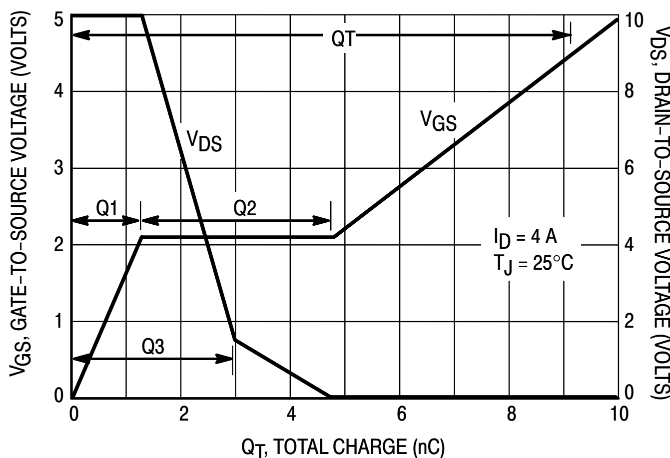



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

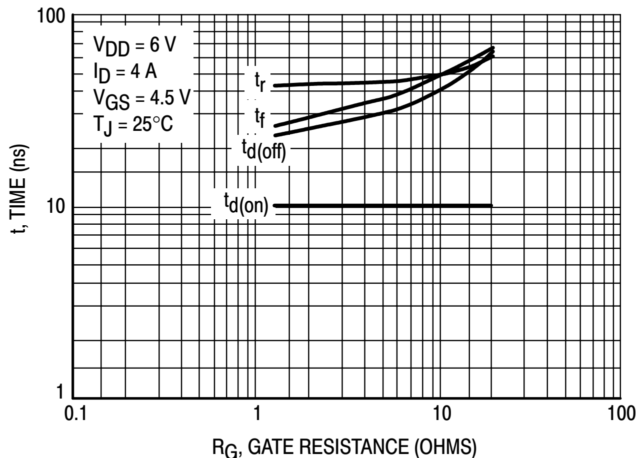



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

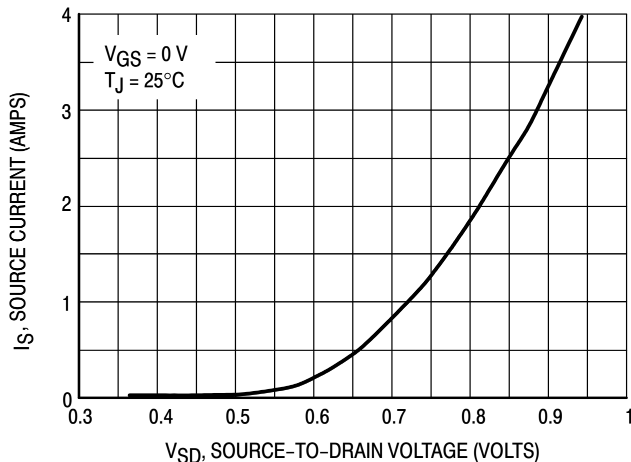



Figure 10. Diode Forward Voltage versus Current

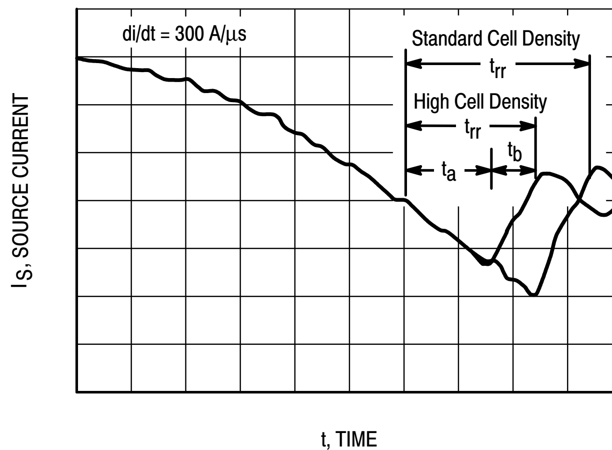



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

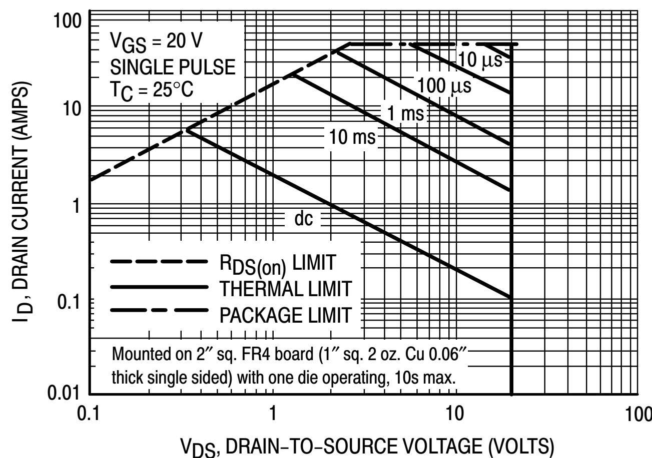



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

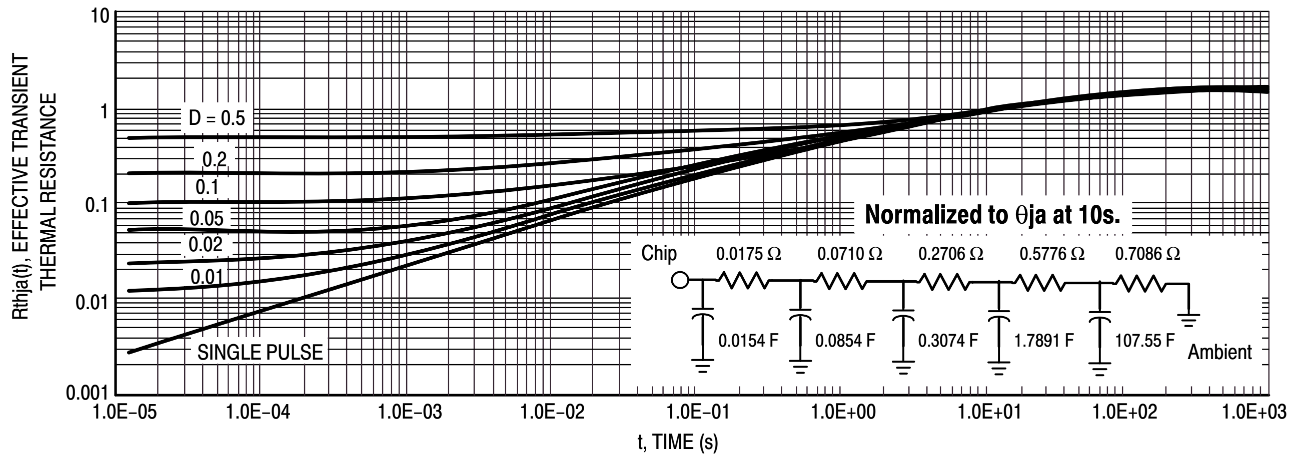



**Figure 13. Thermal Response**

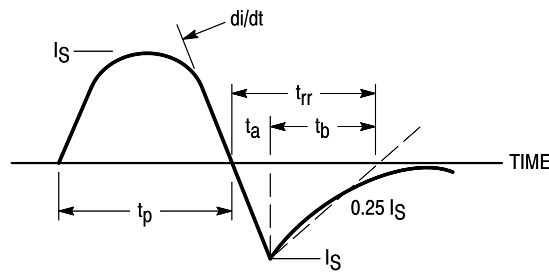
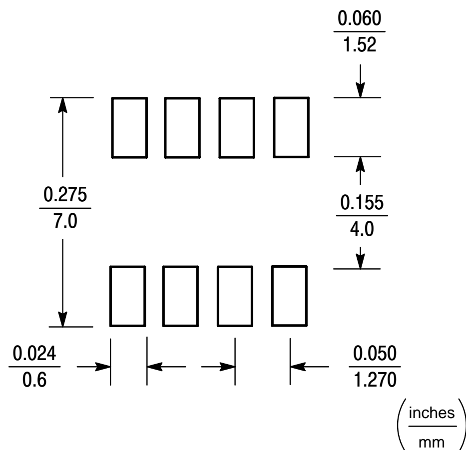



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

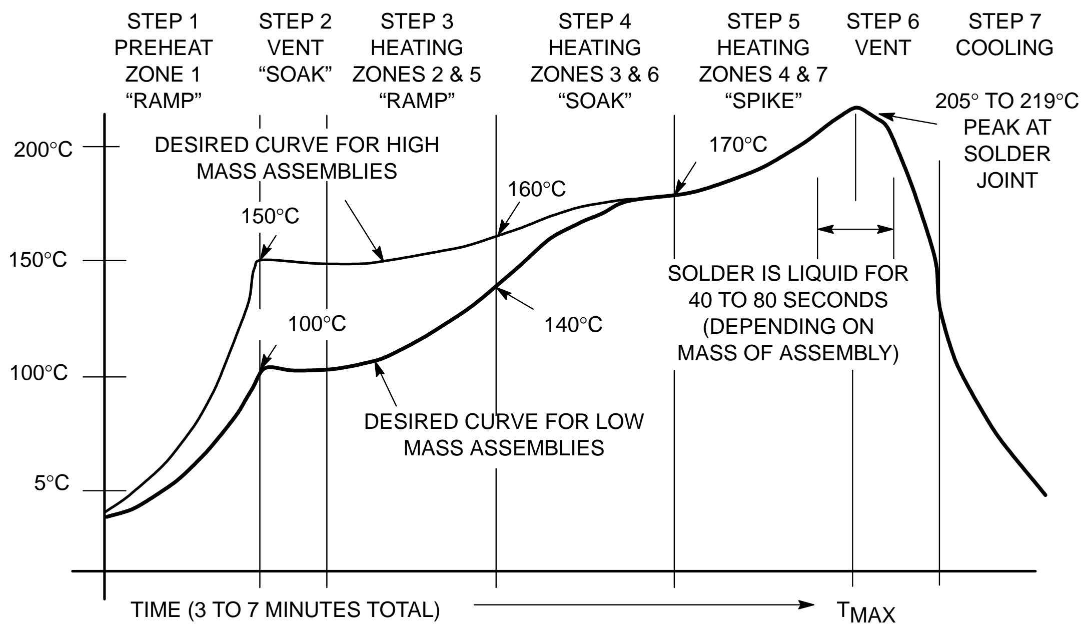



**Figure 15. Typical Solder Heating Profile**

# MMDF5N02Z

# Power MOSFET 5 Amps, 20 Volts

## N–Channel SO–8, Dual

**ON Semiconductor™**

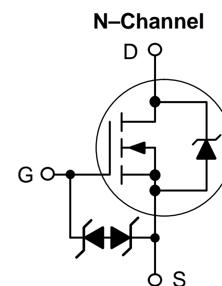
**http://onsemi.com**

**5 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

EZFETs™ are an advanced series of Power MOSFETs which contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important.

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**N–Channel**

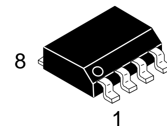



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

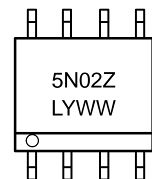
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5.0<br>4.5<br>40 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction to Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Temperature for Soldering | $T_L$ | 260 | °C |

1. When mounted on 1 inch square FR–4 or G–10 board ($V_{GS}$ = 4.5 V, @ 10 Seconds).

**MARKING DIAGRAM**

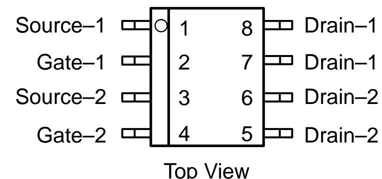



**SO–8, Dual**
**CASE 751**
**STYLE 11**




5N02Z = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF5N02ZR2 | SO–8 | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>20<br>– | <br>–<br>15 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 12 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>–<br>– | <br>–<br>–<br>– | <br>0.5<br>15<br>150 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 1.5 | µAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>0.5<br>– | <br>0.78<br>3.0 | <br>1.1<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc)<br>($V_{GS}$ = 2.7 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>34<br>44 | <br>40<br>50 | mΩ |
| Forward Transconductance ($V_{DS}$ = 9.0 Vdc, $I_D$ = 2.0 Adc) | | $g_{FS}$ | 3.0 | 5.6 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 450 | 630 | pF |
| Output Capacitance | | $C_{oss}$ | – | 330 | 460 | |
| Transfer Capacitance | | $C_{rss}$ | – | 160 | 225 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 6.0 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) | $t_{d(on)}$ | – | 29 | 37 | ns |
| Rise Time | | $t_r$ | – | 182 | 258 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 190 | 238 | |
| Fall Time | | $t_f$ | – | 225 | 274 | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 10.7 | 12 | nC |
| | | $Q_1$ | – | 1.1 | – | |
| | | $Q_2$ | – | 5.4 | – | |
| | | $Q_3$ | – | 3.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.78<br>0.65 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 195 | – | ns |
| | | $t_a$ | – | 72 | – | |
| | | $t_b$ | – | 123 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.5 | – | µC |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

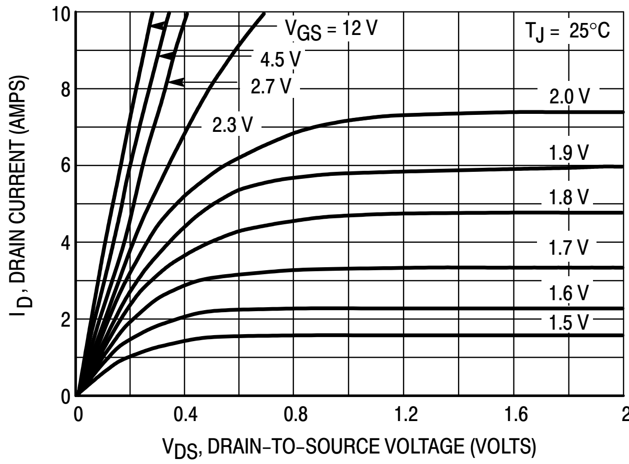



**Figure 1. On–Region Characteristics**

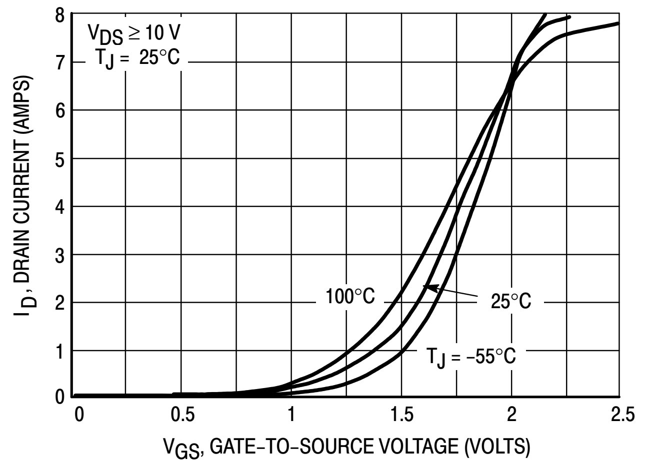



**Figure 2. Transfer Characteristics**

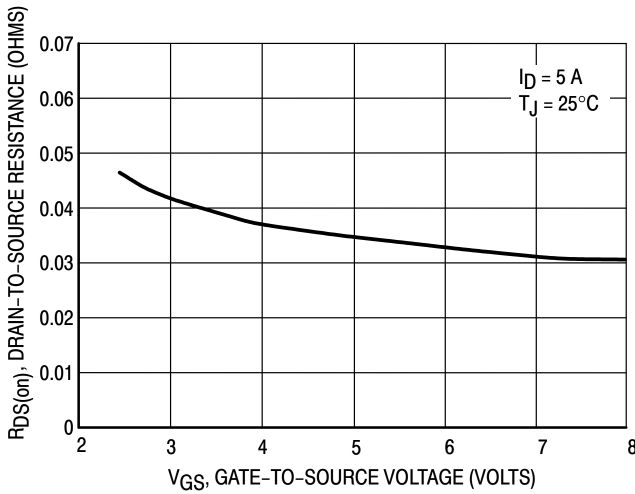



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

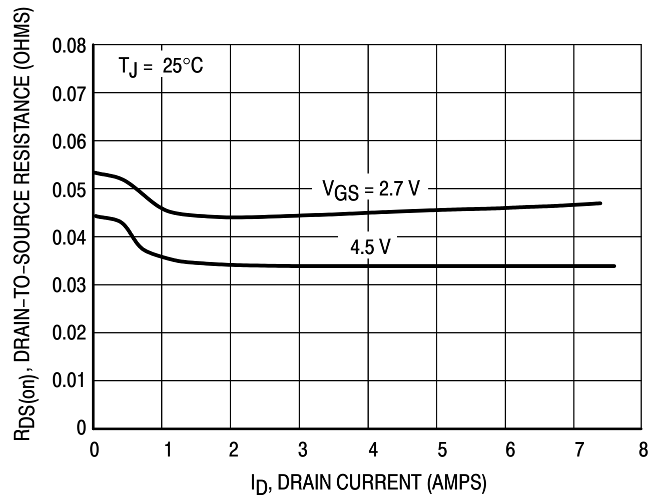



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

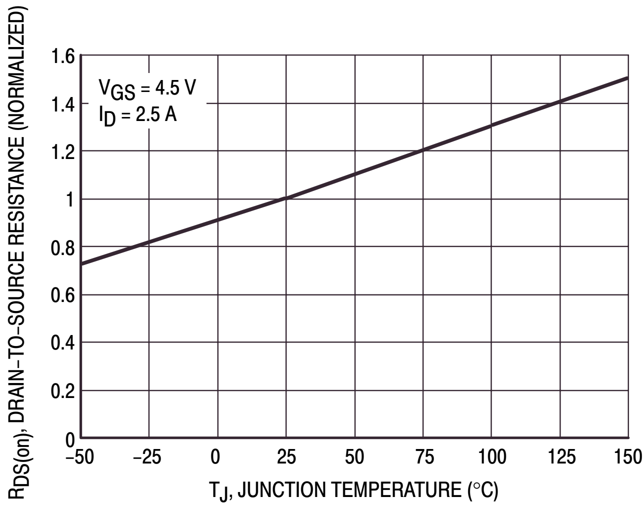



**Figure 5. On–Resistance Variation with Temperature**

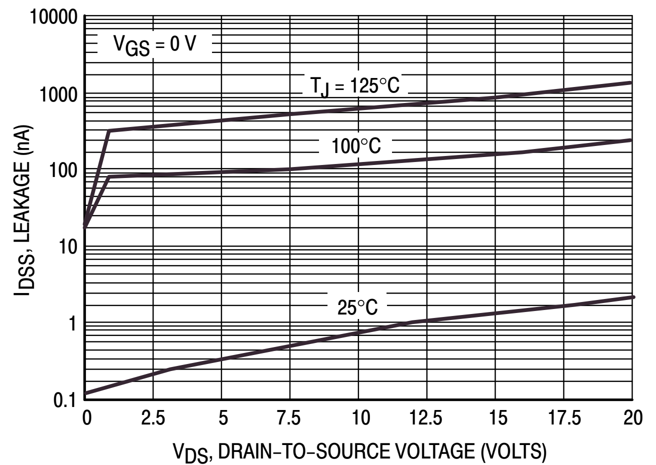



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, In \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, In \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

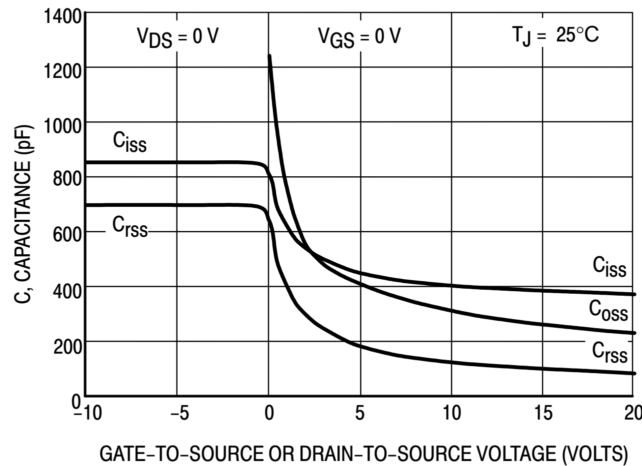



**Figure 7. Capacitance Variation**

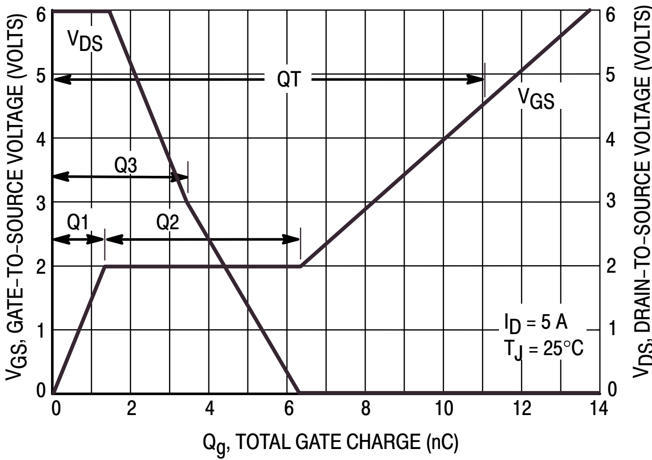



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

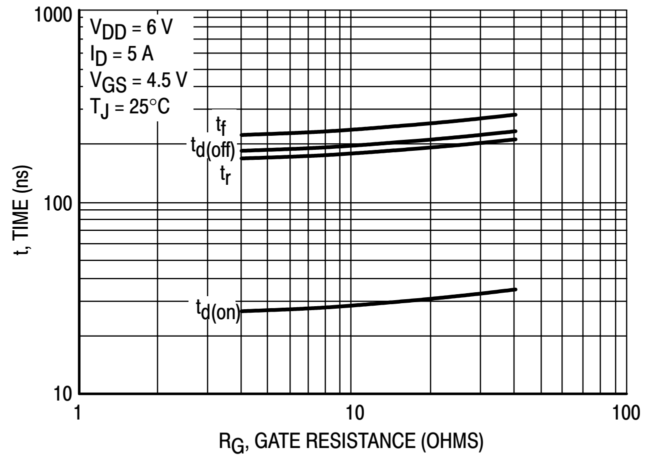



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

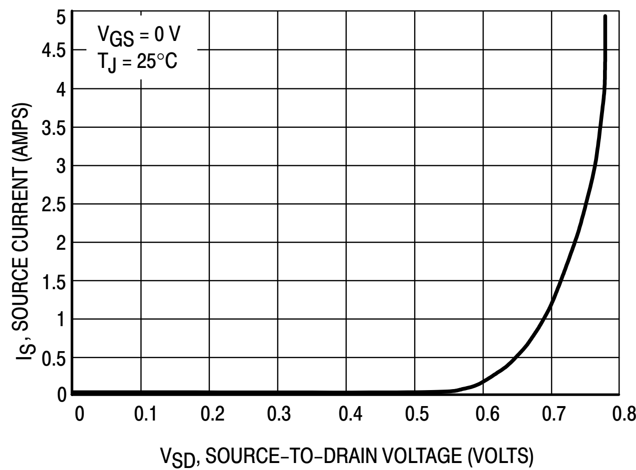



**Figure 10. Diode Forward Voltage versus Current**

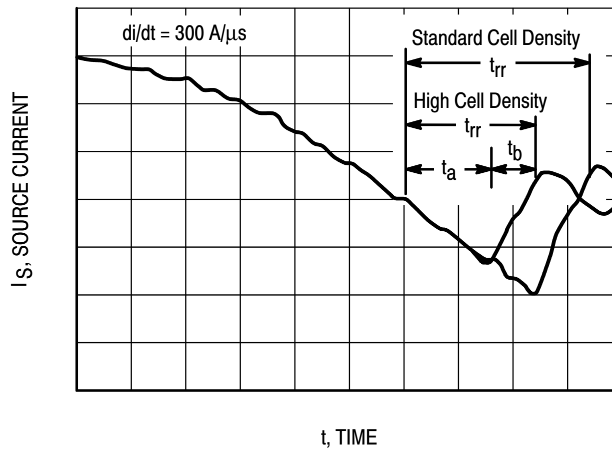



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

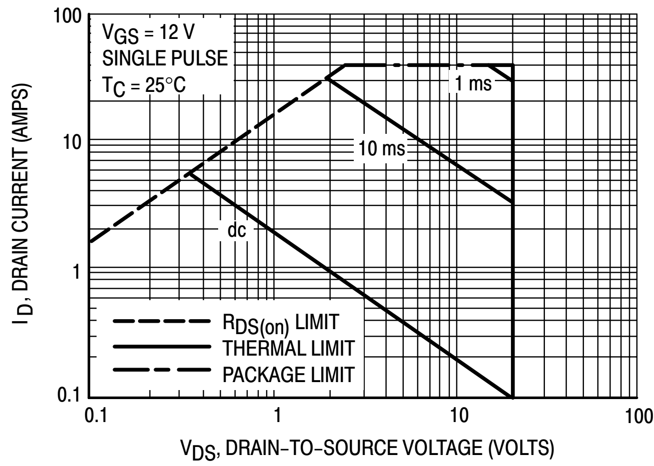



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

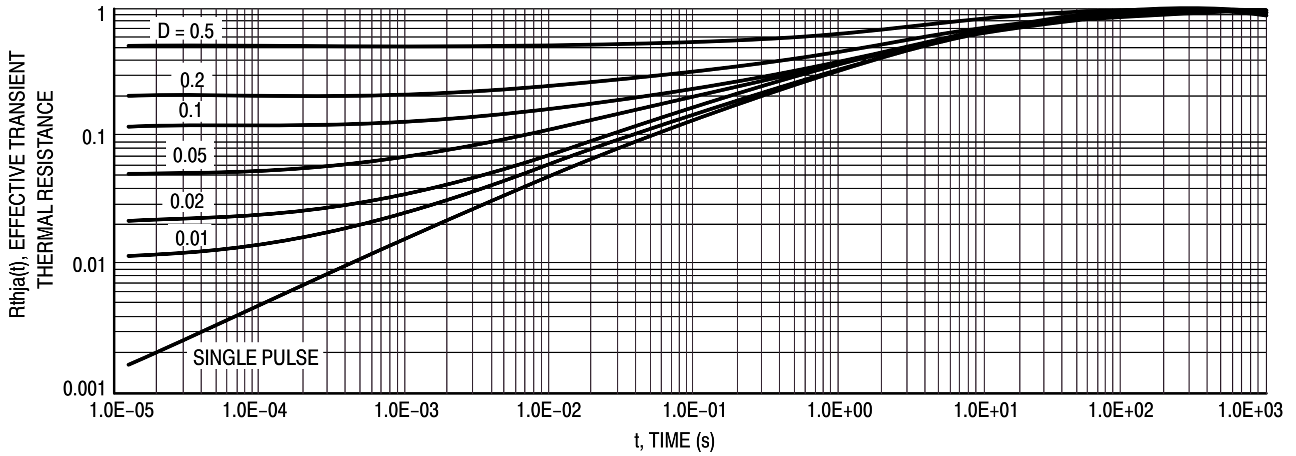



**Figure 13. Thermal Response**

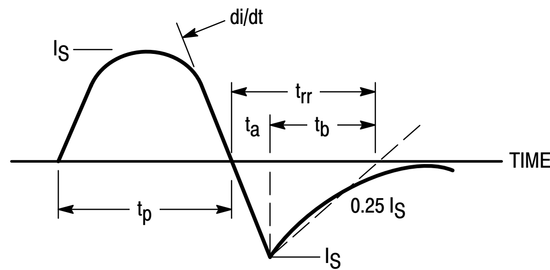
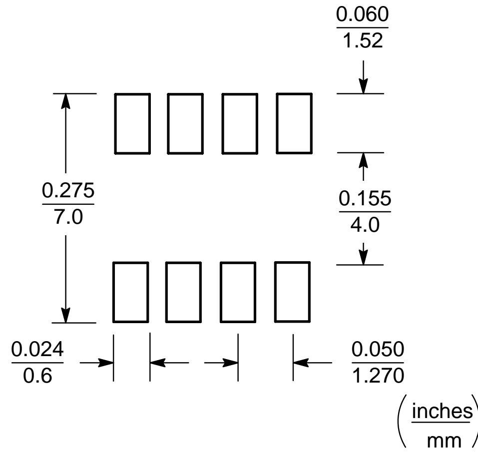



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

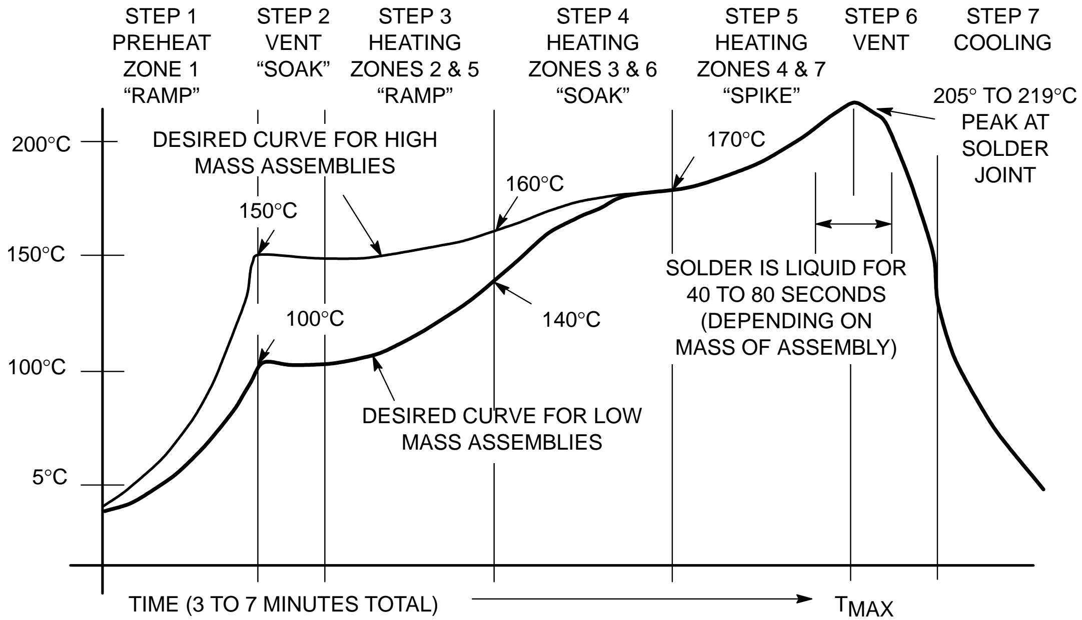



**Figure 15. Typical Solder Heating Profile**

# MMDF6N03HD

**Preferred Device**

# Power MOSFET 6 Amps, 30 Volts
## N–Channel SO–8, Dual

These miniature surface mount MOSFETs feature low $R_{DS(on)}$ and true logic level performance. Dual MOSFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_{DM}$ | 6.0<br>30 | Adc<br>Apk |
| Source Current – Continuous @ $T_A$ = 25°C | $I_S$ | 1.7 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 20 Vdc, $I_L$ = 9.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 325 | mJ |
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 sec. | $T_L$ | 260 | °C |

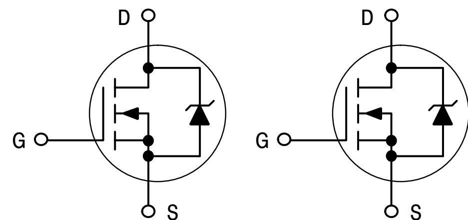
1. Mounted on G10/FR4 glass epoxy board using minimum recommended footprint.

**ON Semiconductor**™

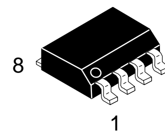
**http://onsemi.com**

**6 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 35 mΩ**

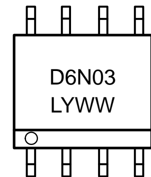
**N–Channel**




**MARKING DIAGRAM**

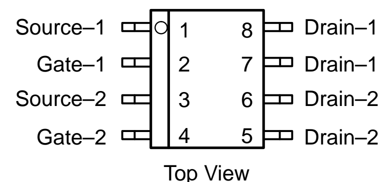



**SO–8, Dual**
**CASE 751**
**STYLE 11**




D6N03 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF6N03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>20 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0 | – | – | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 5.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.9 Adc) | | $R_{DS(on)}$ | –<br>– | 28<br>42 | 35<br>50 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc) | | $g_{FS}$ | – | 9.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 430 | 600 | pF |
| Output Capacitance | | $C_{oss}$ | – | 217 | 300 | |
| Transfer Capacitance | | $C_{rss}$ | – | 67.5 | 135 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $V_{GS}$ = 10 Vdc, $I_D$ = 1.0 Adc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 8.2 | 16.4 | ns |
| Rise Time | | $t_r$ | – | 8.48 | 16.9 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 89.6 | 179 | |
| Fall Time | | $t_f$ | – | 61.1 | 122 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 11.8 | 23 | ns |
| Rise Time | | $t_r$ | – | 51.3 | 102 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 47.2 | 94.5 | |
| Fall Time | | $t_f$ | – | 62 | 104 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 15.7 | 31.4 | nC |
| | | $Q_1$ | – | 2.0 | – | |
| | | $Q_2$ | – | 4.6 | – | |
| | | $Q_3$ | – | 3.86 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.77<br>0.65 | 1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 54.5 | – | ns |
| | | $t_a$ | – | 14.8 | – | |
| | | $t_b$ | – | 39.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.048 | – | µC |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

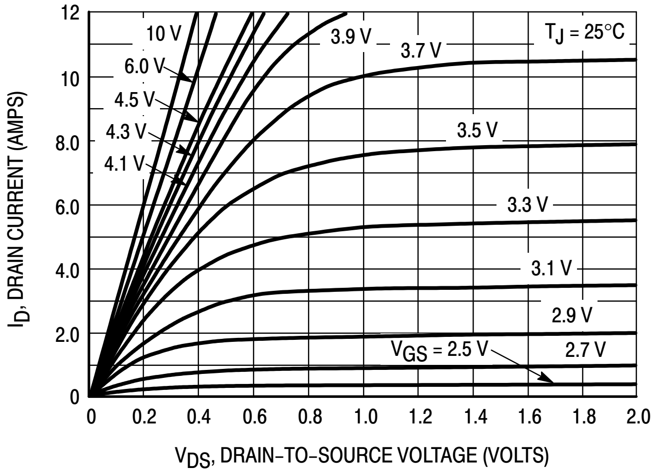



**Figure 1. On−Region Characteristics**

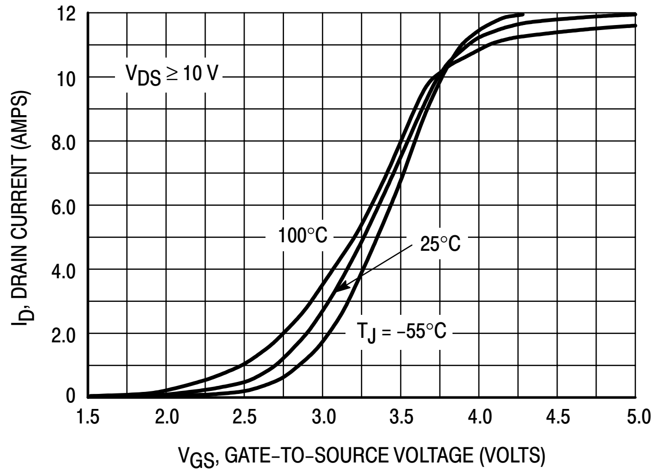



**Figure 2. Transfer Characteristics**

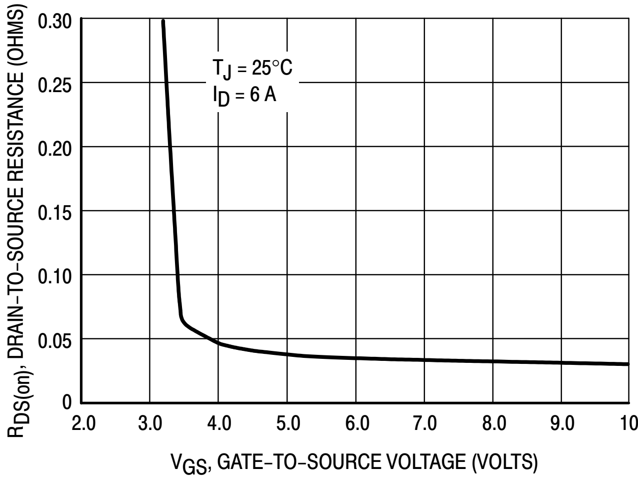



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

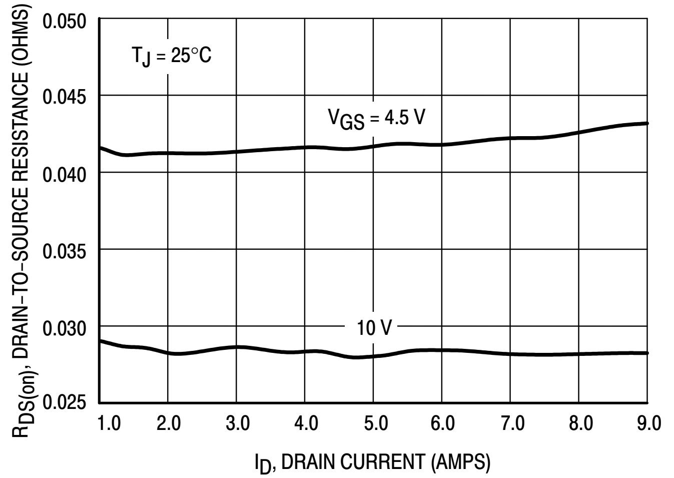



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

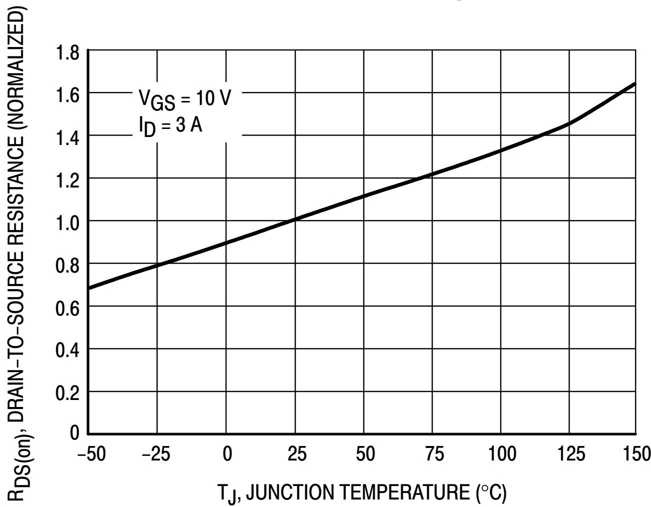



**Figure 5. On−Resistance Variation with Temperature**

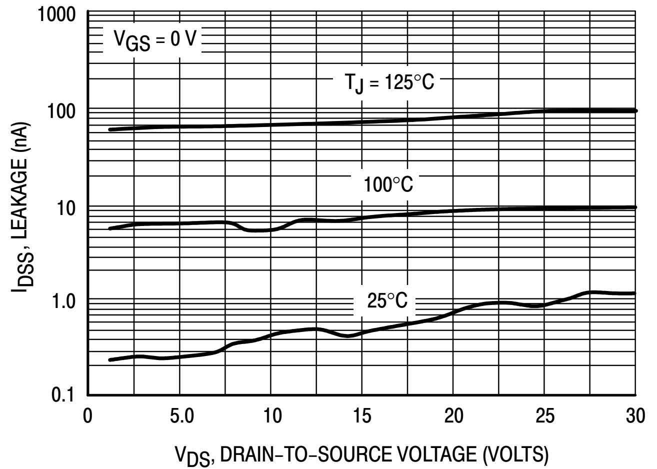



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

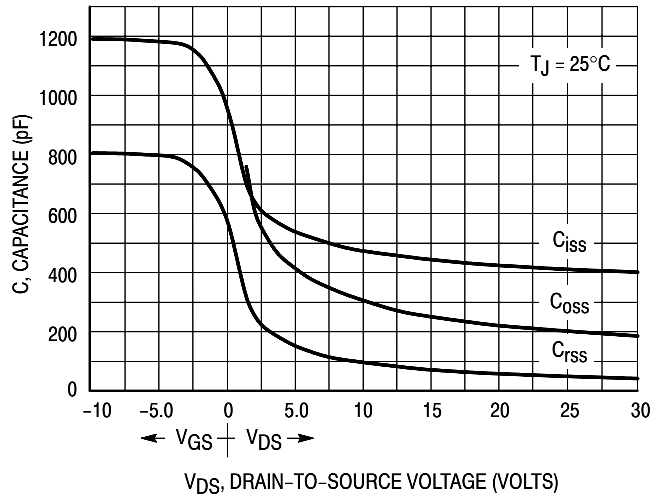



**Figure 7. Capacitance Variation**

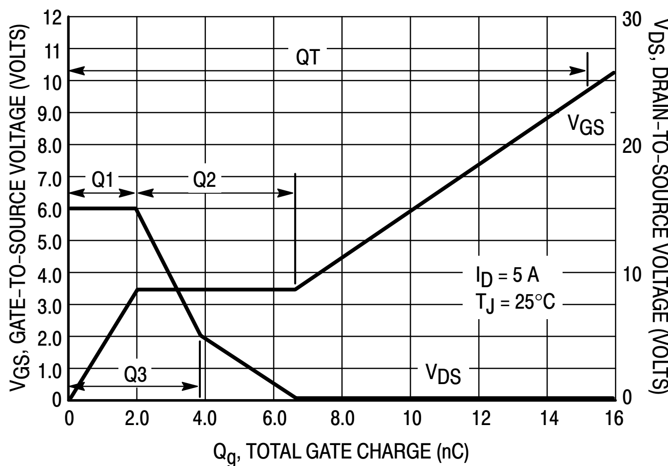



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

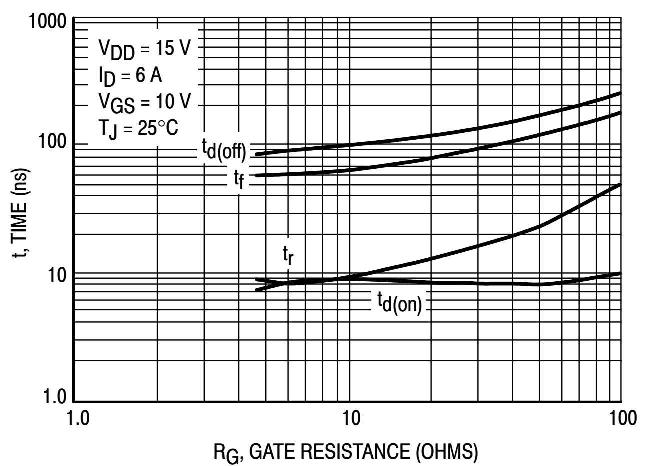



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

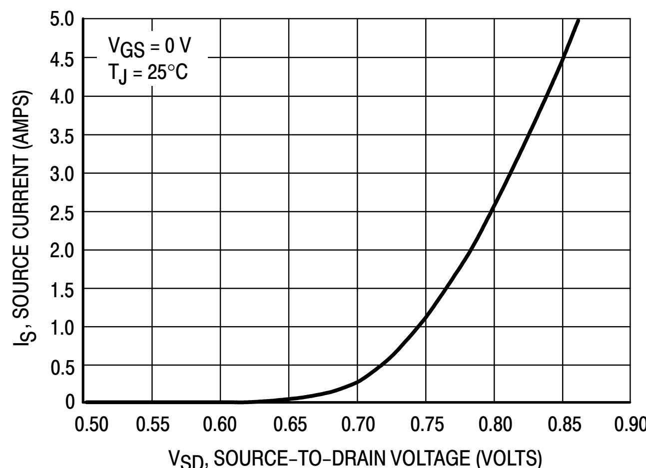



**Figure 10. Diode Forward Voltage versus Current**

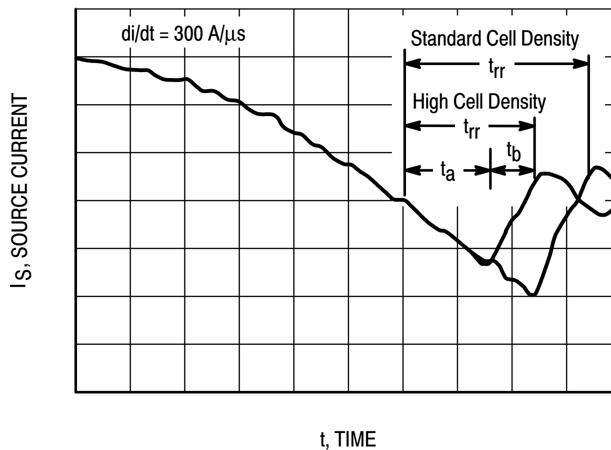



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

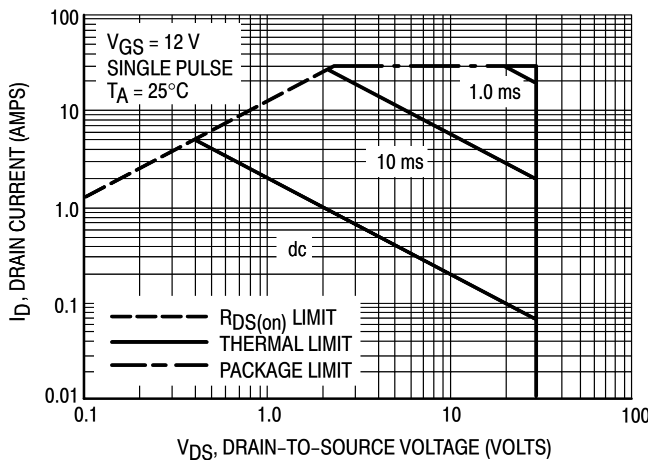



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

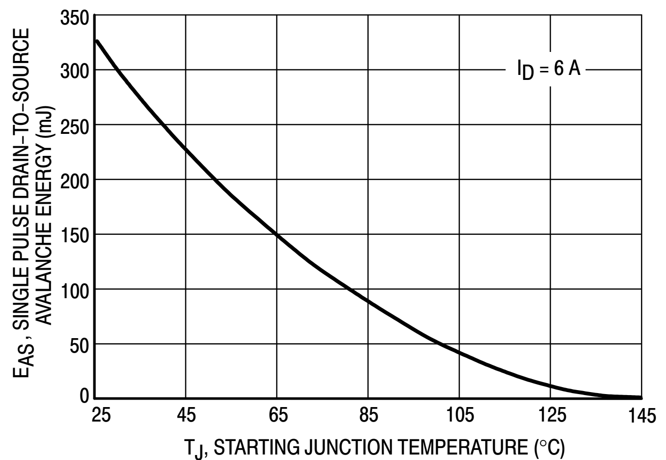



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

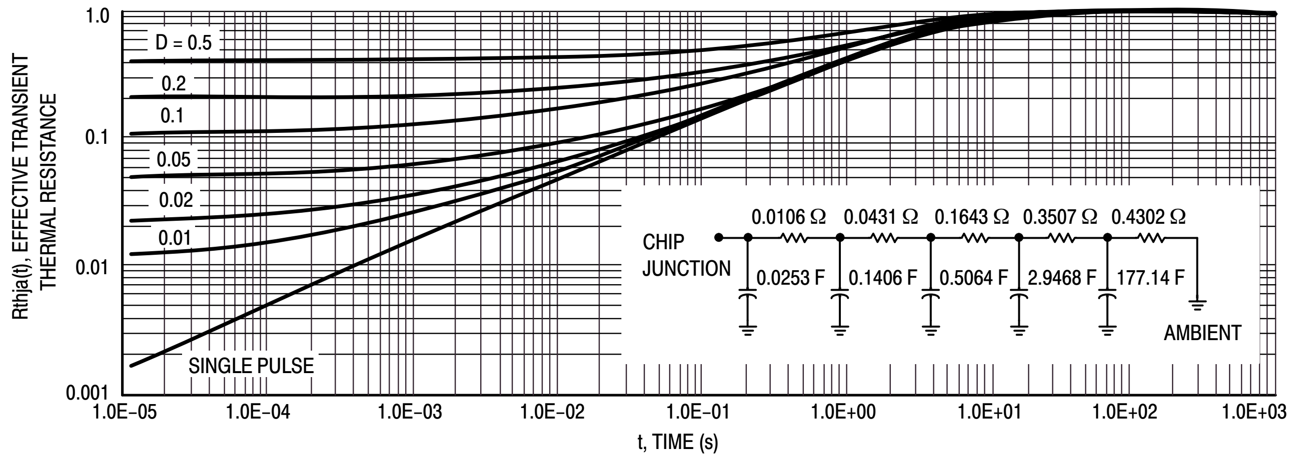



**Figure 14. Thermal Response**

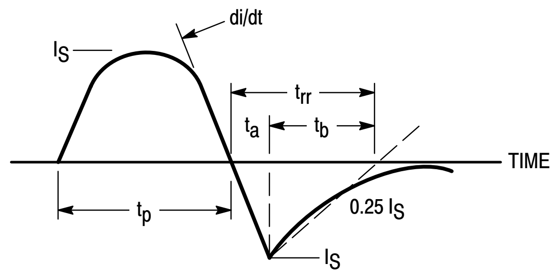
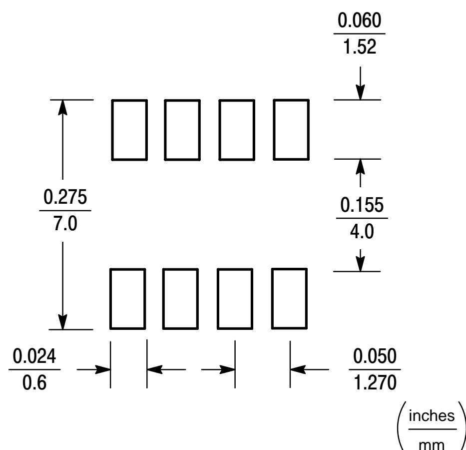



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150°C - 25°C}{62.5°C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

### TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

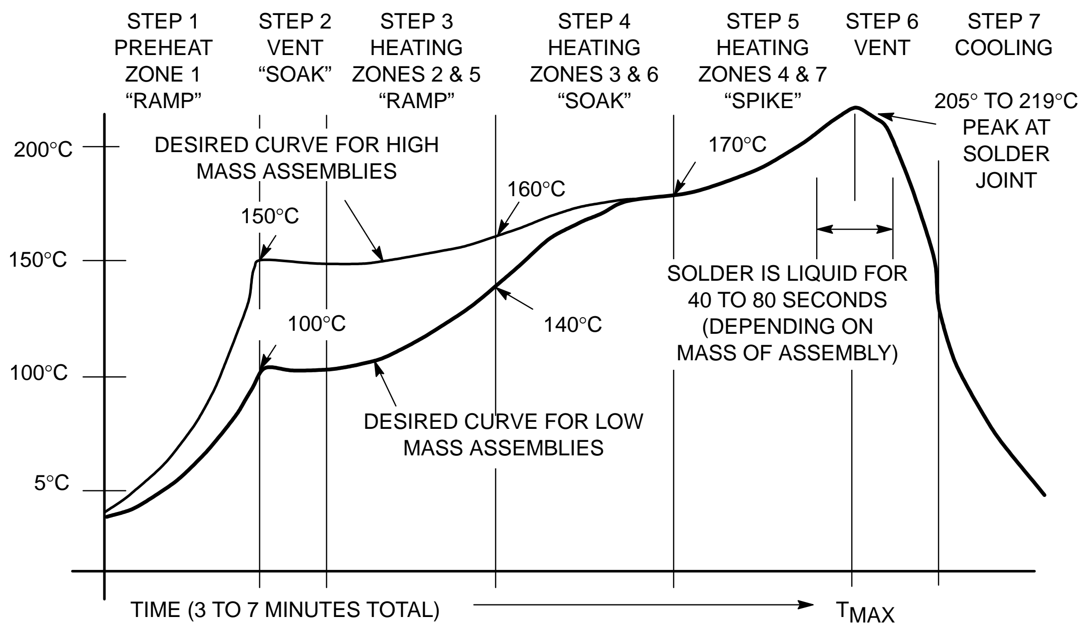



**Figure 16. Typical Solder Heating Profile**

# MMDF7N02Z

**ON Semiconductor™**

**http://onsemi.com**

## Power MOSFET 7 Amps, 20 Volts

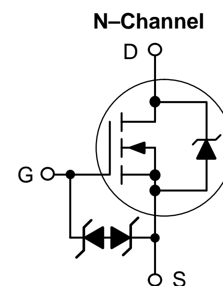
### N–Channel SO–8, Dual

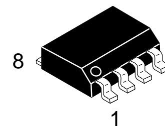
EZFETs™ are an advanced series of Power MOSFETs which contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Designed to Withstand 200 V Machine Model and 2000 V Human Body Model
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode is Characterized for use in Bridge Circuits
- Diode Exhibits High Speed, with Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**7 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 27 mΩ**

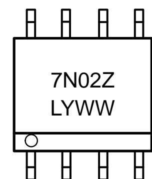
**N–Channel**



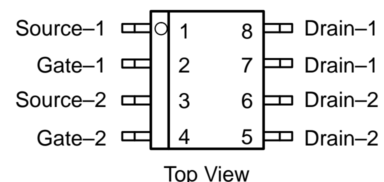

**SO–8, Dual**
**CASE 751**
**STYLE 11**

**MARKING DIAGRAM**




7N02Z = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDF7N02ZR2 | SO–8 | 2500 Tape & Reel |

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±12 | Vdc |
| Drain Current<br>Continuous @ $T_A$ = 25°C (Note 1.)<br>Continuous @ $T_A$ = 70°C (Note 1.)<br>Pulsed Drain Current (Note 3.) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>7.0<br>4.6<br>35 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Linear Derating Factor @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.0<br>16 | Watts<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Linear Derating Factor @ $T_A$ = 25°C (Note 2.) | $P_D$ | 1.39<br>11.11 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |

**THERMAL RESISTANCE**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Junction–to–Ambient (Note 1.)<br>Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | –<br>– | 62.5<br>90 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 5.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>20<br>– | <br>–<br>15 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±12 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 3.0 | µAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 4. & 5.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>0.5<br>– | <br>0.7<br>2.5 | <br>1.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 4. & 5.)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 7.0 Adc)<br>($V_{GS}$ = 2.5 Vdc, $I_D$ = 3.5 Adc) | $R_{DS(on)}$ | <br>–<br>– | <br>23<br>30 | <br>27<br>35 | mΩ |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 6.0 Adc) (Note 4.) | $g_{FS}$ | 5.0 | 11 | – | Mhos |

1. When mounted on 1″ square FR4 or G–10 board ($V_{GS}$ = 10 V, @ 10 seconds).
2. When mounted on minimum recommended FR4 or G–10 board ($V_{GS}$ = 10 V, @ Steady State).
3. Repetitive rating; pulse width limited by maximum junction temperature.
4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 450 | 630 | pF |
| Output Capacitance | | $C_{oss}$ | – | 350 | 490 | |
| Transfer Capacitance | | $C_{rss}$ | – | 110 | 155 | |
| **SWITCHING CHARACTERISTICS** (Note 7.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) (Note 6.) | $t_{d(on)}$ | – | 31 | 62 | ns |
| Rise Time | | $t_r$ | – | 230 | 460 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 725 | 1450 | |
| Fall Time | | $t_f$ | – | 780 | 1560 | |
| Gate Charge See Figure 8 | ($V_{DS}$ = 12 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc) (Note 6.) | $Q_T$ | – | 17 | 24 | nC |
| | | $Q_1$ | – | 1.4 | – | |
| | | $Q_2$ | – | 6.7 | – | |
| | | $Q_3$ | – | 6.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc) (Note 6.)<br>($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.90<br>0.84 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) (Note 6.) | $t_{rr}$ | – | 780 | – | ns |
| | | $t_a$ | – | 190 | – | |
| | | $t_b$ | – | 590 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 5.7 | – | µC |

6. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
7. Switching characteristics are independent of operating junction temperatures.

## TYPICAL ELECTRICAL CHARACTERISTICS

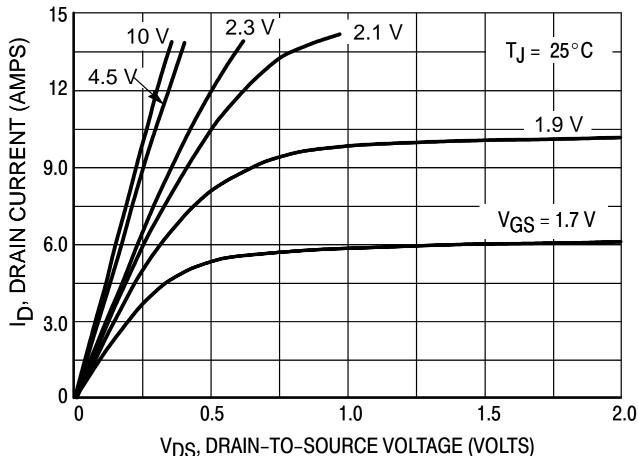


**Figure 1. On–Region Characteristics**

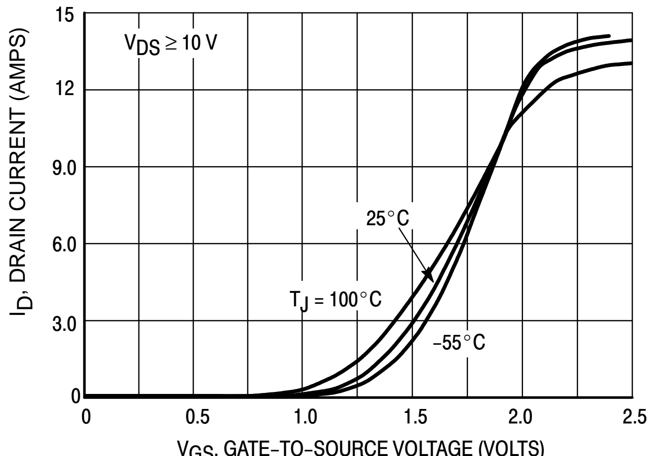


**Figure 2. Transfer Characteristics**

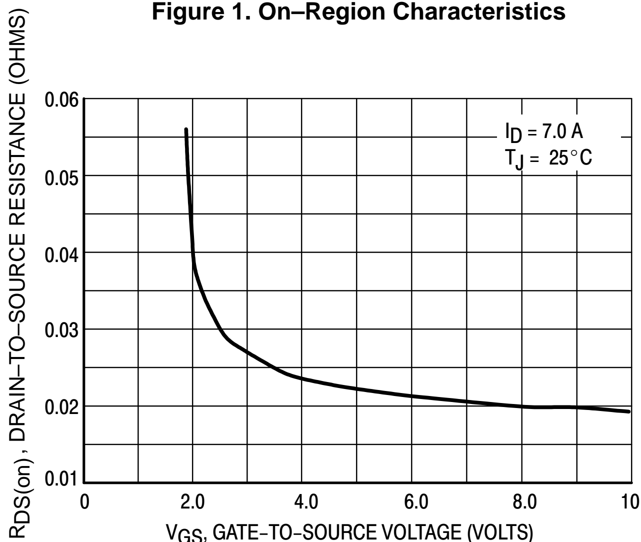


**Figure 3. On–Resistance versus Drain Current**

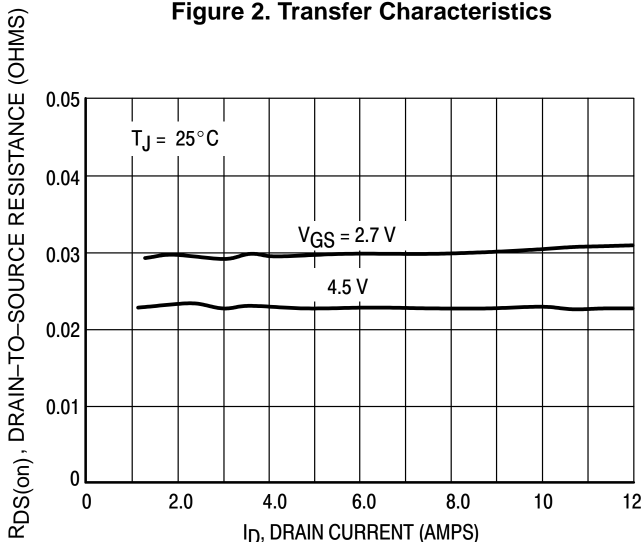


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

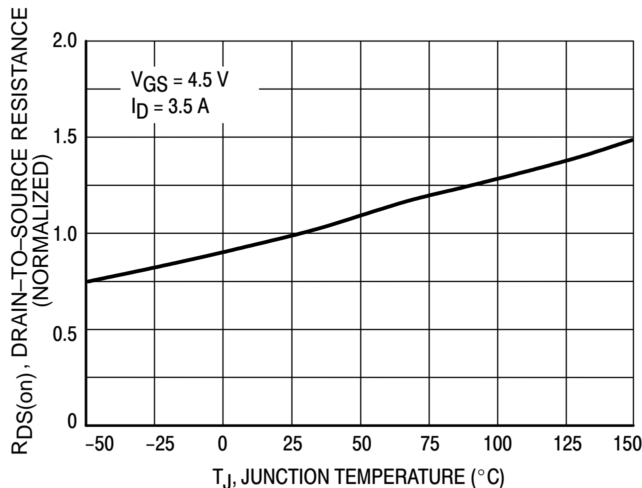


**Figure 5. On–Resistance Variation with Temperature**

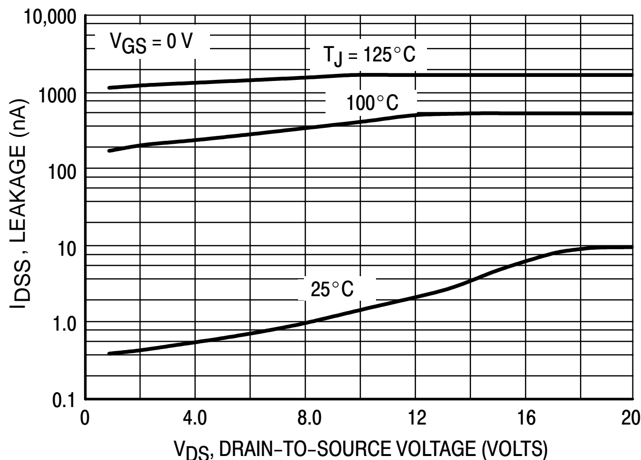


**Figure 6. Drain–To–Source Leakage Current versus Voltage**

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The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

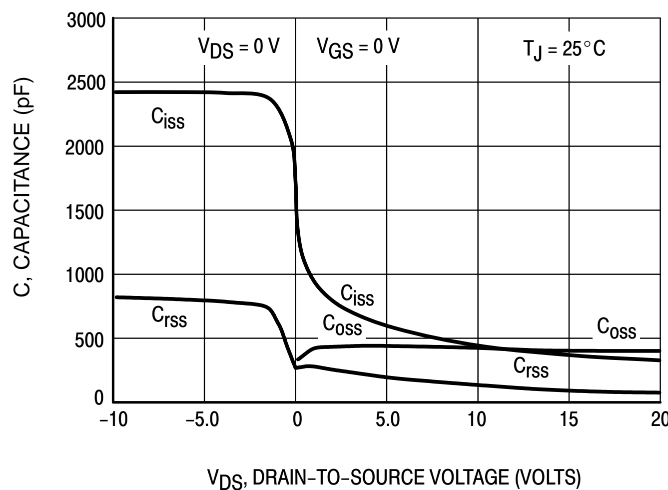



**Figure 7. Capacitance Variation**

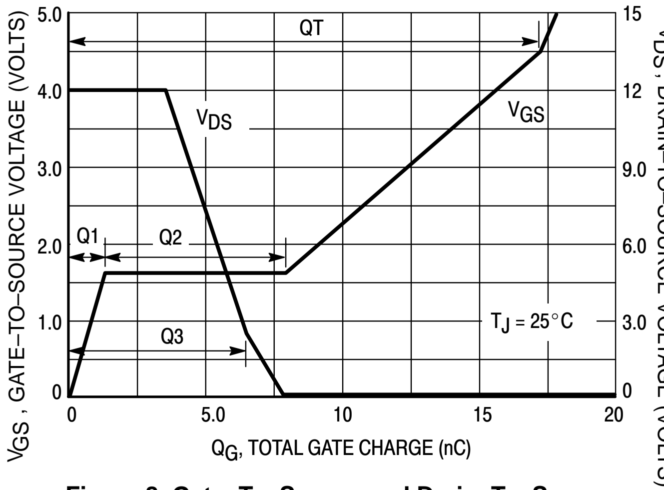



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

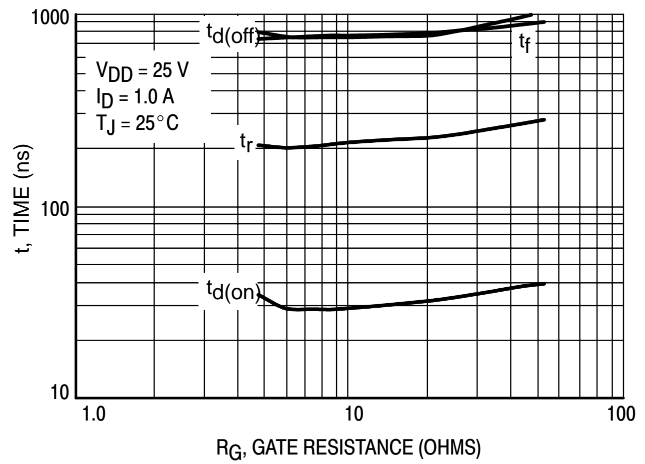



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

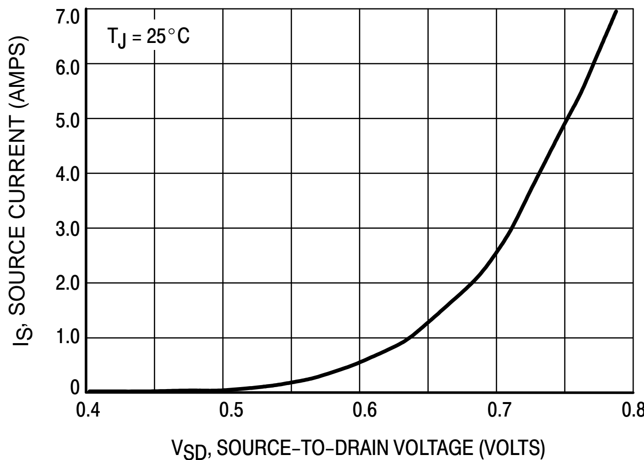



**Figure 10. Diode Forward Voltage versus Current**

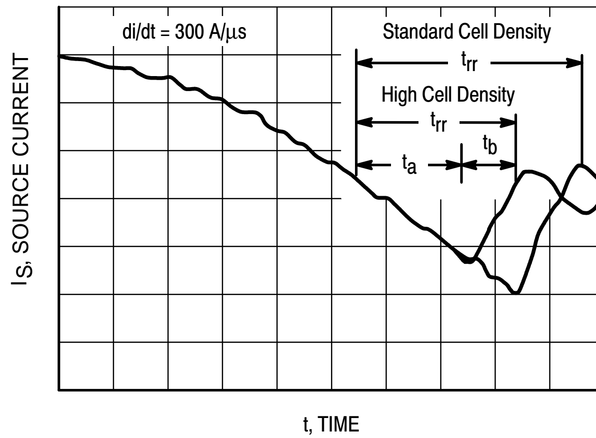



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

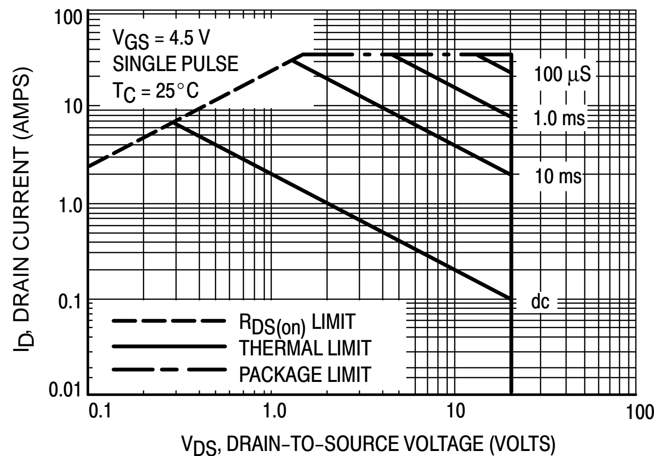



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

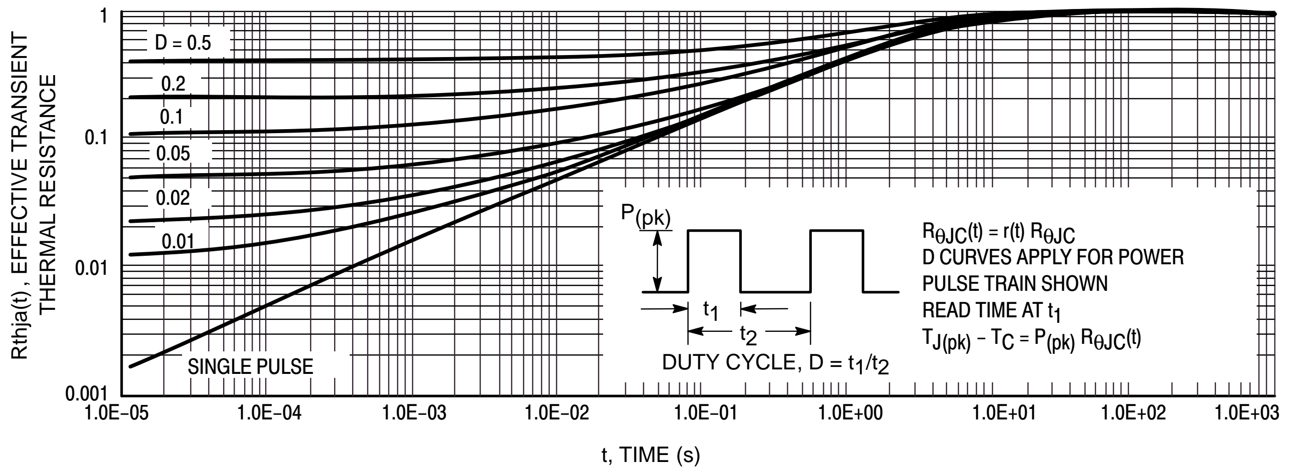



**Figure 13. Thermal Response**

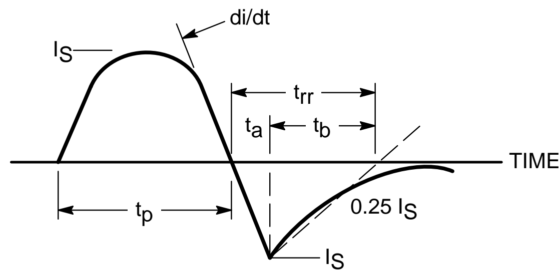
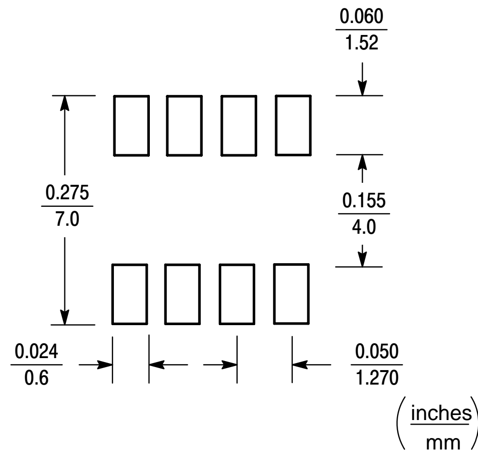



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_J(max) - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.0 Watts.

$$P_D = \frac{150^\circ C - 25^\circ C}{62.5^\circ C/W} = 2.0 \text{ Watts}$$

The 62.5°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.0 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

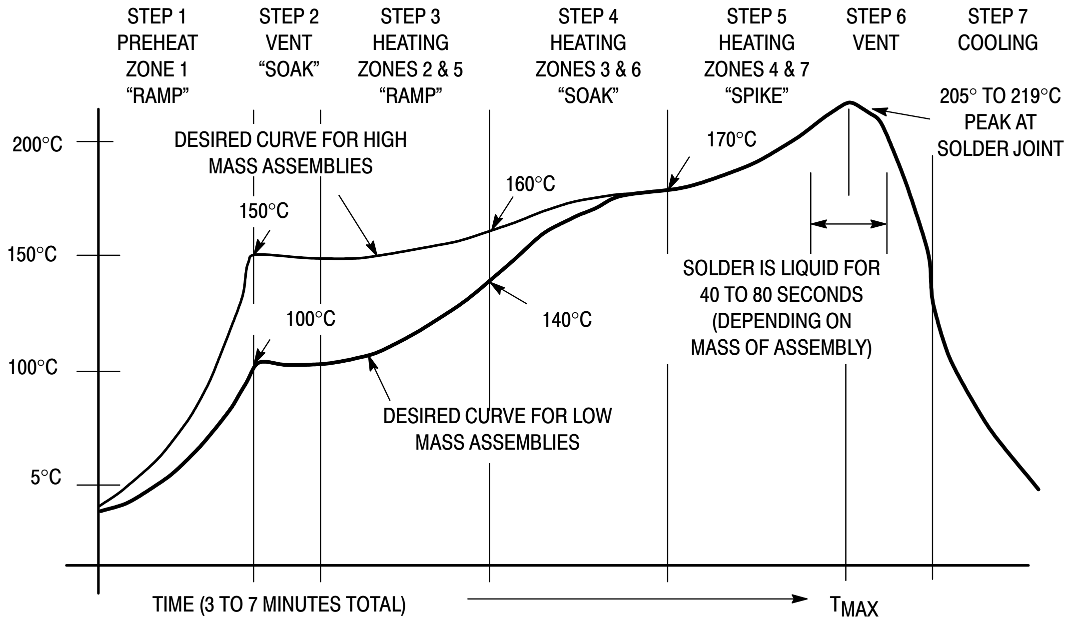



**Figure 15. Typical Solder Heating Profile**

# MMDFS2P102

# Power MOSFET
# 2 Amps, 20 Volts

## P–Channel SO–8, FETKY™

**ON Semiconductor™**

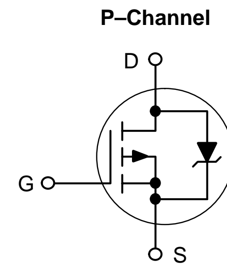
**http://onsemi.com**

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 160 mΩ**
**$V_F$ = 0.39 Volts**

The FETKY product family incorporates low $R_{DS(on)}$, true logic level MOSFETs packaged with industry leading, low forward drop, low leakage Schottky Barrier rectifiers to offer high efficiency components in a space saving configuration. Independent pinouts for MOSFET and Schottky die allow the flexibility to use a single component for switching and rectification functions in a wide variety of applications such as Buck Converter, Buck–Boost, Synchronous Rectification, Low Voltage Motor Control, and Load Management in Battery Packs, Chargers, Cell Phones and other Portable Products.

- Power MOSFET with Low $V_F$, Low $I_R$ Schottky Rectifier
- Lower Component Placement and Inventory Costs along with Board Space Savings
- Logic Level Gate Drive – Can be Driven by Logic ICs
- Mounting Information for SO–8 Package Provided
- $I_{DSS}$ Specified at Elevated Temperature
- Applications Information Provided

**P–Channel**

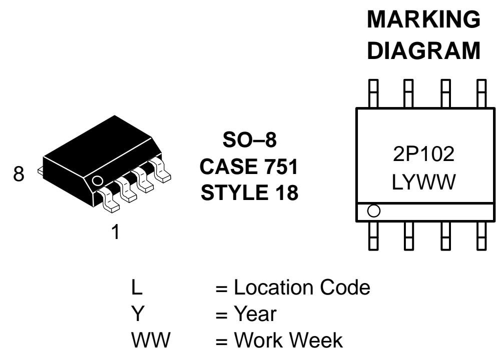



**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current (Note 3.)<br>– Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>3.3<br>2.1<br>20 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Single Pulse Drain–to–Source Avalanche Energy – STARTING $T_J$ = 25°C<br>$V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 20 Vdc, $I_L$ = 9.0 Apk, L = 10 mH, $R_G$ = 25 Ω | $E_{AS}$ | 324 | mJ |

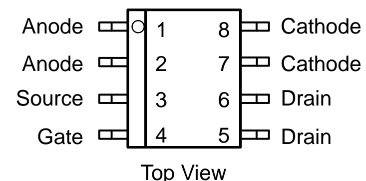
1. Negative sign for P–channel device omitted for clarity.
2. Pulse Test: Pulse Width ≤ 250 µs, Duty Cycle ≤ 2.0%.
3. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDFS2P102R2 | SO–8 | 2500 Tape & Reel |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**SCHOTTKY RECTIFIER MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 20 | Volts |
| Average Forward Current (Note 4.) (Rated $V_R$) $T_A$ = 100°C | $I_O$ | 1.0 | Amps |
| Peak Repetitive Forward Current (Note 3.) (Rated $V_R$, Square Wave, 20 kHz) $T_A$ = 105°C | $I_{frm}$ | 2.0 | Amps |
| Non–Repetitive Peak Surge Current<br>(Surge applied at rated load conditions, halfwave, single phase, 60 Hz) | $I_{fsm}$ | 20 | Amps |

**THERMAL CHARACTERISTICS – SCHOTTKY AND MOSFET**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient (Note 5.) – MOSFET | $R_{\theta JA}$ | 167 | °C/W |
| Thermal Resistance – Junction–to–Ambient (Note 6.) – MOSFET | $R_{\theta JA}$ | 100 | |
| Thermal Resistance – Junction–to–Ambient (Note 3.) – MOSFET | $R_{\theta JA}$ | 62.5 | |
| Thermal Resistance – Junction–to–Ambient (Note 5.) – Schottky | $R_{\theta JA}$ | 204 | |
| Thermal Resistance – Junction–to–Ambient (Note 6.) – Schottky | $R_{\theta JA}$ | 122 | |
| Thermal Resistance – Junction–to–Ambient (Note 4.) – Schottky | $R_{\theta JA}$ | 83 | |
| Operating and Storage Temperature Range | $T_j$, $T_{stg}$ | –55 to 150 | |

4. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.
5. Mounted with minimum recommended pad size, PC Board FR4.
6. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Steady State.

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted) (Note 7.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 25 | – | mV/°C |
| Zero Gate Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | µAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 8.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–Source Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | – | 0.118 | 0.160 | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.5 Adc) | | | – | 0.152 | 0.180 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 2.0 | 3.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 420 | 588 | pF |
| Output Capacitance | | $C_{oss}$ | – | 290 | 406 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 116 | 232 | |
| **SWITCHING CHARACTERISTICS** (Note 9.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 19 | 38 | ns |
| Rise Time | | $t_r$ | – | 66 | 132 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 25 | 50 | |
| Fall Time | | $t_f$ | – | 37 | 74 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 15 | 20 | nC |
| | | $Q_1$ | – | 1.2 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 4.0 | – | |
| **DRAIN SOURCE DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 8.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.5 | 2.1 | V |
| Reverse Recovery Time | ($I_S$ = 2.0 Adc, $V_{DD}$ = 15 V, dIS/dt = 100 A/µs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 17 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.034 | – | µC |

**SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | $T_J$ = 25°C | $T_J$ = 125°C | Unit |
|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage (Note 8.) $I_F$ = 1.0 A | $V_F$ | 0.47 | 0.39 | Volts |
| $I_F$ = 2.0 A | | 0.58 | 0.53 | |
| Maximum Instantaneous Reverse Current (Note 8.) $V_R$ = 20 V | $I_R$ | 0.05 | 10 | mA |
| Maximum Voltage Rate of Change $V_R$ = 20 V | dV/dt | 10,000 | | V/µs |

7. Negative sign for P–channel device omitted for clarity.
8. Pulse Test: Pulse Width ≤ 300 µsec, Duty Cycle ≤ 2.0%.
9. Switching characteristics are independent of operating temperature.

## TYPICAL FET ELECTRICAL CHARACTERISTICS

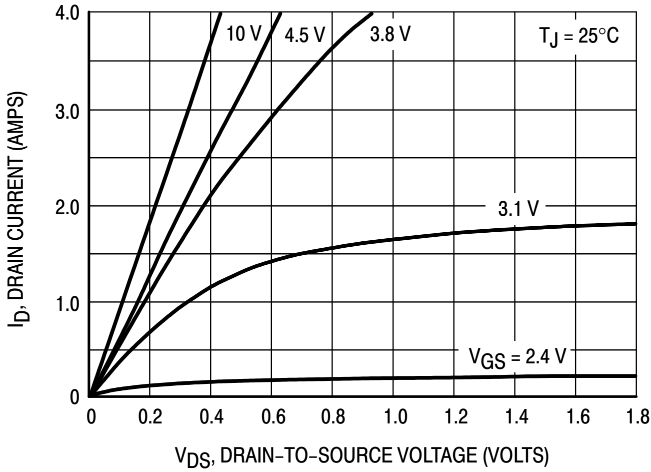



**Figure 1. On–Region Characteristics**

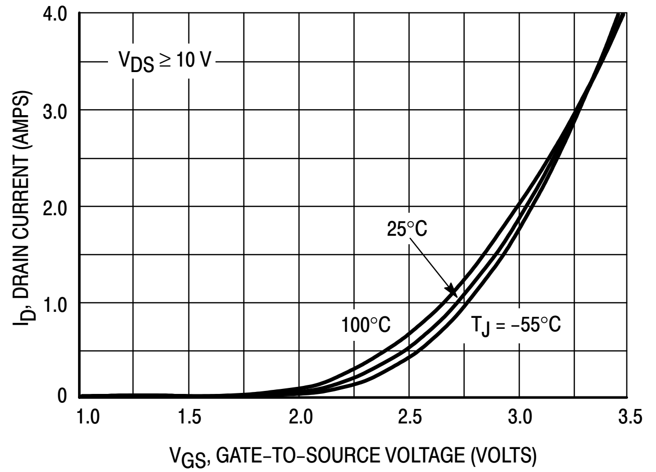



**Figure 2. Transfer Characteristics**

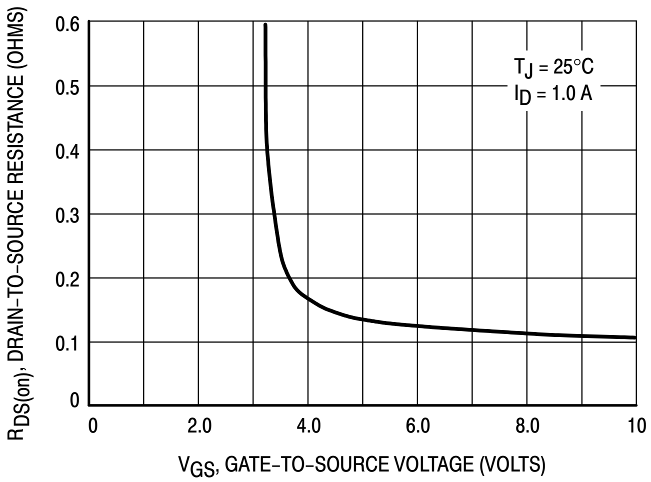



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

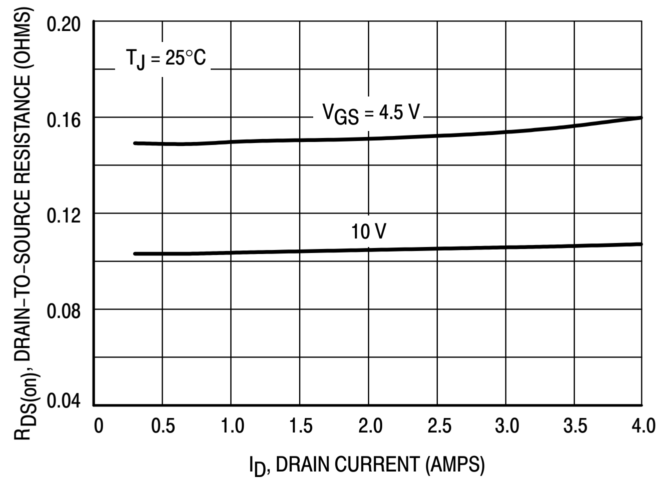



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

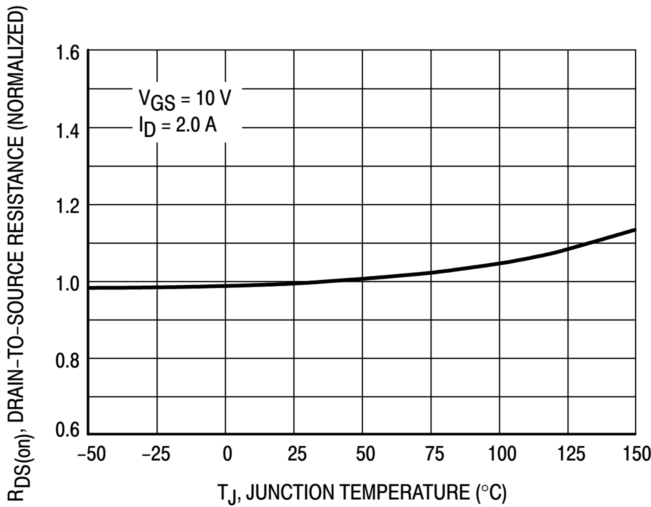



**Figure 5. On–Resistance Variation with Temperature**

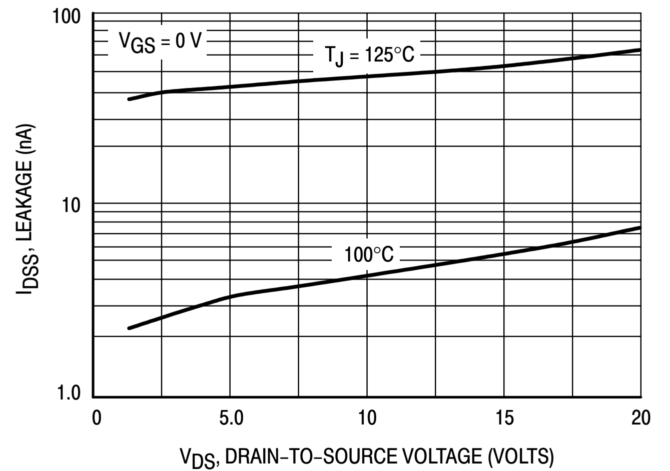



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## TYPICAL FET ELECTRICAL CHARACTERISTICS

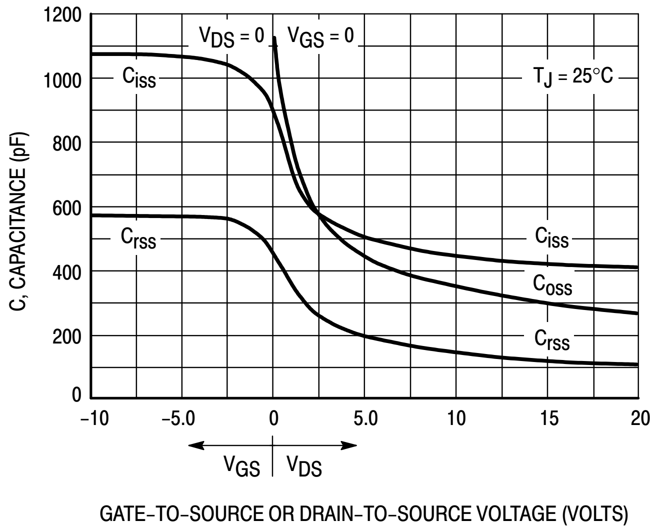



**Figure 7. Capacitance Variation**

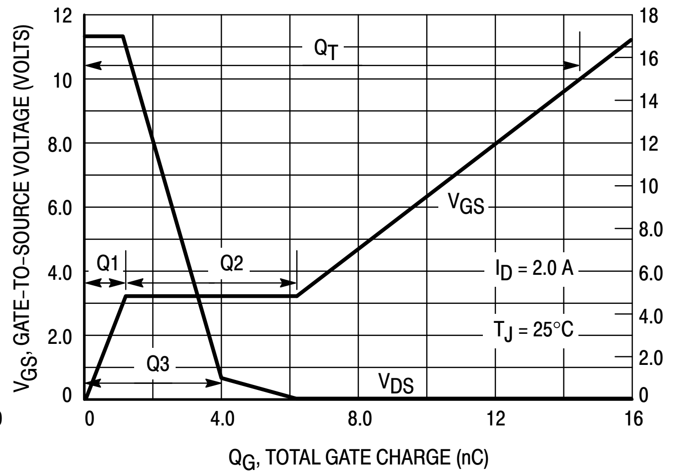



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

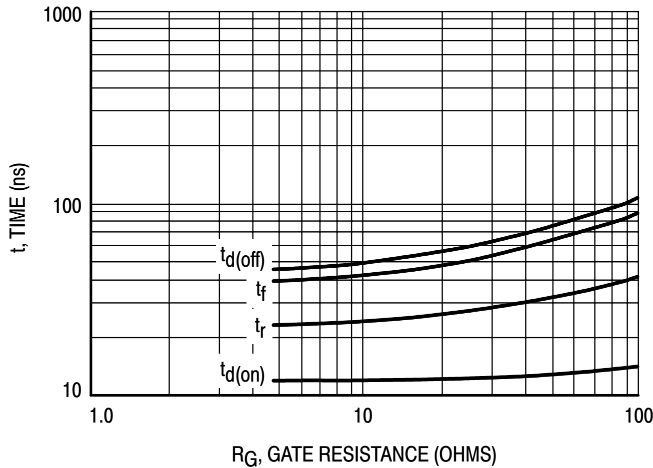



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

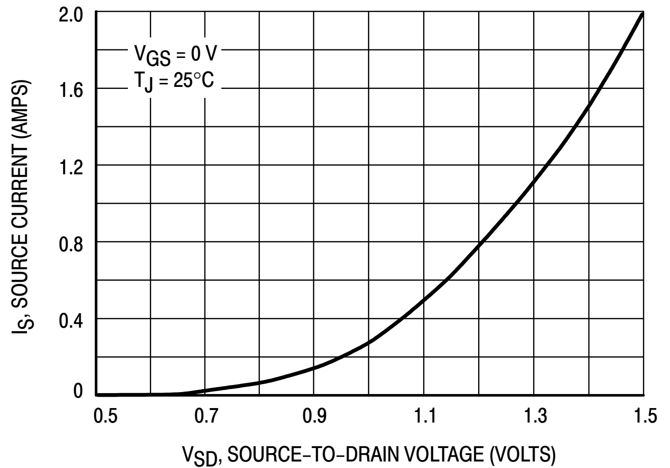



**Figure 10. Diode Forward Voltage versus Current**

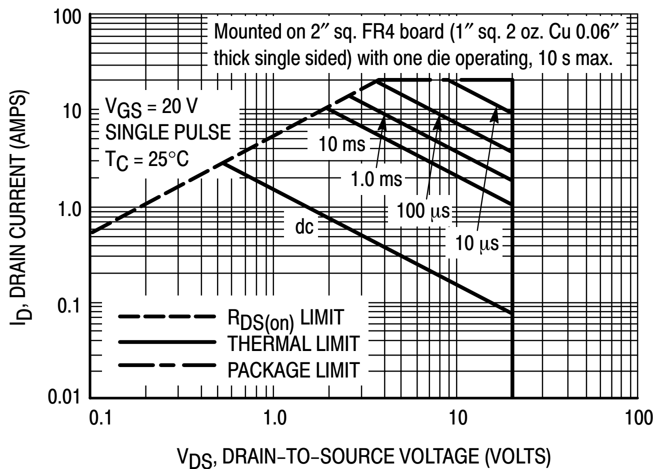



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

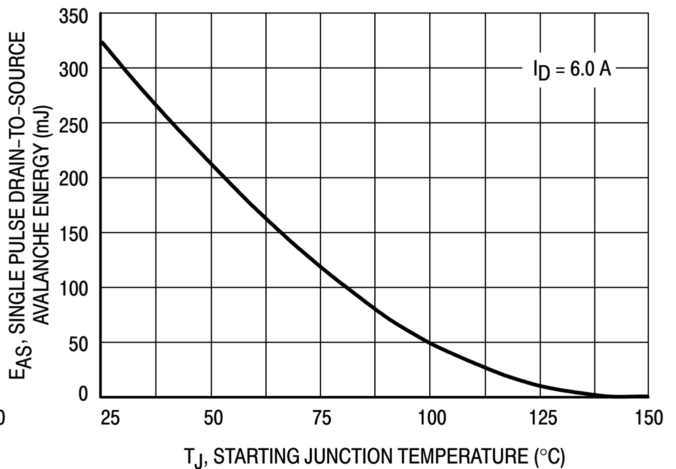



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL FET ELECTRICAL CHARACTERISTICS

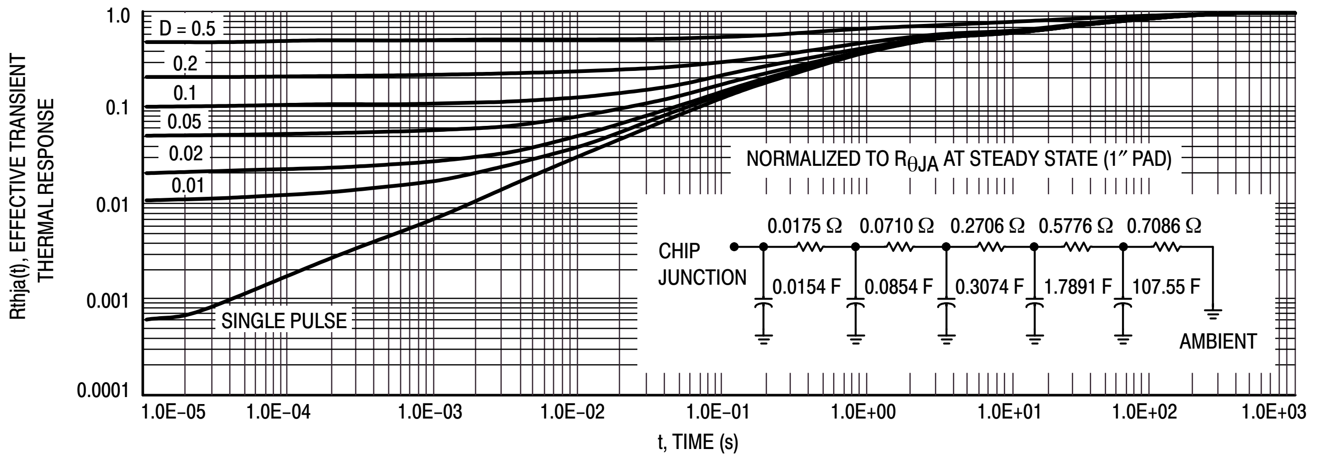



**Figure 13. FET Thermal Response**

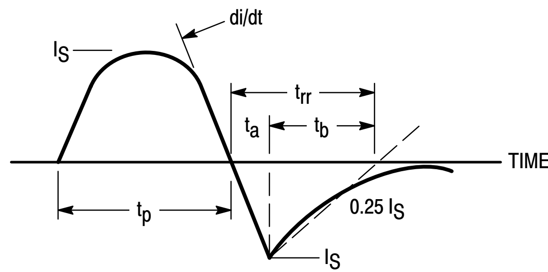



**Figure 14. Diode Reverse Recovery Waveform**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

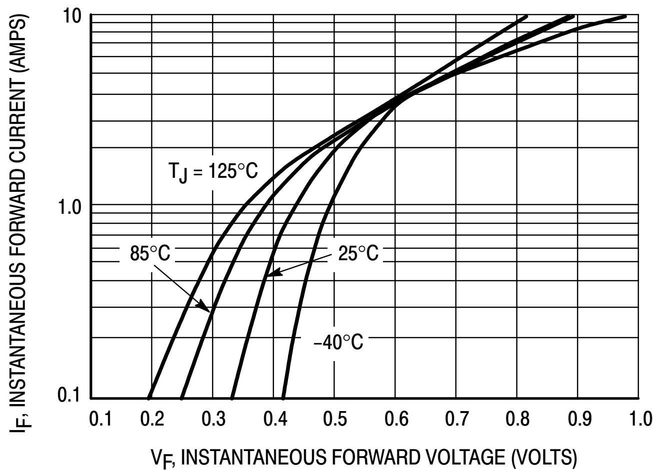



**Figure 15. Typical Forward Voltage**

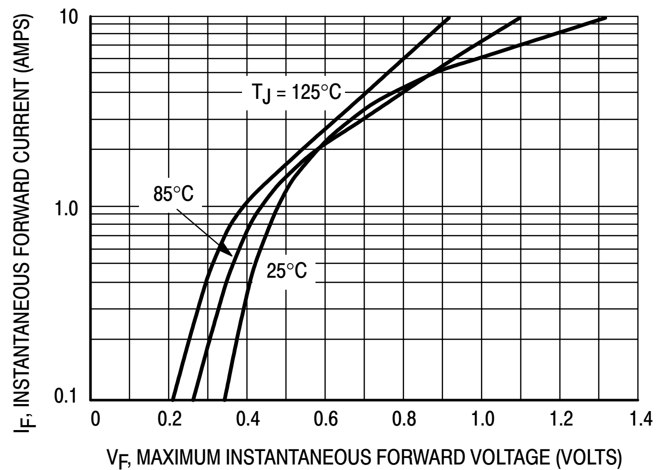



**Figure 16. Maximum Forward Voltage**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

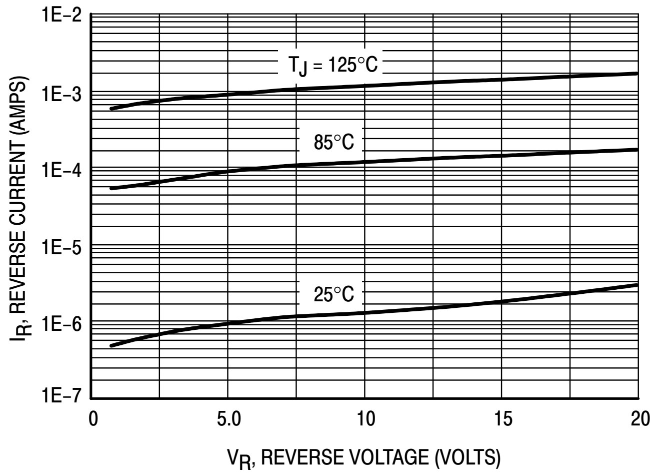



**Figure 17. Typical Reverse Current**

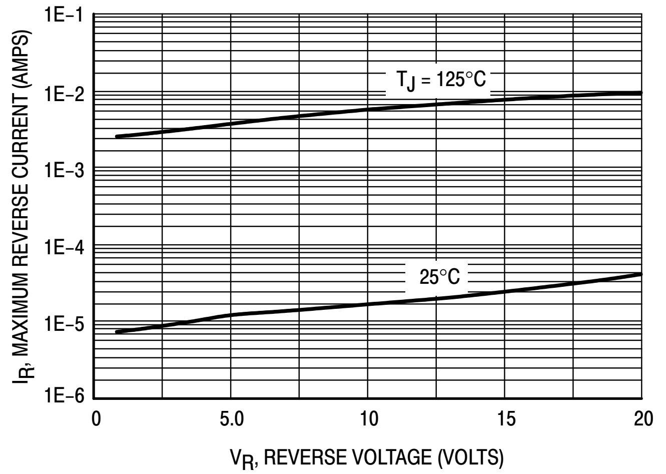



**Figure 18. Maximum Reverse Current**

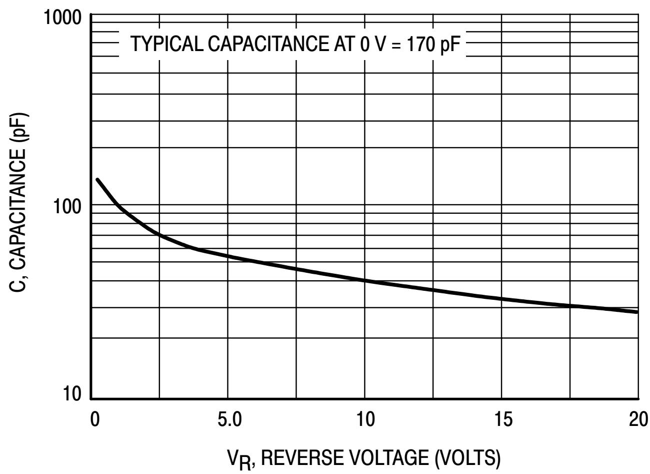



**Figure 19. Typical Capacitance**

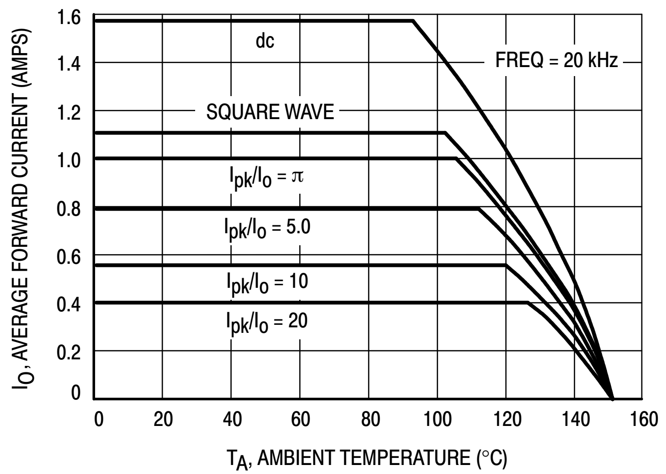



**Figure 20. Current Derating**

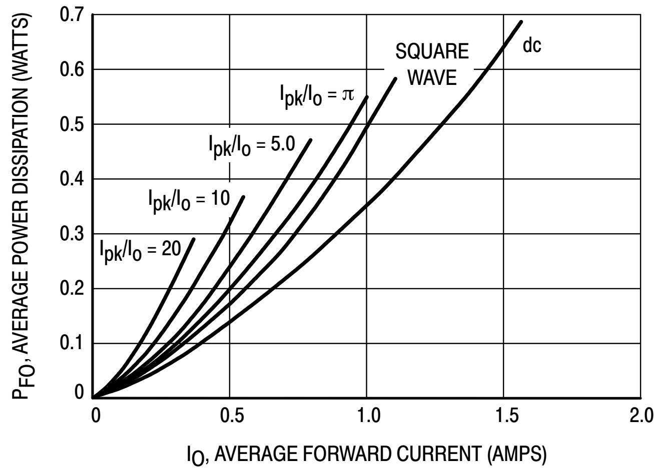



**Figure 21. Forward Power Dissipation**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

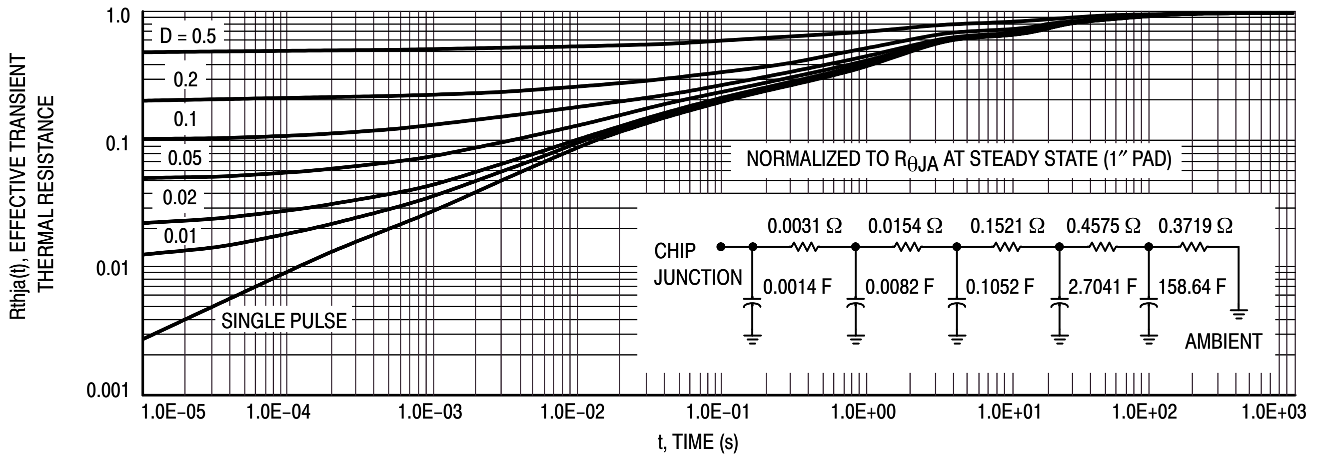
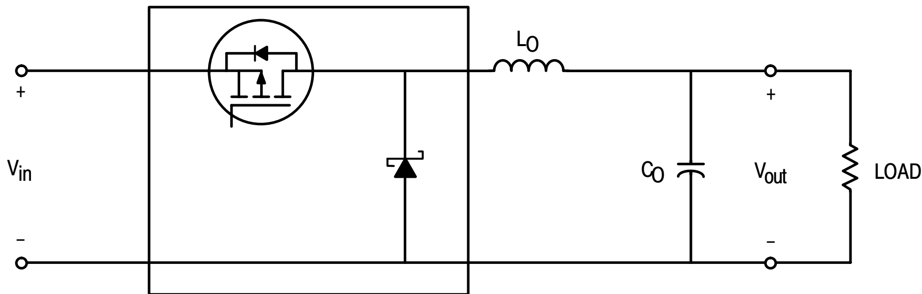


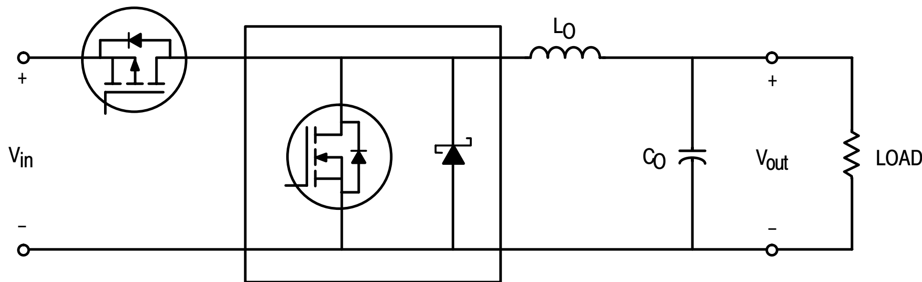

**Figure 22. Schottky Thermal Response**

## TYPICAL APPLICATIONS

## STEP DOWN SWITCHING REGULATORS



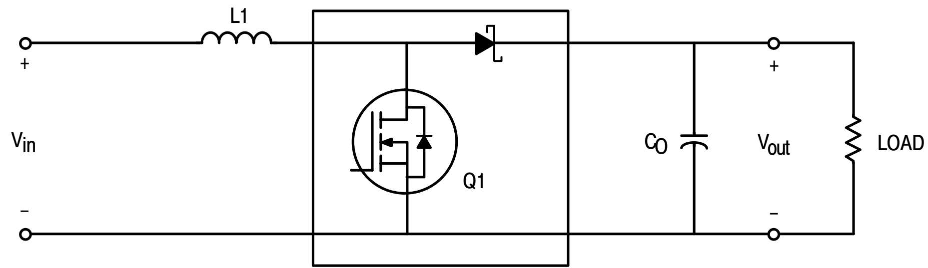

**Buck Regulator**



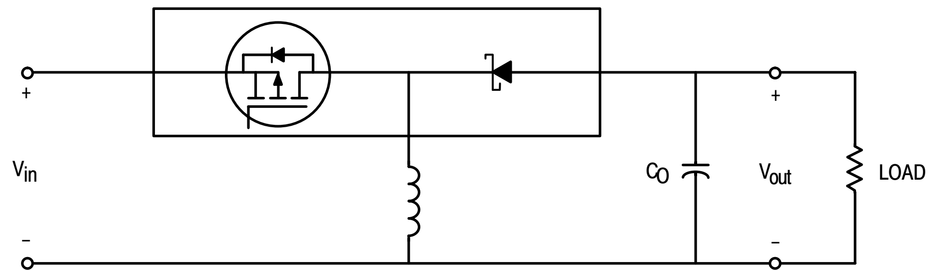

**Synchronous Buck Regulator**

## TYPICAL APPLICATIONS

### STEP UP SWITCHING REGULATORS



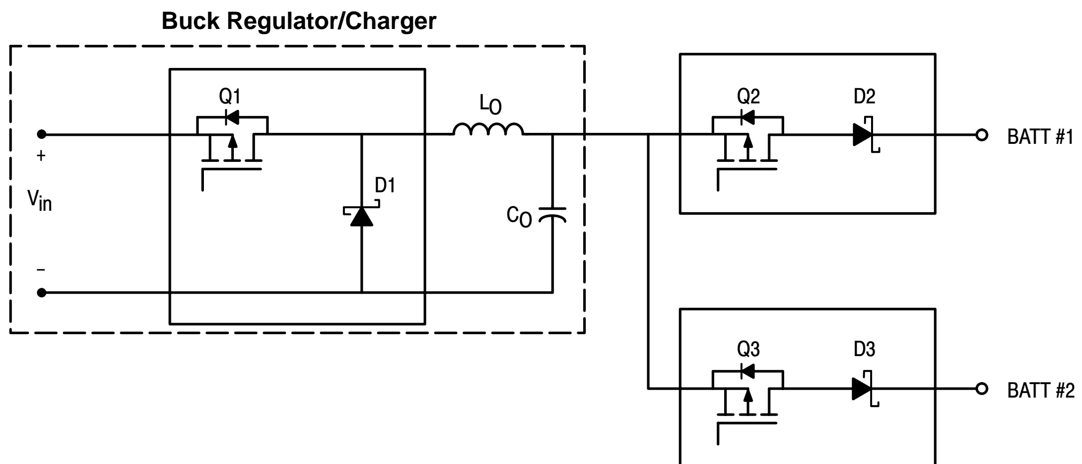

**Boost Regulator**




**Buck–Boost Regulator**

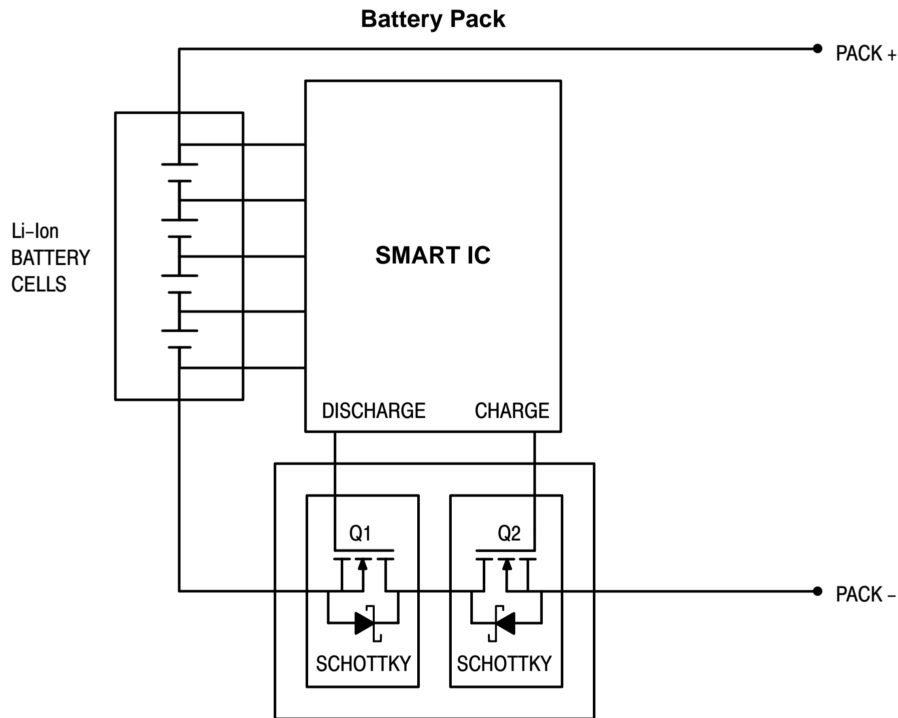
### MULTIPLE BATTERY CHARGERS

**Buck Regulator/Charger**



## TYPICAL APPLICATIONS

### Li–Ion BATTERY PACK APPLICATIONS




- Applicable in battery packs which require a high current level.
- During charge cycle Q2 is on and Q1 is off. Schottky can reduce power loss during fast charge.
- During discharge Q1 is on and Q2 is off. Again, Schottky can reduce power dissipation.
- Under normal operation, both transistors are on.

# MMDFS6N303

*Product Preview*

# Power MOSFET 6 Amps, 30 Volts

## N–Channel SO–8, FETKY™

The FETKY product family incorporates low $R_{DS(on)}$, true logic level MOSFETs packaged with industry leading, low forward drop, low leakage Schottky Barrier rectifiers to offer high efficiency components in a space saving configuration. Independent pinouts for MOSFET and Schottky die allow the flexibility to use a single component for switching and rectification functions in a wide variety of applications such as Buck Converter, Buck–Boost, Synchronous Rectification, Low Voltage Motor Control, and Load Management in Battery Packs, Chargers, Cell Phones and other Portable Products.

- Power MOSFET with Low $V_F$
- Lower Component Placement and Inventory Costs along with Board Space Savings
- Logic Level Gate Drive — Can be Driven by Logic ICs
- Mounting Information for SO–8 Package Provided
- Applications Information Provided
- R2 Suffix for Tape and Reel (2500 units/13″ reel)
- Marking: 6N303

**MOSFET MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage — Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current (Note 2.)<br>– Continuous @ $T_A$ = 25°C<br>– Single Pulse (tp ≤ 10 μs) | <br>$I_D$<br>$I_{DM}$ | <br>6.0<br>30 | <br>Adc<br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.0 | Watts |
| Single Pulse Drain–to–Source Avalanche Energy — Startin $T_J$ = 25°C<br>$V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, $V_{DS}$ = 20 Vdc, $I_L$ = 9.0 Apk, L = 10 mH, $R_G$ = 25 Ω | $E_{AS}$ | 325 | mJ |

1. Pulse Test: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2.0%.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

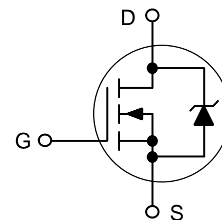
This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

**ON Semiconductor™**

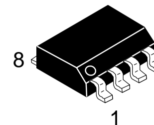
http://onsemi.com

**6 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 35 mΩ**
**$V_F$ = 0.42 Volts**

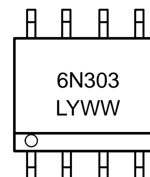
**N–Channel**




**MARKING DIAGRAM**

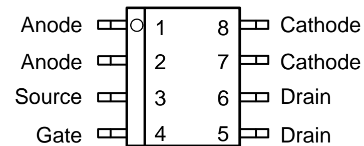



**SO–8**
**CASE 751**
**STYLE 18**




6N303 = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMDFS6N303R2 | SO–8 | 2500 Tape & Reel |

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**SCHOTTKY RECTIFIER MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Peak Repetitive Reverse Voltage<br>DC Blocking Voltage | $V_{RRM}$<br>$V_R$ | 30 | Volts |
| Average Forward Current (Note 3.)<br>(Rated $V_R$) $T_A$ = 104°C | $I_O$ | 2.0 | Amps |
| Peak Repetitive Forward Current (Note 3.)<br>(Rated $V_R$, Square Wave, 20 kHz) $T_A$ = 108°C | $I_{frm}$ | 4.0 | Amps |
| Non–Repetitive Peak Surge Current<br>(Surge applied at rated load conditions, halfwave, single phase, 60 Hz) | $I_{fsm}$ | 30 | Amps |

**THERMAL CHARACTERISTICS — SCHOTTKY AND MOSFET**

| Characteristic | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance — Junction–to–Ambient (Note 4.) — MOSFET | $R_{\theta JA}$ | 167 | °C/W |
| Thermal Resistance — Junction–to–Ambient (Note 5.) — MOSFET | $R_{\theta JA}$ | 97 | |
| Thermal Resistance — Junction–to–Ambient (Note 2.) — MOSFET | $R_{\theta JA}$ | 62.5 | |
| Thermal Resistance — Junction–to–Ambient (Note 4.) — Schottky | $R_{\theta JA}$ | 197 | |
| Thermal Resistance — Junction–to–Ambient (Note 5.) — Schottky | $R_{\theta JA}$ | 97 | |
| Thermal Resistance — Junction–to–Ambient (Note 3.) — Schottky | $R_{\theta JA}$ | 62.5 | |
| Operating and Storage Temperature Range | $T_j$, $T_{stg}$ | –55 to 150 | |

**MOSFET ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 6.)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mA)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>30<br>— | <br>—<br>— | <br>—<br>— | <br>Vdc<br>mV/°C |
| Zero Gate Drain Current<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>—<br>— | <br>—<br>— | <br>1.0<br>20 | µAdc |
| Gate Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | — | — | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 6.) | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>1.0<br>— | <br>—<br>— | <br>—<br>— | Vdc |
| Static Drain–Source Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 5.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.9 Adc) | $R_{DS(on)}$ | <br>—<br>— | <br>28<br>42 | <br>35<br>50 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc) | $g_{FS}$ | — | 9.0 | — | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | — | 430 | 600 | pF |
| Output Capacitance ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{oss}$ | — | 217 | 300 | |
| Reverse Transfer Capacitance ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{rss}$ | — | 67.5 | 135 | |

3. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.
4. Mounted with minimum recommended pad size, PC Board FR4.
5. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), Steady State.
6. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

**MOSFET ELECTRICAL CHARACTERISTICS – continued** ($T_C$ = 25°C unless otherwise noted) (Note 7.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SWITCHING CHARACTERISTICS** (Note 8.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | — | 8.2 | 16.5 | ns |
| Rise Time | | $t_r$ | — | 8.5 | 17 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | — | 89.6 | 179 | |
| Fall Time | | $t_f$ | — | 61.1 | 122 | |
| Gate Charge | ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | — | 15.7 | 31.4 | nC |
| | | $Q_1$ | — | 2.0 | — | |
| | | $Q_2$ | — | 4.6 | — | |
| | | $Q_3$ | — | 3.9 | — | |
| **DRAIN SOURCE DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 7.) | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | — | 0.77 | 1.2 | Vdc |
| Reverse Recovery Time | ($V_{GS}$ = 0 V, $I_S$ = 5.0 A, dIS/dt = 100 A/µs) | $t_{rr}$ | — | 54.5 | — | ns |
| | | $t_a$ | — | 14.8 | — | |
| | | $t_b$ | — | 39.7 | — | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | — | 0.048 | — | µC |

**SCHOTTKY RECTIFIER ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | | | Unit |
|---|---|---|---|---|
| Maximum Instantaneous Forward Voltage (Note 7.) | $V_F$ | **$T_J$ = 25°C** | **$T_J$ = 125°C** | Volts |
| $I_F$ = 100 mAdc | | 0.28 | 0.13 | |
| $I_F$ = 3.0 Adc | | 0.42 | 0.33 | |
| $I_F$ = 6.0 Adc | | 0.50 | 0.45 | |
| Maximum Instantaneous Reverse Current (Note 7.) $V_R$ = 30 V | $I_R$ | **$T_J$ = 25°C** | **$T_J$ = 125°C** | µA |
| | | 250 | — | |
| | | — | 25 | mA |
| Maximum Voltage Rate of Change $V_R$ = 30 V | dV/dt | 10,000 | | V/µs |

7. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.
8. Switching characteristics are independent of operating junction temperature.

## TYPICAL FET ELECTRICAL CHARACTERISTICS

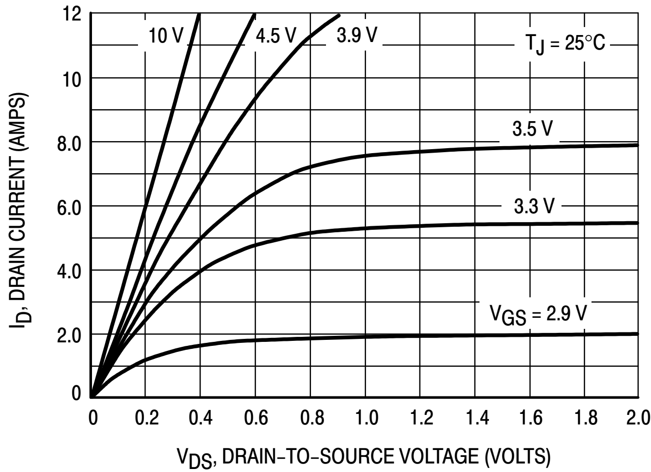



**Figure 1. On−Region Characteristics**

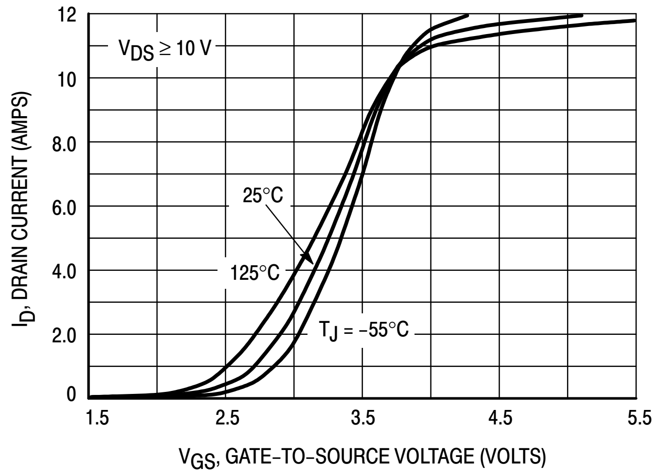



**Figure 2. Transfer Characteristics**

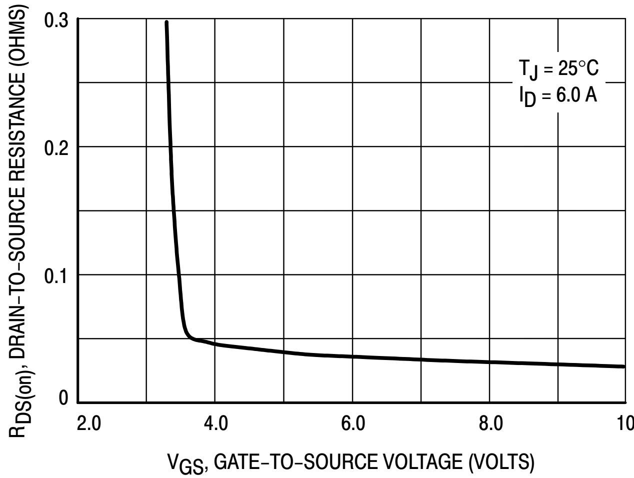



**Figure 3. On−Resistance versus Gate−To−Source Voltage**

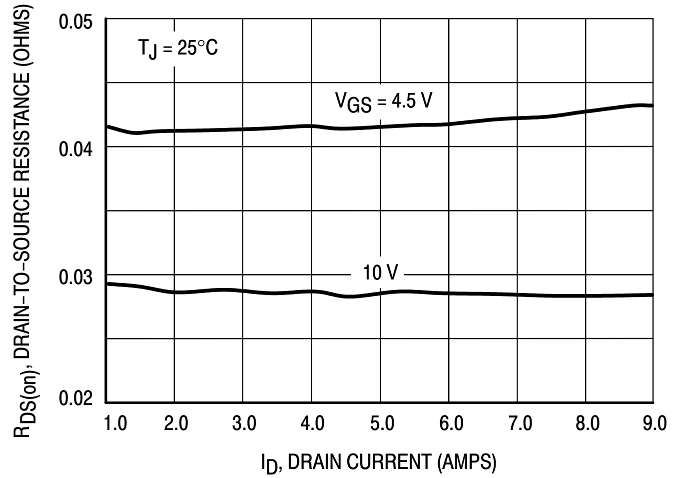



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

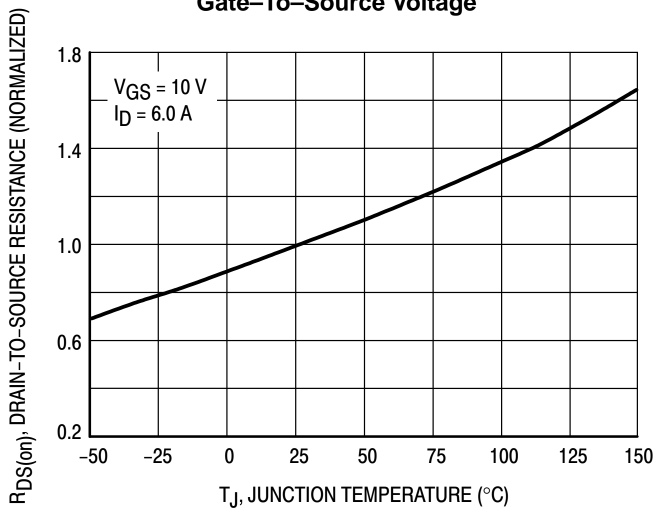



**Figure 5. On−Resistance Variation with Temperature**

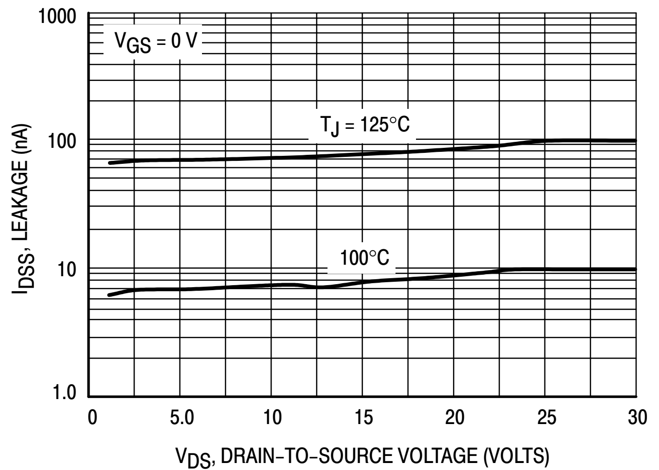



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## TYPICAL FET ELECTRICAL CHARACTERISTICS

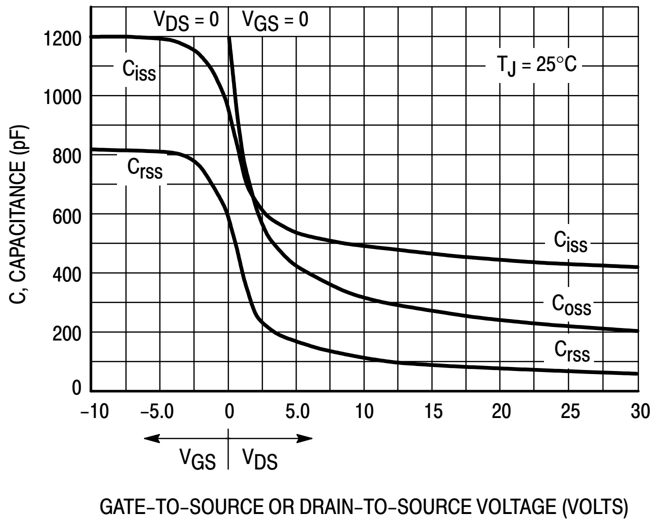



**Figure 7. Capacitance Variation**

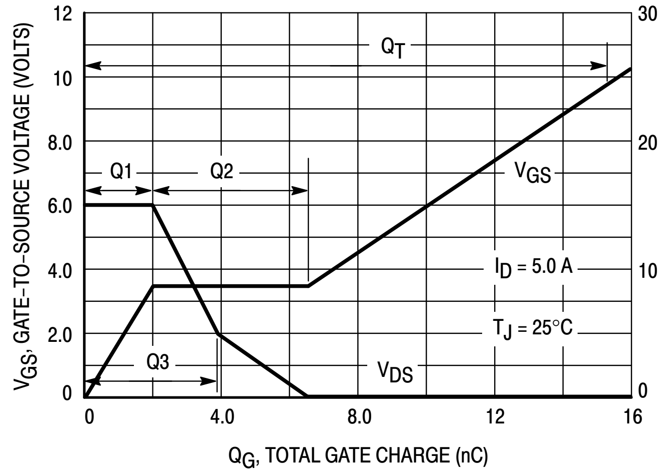



**Figure 8. Gate−To−Source and Drain−To−Source Voltage versus Total Charge**

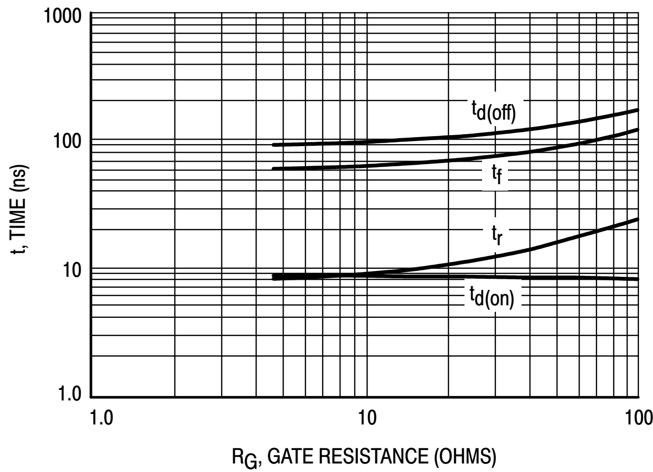



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

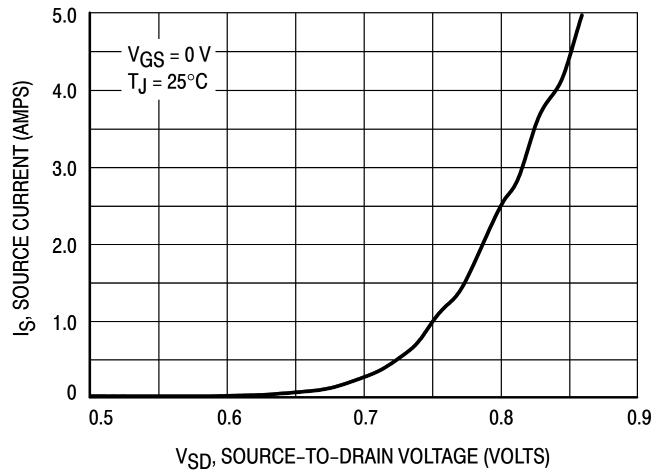



**Figure 10. Diode Forward Voltage versus Current**

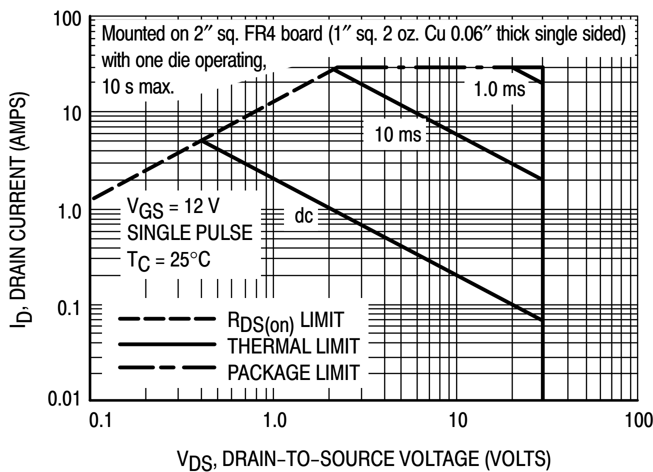



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

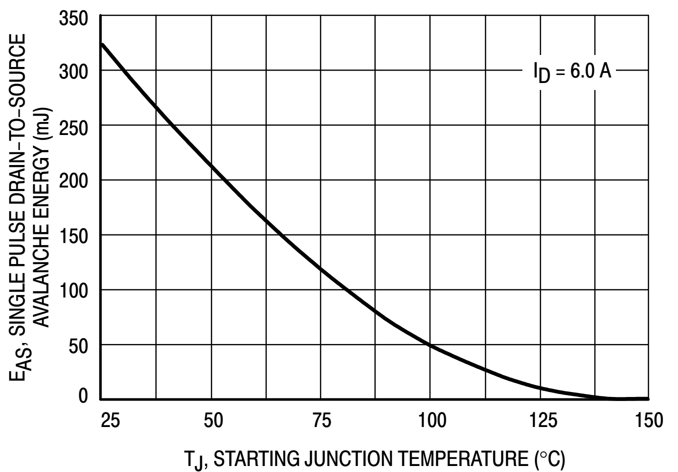



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL FET ELECTRICAL CHARACTERISTICS

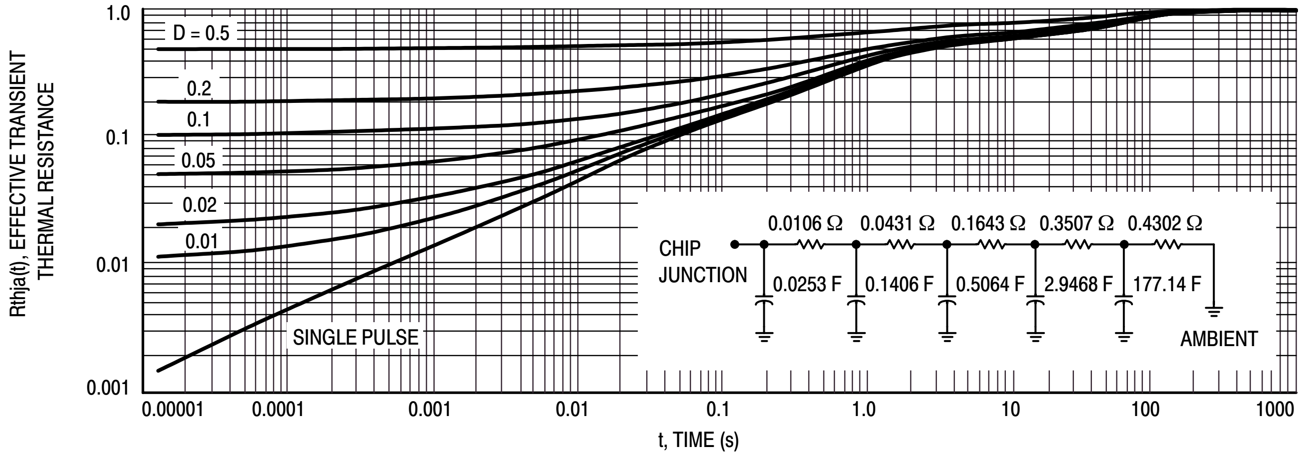



**Figure 13. FET Thermal Response**

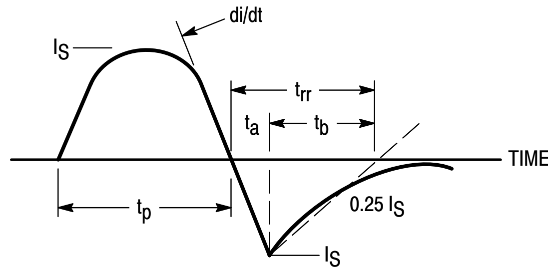



**Figure 14. Diode Reverse Recovery Waveform**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

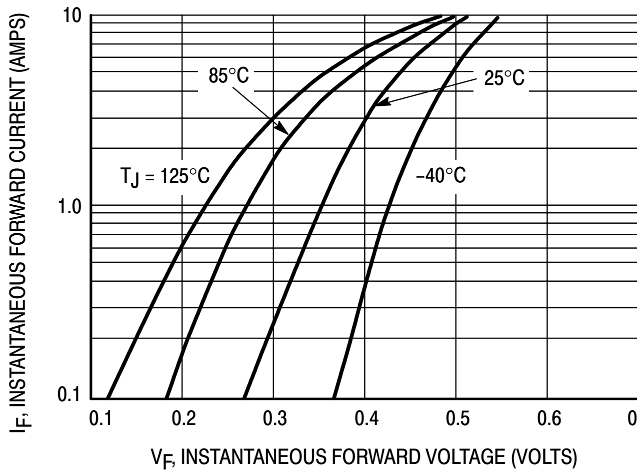



**Figure 15. Typical Forward Voltage**

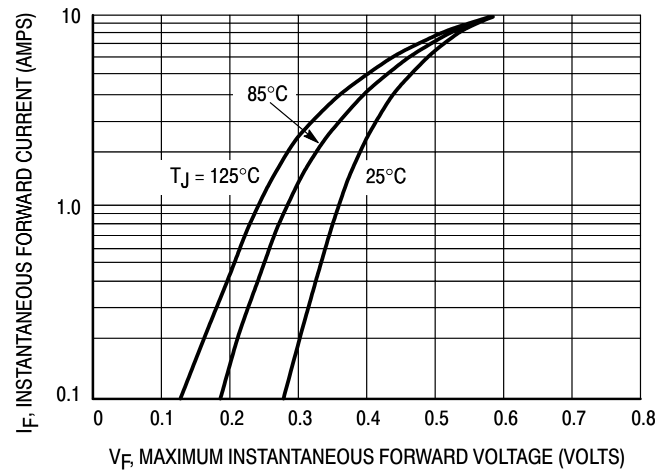



**Figure 16. Maximum Forward Voltage**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

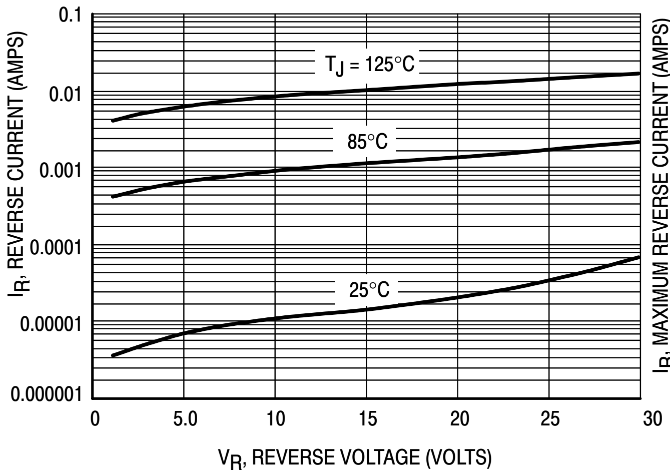



**Figure 17. Typical Reverse Current**

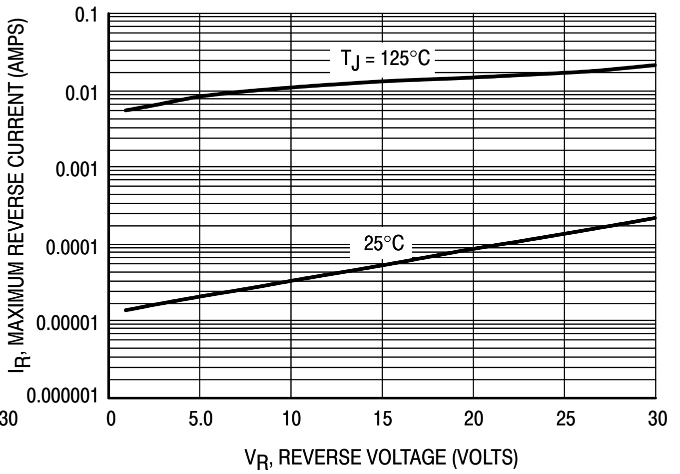



**Figure 18. Maximum Reverse Current**

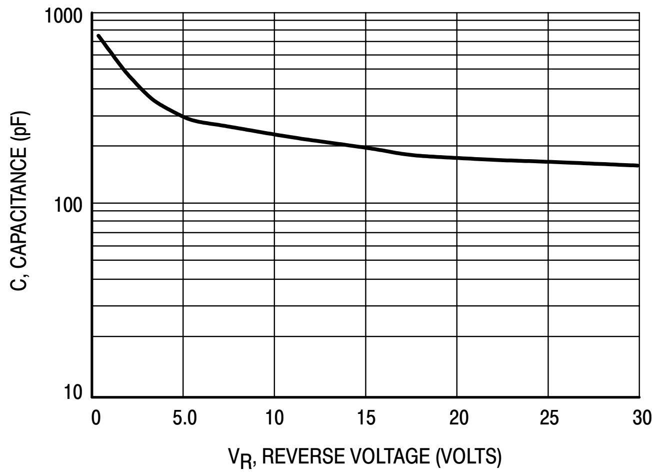



**Figure 19. Typical Capacitance**

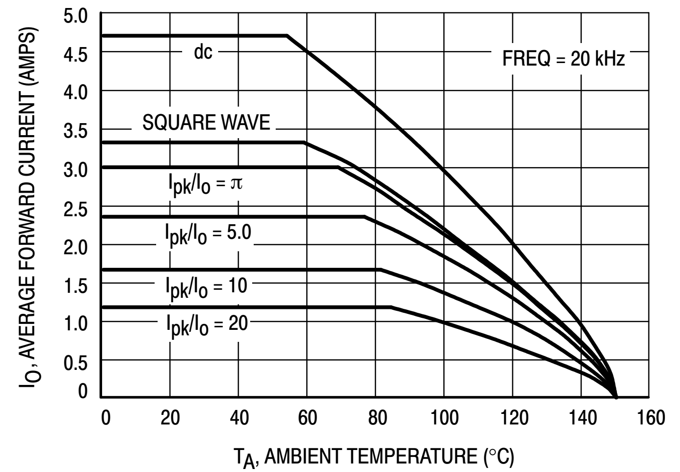



**Figure 20. Current Derating**

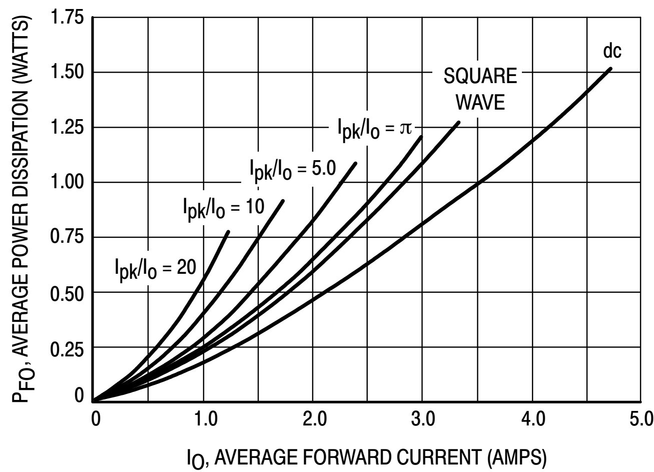



**Figure 21. Forward Power Dissipation**

## TYPICAL SCHOTTKY ELECTRICAL CHARACTERISTICS

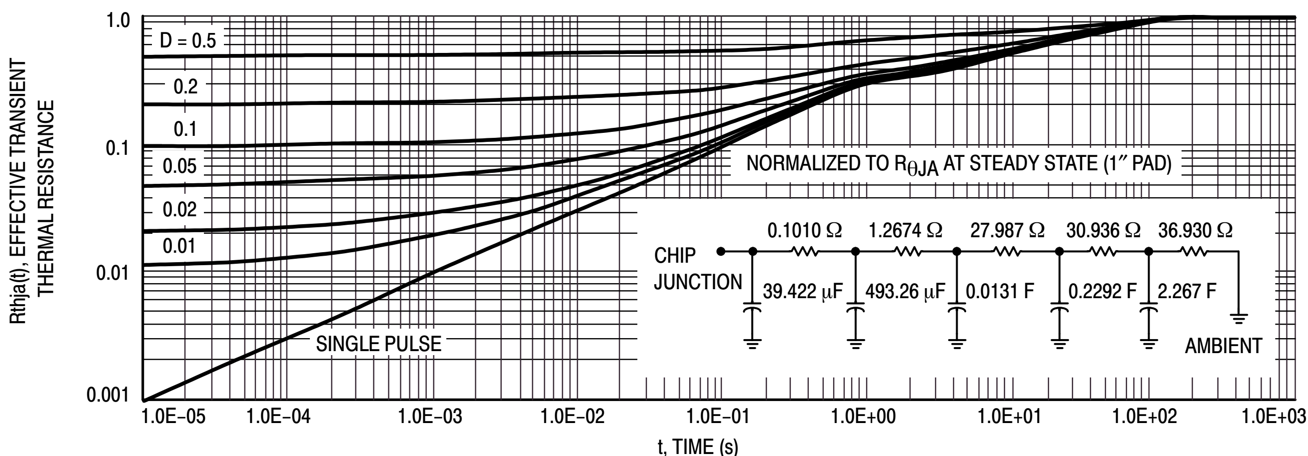
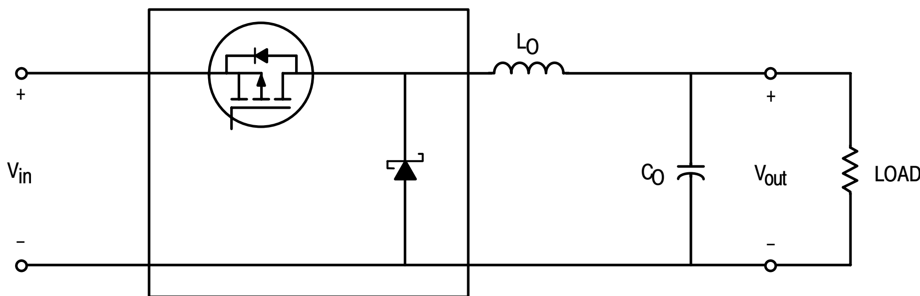


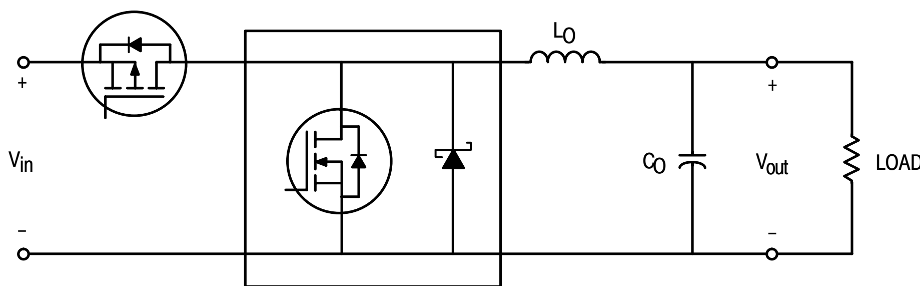

**Figure 22. Schottky Thermal Response**

## TYPICAL APPLICATIONS

## STEP DOWN SWITCHING REGULATORS



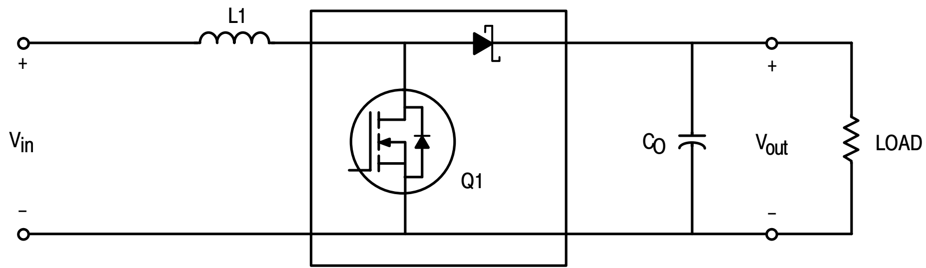

**Buck Regulator**



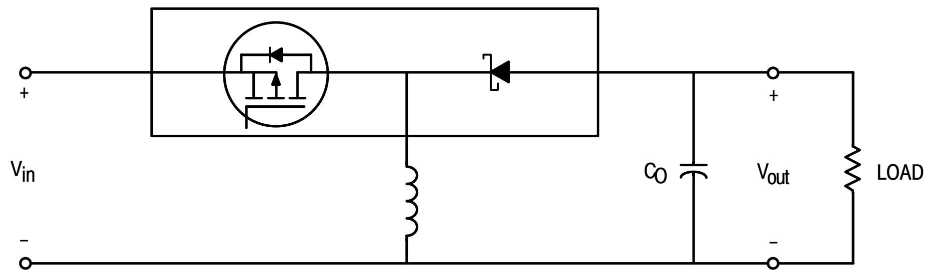

**Synchronous Buck Regulator**

## TYPICAL APPLICATIONS

### STEP UP SWITCHING REGULATORS



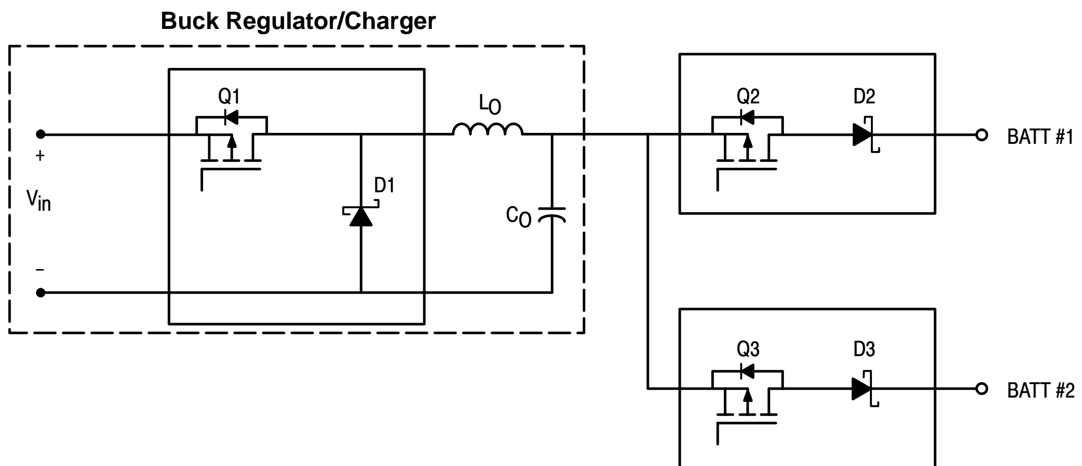

Boost Regulator




Buck–Boost Regulator

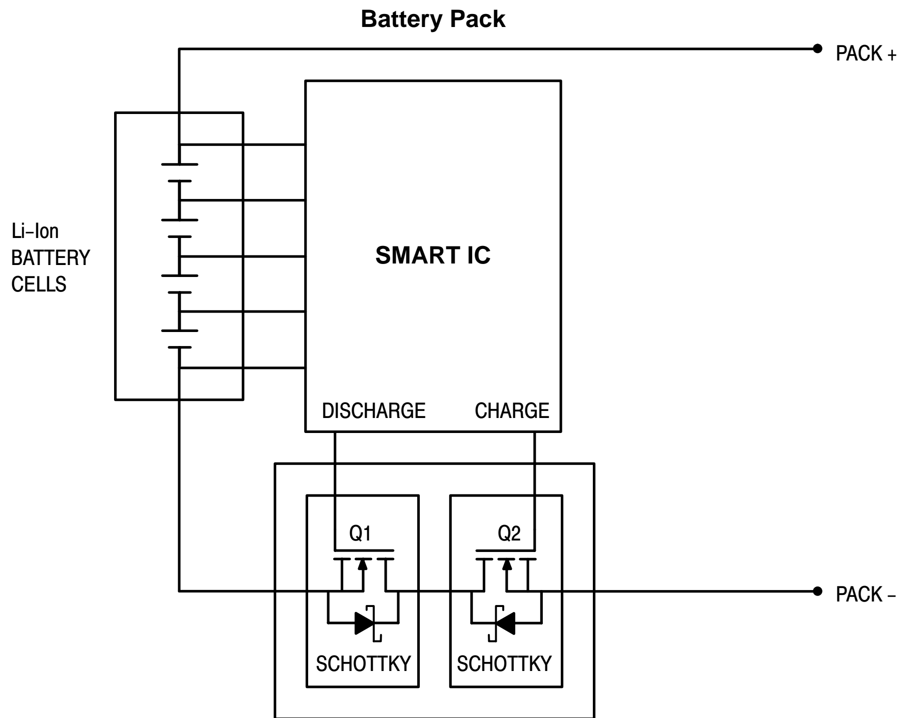
### MULTIPLE BATTERY CHARGERS

Buck Regulator/Charger



## TYPICAL APPLICATIONS

### Li–Ion BATTERY PACK APPLICATIONS




- Applicable in battery packs which require a high current level.
- During charge cycle Q2 is on and Q1 is off. Schottky can reduce power loss during fast charge.
- During discharge Q1 is on and Q2 is off. Again, Schottky can reduce power dissipation.
- Under normal operation, both transistors are on.

# MMFT107T1

Preferred Device

# Power MOSFET 250 mA, 200 Volts

## N–Channel SOT–223

**ON Semiconductor™**

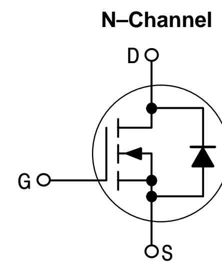
http://onsemi.com

**250 mA**
**200 VOLTS**
**$R_{DS(on)}$ = 14 Ω**

This Power MOSFET is designed for high speed, low loss power switching applications such as switching regulators, dc–dc converters, solenoid and relay drivers. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement
- The SOT–223 Package can be soldered using wave or reflow. The formed leads absorb thermal stress during soldering eliminating the possibility of damage to the die.

**N–Channel**




**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

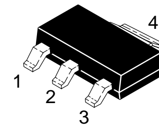
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 200 | Volts |
| Gate–to–Source Voltage – Non–Repetitive | $V_{GS}$ | ±20 | Volts |
| Drain Current | $I_D$ | 250 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Derate above 25°C | $P_D$ | 0.8<br>6.4 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |

**THERMAL CHARACTERISTICS**

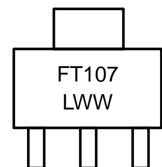
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 156 | °C/W |
| Maximum Temperature for Soldering Purposes<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

1. Device mounted on FR–4 glass epoxy printed circuit using minimum recommended footprint.

**MARKING DIAGRAM**

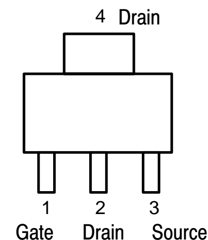



**TO–261AA**
**CASE 318E**
**STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT107T1 | SOT–223 | 1000 Tape & Reel |
| MMFT107T3 | SOT–223 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 200 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 130 V, $V_{GS}$ = 0) | | $I_{DSS}$ | – | – | 30 | nAdc |
| Gate–Body Leakage Current – Reverse ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 10 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 1.0 | – | 3.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 200 mA) | | $R_{DS(on)}$ | – | – | 14 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 V, $I_D$ = 200 mA) | | $V_{DS(on)}$ | – | – | 2.8 | Vdc |
| Forward Transconductance ($V_{DS}$ = 25 V, $I_D$ = 250 mA) | | $g_{fs}$ | – | 300 | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 60 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 30 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 6.0 | – | |
| **SOURCE DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Diode Forward Voltage | ($V_{GS}$ = 0, $I_S$ = 250 mA) | $V_F$ | – | 0.8 | – | V |
| Continuous Source Current, Body Diode | | $I_S$ | – | – | 250 | mA |
| Pulsed Source Current, Body Diode | | $I_{SM}$ | – | – | 500 | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

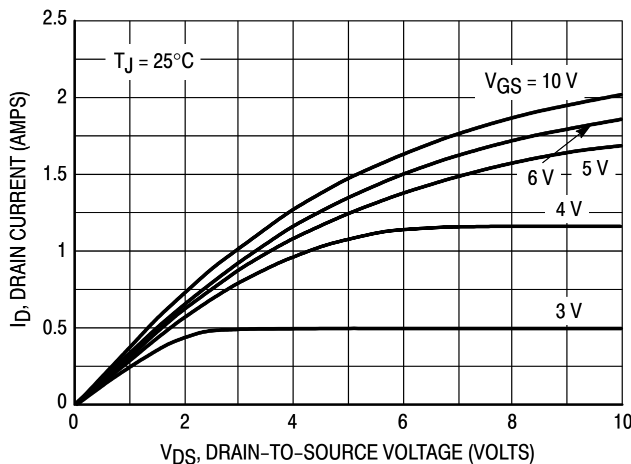



**Figure 1. On–Region Characteristics**

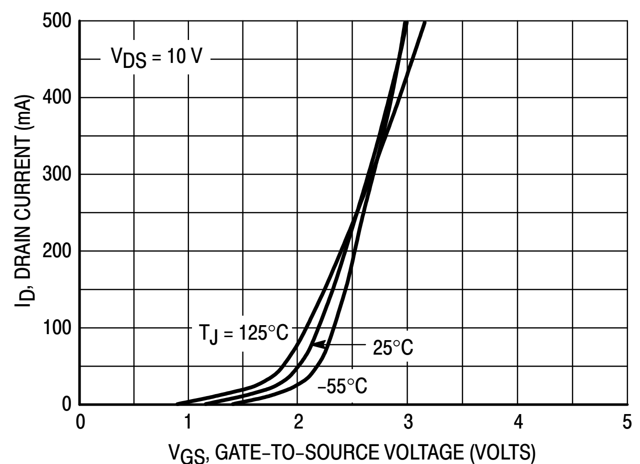



**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

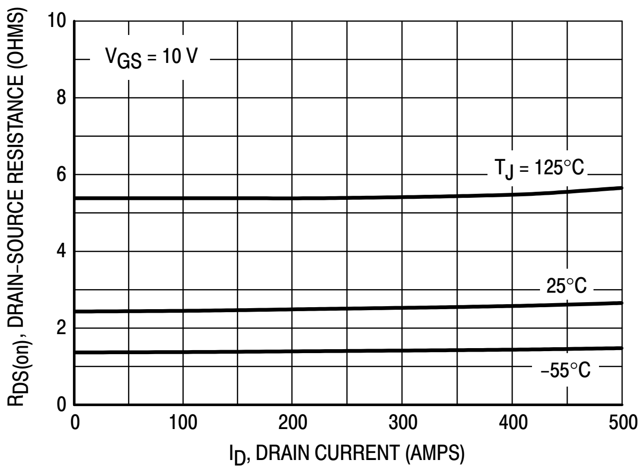



**Figure 3. On–Resistance versus Drain Current**

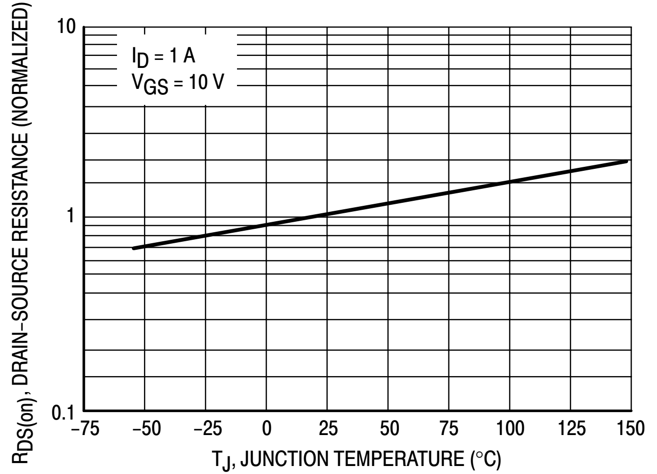



**Figure 4. On–Resistance Variation with Temperature**

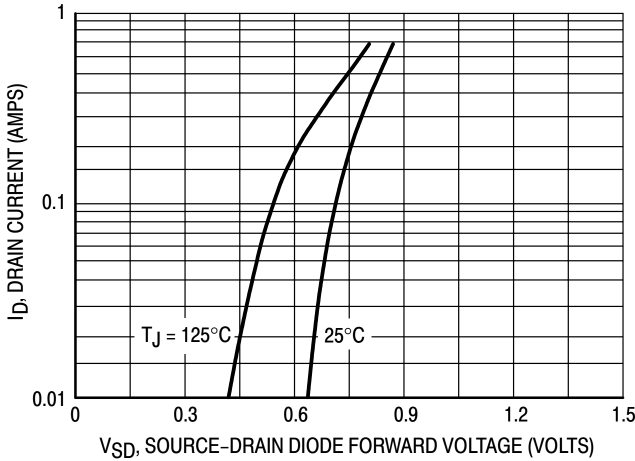



**Figure 5. Source–Drain Diode Forward Voltage**

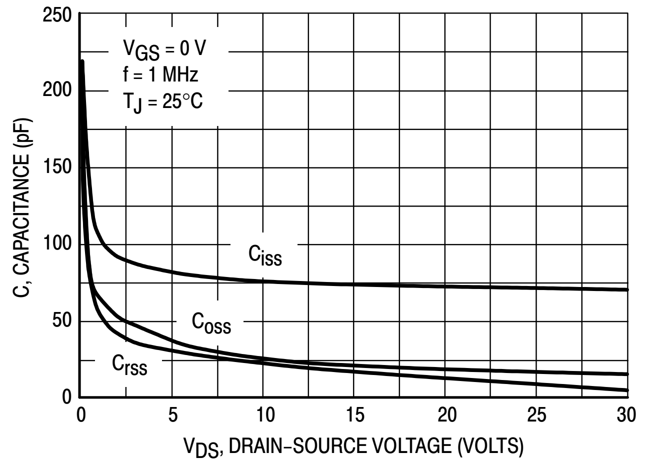



**Figure 6. Capacitance Variation**

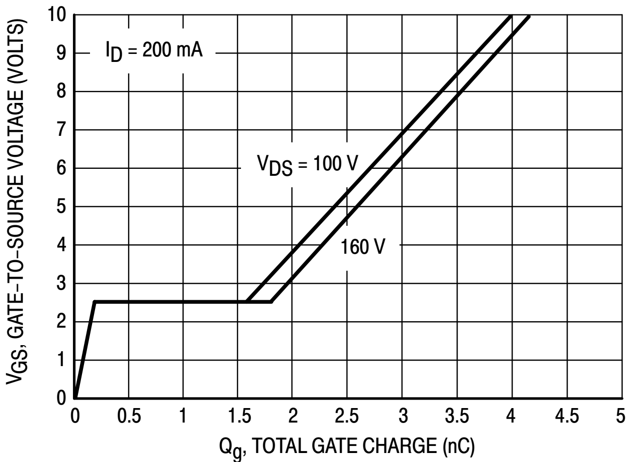



**Figure 7. Gate Charge versus Gate–to–Source Voltage**

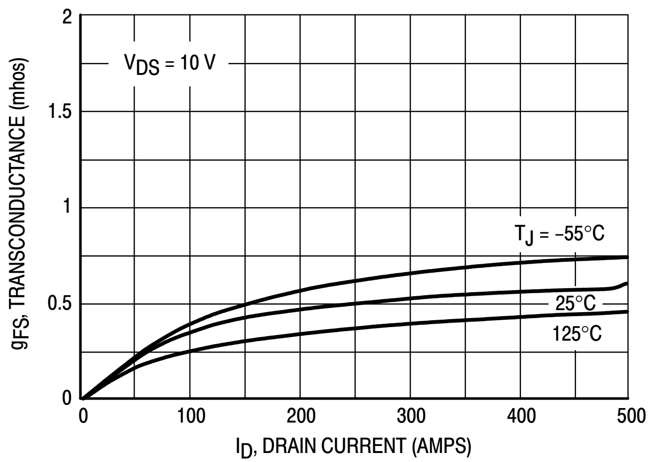
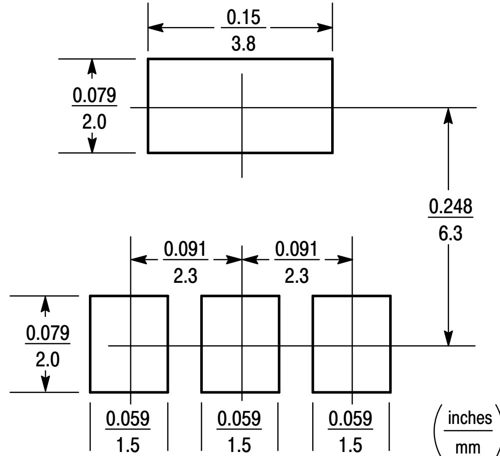



**Figure 8. Transconductance**

# INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT-223 POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT-223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.8 watts.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 0.8 \text{ watts}$$

The 156°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.8 watts. There are other alternatives to achieving higher power dissipation from the SOT-223 package. One is to increase the area of the collector pad. By increasing the area of the collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus collector pad area is shown in Figure 9.

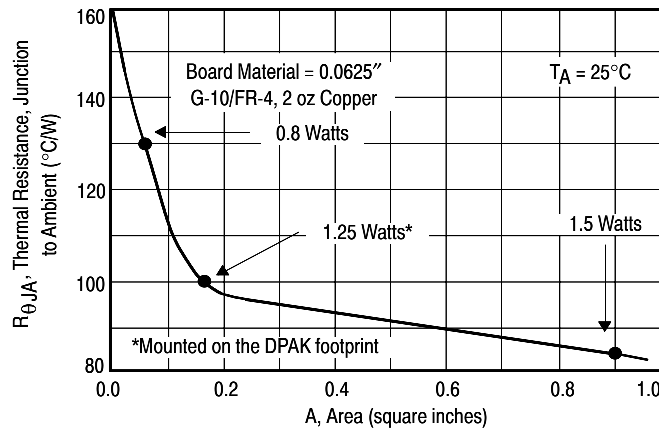



**Figure 9. Thermal Resistance versus Collector Pad Area for the SOT-223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT-223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 10 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

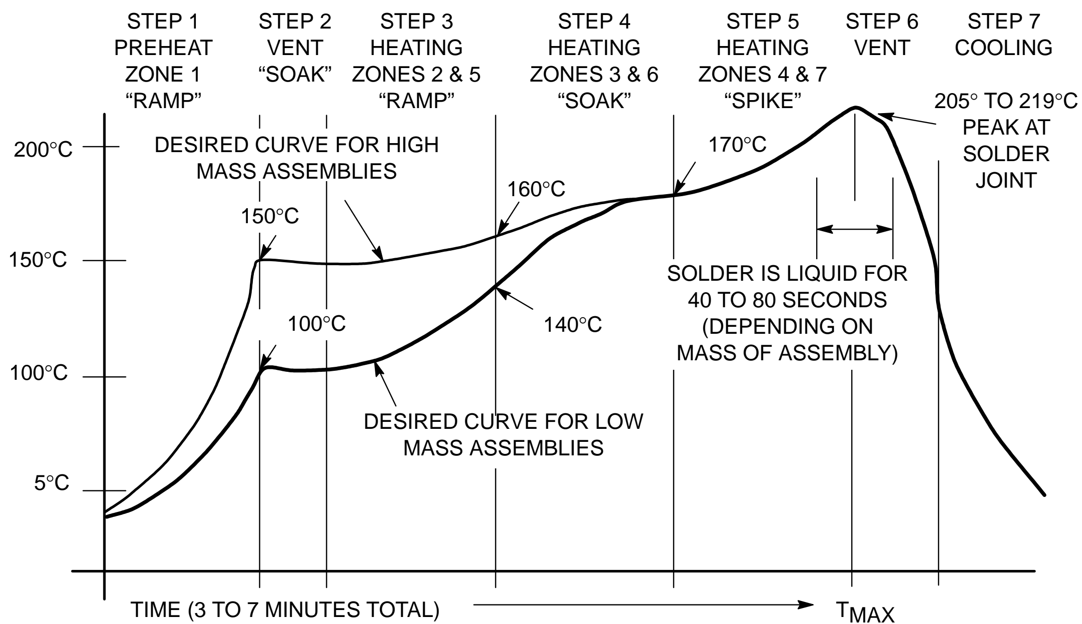



**Figure 10. Typical Solder Heating Profile**

# MMFT2406T1

Preferred Device

# Power MOSFET 700 mA, 240 Volts

## N–Channel SOT–223

This Power MOSFET is designed for high speed, low loss power switching applications such as switching regulators, converters, solenoid and relay drivers. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- High Voltage – 240 Vdc
- Low Drive Requirement
- The SOT–223 Package can be soldered using wave or reflow. The formed leads absorb thermal stress during soldering, eliminating the possibility of damage to the die.

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 240 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current | $I_D$ | 700 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Derate above 25°C | $P_D$ | 1.5<br>12 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |

**THERMAL CHARACTERISTICS**

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient (surface mounted) (Note 1.) | $R_{\theta JA}$ | 83.3 | °C/W |
| Lead Temperature for Soldering Purposes, 1/16″ from case<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

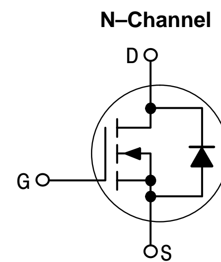
1. Device mounted on a glass epoxy printed circuit board 1.575 in. x 1.575 in. x 0.059 in.; mounting pad for the collector lead min. 0.93 sq. in.

**ON Semiconductor™**

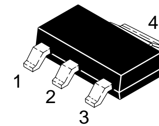
http://onsemi.com

**700 mA**
**240 VOLTS**
**$R_{DS(on)}$ = 6.0 Ω**

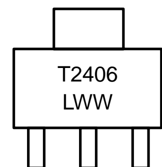
N–Channel




**MARKING DIAGRAM**

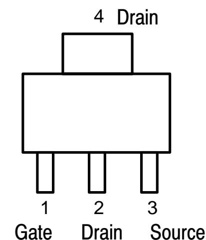



**TO–261AA CASE 318E STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT2406T1 | SOT–223 | 1000 Tape & Reel |
| MMFT2406T3 | SOT–223 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

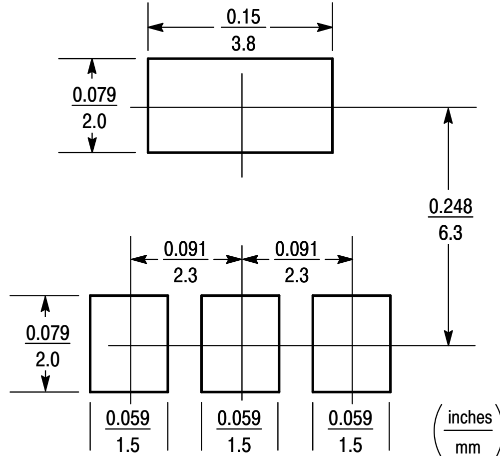
| Characteristics | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 μA) | | $V_{(BR)DSS}$ | 240 | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 120 V, $V_{GS}$ = 0) | | $I_{DSS}$ | – | 10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 0.8 | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance | | $R_{DS(on)}$ | | | Ohms |
| ($V_{GS}$ = 2.5 Vdc, $I_D$ = 0.1 Adc) | | | – | 10 | |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 0.5 Adc) | | | – | 6.0 | |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 V, $I_D$ = 0.5 A) | | $V_{DS(on)}$ | – | 3.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.0 V, $I_D$ = 0.5 A) | | $g_{FS}$ | 300 | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 125 | pF |
| Output Capacitance | | $C_{oss}$ | – | 50 | |
| Transfer Capacitance | | $C_{rss}$ | – | 20 | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

# INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT-223 POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT-223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 1.5 watts.

$$P_D = \frac{150°C - 25°C}{83.3°C/W} = 1.5 \text{ watts}$$

The 83.3°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.5 watts. There are other alternatives to achieving higher power dissipation from the SOT-223 package. One is to increase the area of the collector pad. By increasing the area of the collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus collector pad area is shown in Figure 1.

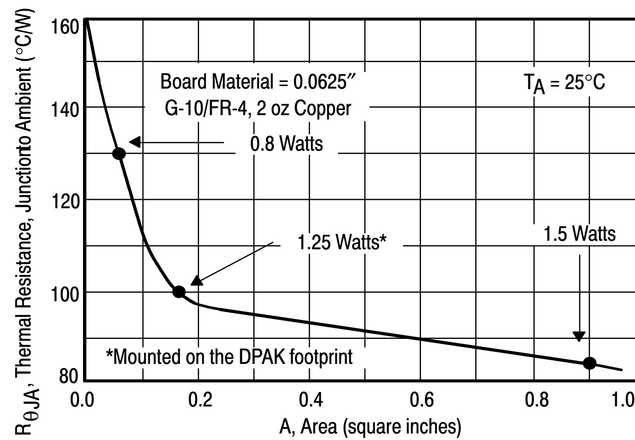



**Figure 1. Thermal Resistance versus Collector Pad Area for the SOT-223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT-223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 2 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

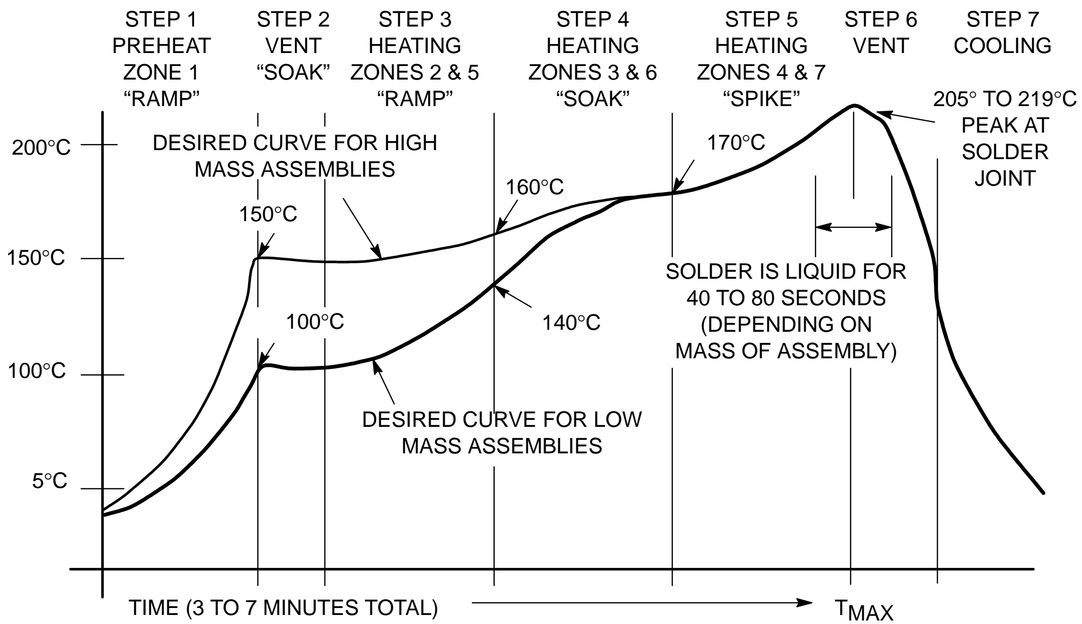



**Figure 2. Typical Solder Heating Profile**

# MMFT2955E

Preferred Device

# Power MOSFET 1 Amp, 60 Volts

## P–Channel SOT–223

**ON Semiconductor™**

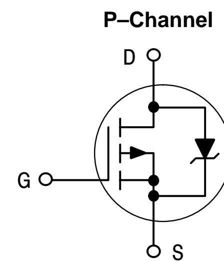
http://onsemi.com

**1 AMPERE**
**60 VOLTS**
**$R_{DS(on)}$ = 300 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die

**P–Channel**




**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

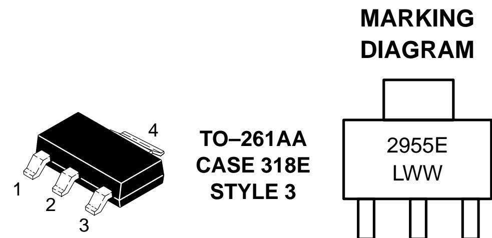
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 60 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±15 | |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 1.2<br>4.8 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$<br>(Note 1.) | 0.8<br>6.4 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 V, $V_{GS}$ = 10 V, Peak $I_L$= 1.2 A, L = 0.2 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 108 | mJ |

**THERMAL CHARACTERISTICS**

| | | | |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient (surface mounted) | $R_{\theta JA}$ | 156 | °C/W |
| Maximum Temperature for Soldering Purposes,<br>Time in Solder Bath | $T_L$ | 260<br><br>10 | °C<br><br>Sec |

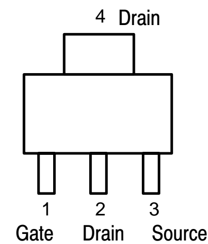
1. Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

**MARKING DIAGRAM**




2955E = Device Code
L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT2955ET1 | SOT–223 | 1000 Tape & Reel |
| MMFT2955ET3 | SOT–223 | 1000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 5

Publication Order Number:
MMFT2955E/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage, ($V_{GS}$ = 0, $I_D$ = 250 μA) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current,<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>50 | μAdc |
| Gate–Body Leakage Current,<br>($V_{GS}$ = 15 V, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage, ($V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA) | | $V_{GS(th)}$ | 2.0 | – | 4.5 | Vdc |
| Static Drain–to–Source On–Resistance, ($V_{GS}$ = 10 V, $I_D$ = 0.6 A) | | $R_{DS(on)}$ | – | – | 0.3 | Ohms |
| Drain–to–Source On–Voltage, ($V_{GS}$ = 10 V, $I_D$ = 1.2 A) | | $V_{DS(on)}$ | – | – | 0.48 | Vdc |
| Forward Transconductance, ($V_{DS}$ = 15 V, $I_D$ = 0.6 A) | | $g_{FS}$ | – | 7.5 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 20 V, $V_{GS}$ = 0, f = 1 MHz) | $C_{iss}$ | – | 460 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 210 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 84 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 1.6 A $V_{GS}$ = 10 V, $R_G$ = 50 ohms, $R_{GS}$ = 25 ohms) | $t_{d(on)}$ | – | 18 | – | ns |
| Rise Time | | $t_r$ | – | 29 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 44 | – | |
| Fall Time | | $t_f$ | – | 32 | – | |
| Total Gate Charge | ($V_{DS}$ = 48 V, $I_D$ = 1.2 A, $V_{GS}$ = 10 Vdc) See Figures 15 and 16 | $Q_g$ | – | 18 | – | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 2.8 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 7.5 | – | |
| **SOURCE DRAIN DIODE CHARACTERISTICS** (Note 3.) | | | | | | |
| Forward On–Voltage | $I_S$ = 1.2 A, $V_{GS}$ = 0 | $V_{SD}$ | – | 1.0 | – | Vdc |
| Forward Turn–On Time | $I_S$ = 1.2 A, $V_{GS}$ = 0, $dI_S/dt$ = 400 A/μs, $V_R$ = 30 V | $t_{on}$ | Limited by stray inductance | | | |
| Reverse Recovery Time | | $t_{rr}$ | – | 90 | – | ns |

2. Switching characteristics are independent of operating junction temperature.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

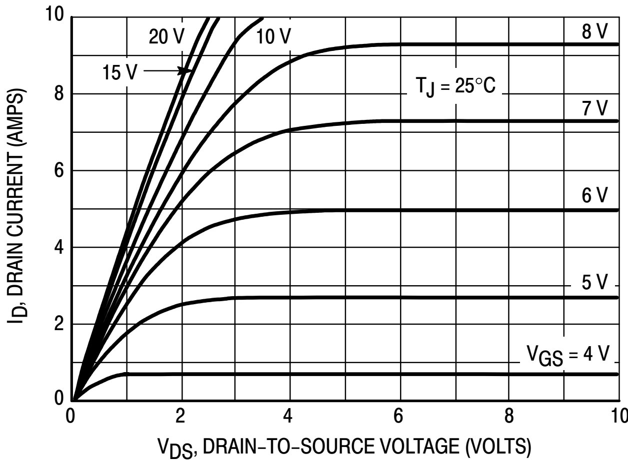



**Figure 1. On Region Characteristics**

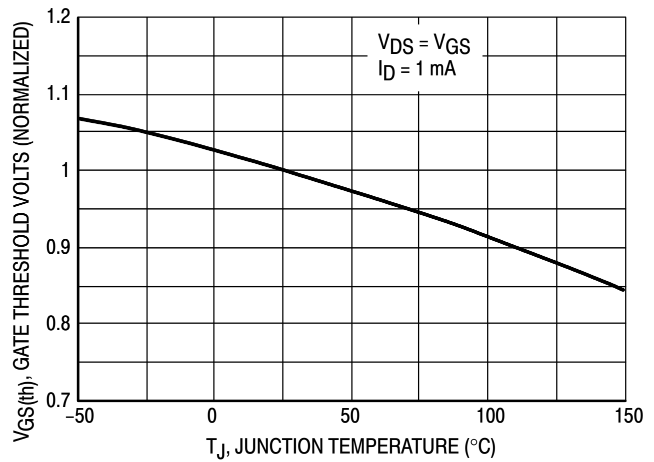



**Figure 2. Gate–Threshold Voltage Variation With Temperature**

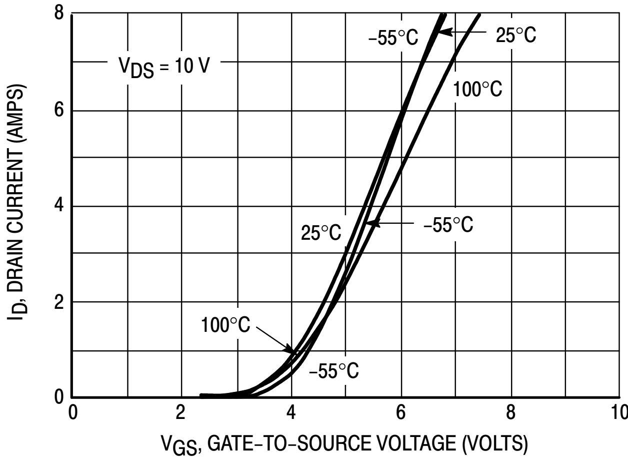



**Figure 3. Transfer Characteristics**

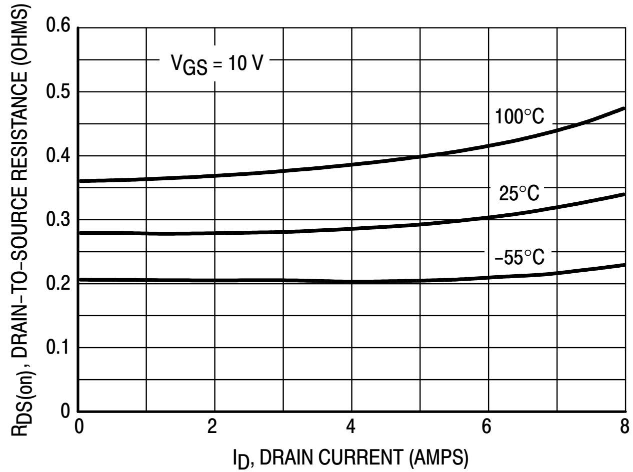



**Figure 4. On–Resistance versus Drain Current**

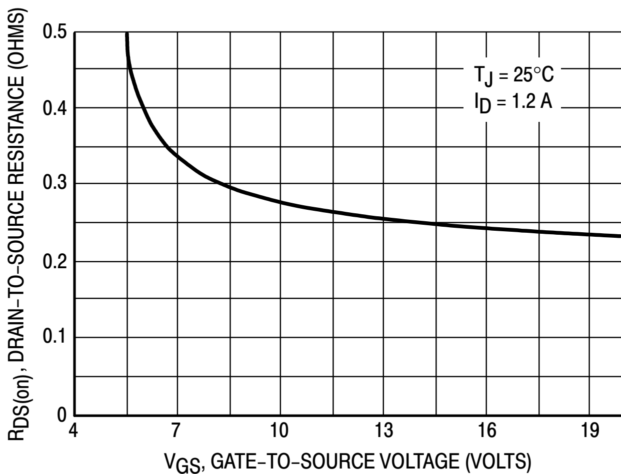



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

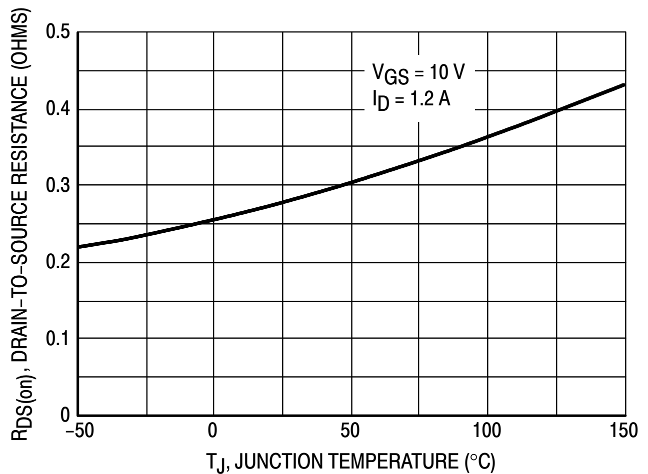



**Figure 6. On–Resistance versus Junction Temperature**

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, IDM and the breakdown voltage, BVDSS. The switching SOA is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

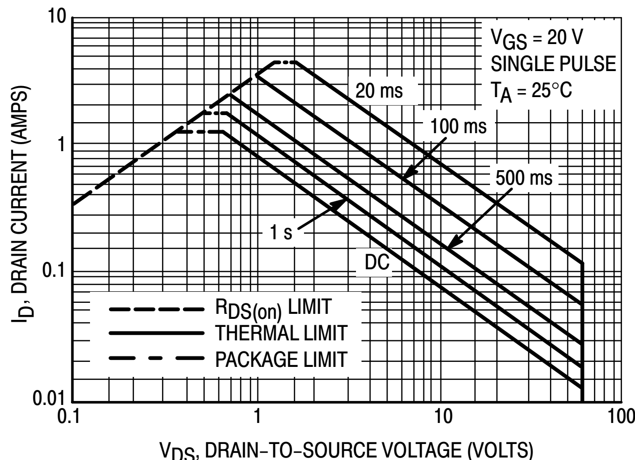



**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

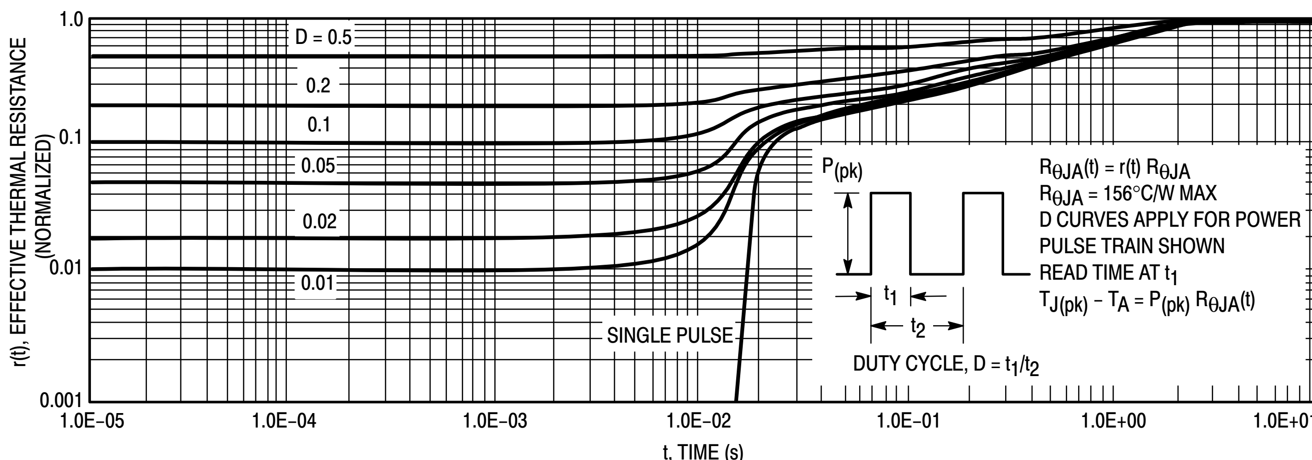



**Figure 8. Thermal Response**

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of $I_{FM}$ and peak $V_{DS}$ for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dI_S/dt$ is specified with a maximum value. Higher values of $dI_S/dt$ require an appropriate derating of $I_{FM}$, peak $V_{DS}$ or both. Ultimately $dI_S/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{rr}$ as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; $I_{FM}$ is the maximum forward source–drain diode current just prior to the onset of commutation.

$V_R$ is specified at 80% rated $BV_{DSS}$ to ensure that the CSOA stress is maximized as $I_S$ decays from $I_{RM}$ to zero.

$R_{GS}$ should be minimized during commutation. $T_J$ has only a second order effect on CSOA.

Stray inductances in ON Semiconductor’s test circuit are assumed to be practical minimums. $dV_{DS}/dt$ in excess of 10 V/ns was attained with $dI_S/dt$ of 400 A/µs.

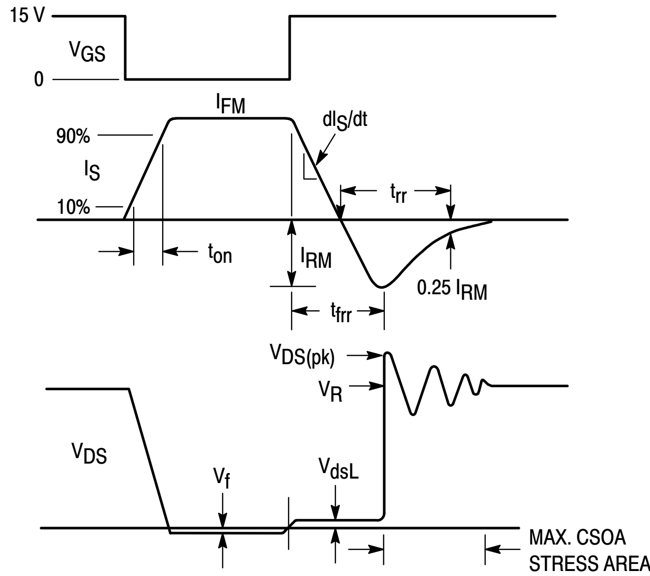



**Figure 9. Commutating Waveforms**

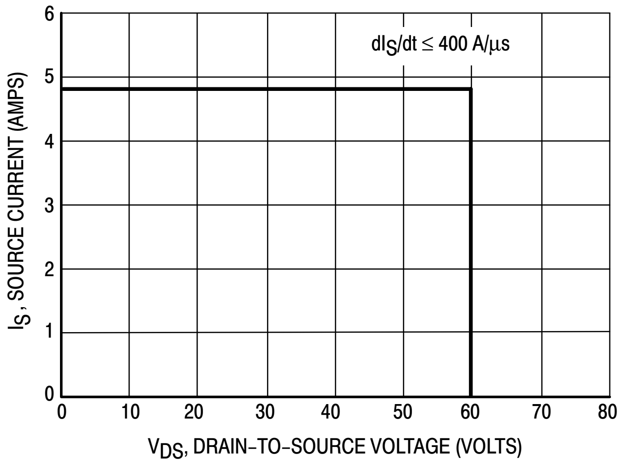



**Figure 10. Commutating Safe Operating Area (CSOA)**

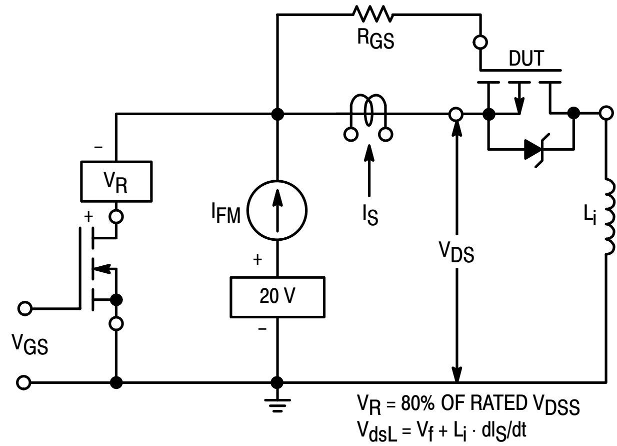



**Figure 11. Commutating Safe Operating Area Test Circuit**

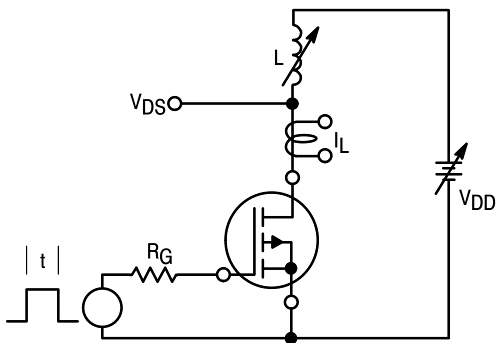



**Figure 12. Unclamped Inductive Switching Test Circuit**

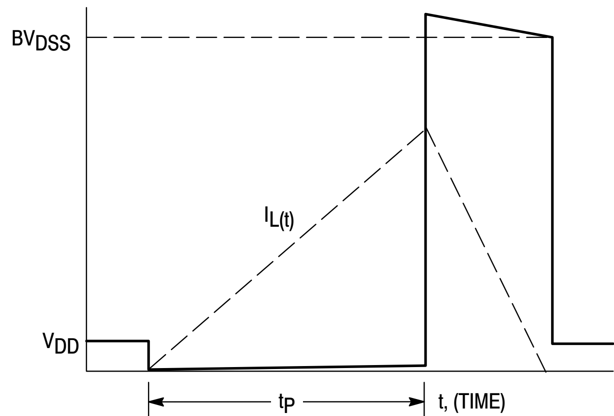



**Figure 13. Unclamped Inductive Switching Waveforms**

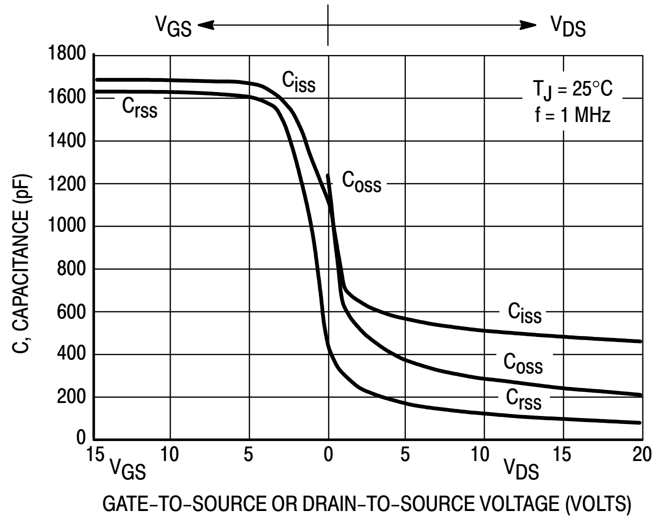



**Figure 14. Capacitance Variation with Voltage**

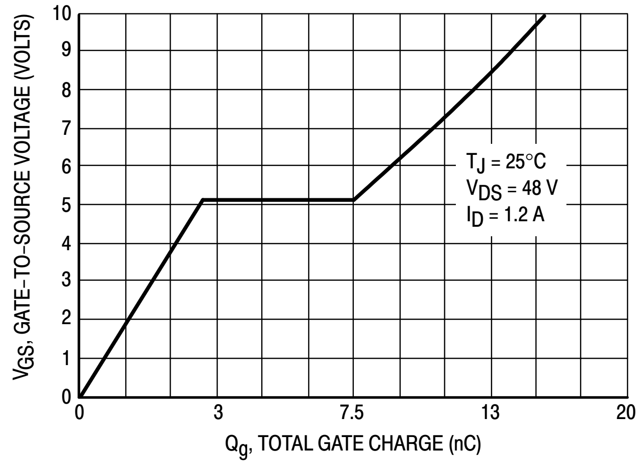



**Figure 15. Gate Charge versus Gate–To–Source Voltage**

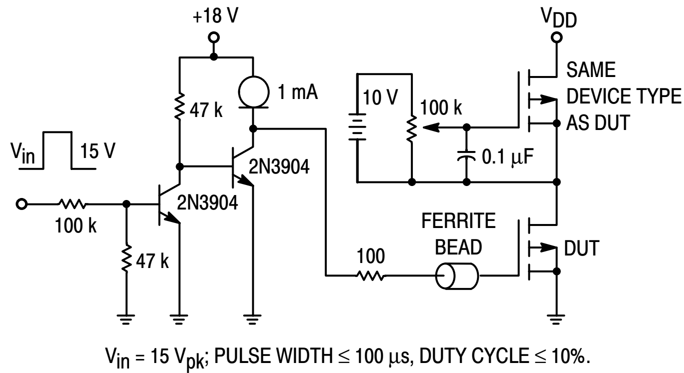
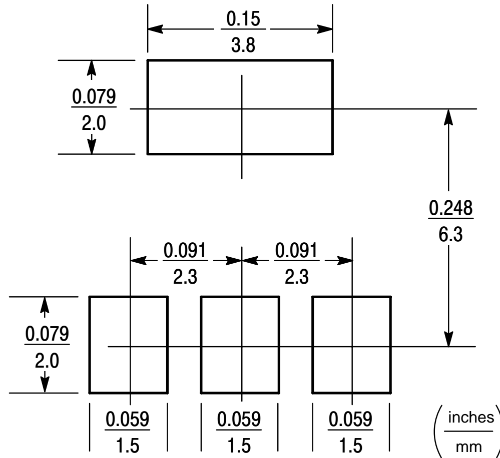



**Figure 16. Gate Charge Test Circuit**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 800 milliwatts.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

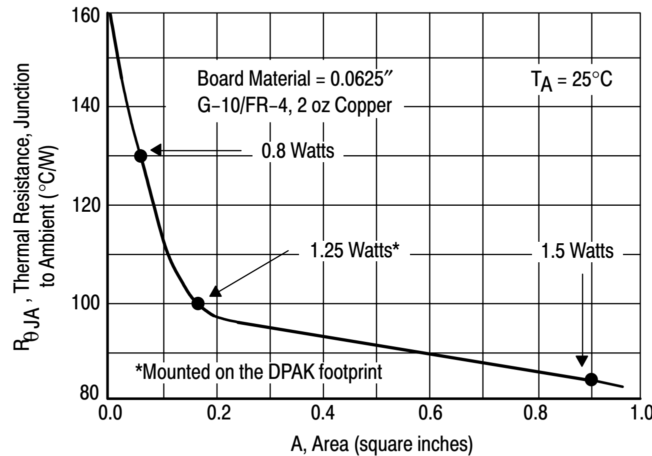



**Figure 17. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT–223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

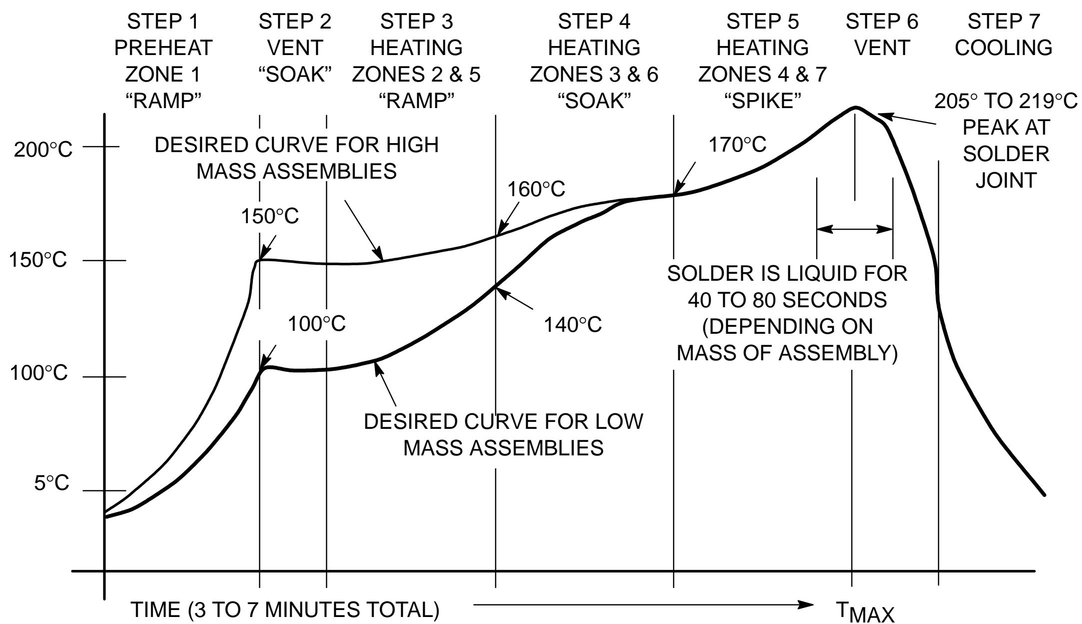



**Figure 18. Typical Solder Heating Profile**

# MMFT2N02EL

**Preferred Device**

# Power MOSFET 2 Amps, 20 Volts

## N–Channel SOT–223

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This device is also designed with a low threshold voltage so it is fully enhanced with 5 Volts. This new energy efficient device also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, dc–dc converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

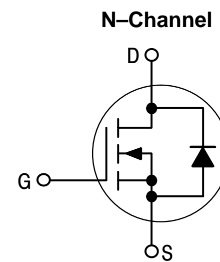
- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement to Interface Power Loads to Logic Level ICs, $V_{GS(th)}$ = 2 Volts Max
- The SOT–223 Package can be Soldered Using Wave or Reflow. The Formed Leads Absorb Thermal Stress During Soldering, Eliminating the Possibility of Damage to the Die

**ON Semiconductor™**

http://onsemi.com

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 150 mΩ**

**N–Channel**




**MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise noted)

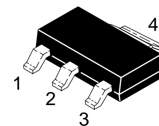
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±15 | Vdc |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 1.6<br>6.4 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$<br>(Note 1.) | 0.8<br>6.4 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 10 V, $V_{GS}$ = 5 V, Peak $I_L$= 2 A, L = 0.2 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 66 | mJ |

**THERMAL CHARACTERISTICS**

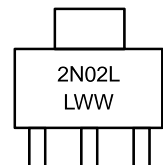
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient (surface mounted) | $R_{\theta JA}$ | 156 | °C/W |
| Maximum Temperature for Soldering Purposes,<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

1. Power rating when mounted on FR–4 glass epoxy printed circuit board using recommended footprint.

**MARKING DIAGRAM**

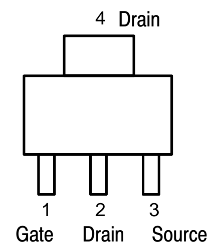



**TO–261AA**
**CASE 318E**
**STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT2N02ELT1 | SOT–223 | 1000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage, ($V_{GS}$ = 0, $I_D$ = 250 μA) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Zero Gate Voltage Drain Current, ($V_{DS}$ = 20 V, $V_{GS}$ = 0) | | $I_{DSS}$ | – | – | 10 | μAdc |
| Gate–Body Leakage Current, ($V_{GS}$ = 15 V, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** | | | | | | |
| Gate Threshold Voltage, ($V_{DS}$ = $V_{GS}$, $I_D$ = 1 mA) | | $V_{GS(th)}$ | 1 | – | 2 | Vdc |
| Static Drain–to–Source On–Resistance, ($V_{GS}$ = 5 V, $I_D$ = 0.8 A) | | $R_{DS(on)}$ | – | – | 0.15 | Ohms |
| Drain–to–Source On–Voltage, ($V_{GS}$ = 5 V, $I_D$ = 1.6 A) | | $V_{DS(on)}$ | – | – | 0.32 | Vdc |
| Forward Transconductance, ($V_{DS}$ = 10 V, $I_D$ = 0.8 A) | | $g_{FS}$ | – | 2.6 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 15 V, $V_{GS}$ = 0, f = 1 MHz) | $C_{iss}$ | – | 580 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 430 | – | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 250 | – | |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 V, $I_D$ = 1.6 A $V_{GS}$ = 5 V, $R_G$ = 50 ohms, $R_{GS}$ = 25 ohms) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 73 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 77 | – | |
| Fall Time | | $t_f$ | – | 107 | – | |
| Total Gate Charge | ($V_{DS}$ = 16 V, $I_D$ = 1.6 A, $V_{GS}$ = 5 Vdc) See Figures 15 and 16 | $Q_g$ | – | 20 | – | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.7 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 6 | – | |
| **SOURCE DRAIN DIODE CHARACTERISTICS** (Note 2.) | | | | | | |
| Forward On–Voltage | $I_S$ = 1.6 A, $V_{GS}$ = 0 | $V_{SD}$ | – | 0.9 | – | Vdc |
| Forward Turn–On Time | $I_S$ = 1.6 A, $V_{GS}$ = 0, $dI_S/dt$ = 400 A/μs, $V_R$ = 16 V | $t_{on}$ | Limited by stray inductance | | | |
| Reverse Recovery Time | | $t_{rr}$ | – | 55 | – | ns |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%

## TYPICAL ELECTRICAL CHARACTERISTICS

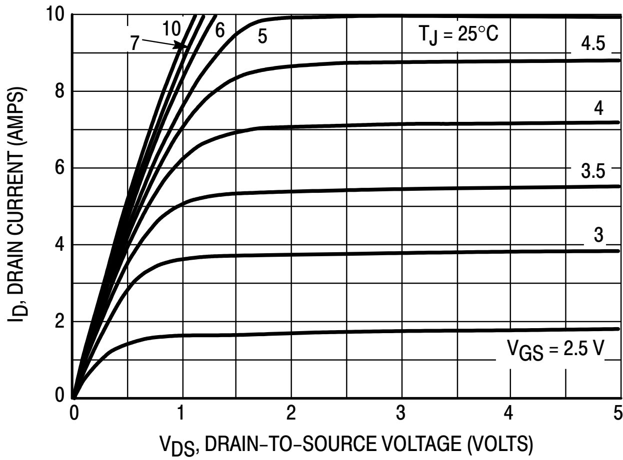



**Figure 1. On Region Characteristics**

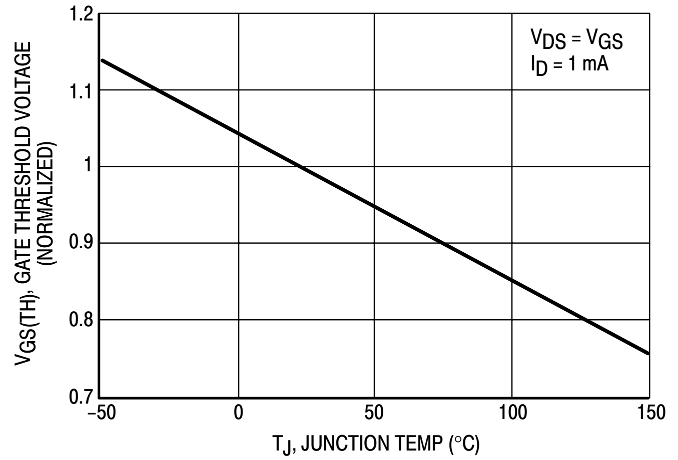



**Figure 2. Gate–Threshold Voltage Variation With Temperature**

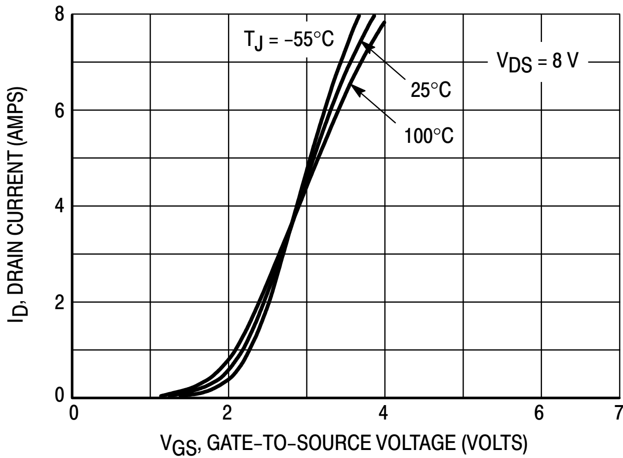



**Figure 3. Transfer Characteristics**

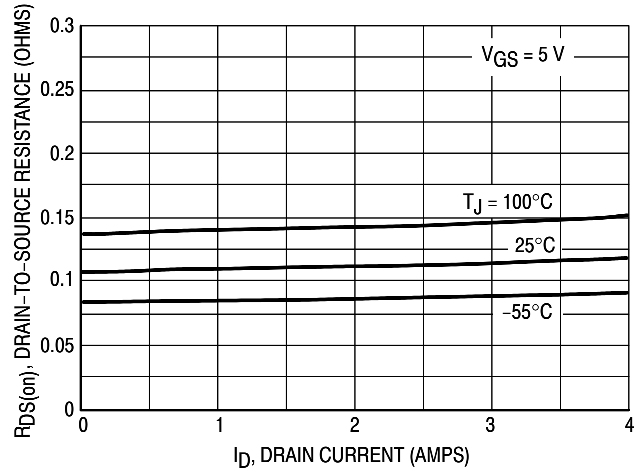



**Figure 4. On–Resistance versus Drain Current**

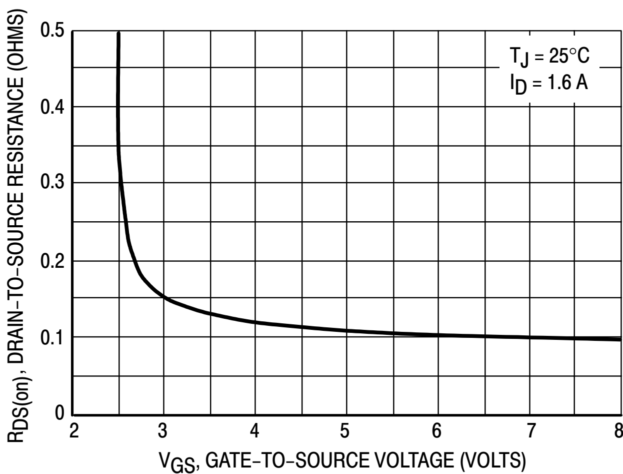



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

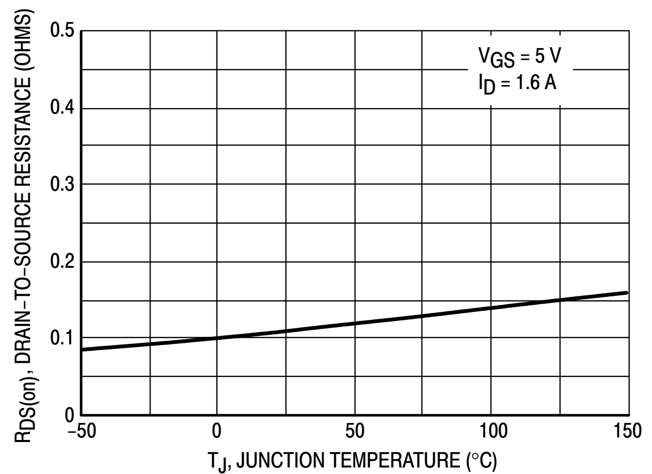



**Figure 6. On–Resistance versus Junction Temperature**

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on an ambient temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various ambient temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $BV_{DSS}$. The switching SOA is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

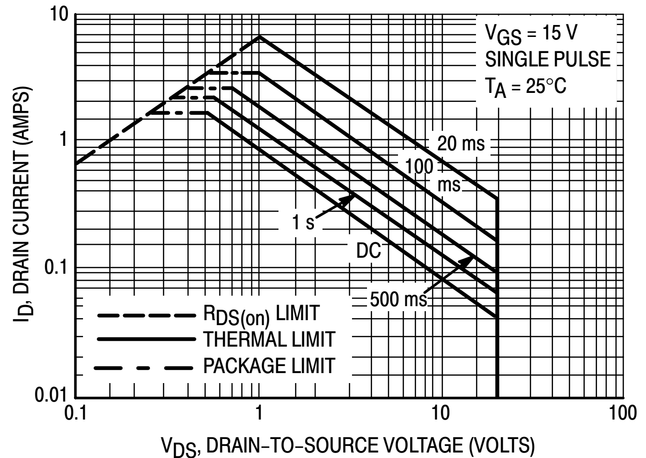



**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

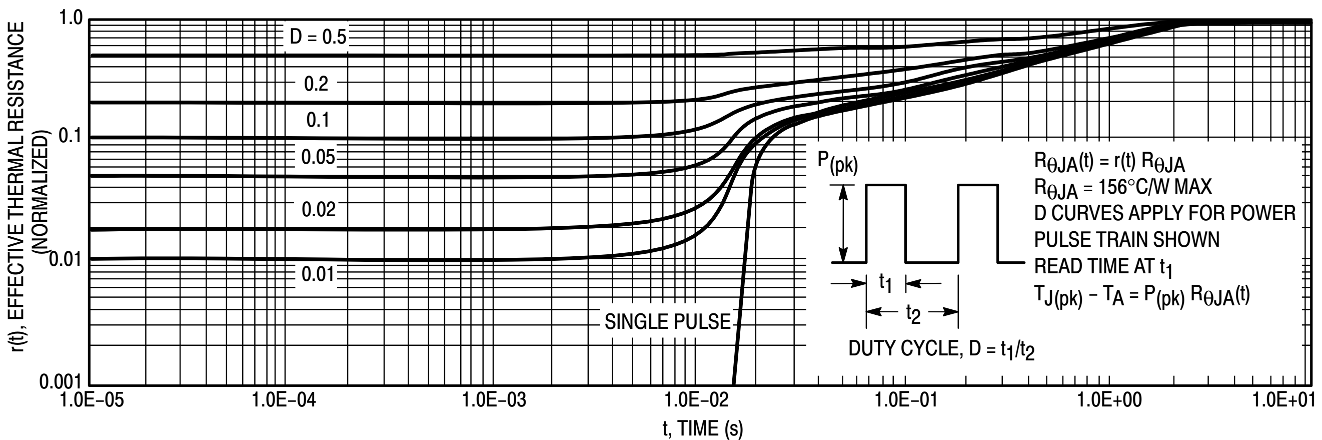



**Figure 8. Thermal Response**

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 10 defines the limits of safe operation for commutated source–drain current versus re–applied drain voltage when the source–drain diode has undergone forward bias. The curve shows the limitations of $I_{FM}$ and peak $V_{DS}$ for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 9 are present. Full or half–bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dI_S/dt$ is specified with a maximum value. Higher values of $dI_S/dt$ require an appropriate derating of $I_{FM}$, peak $V_{DS}$ or both. Ultimately $dI_S/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{rr}$ as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; $I_{FM}$ is the maximum forward source–drain diode current just prior to the onset of commutation.

$V_R$ is specified at 80% rated $BV_{DSS}$ to ensure that the CSOA stress is maximized as $I_S$ decays from $I_{RM}$ to zero.

$R_{GS}$ should be minimized during commutation. $T_J$ has only a second order effect on CSOA.

Stray inductances in ON Semiconductor's test circuit are assumed to be practical minimums. dVDS/dt in excess of 10 V/ns was attained with $dI_S/dt$ of 400 A/µs.

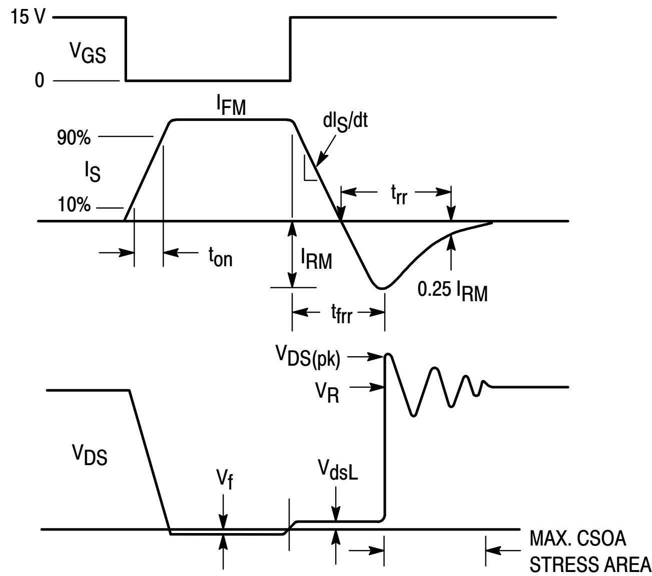



**Figure 9. Commutating Waveforms**

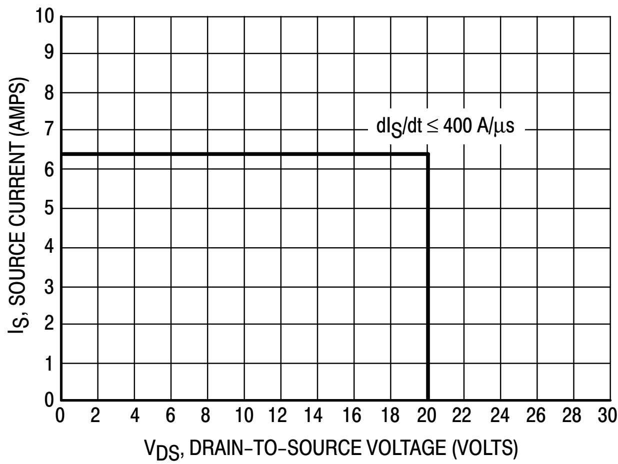



**Figure 10. Commutating Safe Operating Area (CSOA)**

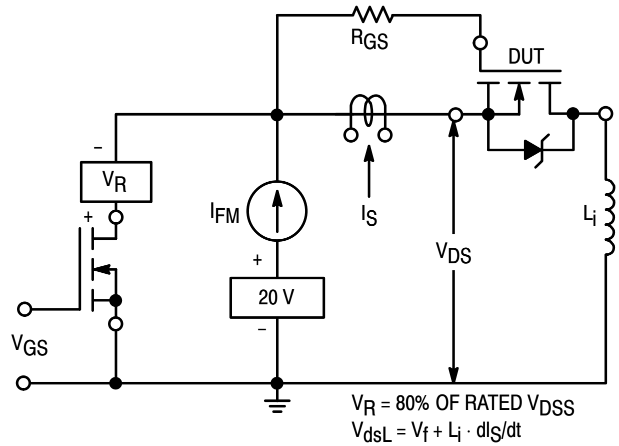



**Figure 11. Commutating Safe Operating Area Test Circuit**

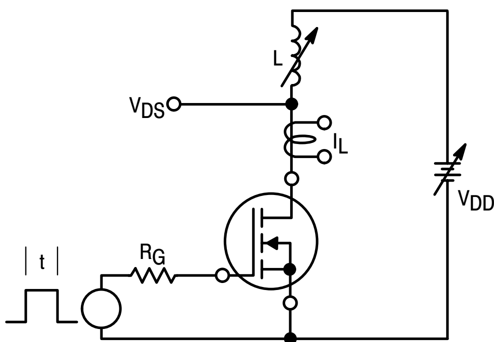



**Figure 12. Unclamped Inductive Switching Test Circuit**

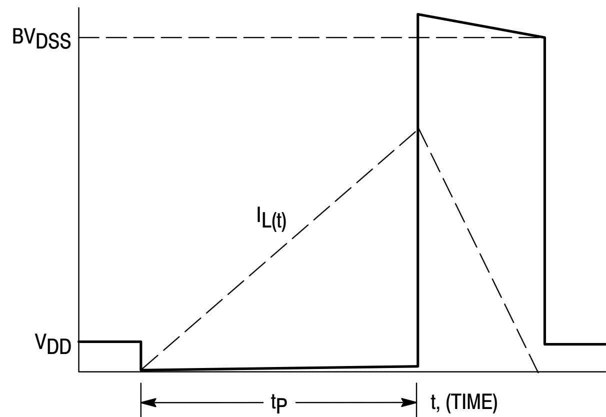



**Figure 13. Unclamped Inductive Switching Waveforms**

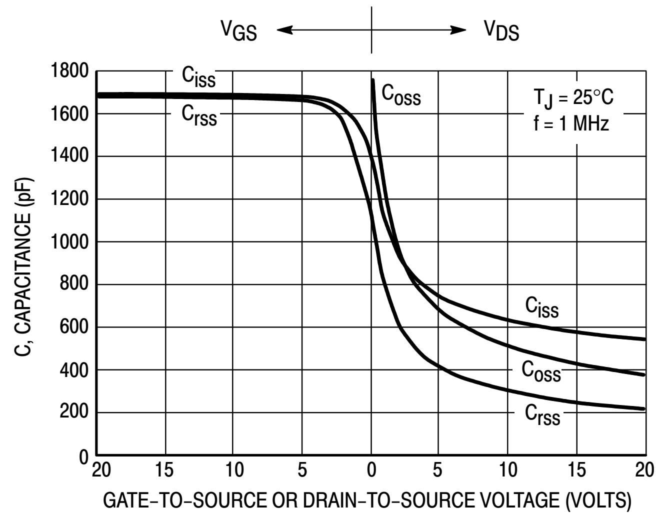



**Figure 14. Capacitance Variation With Voltage**

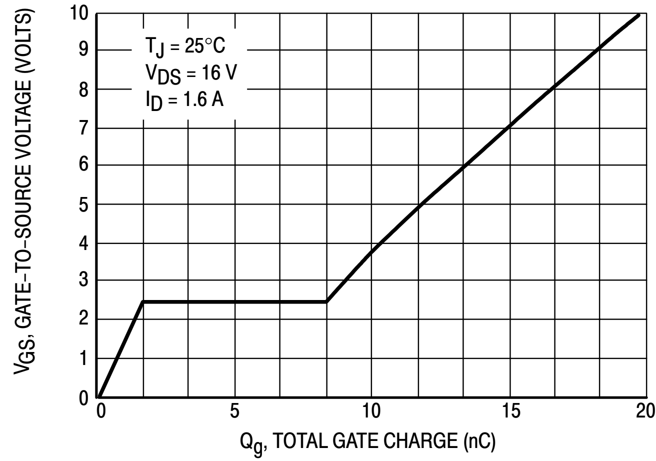



**Figure 15. Gate Charge versus Gate–To–Source Voltage**

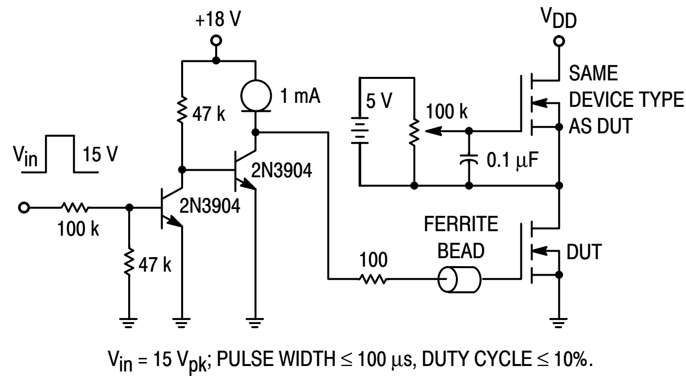
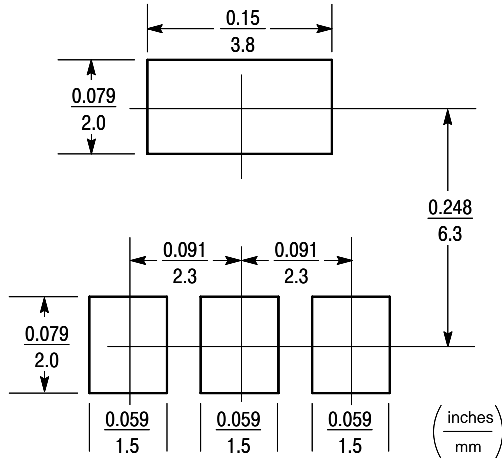



**Figure 16. Gate Charge Test Circuit**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 800 milliwatts.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 800 \text{ milliwatts}$$

The 156°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 800 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

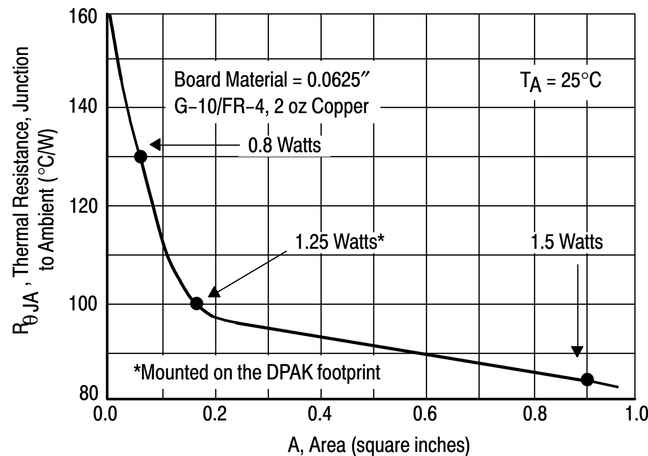



**Figure 17. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT–223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

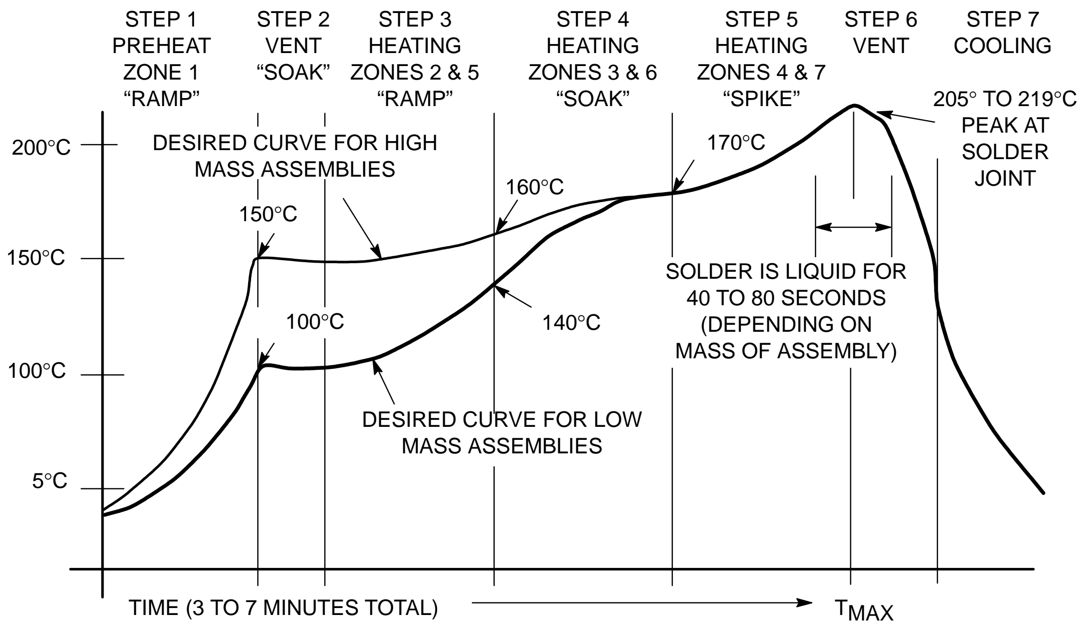



**Figure 18. Typical Solder Heating Profile**

# MMFT3055V

## Power MOSFET 1 Amp, 60 Volts

### N–Channel SOT–223

These Power MOSFETs are designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

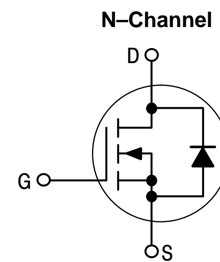
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**ON Semiconductor™**

http://onsemi.com

**1 AMPERE**
**60 VOLTS**
**$R_{DS(on)}$ = 130 mΩ**

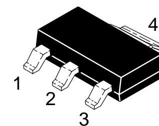
N–Channel



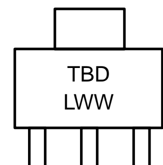

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 1.7<br>1.4<br>6.0 | Adc<br><br>Apk |
| Total PD @ $T_A$ = 25°C mounted on 1″ sq. Drain pad on FR–4 bd material<br>Total PD @ $T_A$ = 25°C mounted on 0.70″ sq. Drain pad on FR–4 bd material<br>Total PD @ $T_A$ = 25°C mounted on min. Drain pad on FR–4 bd material<br>Derate above 25°C | $P_D$ | 2.1<br>1.7<br>0.94<br>6.3 | Watts<br><br><br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 3.4 Apk, L = 10 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 58 | mJ |
| Thermal Resistance<br>– Junction to Ambient on 1″ sq. Drain pad on FR–4 bd material<br>– Junction to Ambient on 0.70″ sq. Drain pad on FR–4 bd material<br>– Junction to Ambient on min. Drain pad on FR–4 bd material | <br>$R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>70<br>88<br>159 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM**

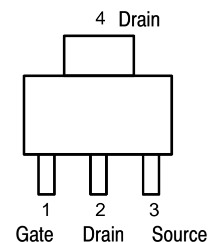



**TO–261AA**
**CASE 318E**
**STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT3055VT1 | SOT–223 | 1000 Tape & Reel |
| MMFT3055VT3 | SOT–223 | 4000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>63 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>5.6 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 0.85 Adc) | | $R_{DS(on)}$ | – | 0.115 | 0.13 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 1.7 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 0.85 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 0.27<br>0.25 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 1.7 Adc) | | $g_{FS}$ | 1.0 | 2.7 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 360 | 500 | pF |
| Output Capacitance | | $C_{oss}$ | – | 110 | 150 | |
| Transfer Capacitance | | $C_{rss}$ | – | 25 | 50 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 8.0 | 20 | ns |
| Rise Time | | $t_r$ | – | 9.0 | 20 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | 60 | |
| Fall Time | | $t_f$ | – | 18 | 40 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 13 | 20 | nC |
| | | $Q_1$ | – | 2.0 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 4.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 0.85<br>0.7 | 1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 40 | – | ns |
| | | $t_a$ | – | 34 | – | |
| | | $t_b$ | – | 6.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.089 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

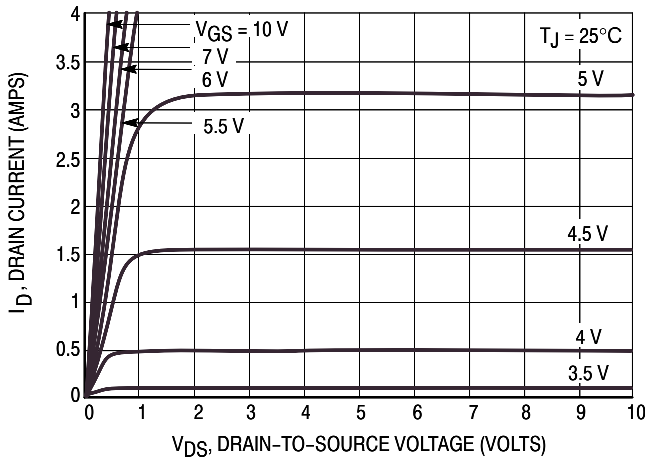



**Figure 1. On–Region Characteristics**

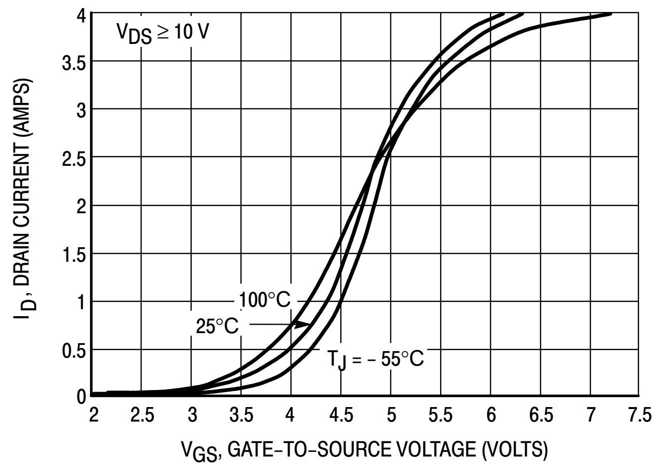



**Figure 2. Transfer Characteristics**

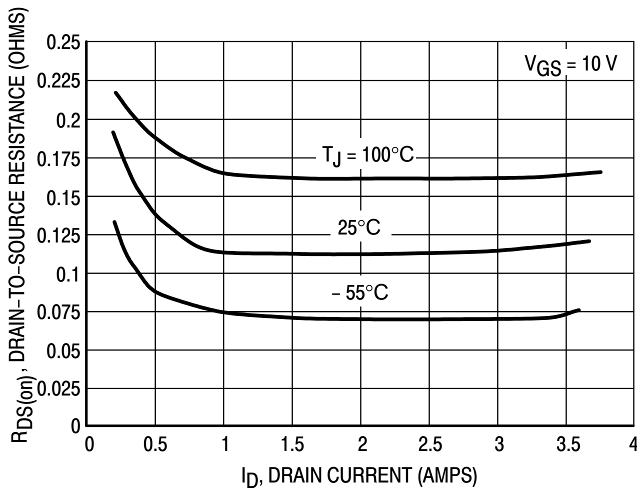



**Figure 3. On–Resistance versus Drain Current and Temperature**

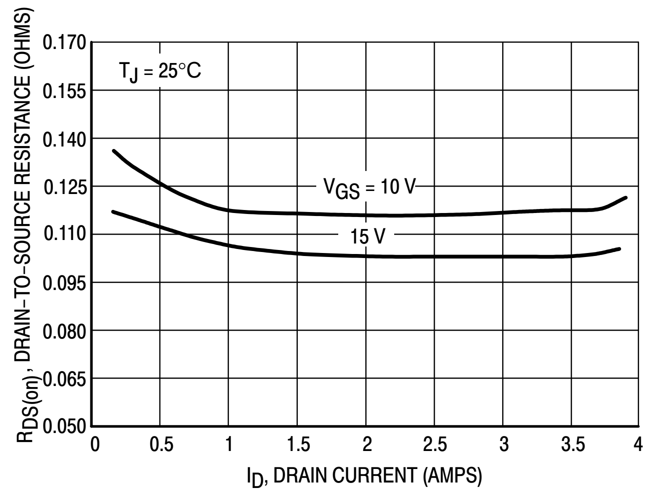



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

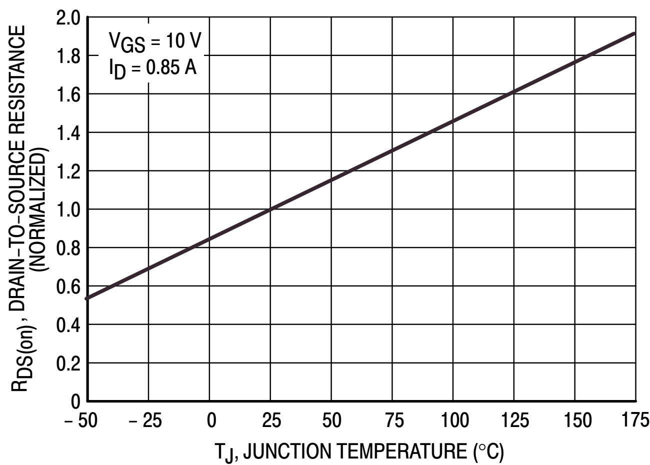



**Figure 5. On–Resistance Variation with Temperature**

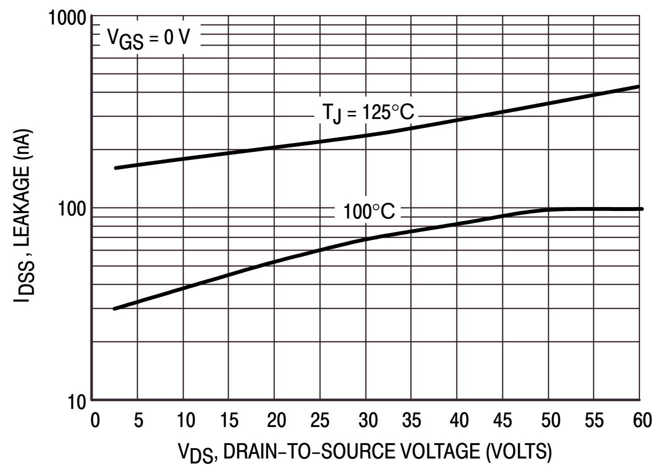



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

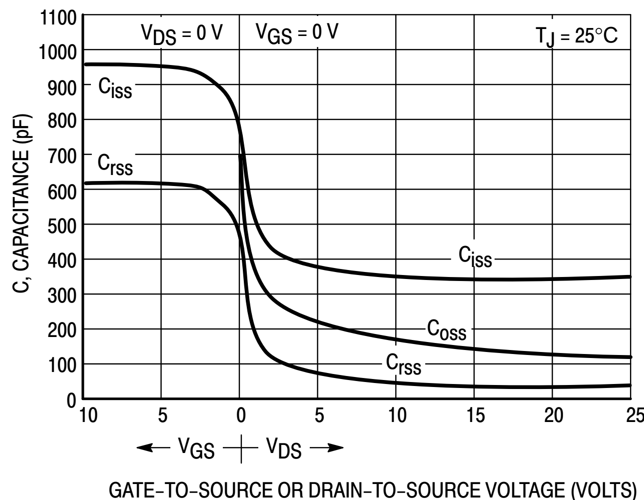



**Figure 7. Capacitance Variation**

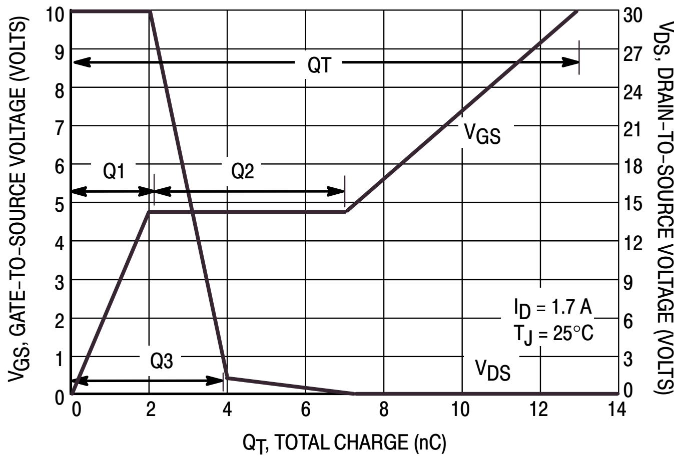



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

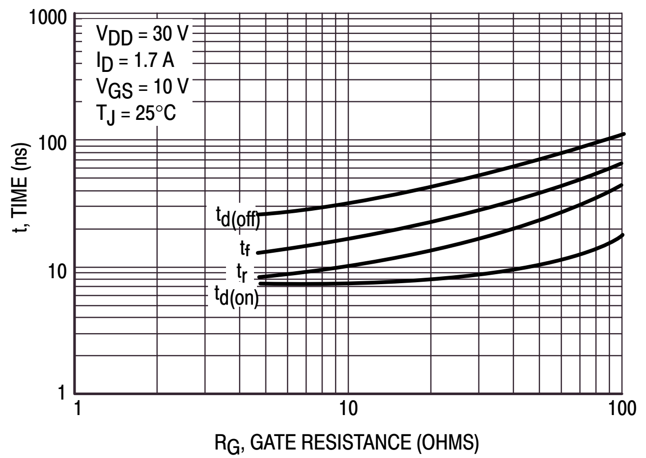



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

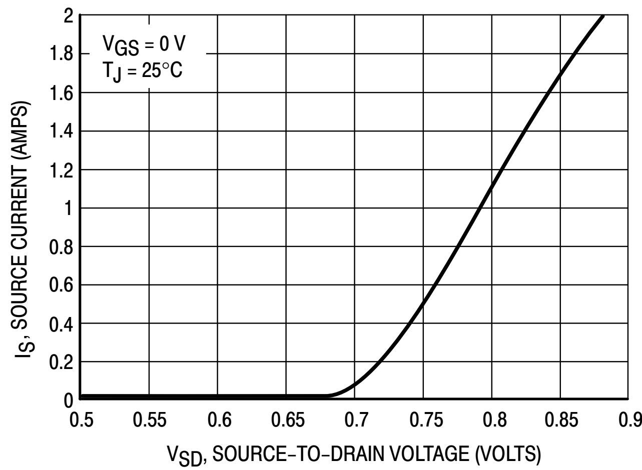



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

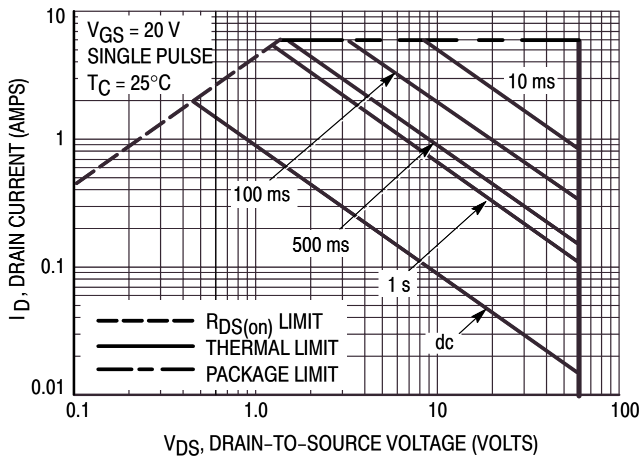



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

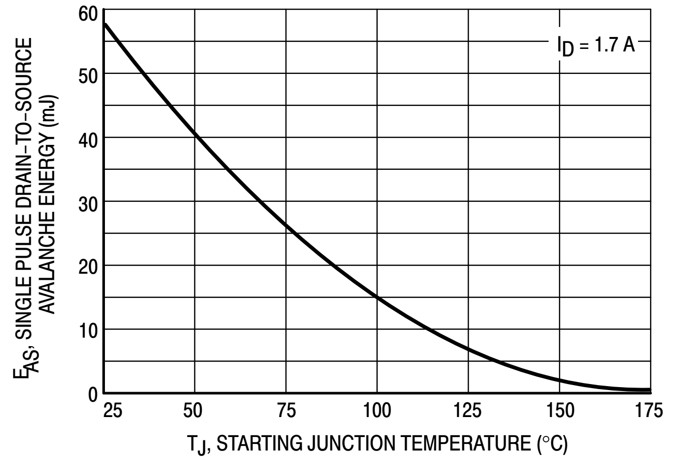



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

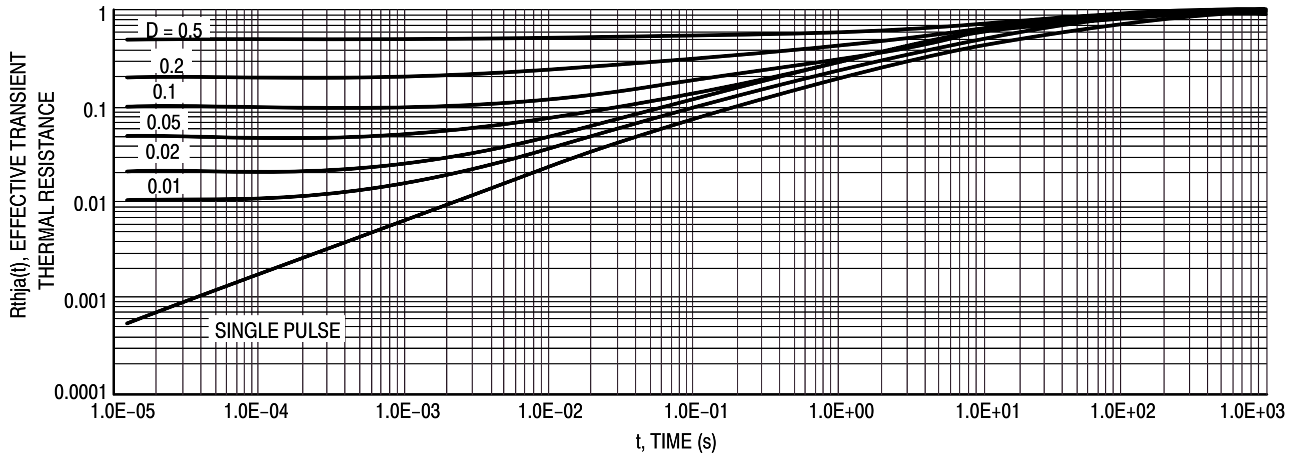



**Figure 13. Thermal Response**

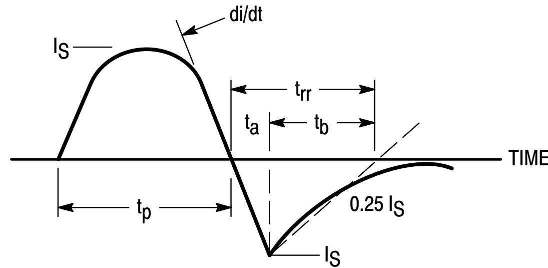
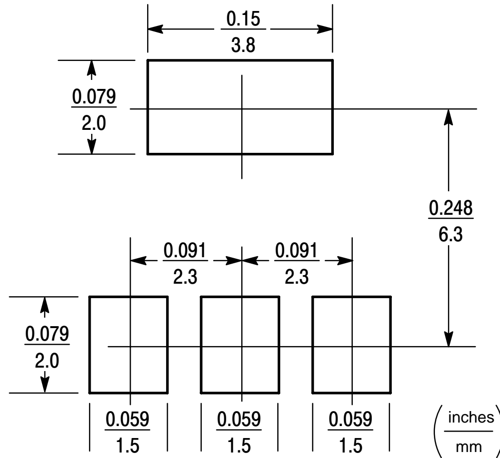



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 943 milliwatts.

$$P_D = \frac{175°C - 25°C}{159°C/W} = 943 \text{ milliwatts}$$

The 159°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 943 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

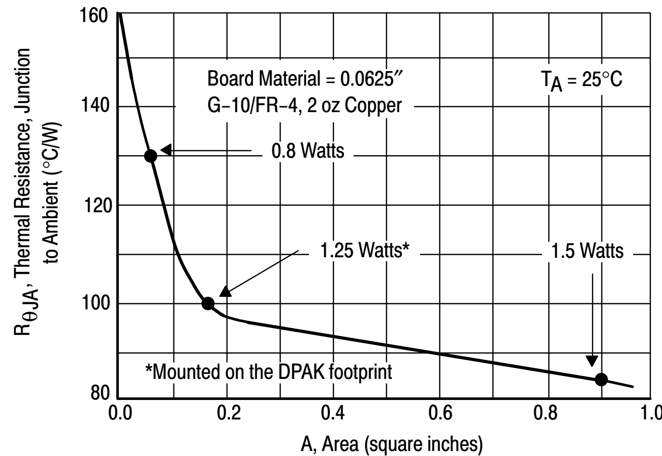



**Figure 15. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT–223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

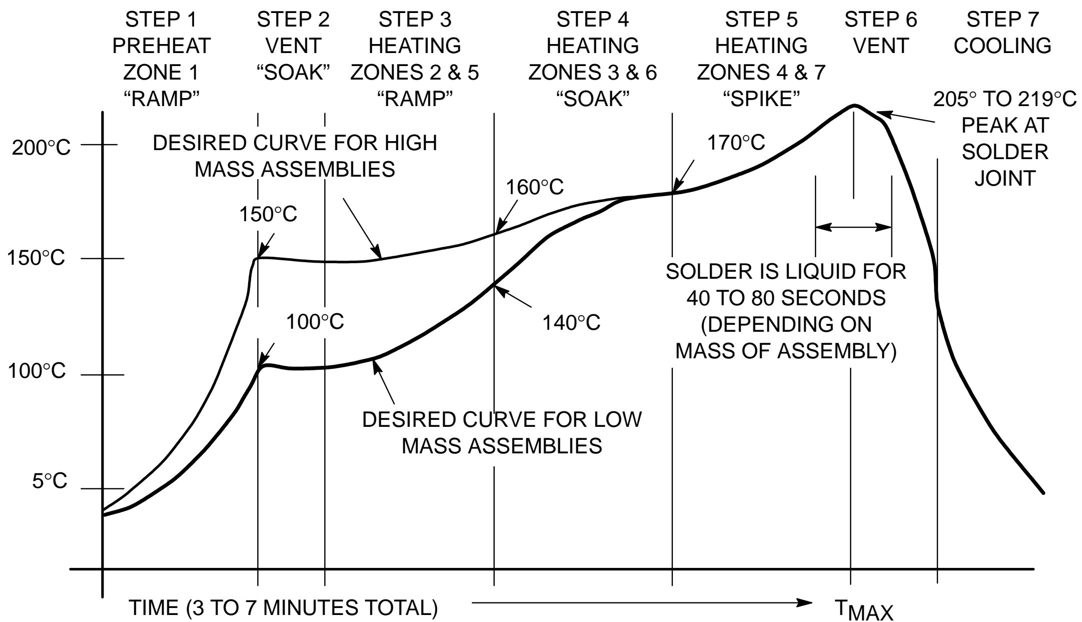



**Figure 16. Typical Solder Heating Profile**

# MMFT3055VL

**ON Semiconductor™**

http://onsemi.com

## Power MOSFET 1 Amp, 60 Volts

### N–Channel SOT–223

These Power MOSFETs are designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

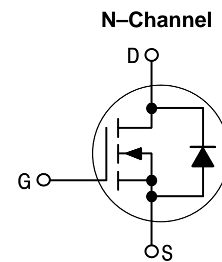
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**1 AMPERE**
**60 VOLTS**
**$R_{DS(on)}$ = 140 mΩ**

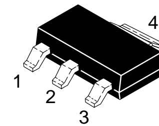
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 1.5<br>1.2<br>5.0 | Adc<br><br>Apk |
| Total PD @ $T_A$ = 25°C mounted on 1″ sq. Drain pad on FR–4 bd material<br>Total PD @ $T_A$ = 25°C mounted on 0.70″ sq. Drain pad on FR–4 bd material<br>Total PD @ $T_A$ = 25°C mounted on min. Drain pad on FR–4 bd material<br>Derate above 25°C | $P_D$ | 2.1<br>1.7<br>0.94<br>6.3 | Watts<br><br><br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 3.4 Apk, L = 10 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 58 | mJ |
| Thermal Resistance<br>– Junction to Ambient on 1″ sq. Drain pad on FR–4 bd material<br>– Junction to Ambient on 0.70″ sq. Drain pad on FR–4 bd material<br>– Junction to Ambient on min. Drain pad on FR–4 bd material | <br>$R_{\theta JA}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>70<br>88<br>159 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

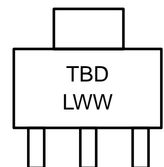
N–Channel




**MARKING DIAGRAM**

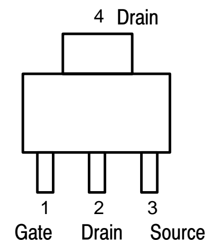



**TO–261AA**
**CASE 318E**
**STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT3055VLT1 | SOT–223 | 1000 Tape & Reel |
| MMFT3055VLT3 | SOT–223 | 4000 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.) ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 65 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 3.7 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.) ($V_{GS}$ = 5.0 Vdc, $I_D$ = 0.75 Adc) | | $R_{DS(on)}$ | – | 0.125 | 0.14 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5.0 Vdc, $I_D$ = 1.5 Adc) | | $V_{DS(on)}$ | – | – | 0.25 | Vdc |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 0.75 Adc, $T_J$ = 150°C) | | | – | – | 0.24 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | 1.0 | 3.5 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 350 | 490 | pF |
| Output Capacitance | | $C_{oss}$ | – | 110 | 150 | |
| Transfer Capacitance | | $C_{rss}$ | – | 29 | 60 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 1.5 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 9.5 | 20 | ns |
| Rise Time | | $t_r$ | – | 18 | 40 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | 70 | |
| Fall Time | | $t_f$ | – | 22 | 40 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 1.5 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 9.0 | 10 | nC |
| | | $Q_1$ | – | 1.0 | – | |
| | | $Q_2$ | – | 4.0 | – | |
| | | $Q_3$ | – | 3.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.82 | 1.2 | Vdc |
| | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 0.68 | – | |
| Reverse Recovery Time | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 41 | – | ns |
| | | $t_a$ | – | 29 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.066 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

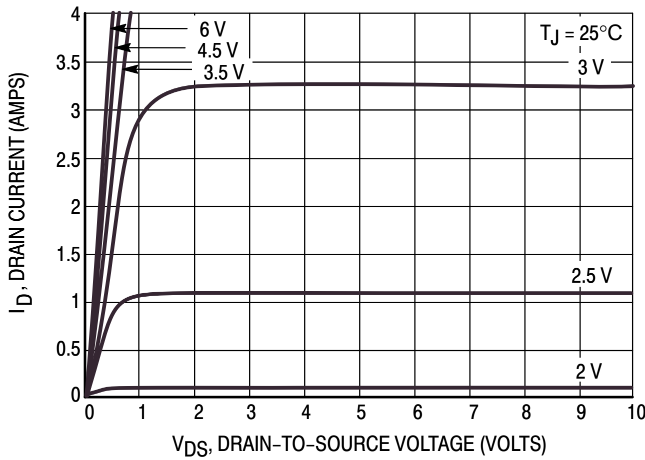



**Figure 1. On–Region Characteristics**

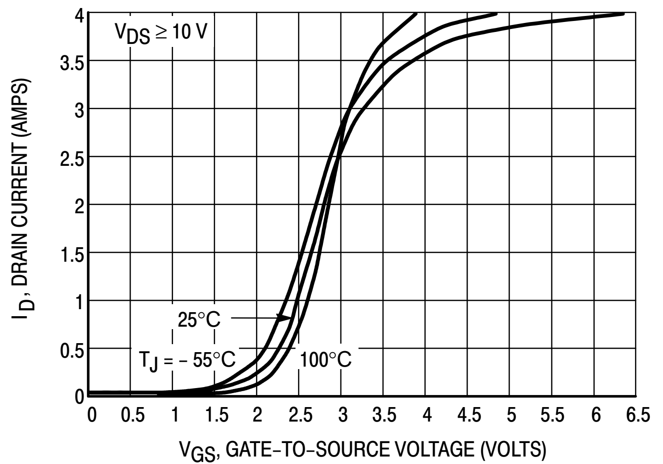



**Figure 2. Transfer Characteristics**

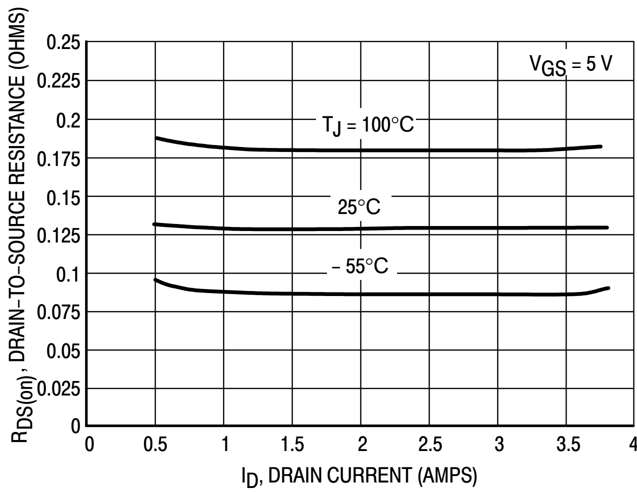



**Figure 3. On–Resistance versus Drain Current and Temperature**

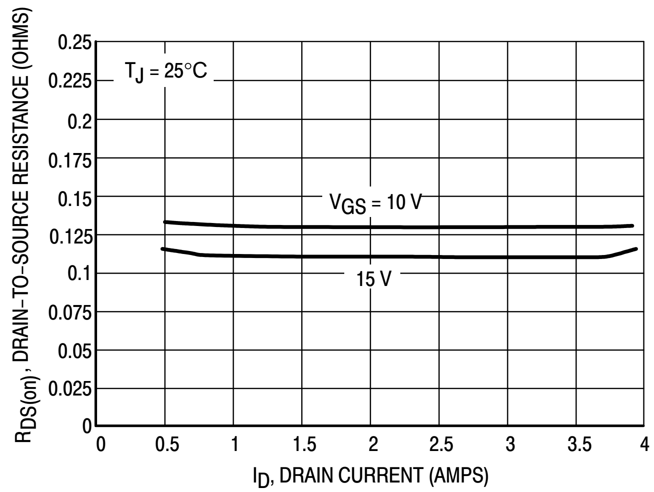



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

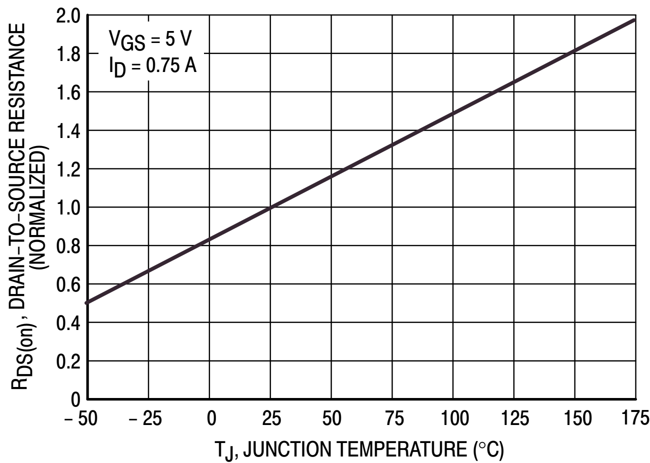



**Figure 5. On–Resistance Variation with Temperature**

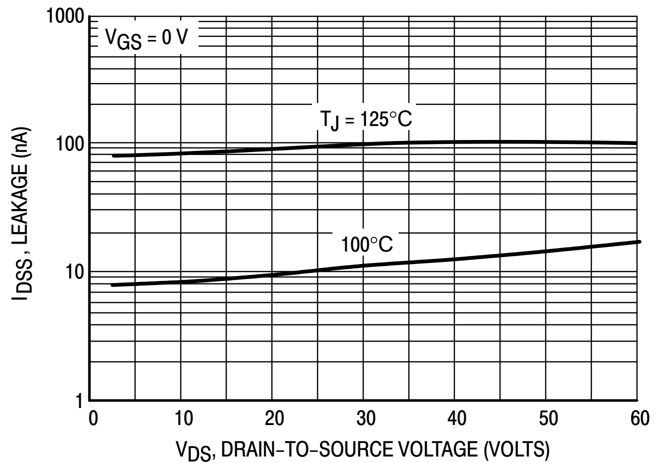



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \mathrm{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \mathrm{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

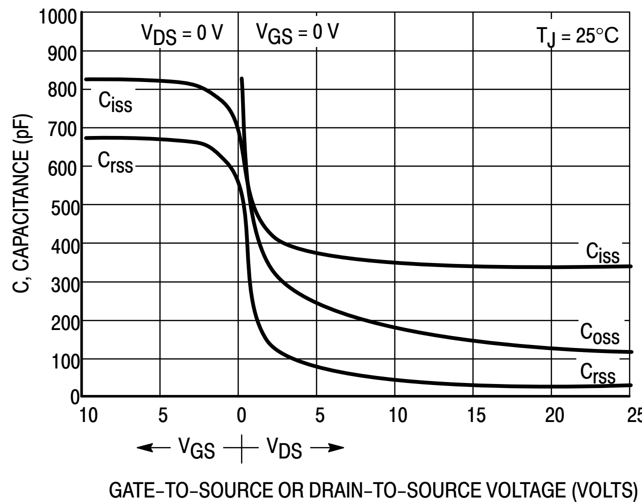



**Figure 7. Capacitance Variation**

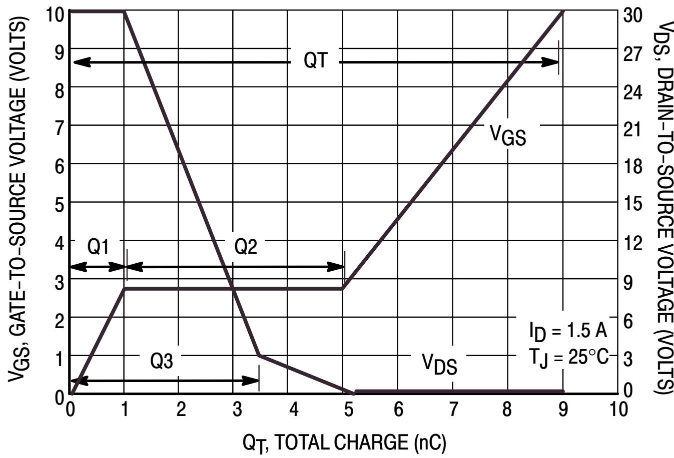



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

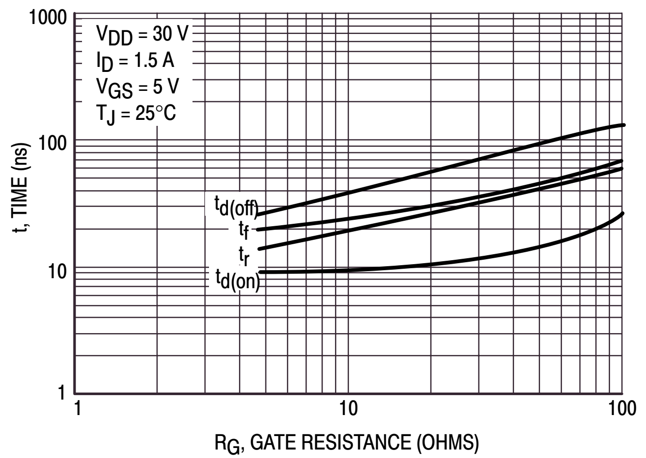



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

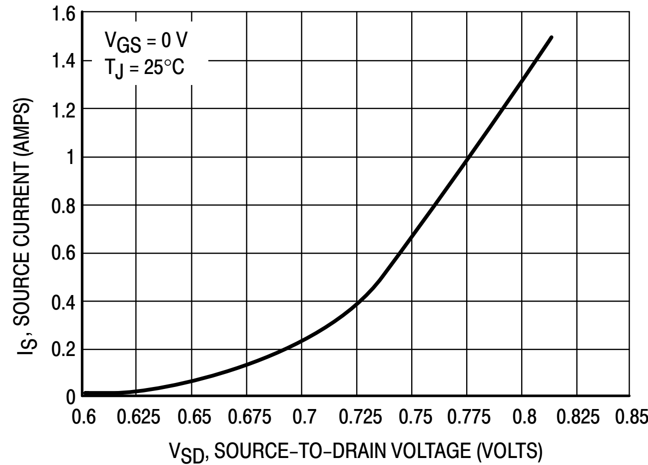



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

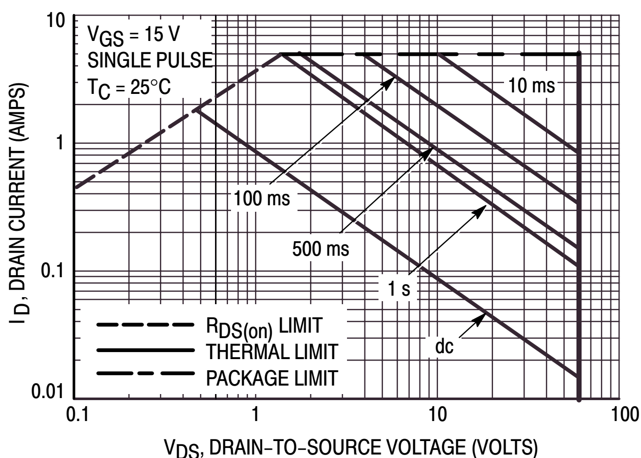



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

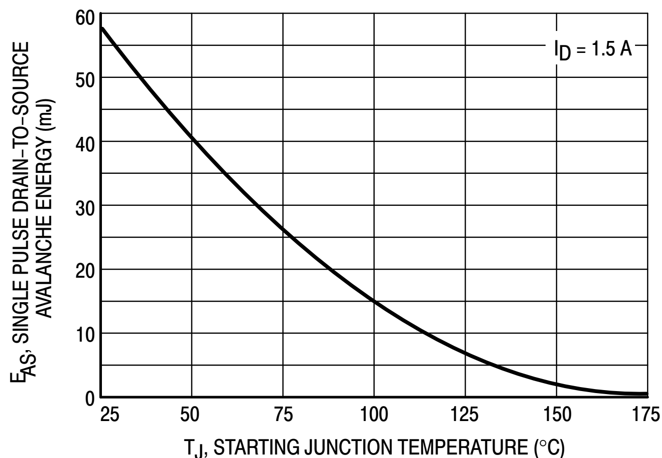



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

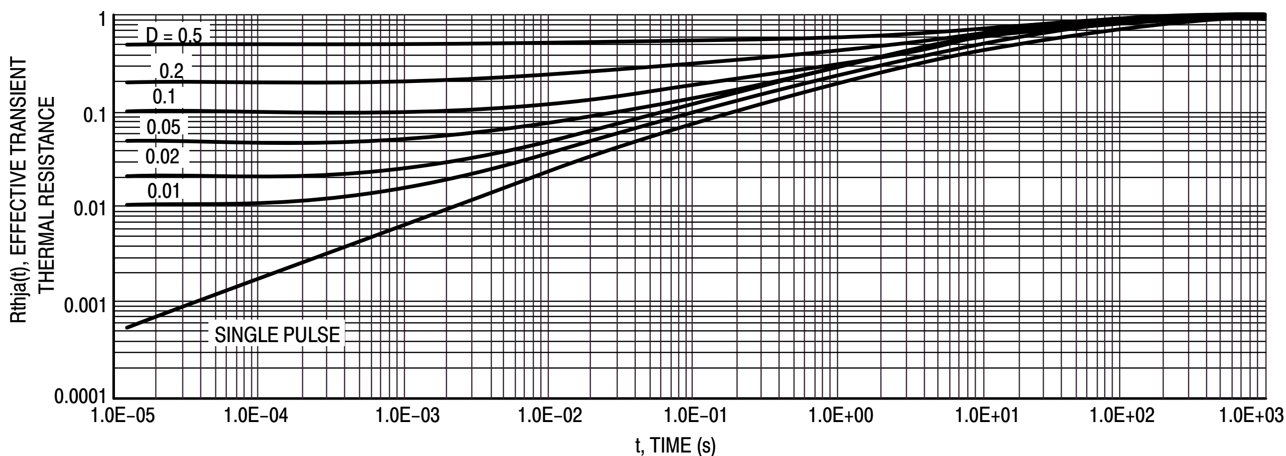



**Figure 13. Thermal Response**

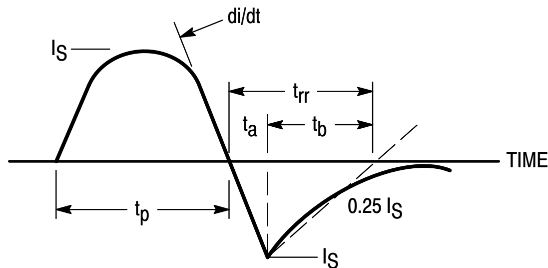
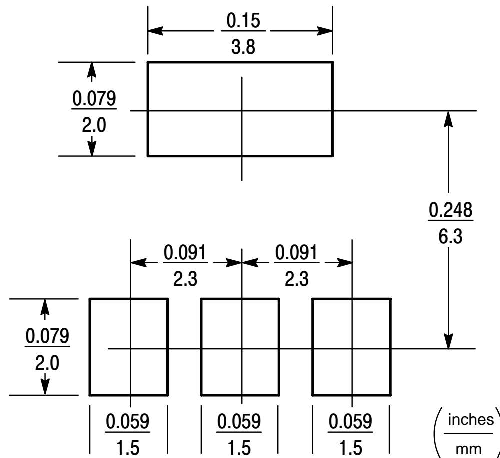



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 943 milliwatts.

$$P_D = \frac{175°C - 25°C}{159°C/W} = 943 \text{ milliwatts}$$

The 159°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 943 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

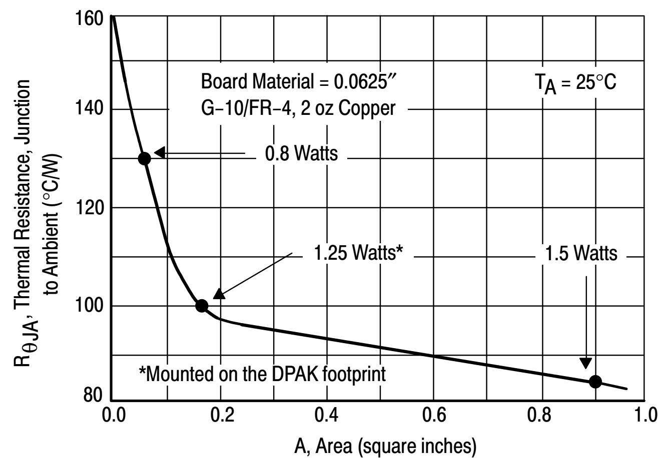



**Figure 15. Thermal Resistance versus Drain Pad Area for the SOT–223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT–223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

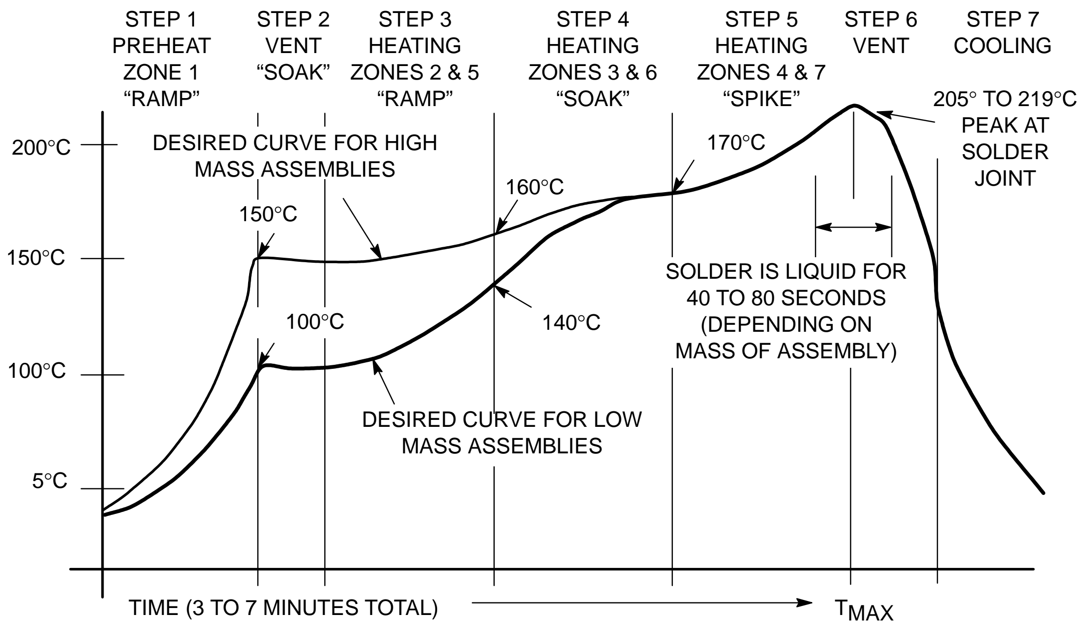



**Figure 16. Typical Solder Heating Profile**

# MMFT5P03HD

**Preferred Device**

# Power MOSFET 5 Amps, 30 Volts

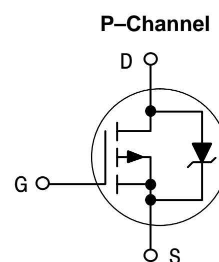
## P–Channel SOT–223

**ON Semiconductor™**

**http://onsemi.com**

**5 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 100 mΩ**

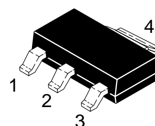
**P–Channel**



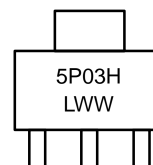

This miniature surface mount MOSFET features ultra low $R_{DS(on)}$ and true logic level performance. It is capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MMFT5P03HD devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SOT–223 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified

**MARKING DIAGRAM**

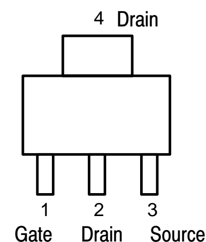



**TO–261AA**
**CASE 318E**
**STYLE 3**




L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT5P03HDT3 | SOT–223 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)
**Negative sign for P–Channel devices omitted for clarity**

| Rating | | Symbol | Max | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | | $V_{DSS}$ | 30 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | | $V_{DGR}$ | 30 | V |
| Gate–to–Source Voltage – Continuous | | $V_{GS}$ | ± 20 | V |
| 1″ SQ.<br>FR–4 or G–10 PCB<br><br><br>10 seconds | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 40<br>3.13<br>25<br>5.2<br>4.1<br>26 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Minimum<br>FR–4 or G–10 PCB<br><br><br>10 seconds | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 80<br>1.56<br>12.5<br>3.7<br>2.9<br>19 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Operating and Storage Temperature Range | | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 12 Apk, L = 3.5 mH, $R_G$ = 25 Ω) | | $E_{AS}$ | 250 | mJ |

1. Repetitive rating; pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>28 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS(1)** | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.75<br>3.5 | <br>3.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 5.2 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.6 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>79<br>119 | <br>100<br>150 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 2.0 Adc) (Note 2.) | | $g_{FS}$ | 2.0 | 4.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 475 | 950 | pF |
| Output Capacitance | | $C_{oss}$ | – | 220 | 440 | |
| Transfer Capacitance | | $C_{rss}$ | – | 70 | 140 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) (Note 2.) | $t_{d(on)}$ | – | 12 | 24 | ns |
| Rise Time | | $t_r$ | – | 24 | 48 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 47 | 94 | |
| Fall Time | | $t_f$ | – | 46 | 92 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) (Note 2.) | $t_{d(on)}$ | – | 19 | 38 | |
| Rise Time | | $t_r$ | – | 55 | 110 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 60 | |
| Fall Time | | $t_f$ | – | 40 | 80 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 10 Vdc) (Note 2.) | $Q_T$ | – | 17 | 24 | nC |
| | | $Q_1$ | – | 1.7 | – | |
| | | $Q_2$ | – | 6.3 | – | |
| | | $Q_3$ | – | 4.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.1<br>0.89 | 1.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 39 | – | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 19 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.042 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

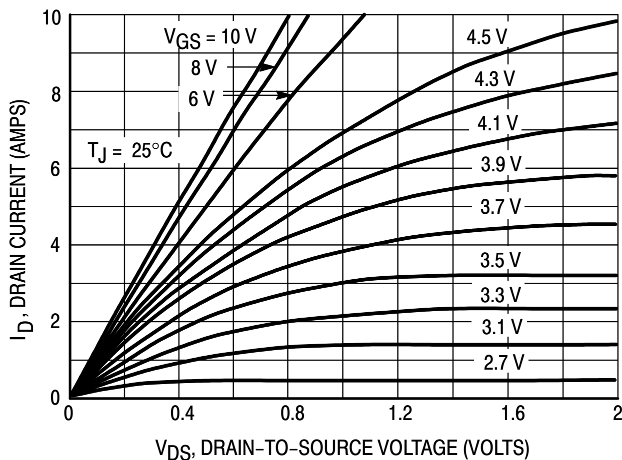



**Figure 1. On–Region Characteristics**

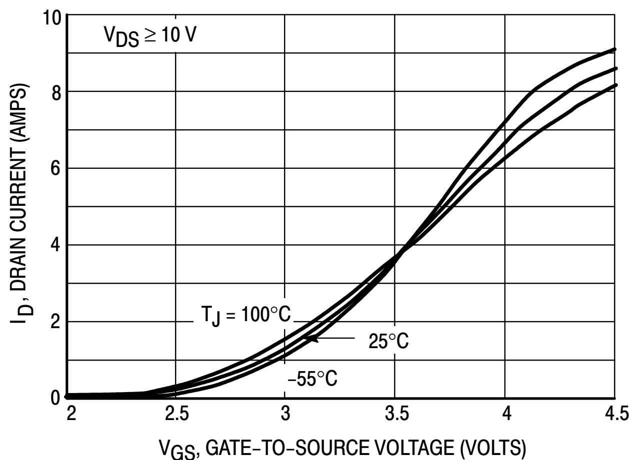



**Figure 2. Transfer Characteristics**

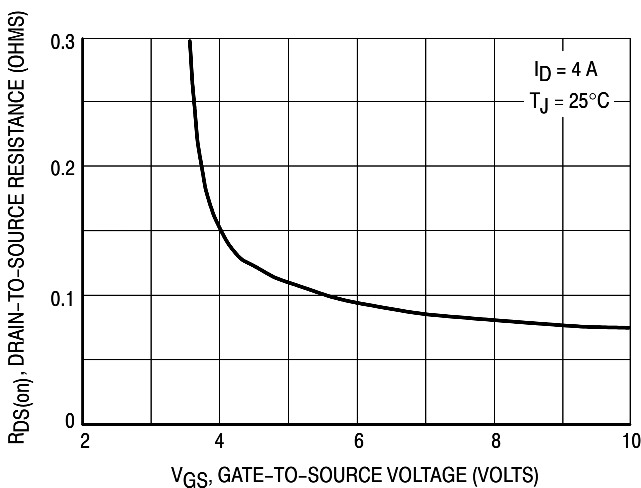



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

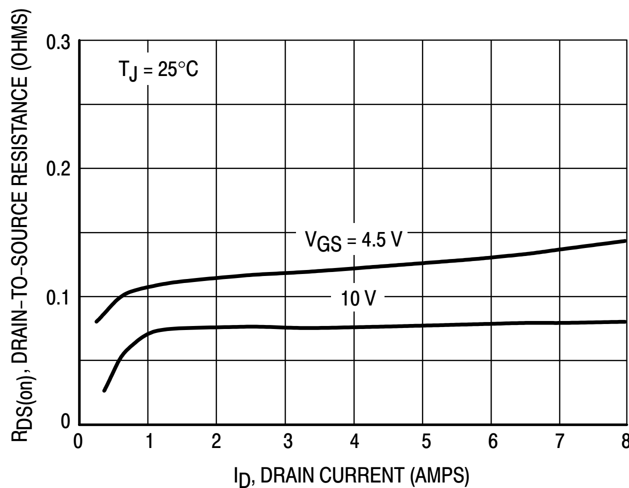



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

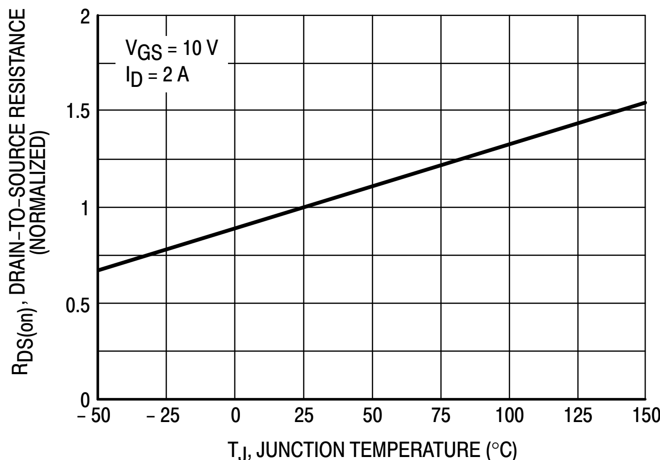



**Figure 5. On–Resistance Variation with Temperature**

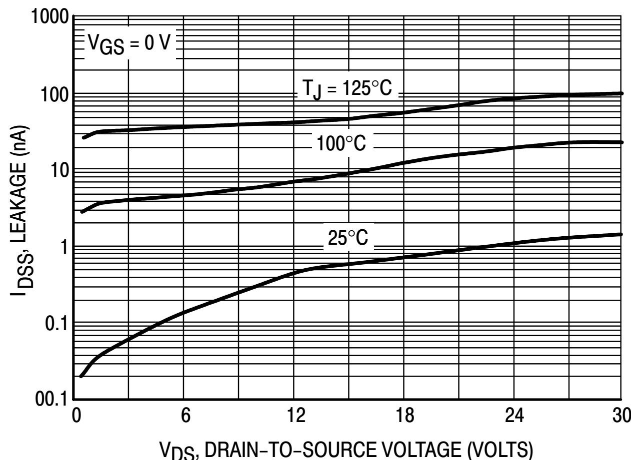



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{ In } [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \text{ In } (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

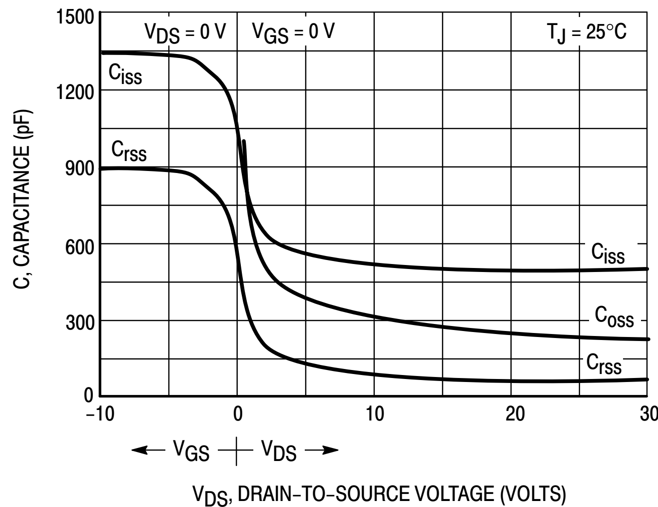



**Figure 7. Capacitance Variation**

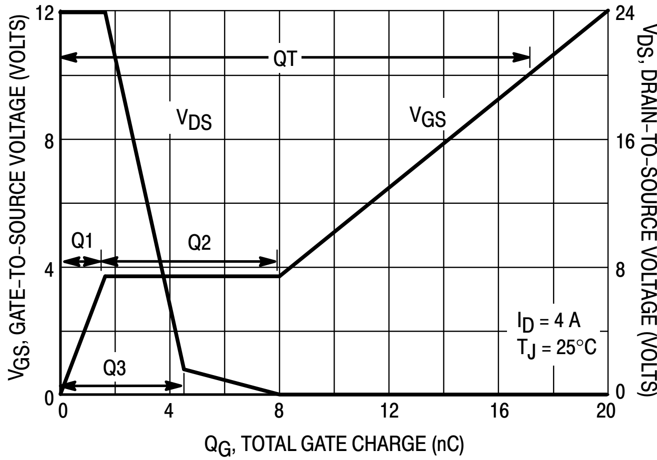



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

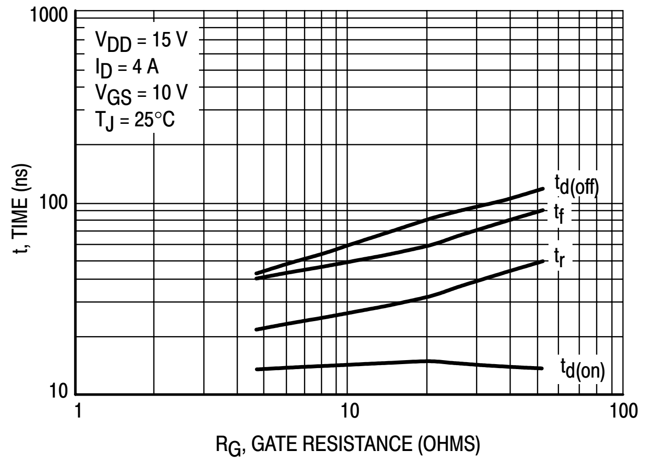



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

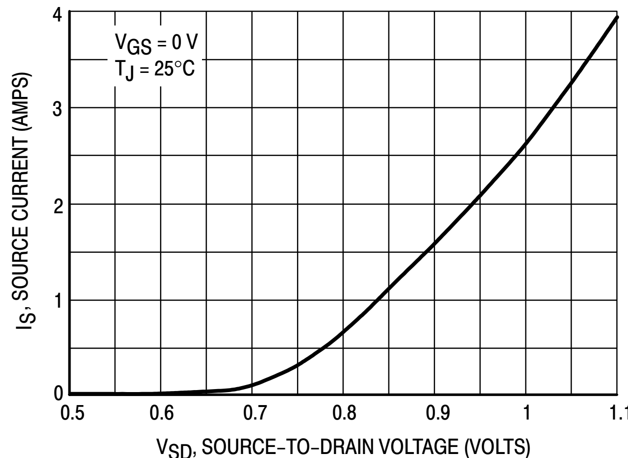



Figure 10. Diode Forward Voltage versus Current

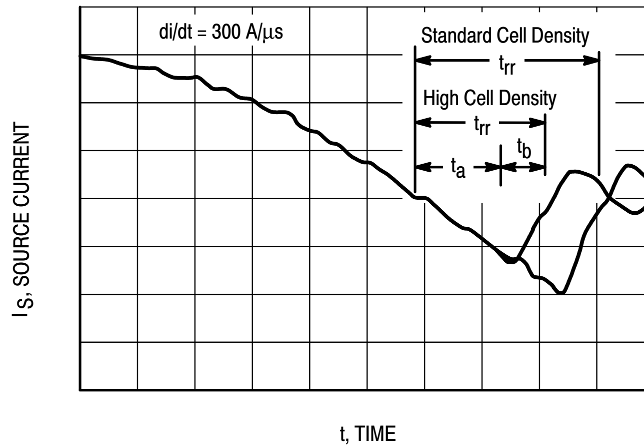



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

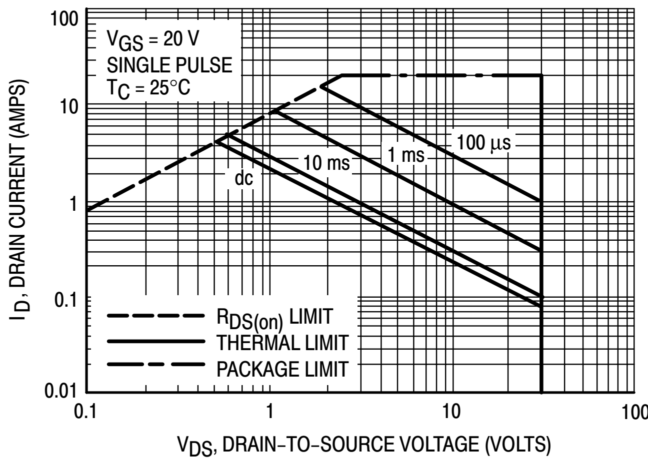



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

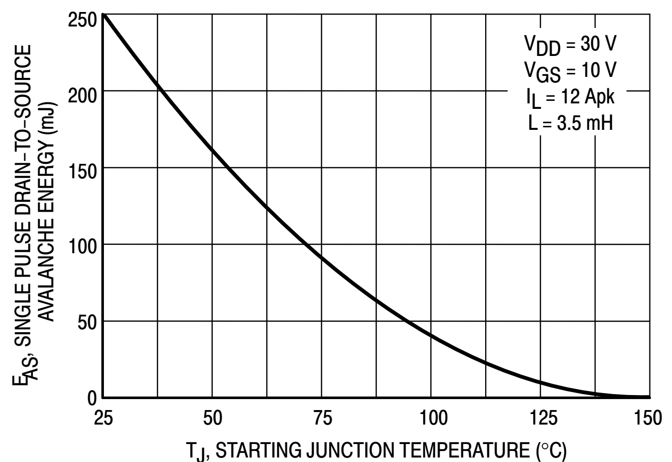



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

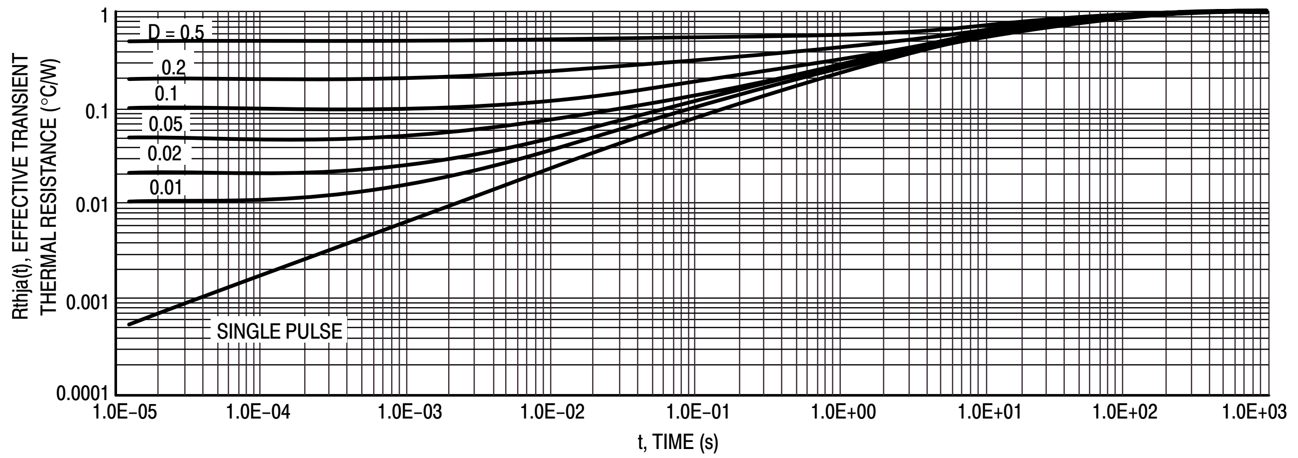



**Figure 14. Thermal Response**

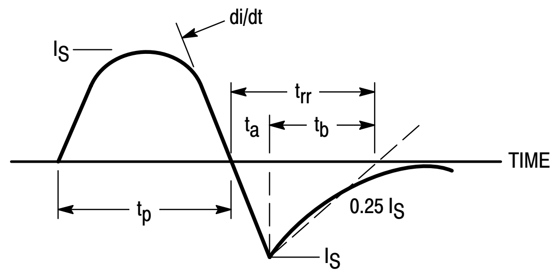
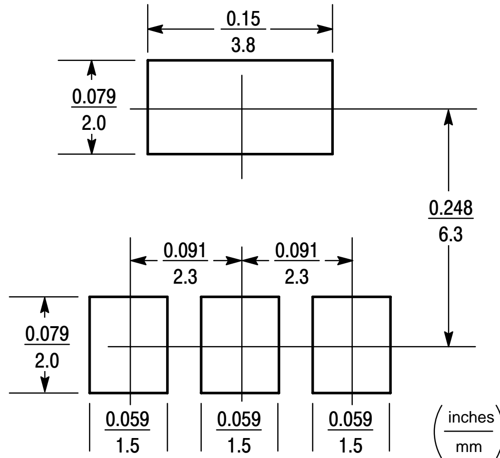



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SOT–223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## SOT–223 POWER DISSIPATION

The power dissipation of the SOT–223 is a function of the drain pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT–223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 3.13 watts.

$$P_D = \frac{150°C - 25°C}{40°C/W} = 3.13 \text{ watts}$$

The 40°C/W for the SOT–223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.13 watts. There are other alternatives to achieving higher power dissipation from the SOT–223 package. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology.

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

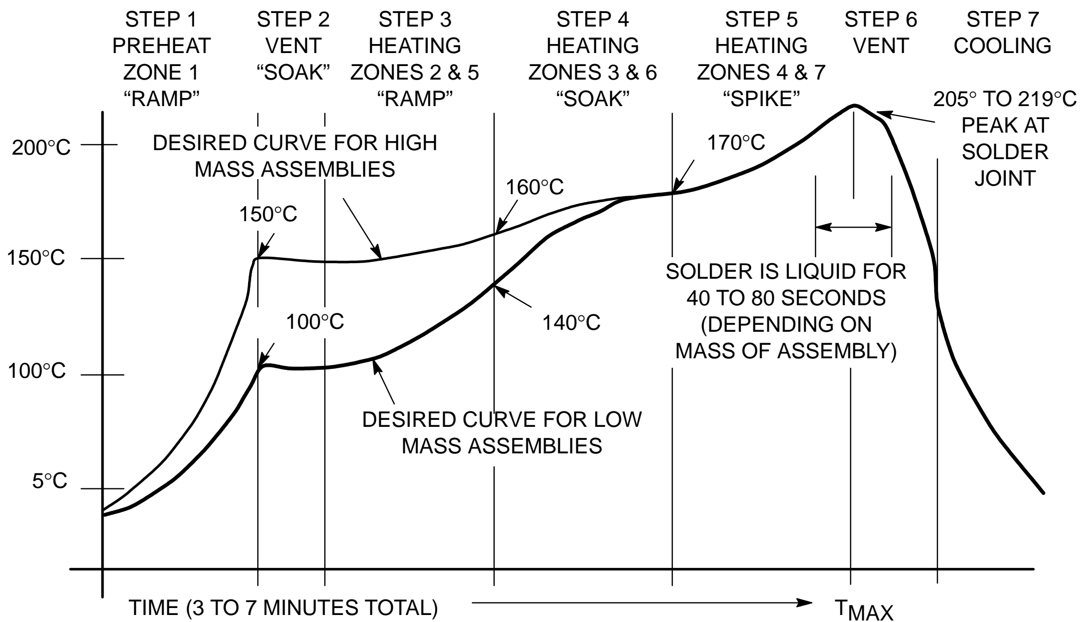



**Figure 16. Typical Solder Heating Profile**

# MMFT960T1

Preferred Device

# Power MOSFET 300 mA, 60 Volts

## N–Channel SOT–223

**ON Semiconductor™**

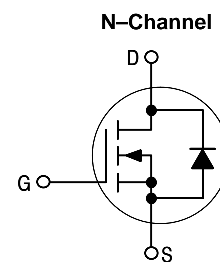
http://onsemi.com

This Power MOSFET is designed for high speed, low loss power switching applications such as switching regulators, dc–dc converters, solenoid and relay drivers. The device is housed in the SOT–223 package which is designed for medium power surface mount applications.

- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement
- The SOT–223 Package can be soldered using wave or reflow. The formed leads absorb thermal stress during soldering eliminating the possibility of damage to the die.

**300 mA**
**60 VOLTS**
**$R_{DS(on)}$ = 1.7 Ω**

N–Channel




**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

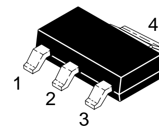
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DS}$ | 60 | Volts |
| Gate–to–Source Voltage – Non–Repetitive | $V_{GS}$ | ±30 | Volts |
| Drain Current | $I_D$ | 300 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Derate above 25°C | $P_D$ | 0.8<br>6.4 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |

**THERMAL CHARACTERISTICS**

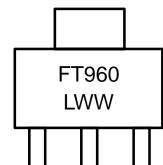
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance – Junction–to–Ambient | $R_{\theta JA}$ | 156 | °C/W |
| Maximum Temperature for Soldering Purposes<br>Time in Solder Bath | $T_L$ | 260<br>10 | °C<br>Sec |

1. Device mounted on a FR–4 glass epoxy printed circuit board using minimum recommended footprint.

**MARKING DIAGRAM**

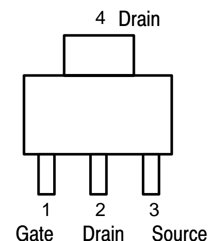



**TO–261AA**
**CASE 318E**
**STYLE 3**




FT960 = Device Code
L = Location Code
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMFT960T1 | SOT–223 | 1000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 μA) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 V, $V_{GS}$ = 0) | | $I_{DSS}$ | – | – | 10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 50 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 1.0 | – | 3.5 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1.0 A) | | $R_{DS(on)}$ | – | – | 1.7 | Ohms |
| Drain–to–Source On–Voltage | | $V_{DS(on)}$ | | | | Vdc |
| ($V_{GS}$ = 10 V, $I_D$ = 0.5 A) | | | – | – | 0.8 | |
| ($V_{GS}$ = 10 V, $I_D$ = 1.0 A) | | | – | – | 1.7 | |
| Forward Transconductance ($V_{DS}$ = 25 V, $I_D$ = 0.5 A) | | $g_{fs}$ | – | 600 | – | mmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 65 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 33 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 7.0 | – | |
| Total Gate Charge | ($V_{GS}$ = 10 V, $I_D$ = 1.0 A, $V_{DS}$ = 48 V) | $Q_g$ | – | 3.2 | – | nC |
| Gate–Source Charge | | $Q_{gs}$ | – | 1.2 | – | |
| Gate–Drain Charge | | $Q_{gd}$ | – | 2.0 | – | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

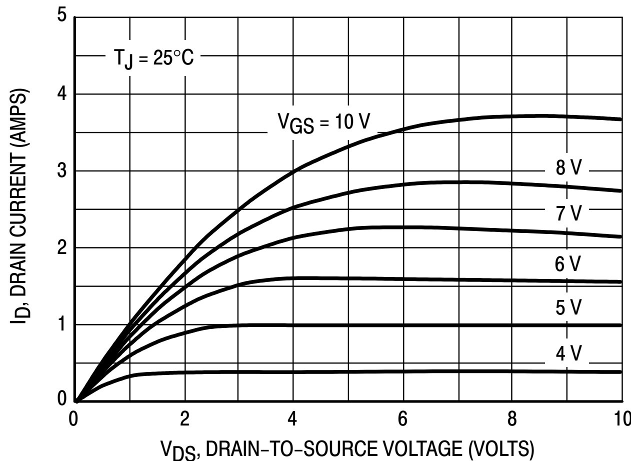


**Figure 1. On–Region Characteristics**

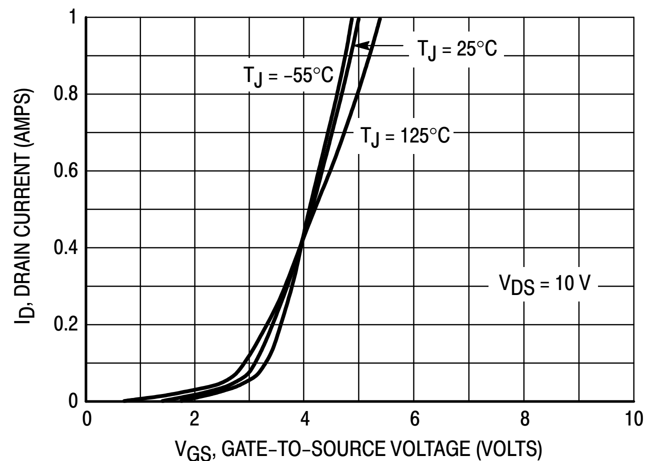


**Figure 2. Transfer Characteristics**

## TYPICAL ELECTRICAL CHARACTERISTICS

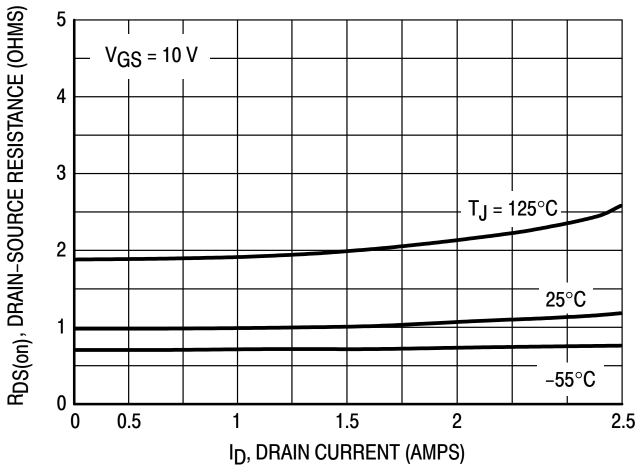


**Figure 3. On–Resistance versus Drain Current**

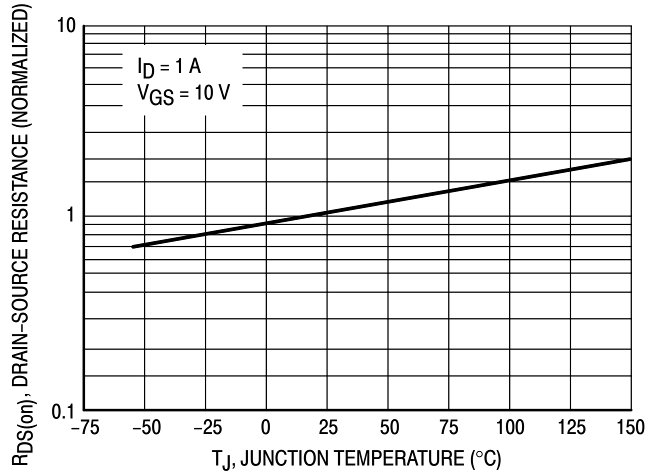


**Figure 4. On–Resistance Variation with Temperature**

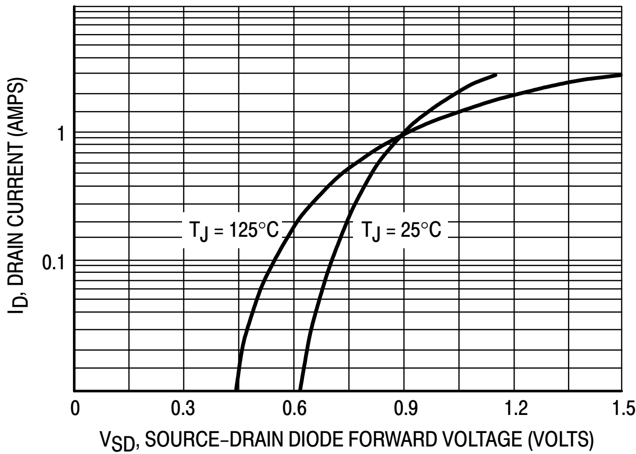


**Figure 5. Source–Drain Diode Forward Voltage**

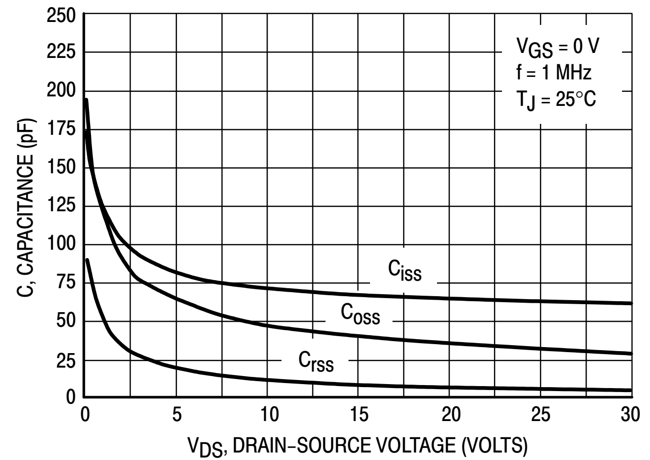


**Figure 6. Capacitance Variation**

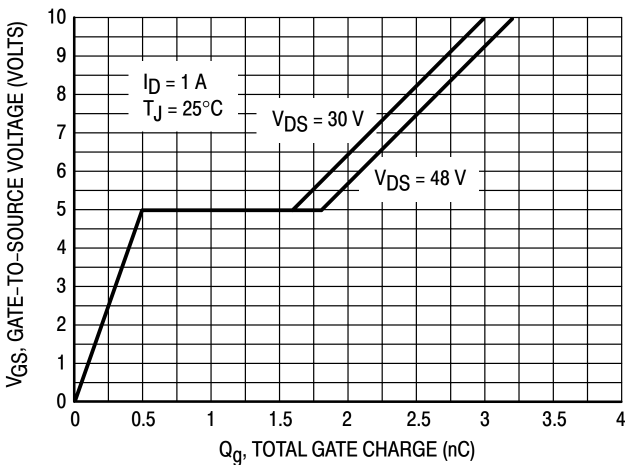


**Figure 7. Gate Charge versus Gate–to–Source Voltage**

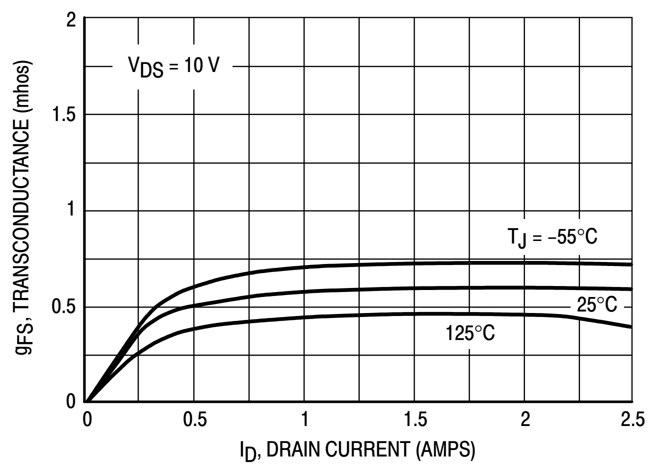


**Figure 8. Transconductance**

# INFORMATION FOR USING THE SOT-223 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

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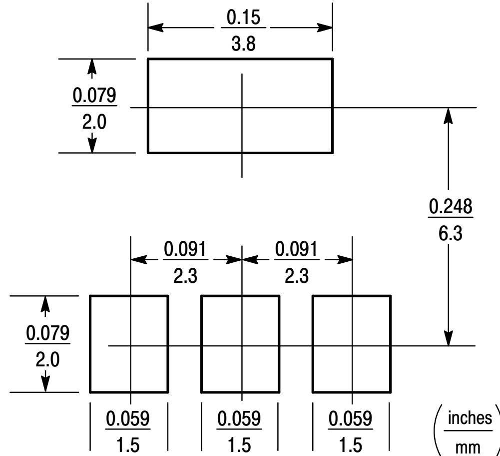



## SOT-223 POWER DISSIPATION

The power dissipation of the SOT-223 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet for the SOT-223 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.8 watts.

$$P_D = \frac{150°C - 25°C}{156°C/W} = 0.8 \text{ watts}$$

The 156°C/W for the SOT-223 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.8 watts. There are other alternatives to achieving higher power dissipation from the SOT-223 package. One is to increase the area of the collector pad. By increasing the area of the collector pad, the power dissipation can be increased. Although the power dissipation can almost be doubled with this method, area is taken up on the printed circuit board which can defeat the purpose of using surface mount technology. A graph of $R_{\theta JA}$ versus collector pad area is shown in Figure 9.

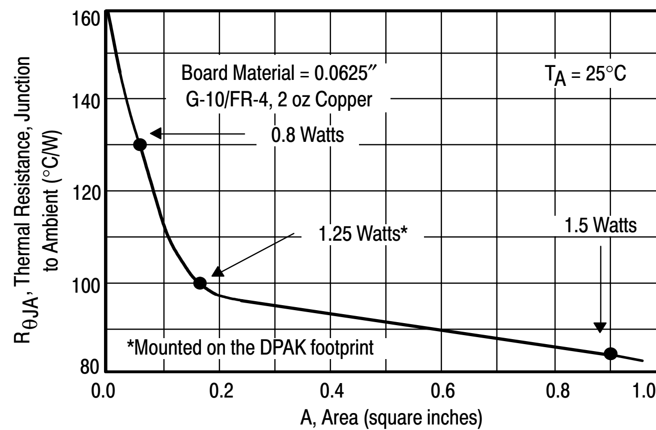



**Figure 9. Thermal Resistance versus Collector Pad Area for the SOT-223 Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. A solder stencil is required to screen the optimum amount of solder paste onto the footprint. The stencil is made of brass or stainless steel with a typical thickness of 0.008 inches. The stencil opening size for the SOT-223 package should be the same as the pad size on the printed circuit board, i.e., a 1:1 registration.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference should be a maximum of 10°C.
- The soldering temperature and time should not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient should be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 10 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

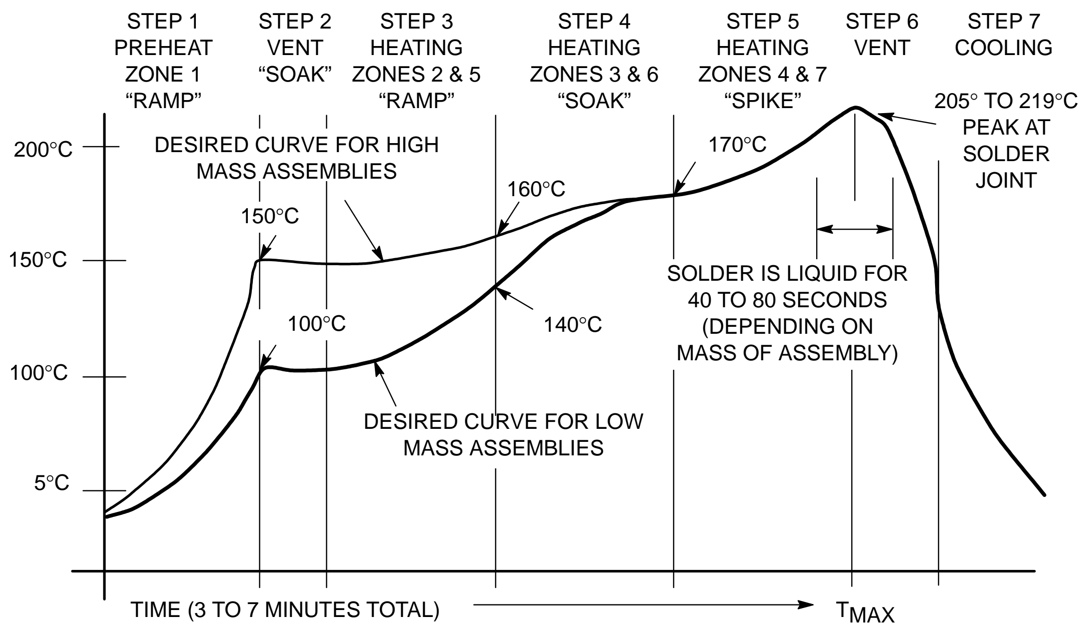



**Figure 10. Typical Solder Heating Profile**

# MMSF10N02Z

Preferred Device

# Power MOSFET
# 10 Amps, 20 Volts
## N–Channel SO–8

**ON Semiconductor™**

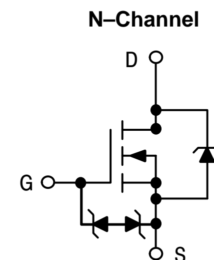
http://onsemi.com

**10 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 15 mΩ**

EZFETs™ are an advanced series of Power MOSFETs which contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important.

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**N–Channel**

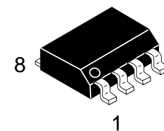



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

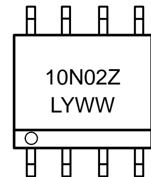
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 12 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 70°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 10<br>7.0<br>80 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Thermal Resistance – Junction to Ambient | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Temperature for Soldering | $T_L$ | 260 | °C |

1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 4.5 V, @ 10 Seconds)

**MARKING DIAGRAM**

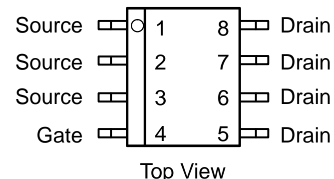



**SO–8**
**CASE 751**
**STYLE 12**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF10N02ZR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>20<br>– | <br>–<br>17 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 12 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | 0.6 | 1.5 | µAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>0.5<br>– | <br>0.72<br>2.86 | <br>1.1<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 2.7 Vdc, $I_D$ = 5.0 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>13<br>16 | <br>15<br>19 | mΩ |
| Forward Transconductance ($V_{DS}$ = 9.0 Vdc, $I_D$ = 5.0 Adc) | | $g_{FS}$ | 11 | 14 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1150 | 1225 | pF |
| Output Capacitance | | $C_{oss}$ | – | 775 | 810 | |
| Transfer Capacitance | | $C_{rss}$ | – | 375 | 480 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.0 Vdc, $R_G$ = 10 Ω) | $t_{d(on)}$ | – | 65 | 75 | ns |
| Rise Time | | $t_r$ | – | 360 | 440 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 325 | 640 | |
| Fall Time | | $t_f$ | – | 575 | 860 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 10 Adc, $V_{GS}$ = 4.0 Vdc) | $Q_T$ | – | 26 | 32 | nC |
| | | $Q_1$ | – | 2.5 | – | |
| | | $Q_2$ | – | 13 | – | |
| | | $Q_3$ | – | 9.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.83<br>0.68 | <br>1.2<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 765 | – | ns |
| | | $t_a$ | – | 240 | – | |
| | | $t_b$ | – | 530 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 8.7 | – | µC |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

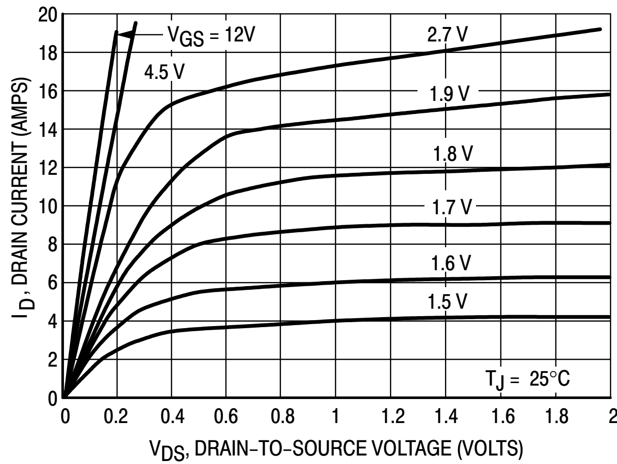



**Figure 1. On–Region Characteristics**

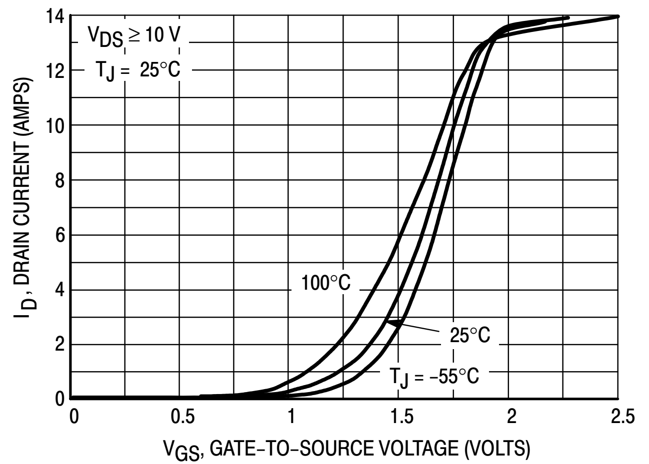



**Figure 2. Transfer Characteristics**

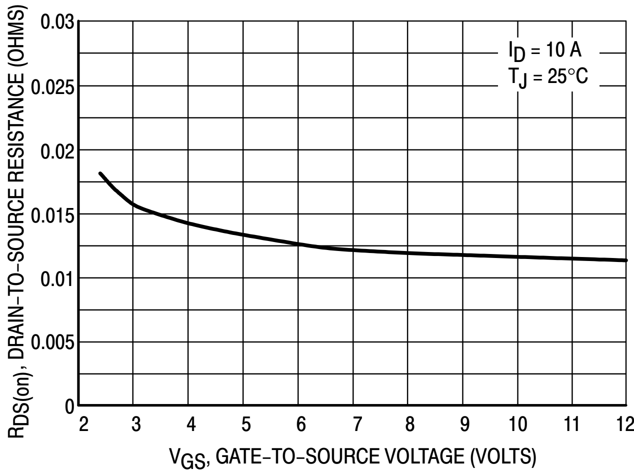



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

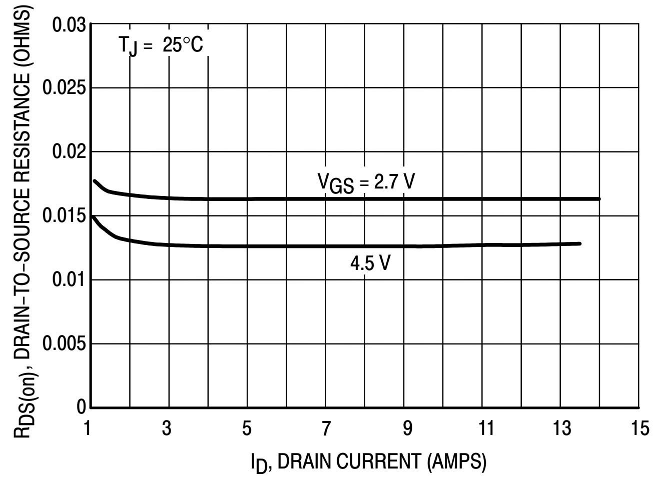



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

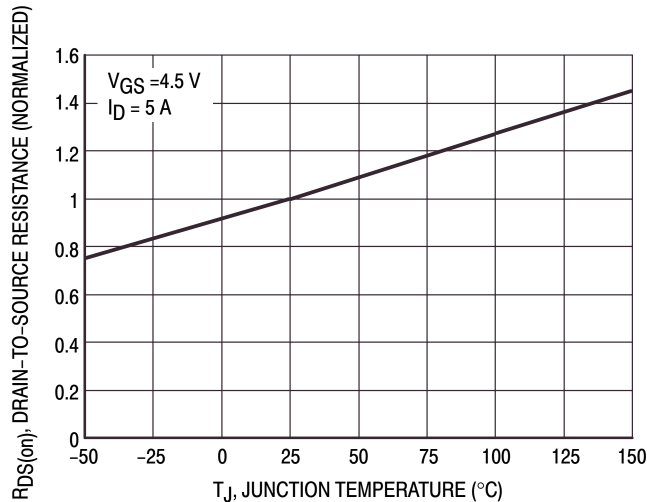



**Figure 5. On–Resistance Variation with Temperature**

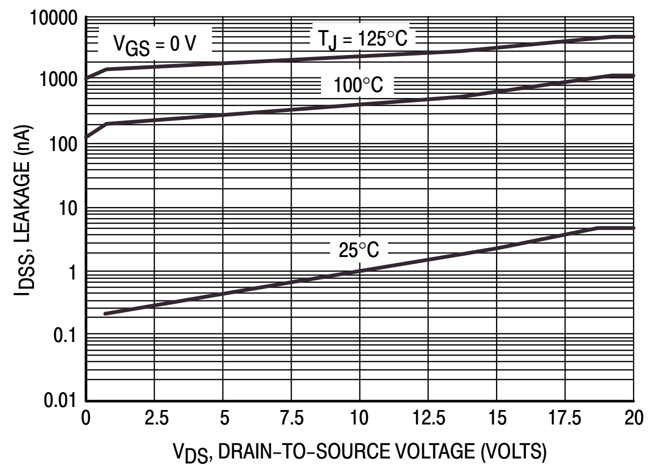



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{In} [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \text{In} (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

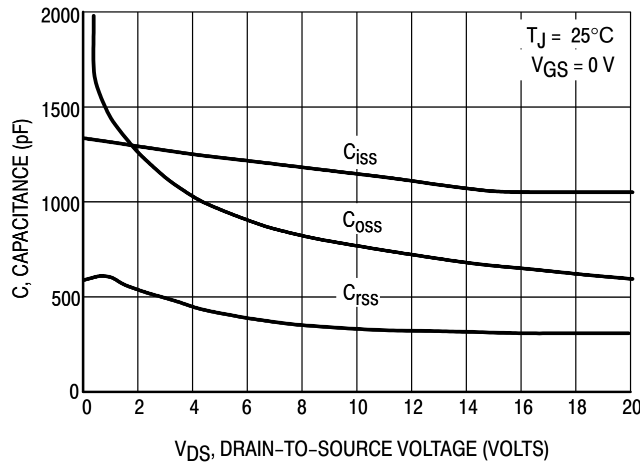



**Figure 7. Capacitance Variation**

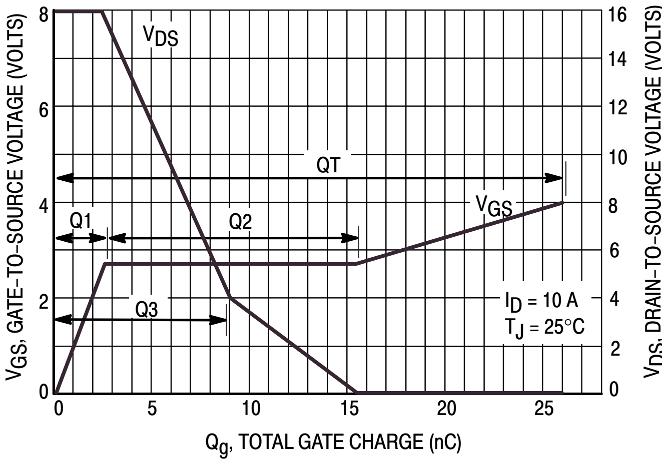



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

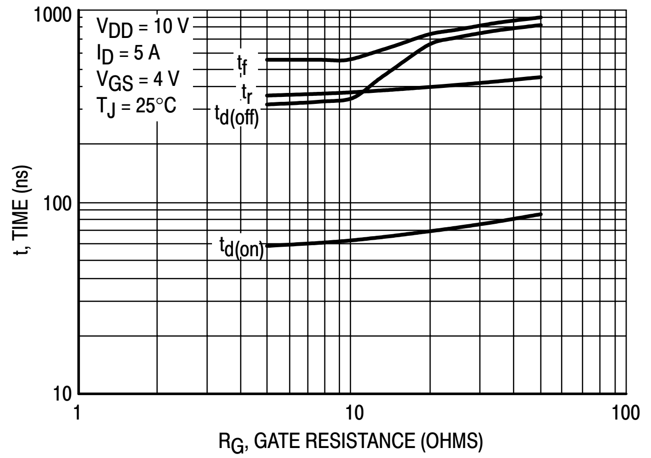



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

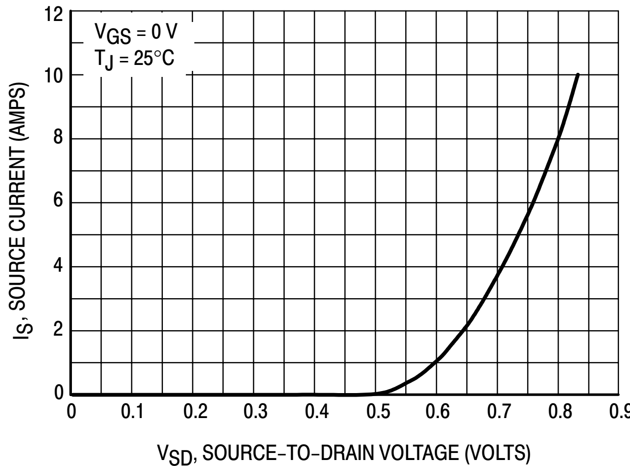



Figure 10. Diode Forward Voltage versus Current

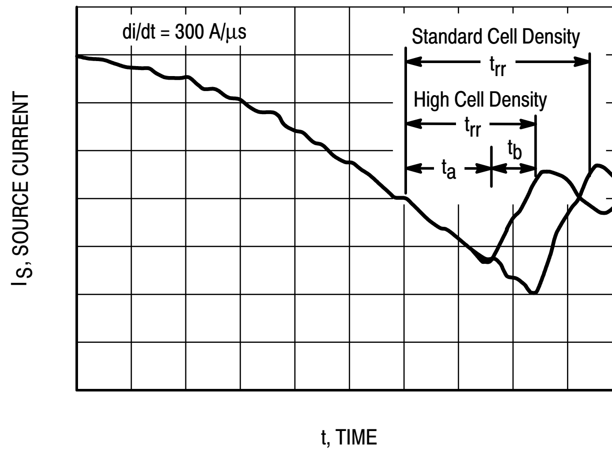



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

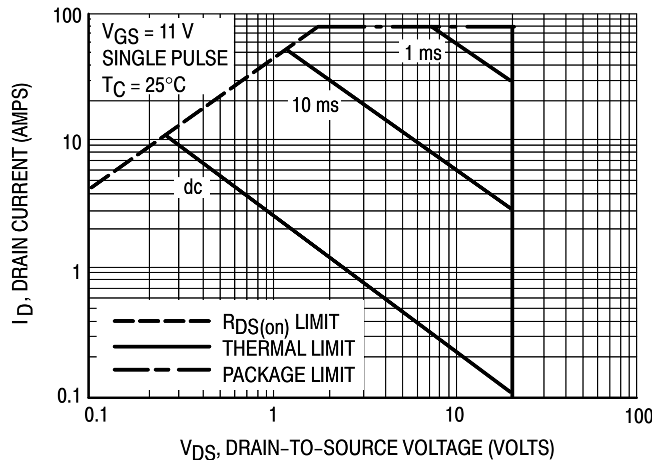



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

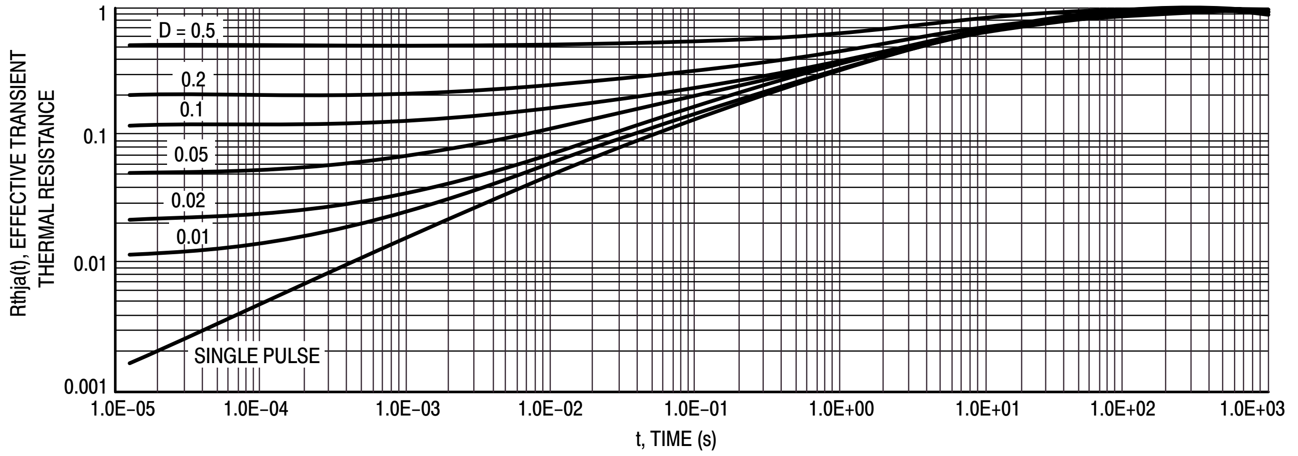



**Figure 13. Thermal Response**

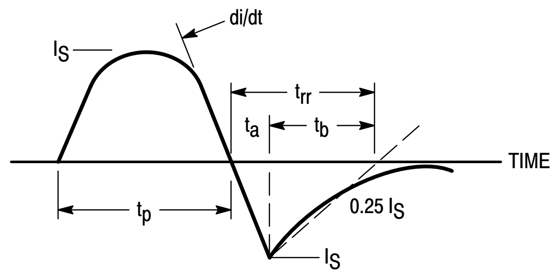
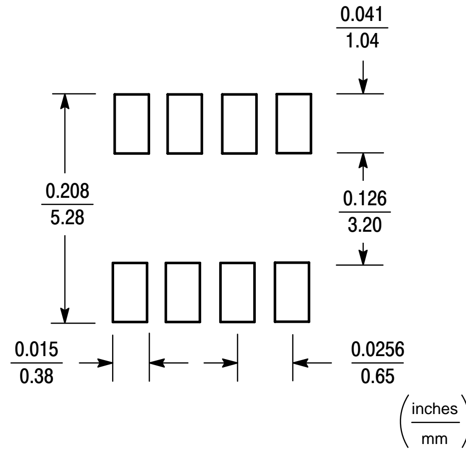



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

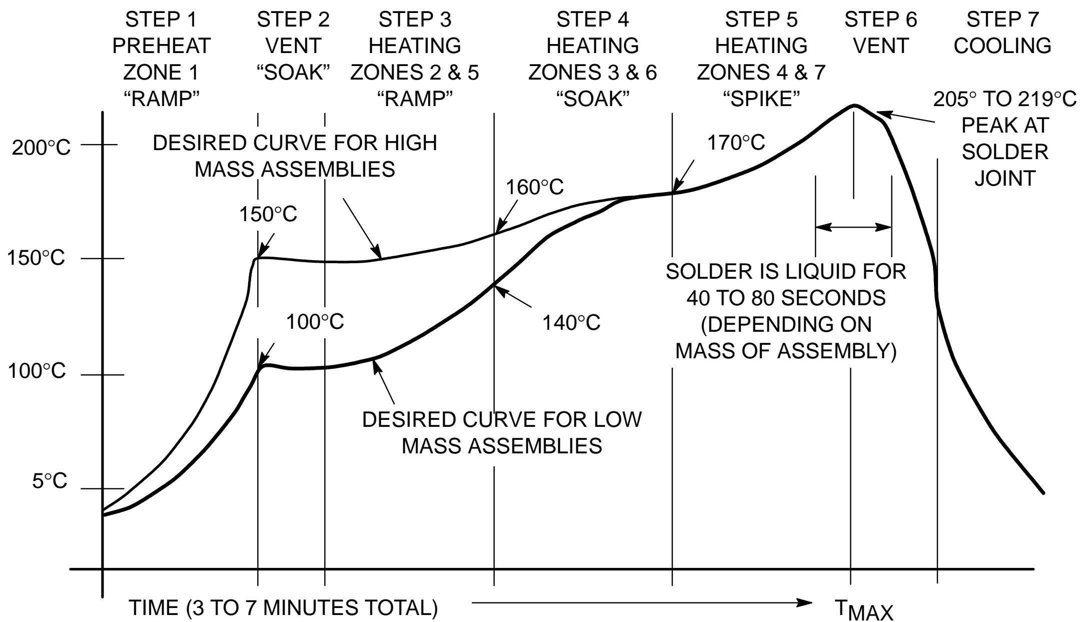



**Figure 15. Typical Solder Heating Profile**

# MMSF10N03Z

**Preferred Device**

*Advance Information*

# Power MOSFET 10 Amps, 30 Volts

## N–Channel SO–8

**ON Semiconductor™**

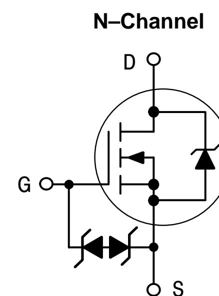
**http://onsemi.com**

**10 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 13 mΩ**

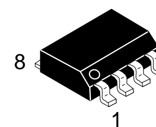
EZFETs™ are an advanced series of Power MOSFETs contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Zener Protected Gates Provide Electrostatic Discharge Protection
- Designed to Withstand 200 V Machine Model and 2000 V Human Body Model
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

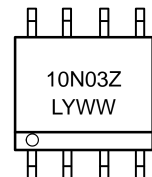
**N–Channel**




**MARKING DIAGRAM**

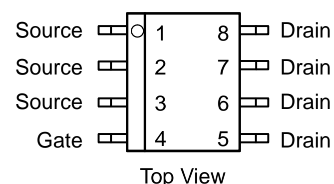



**SO–8**
**CASE 751**
**STYLE 12**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF10N03ZR2 | SO–8 | 2500 Tape & Reel |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C (Note 1.)<br>– Continuous @ $T_A$ = 70°C (Note 1.)<br>– Pulsed Drain Current (Note 3.) | $I_D$<br>$I_D$<br>$I_{DM}$ | 10<br>7.7<br>50 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Linear Derating Factor @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5<br>20 | Watts<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Linear Derating Factor @ $T_A$ = 25°C (Note 2.) | $P_D$ | 1.6<br>12 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 10 Apk, L = 20 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 1000 | mJ |

**THERMAL RESISTANCE**

| Parameter | Symbol | Typ | Max | Unit |
|---|---|---|---|---|
| Junction–to–Ambient (Note 1.)<br>Junction–to–Ambient (Note 2.) | $R_{\theta JA}$ | –<br>– | 50<br>80 | °C/W |

1. When mounted on 1″ square FR4 or G–10 board ($V_{GS}$ = 10 V, @ 10 seconds).
2. When mounted on minimum recommended FR4 or G–10 board ($V_{GS}$ = 10 V, @ Steady State).
3. Repetitive rating; pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>65 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 3.0 | μAdc |
| **ON CHARACTERISTICS(1)** | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.2<br>3.5 | <br>1.7<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>10<br>13 | <br>13<br>18 | mΩ |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc) (Note 4.) | | $g_{FS}$ | 7.0 | 13 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 720 | 1010 | pF |
| Output Capacitance | | $C_{oss}$ | – | 570 | 800 | |
| Transfer Capacitance | | $C_{rss}$ | – | 78 | 110 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) (Note 4.) | $t_{d(on)}$ | – | 35 | 70 | ns |
| Rise Time | | $t_r$ | – | 105 | 210 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 970 | 1940 | |
| Fall Time | | $t_f$ | – | 550 | 1100 | |
| Gate Charge<br>See Figure 8 | ($V_{DS}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) (Note 4.) | $Q_T$ | – | 46 | 64 | nC |
| | | $Q_1$ | – | 3.8 | – | |
| | | $Q_2$ | – | 11 | – | |
| | | $Q_3$ | – | 8.1 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.80<br>0.70 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4.) | $t_{rr}$ | – | 460 | – | ns |
| | | $t_a$ | – | 180 | – | |
| | | $t_b$ | – | 280 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 4.2 | – | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
6. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

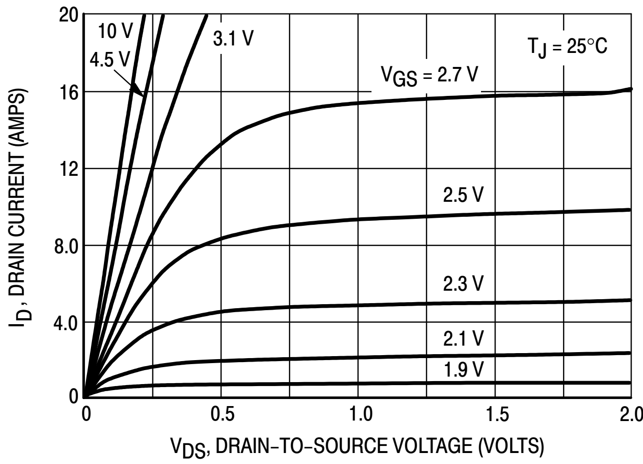



**Figure 1. On–Region Characteristics**

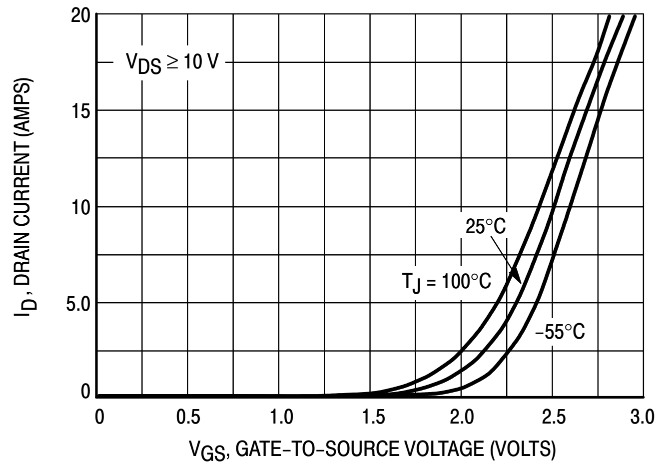



**Figure 2. Transfer Characteristics**

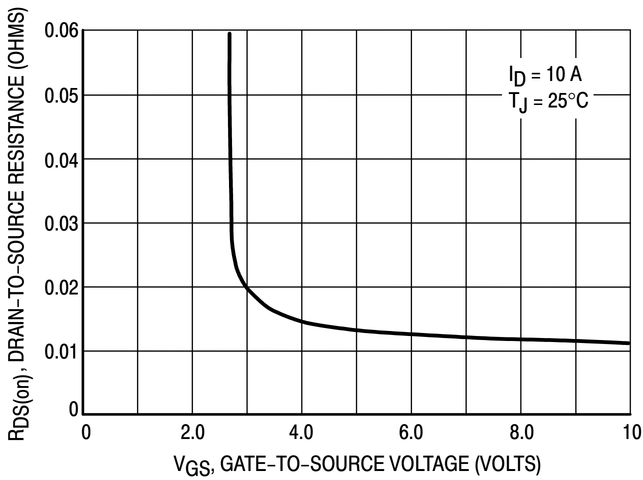



**Figure 3. On–Resistance versus Drain Current**

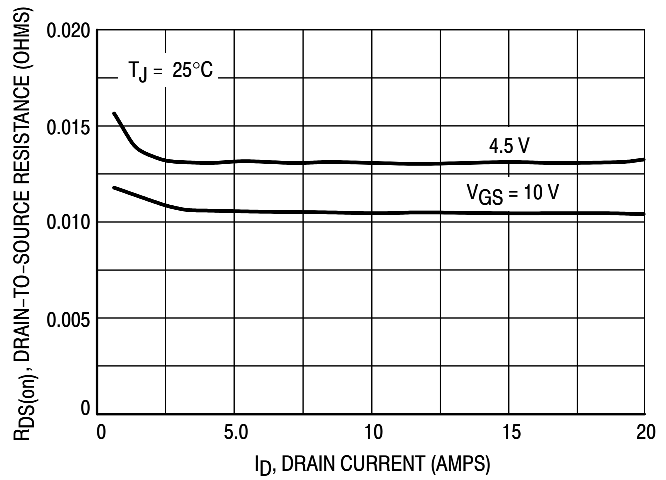



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

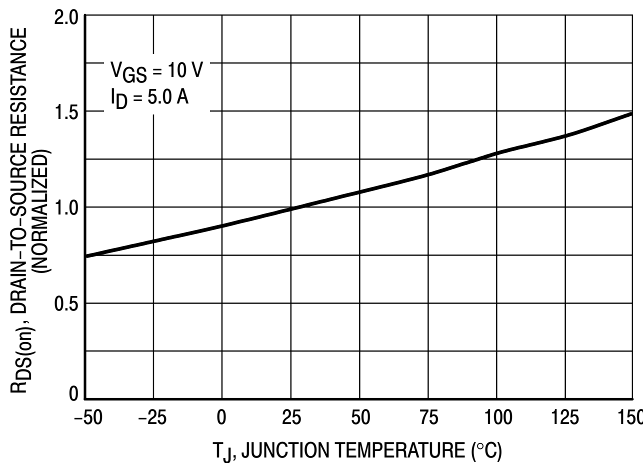



**Figure 5. On–Resistance Variation with Temperature**

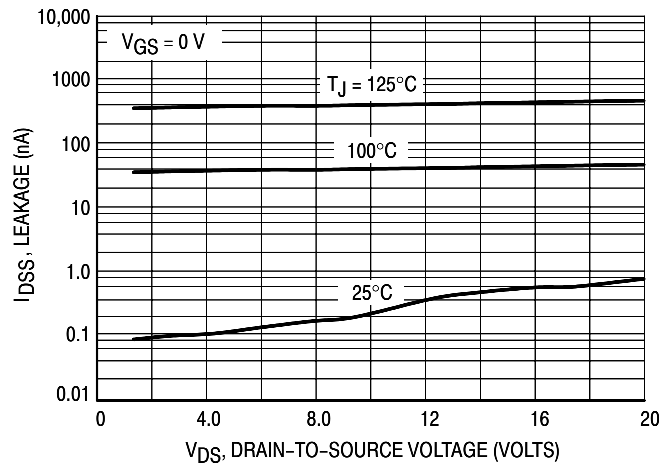



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \ln \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \ln \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

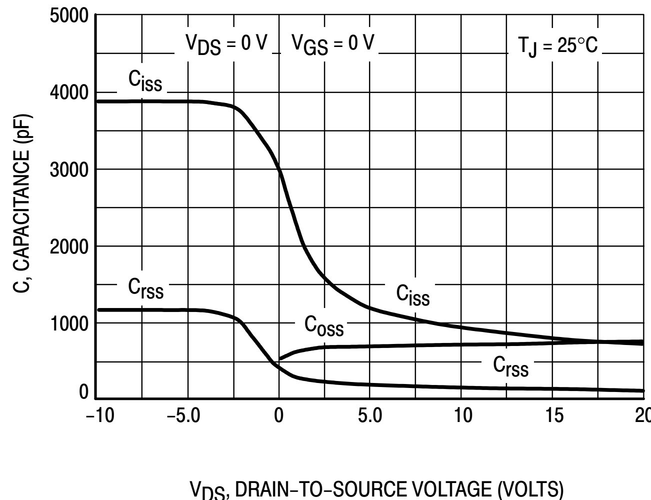



**Figure 7. Capacitance Variation**

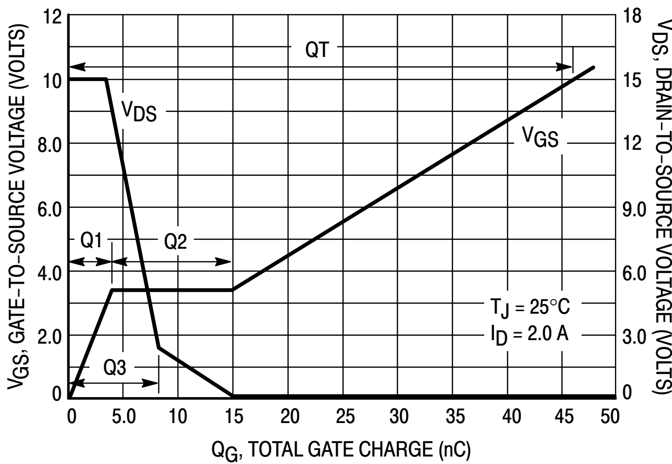



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

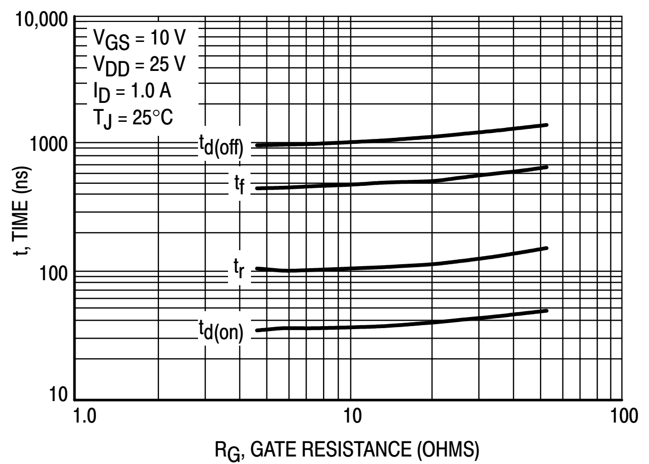



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

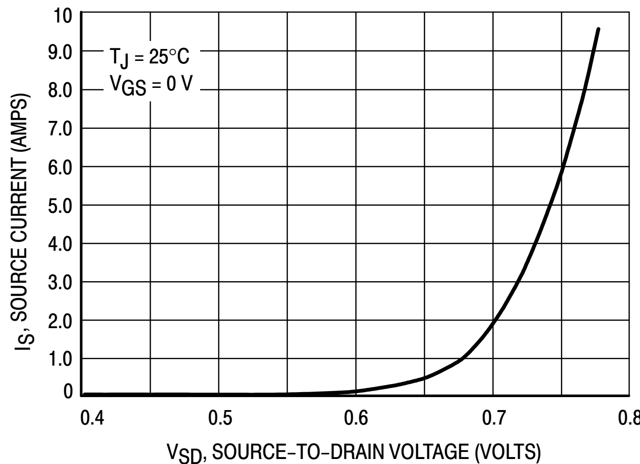



**Figure 10. Diode Forward Voltage versus Current**

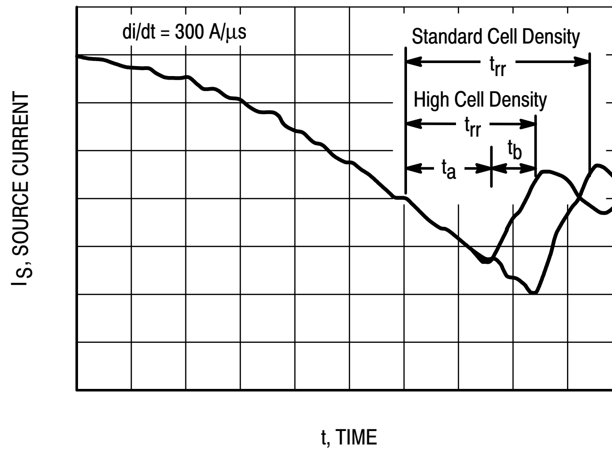



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

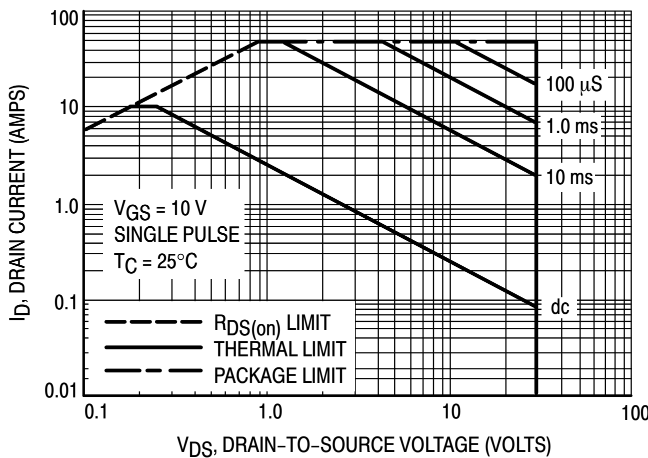



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

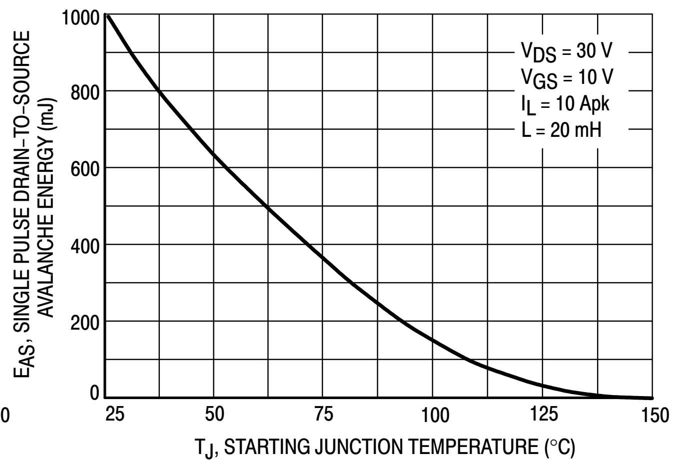



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

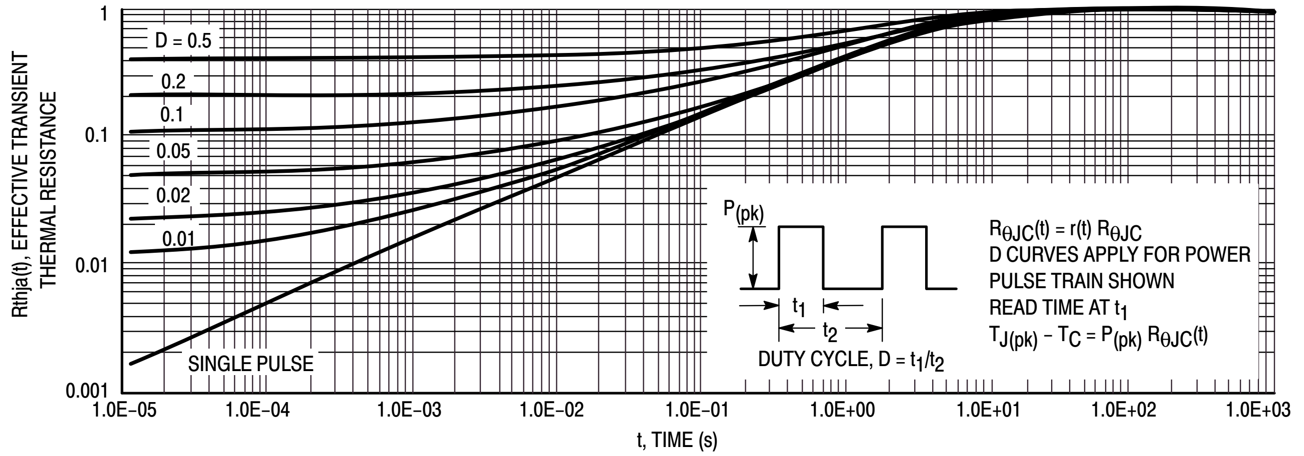



**Figure 14. Thermal Response**

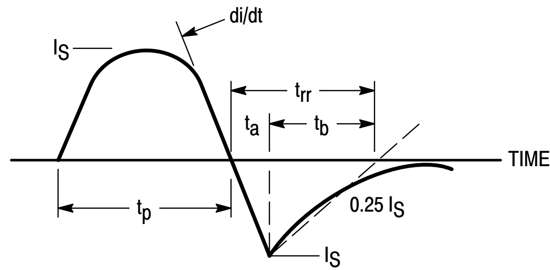
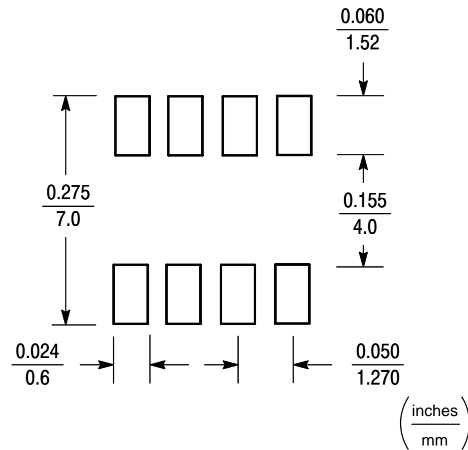



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 1.6 Watts.

$$P_D = \frac{150°C - 25°C}{80°C/W} = 1.6 \text{ Watts}$$

The 80°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.6 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

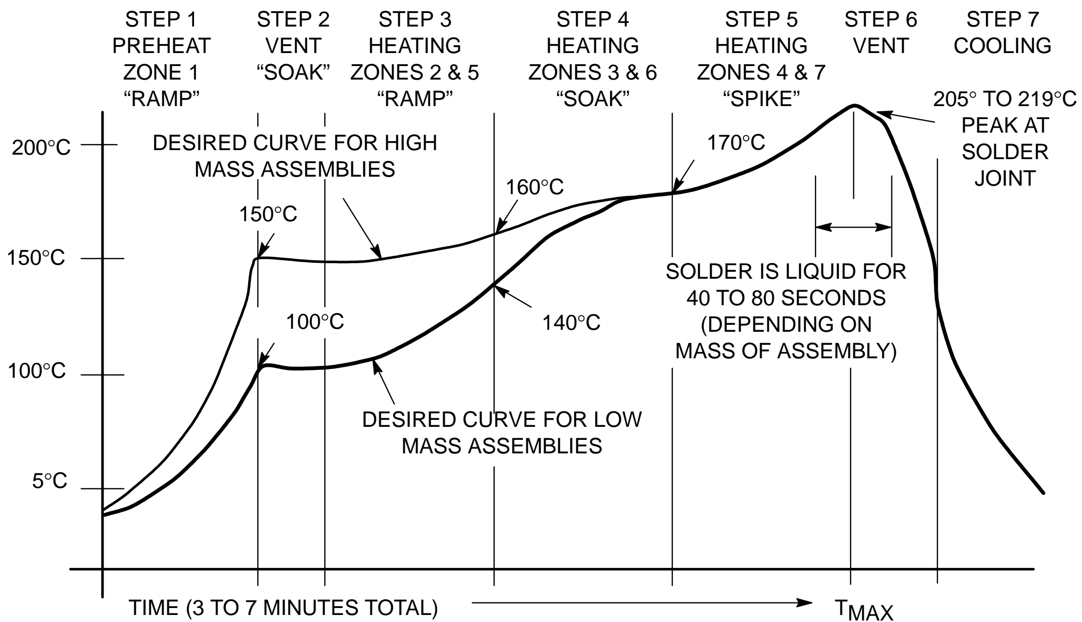



**Figure 16. Typical Solder Heating Profile**

# MMSF1308

**Preferred Device**

# Power MOSFET 7 Amps, 30 Volts

## N–Channel SO–8

**ON Semiconductor™**

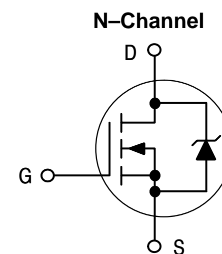
http://onsemi.com

**7 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 30 mΩ**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- High Speed Switching Provides High Efficiency for DC/DC Converter
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed, With Soft Recovery

**N–Channel**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

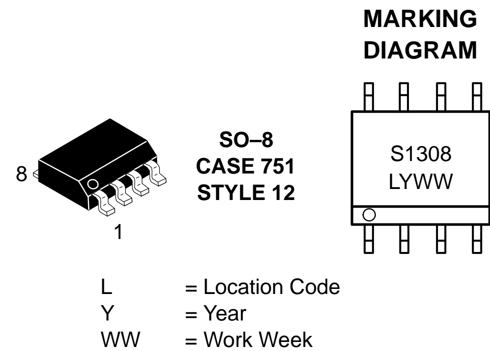
| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Continuous Drain Current @ $T_A$ = 25°C (Note 1.)<br>Pulsed Drain Current (Note 2.) | $I_D$<br>$I_{DM}$ | 7.0<br>50 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |

**THERMAL RESISTANCE**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |

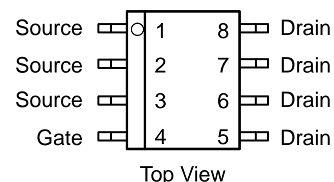
1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ 10 Seconds)
2. Repetitive rating; pulse width limited by maximum junction temperature.

**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF1308R2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 30 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | | $V_{GS(th)}$ | 1.0 | 1.6 | 2.5 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.3 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 7.0 Adc) | | $R_{DS(on)}$ | – | 22 | 30 | mΩ |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.5 Adc) | | | – | 30 | 39 | |
| Forward Transconductance ($V_{DS}$ = 5.0 Vdc, $I_D$ = 1.0 Adc) (Note 3.) | | $g_{FS}$ | – | 4.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 V, f = 1.0 MHz) | $C_{iss}$ | – | 690 | 970 | pF |
| Output Capacitance | | $C_{oss}$ | – | 290 | 410 | |
| Transfer Capacitance | | $C_{rss}$ | – | 90 | 130 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 21 Vdc, $I_D$ = 7.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) (Note 3.) | $t_{d(on)}$ | – | 7.5 | 15 | ns |
| Rise Time | | $t_r$ | – | 24 | 48 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 60 | |
| Fall Time | | $t_f$ | – | 46 | 92 | |
| Gate Charge | ($V_{DS}$ = 15 Vdc, $I_D$ = 7.0 Adc, $V_{GS}$ = 10 Vdc) (Note 3.) | $Q_T$ | – | 20 | 30 | nC |
| | | $Q_1$ | – | 2.5 | – | |
| | | $Q_2$ | – | 6.0 | – | |
| | | $Q_3$ | – | 8.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc) (Note 3.) | $V_{SD}$ | – | 0.85 | 1.0 | Vdc |
| | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.71 | – | |
| Reverse Recovery Time | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3.) | $t_{rr}$ | – | 35 | – | ns |
| | | $t_a$ | – | 20 | – | |
| | | $t_b$ | – | 15 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.03 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$
6. Repetitive rating; pulse width limited by maximum junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

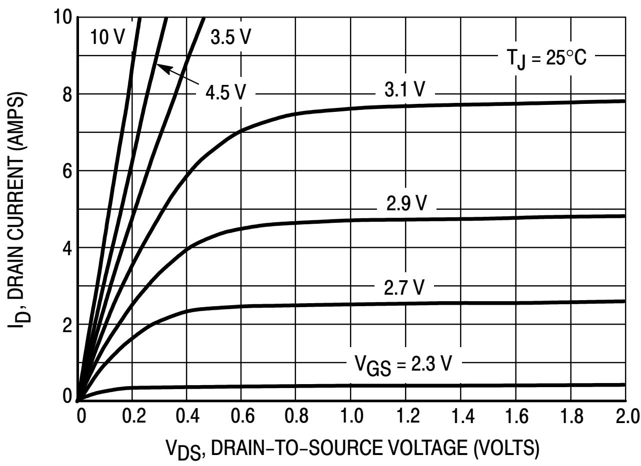



**Figure 1. On–Region Characteristics**

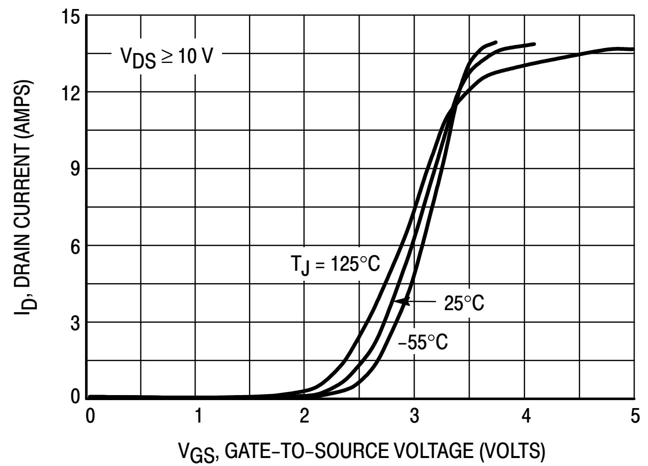



**Figure 2. Transfer Characteristics**

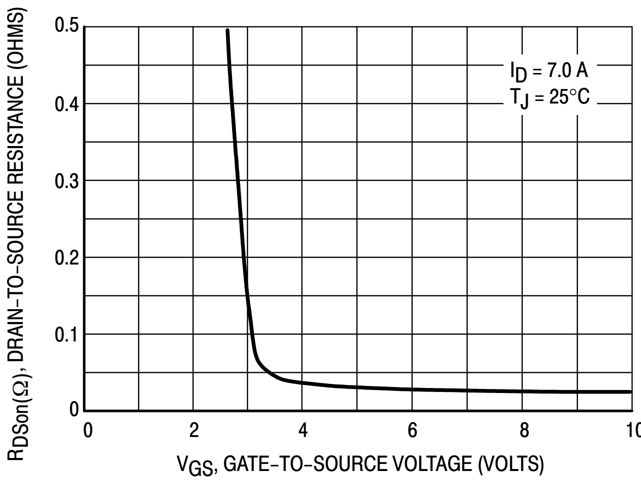



**Figure 3. On–Resistance versus Drain Current**

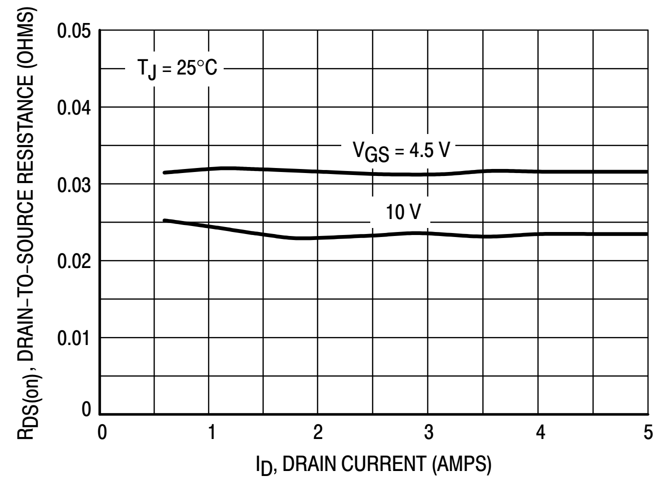



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

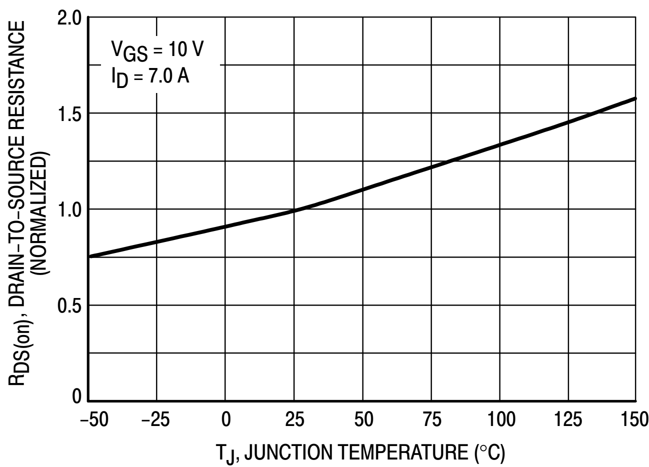



**Figure 5. On–Resistance Variation with Temperature**

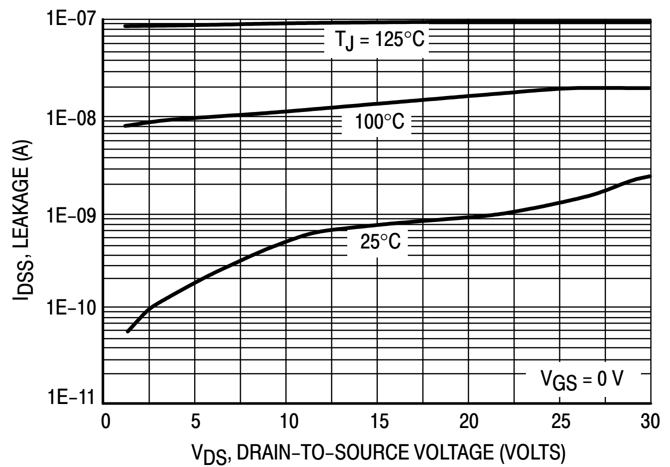



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

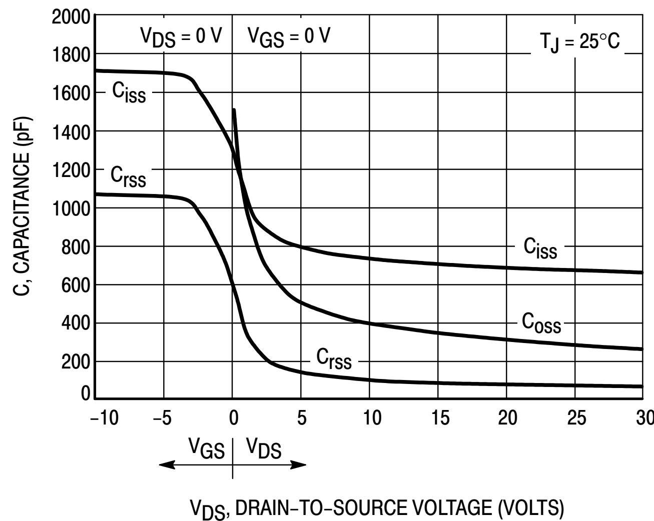



**Figure 7. Capacitance Variation**

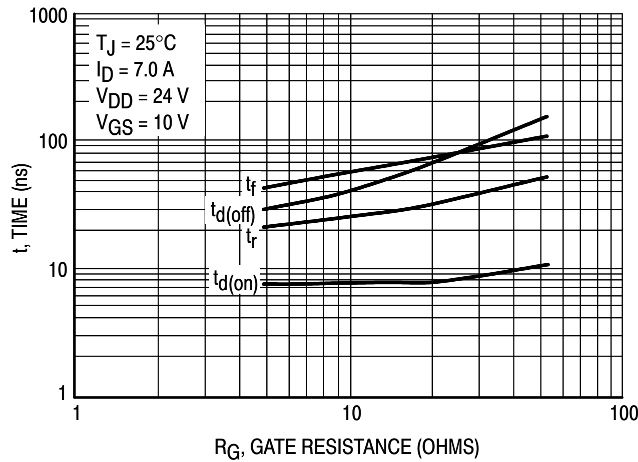



**Figure 8. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

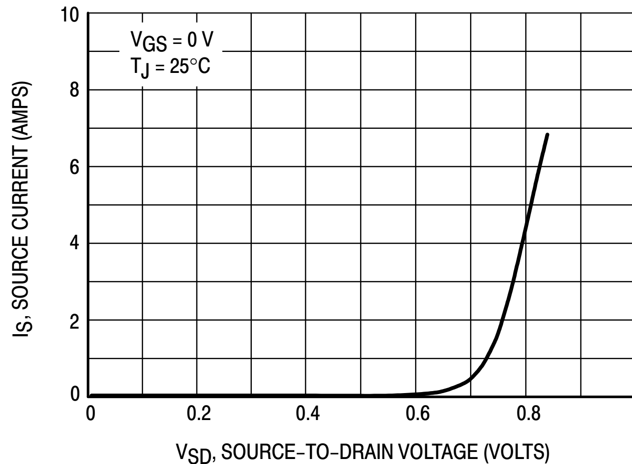



**Figure 9. Diode Forward Voltage versus Current**

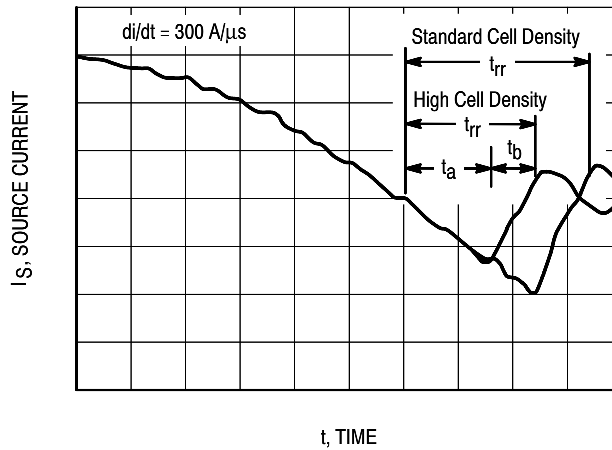



Figure 10. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

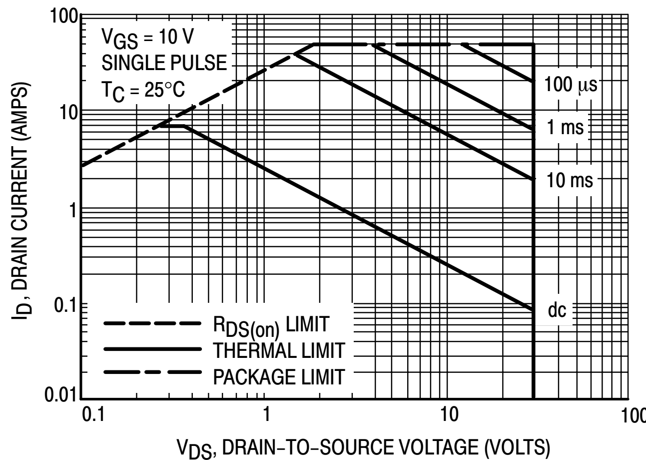
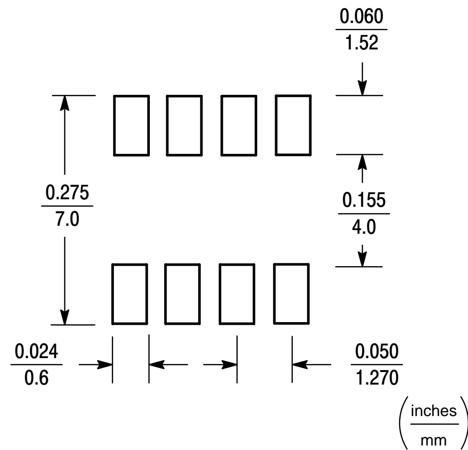



Figure 11. Maximum Rated Forward Biased Safe Operating Area

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

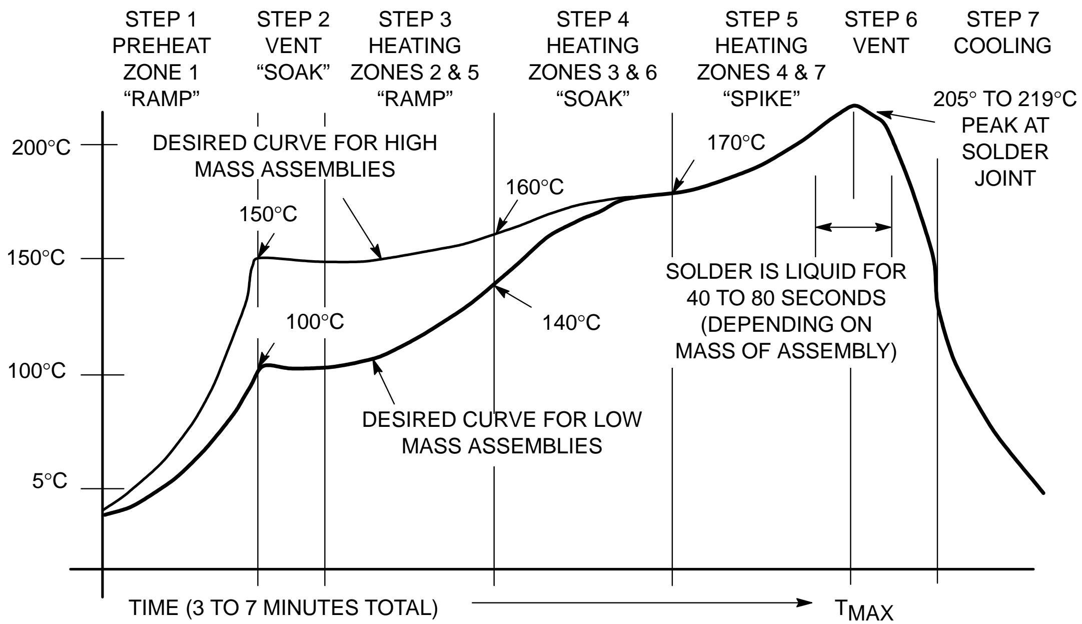



Figure 12. Typical Solder Heating Profile

# MMSF1310

**Preferred Device**

# Power MOSFET 10 Amps, 30 Volts

## N–Channel SO–8

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- High Speed Switching Provides High Efficiency for DC/DC Converter
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Exhibits High Speed, With Soft Recovery

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Continuous Drain Current @ $T_A$ = 25°C (Note 1.)<br>Pulsed Drain Current (Note 2.) | $I_D$<br>$I_{DM}$ | 10<br>50 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |

**THERMAL RESISTANCE**

| | | | |
|---|---|---|---|
| Junction–to–Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |

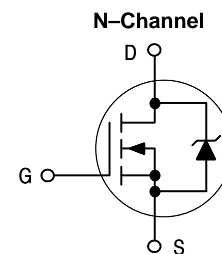
1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ 10 Seconds)
2. Repetitive rating; pulse width limited by maximum junction temperature.

**ON Semiconductor™**

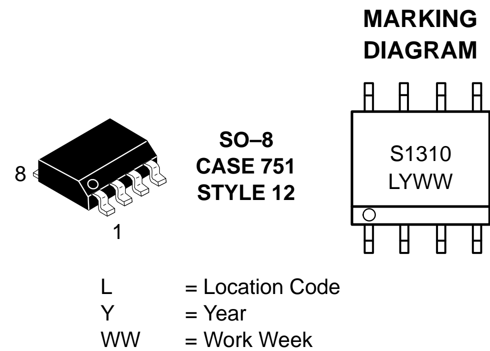
**http://onsemi.com**

**10 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 15 mΩ**

**N–Channel**

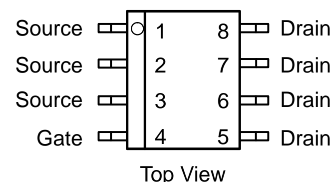



**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF1310R2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 27 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | | $V_{GS(th)}$ | 1.0 | 1.3 | 2.5 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.4 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 9.5 | 15 | mΩ |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | | – | 12.5 | 19 | |
| Forward Transconductance ($V_{DS}$ = 5.0 Vdc, $I_D$ = 1.0 Adc) (Note 3.) | | $g_{FS}$ | – | 5.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 V, f = 1.0 MHz) | $C_{iss}$ | – | 1440 | 2020 | pF |
| Output Capacitance | | $C_{oss}$ | – | 680 | 960 | |
| Transfer Capacitance | | $C_{rss}$ | – | 195 | 280 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 24 Vdc, $I_D$ = 10 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) (Note 3.) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 36 | 72 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 82 | 164 | |
| Fall Time | | $t_f$ | – | 95 | 190 | |
| Gate Charge | ($V_{DS}$ = 15 Vdc, $I_D$ = 10 Adc, $V_{GS}$ = 10 Vdc) (Note 3.) | $Q_T$ | – | 48 | 68 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 4.0 | – | |
| | | $Q_3$ | – | 7.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc) (Note 3.) | $V_{SD}$ | – | 0.82 | 1.0 | Vdc |
| | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.67 | – | |
| Reverse Recovery Time | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 3.) | $t_{rr}$ | – | 52 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 30 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.05 | – | μC |

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.
5. Reflects typical values. $C_{pk} = \left| \dfrac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$
6. Repetitive rating; pulse width limited by maximum junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

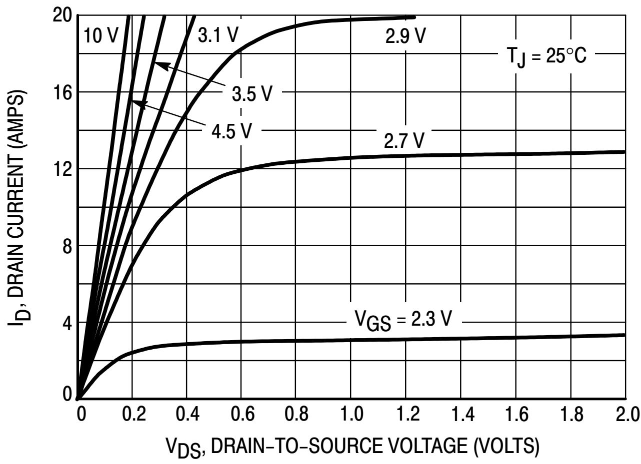



**Figure 1. On–Region Characteristics**

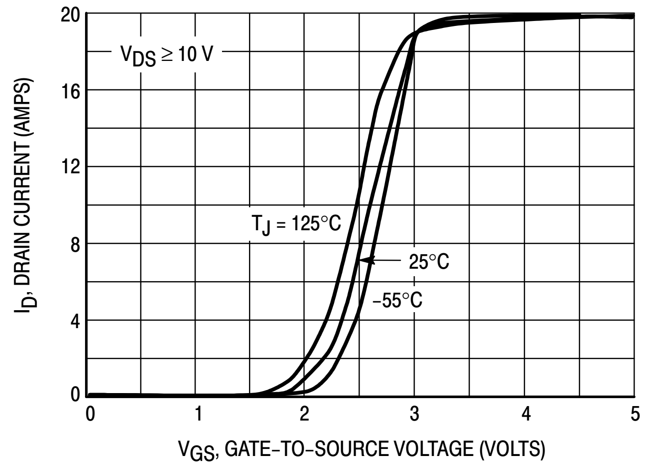



**Figure 2. Transfer Characteristics**

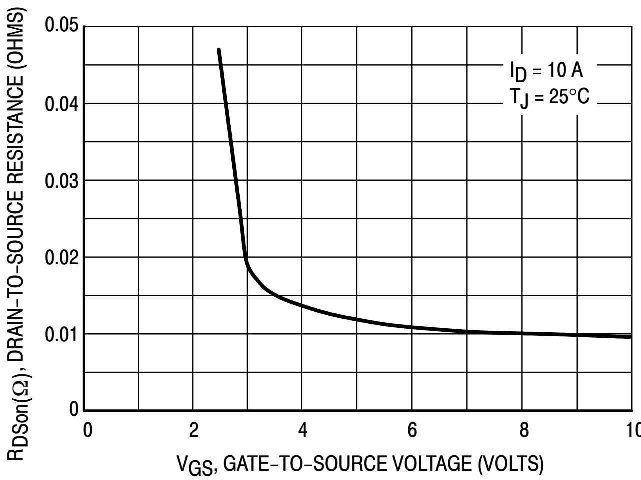



**Figure 3. On–Resistance versus Drain Current**

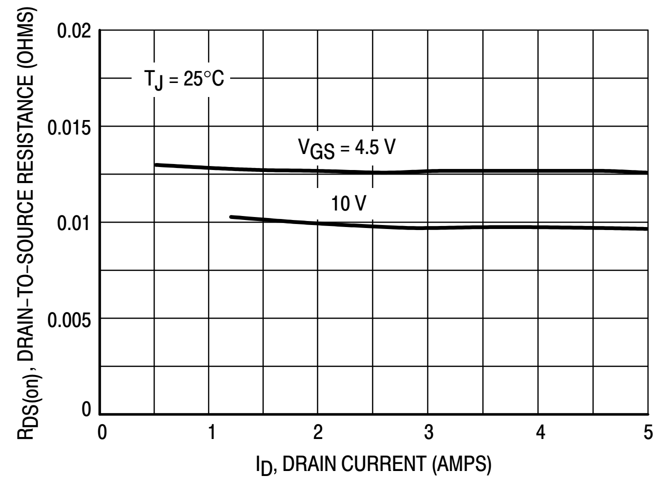



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

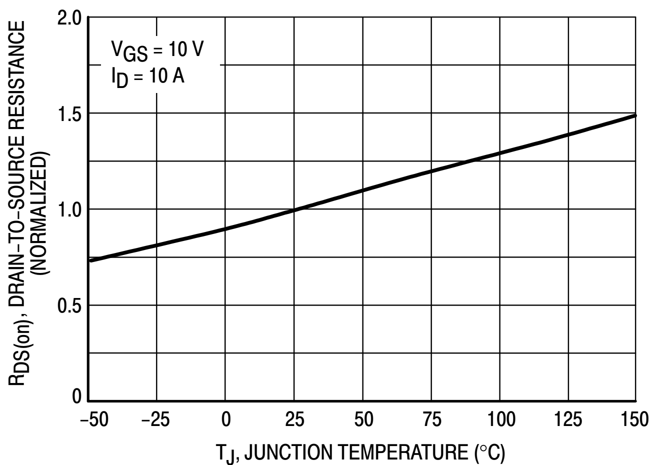



**Figure 5. On–Resistance Variation with Temperature**

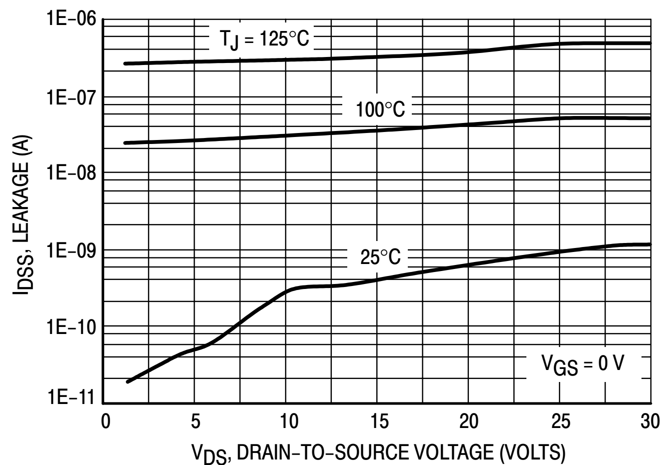



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \ln\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \ln\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

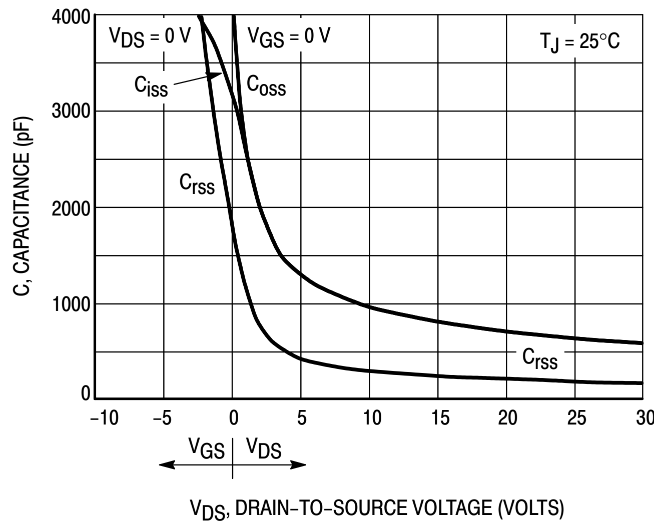



**Figure 7. Capacitance Variation**

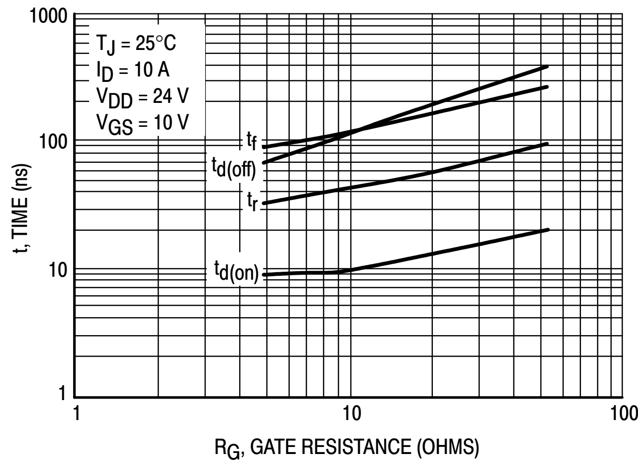



**Figure 8. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

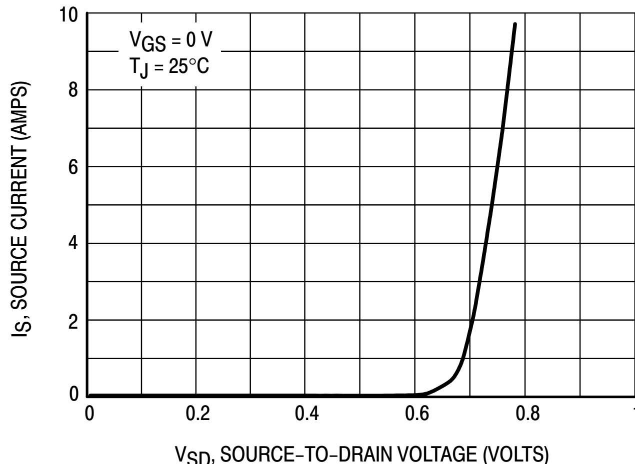



**Figure 9. Diode Forward Voltage versus Current**

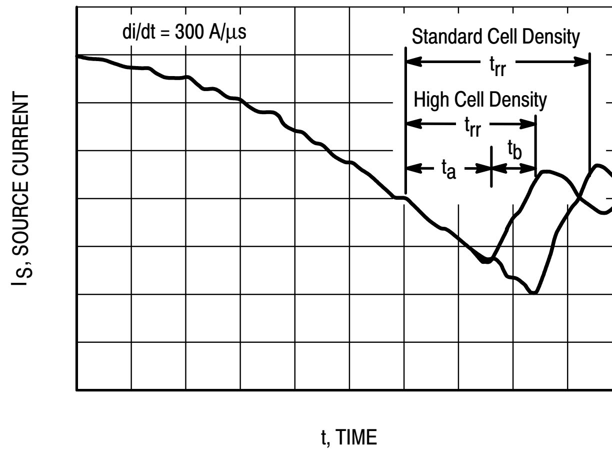



**Figure 10. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

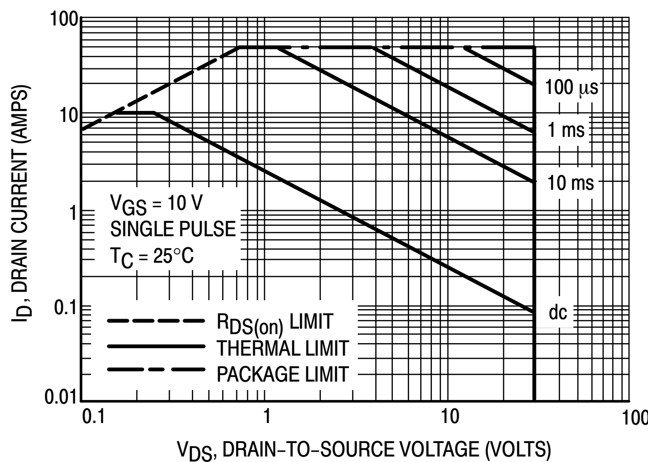
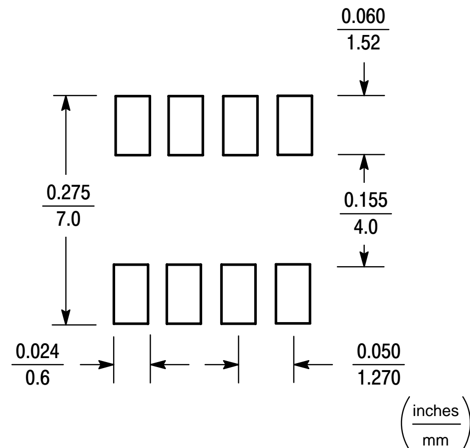



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 12 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

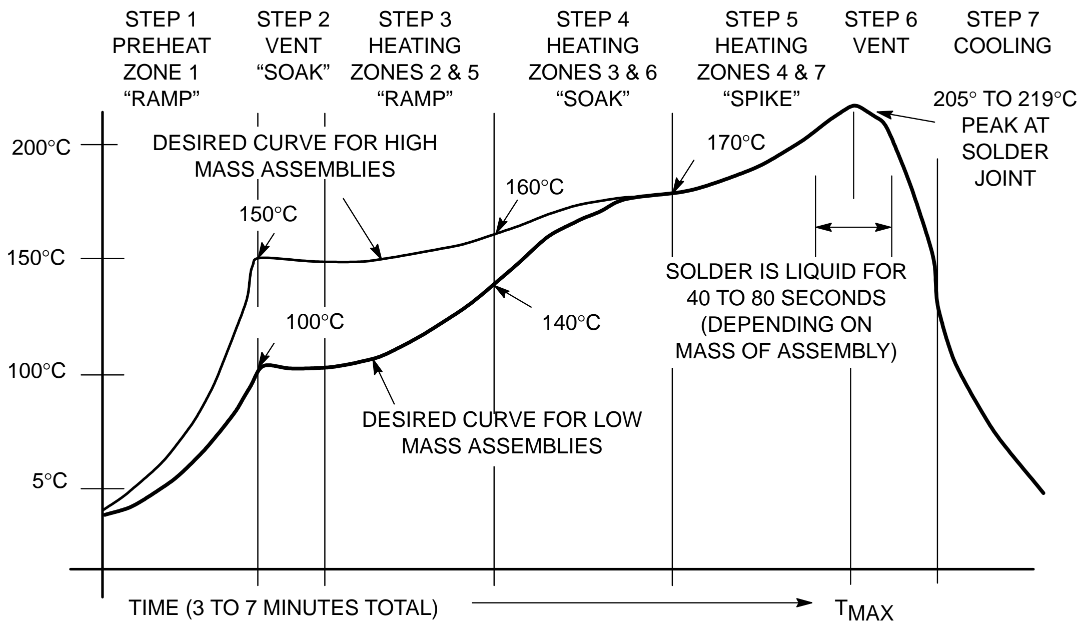



**Figure 12. Typical Solder Heating Profile**

# MMSF2P02E

**Preferred Device**

# Power MOSFET 2 Amps, 20 Volts

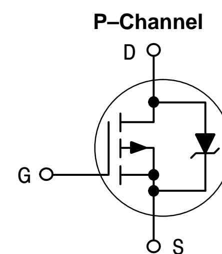
## P–Channel SO–8

**ON Semiconductor™**

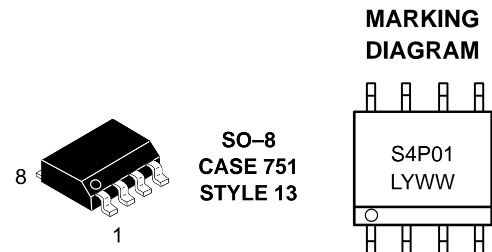
**http://onsemi.com**

**2 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 250 mΩ**

**P–Channel**

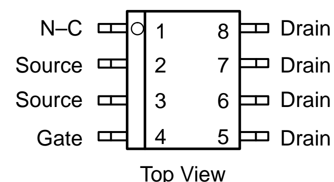



**MARKING DIAGRAM**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF2P02ER2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided
- $I_{DSS}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C (Note 2.)<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>2.5<br>1.7<br>13 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 6.0 Apk, L = 12 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 216 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 24.7 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 2.0 | 3.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.7 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | – | 0.19 | 0.25 | Ohm |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.0 Adc) | | | – | 0.3 | 0.4 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 1.0 | 2.8 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 340 | 475 | pF |
| Output Capacitance | | $C_{oss}$ | – | 220 | 300 | |
| Transfer Capacitance | | $C_{rss}$ | – | 75 | 150 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | 40 | ns |
| Rise Time | | $t_r$ | – | 40 | 80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 53 | 106 | |
| Fall Time | | $t_f$ | – | 41 | 82 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 13 | 26 | ns |
| Rise Time | | $t_r$ | – | 29 | 58 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 30 | 60 | |
| Fall Time | | $t_f$ | – | 28 | 56 | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 10 | 15 | nC |
| | | $Q_1$ | – | 1.1 | – | |
| | | $Q_2$ | – | 3.3 | – | |
| | | $Q_3$ | – | 2.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.5 | 2.0 | Vdc |
| Reverse Recovery Time | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 34 | 64 | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.035 | – | μC |

3. Negative sign for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

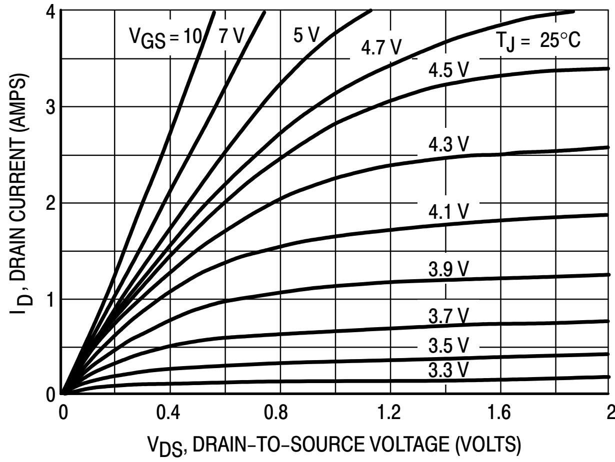



**Figure 1. On–Region Characteristics**

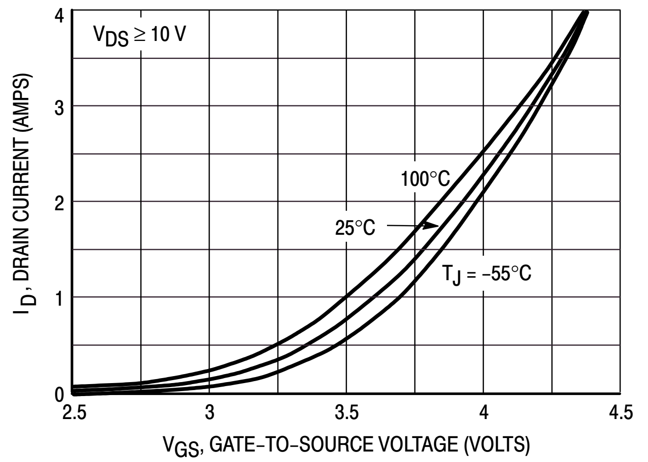



**Figure 2. Transfer Characteristics**

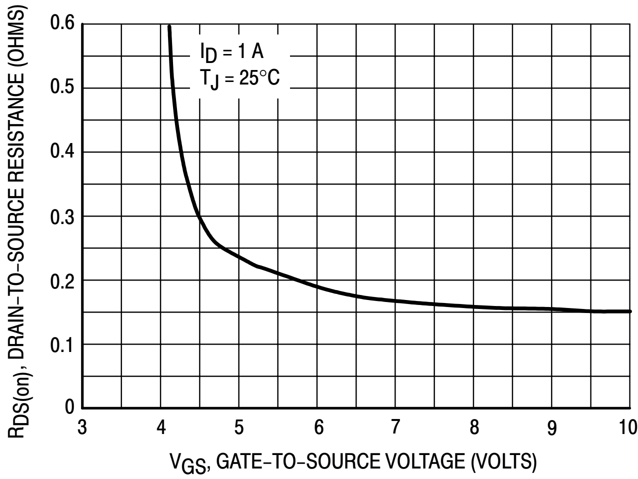



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

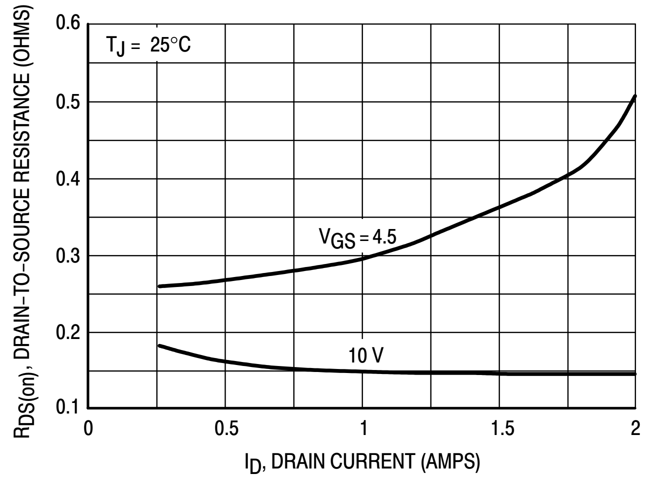



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

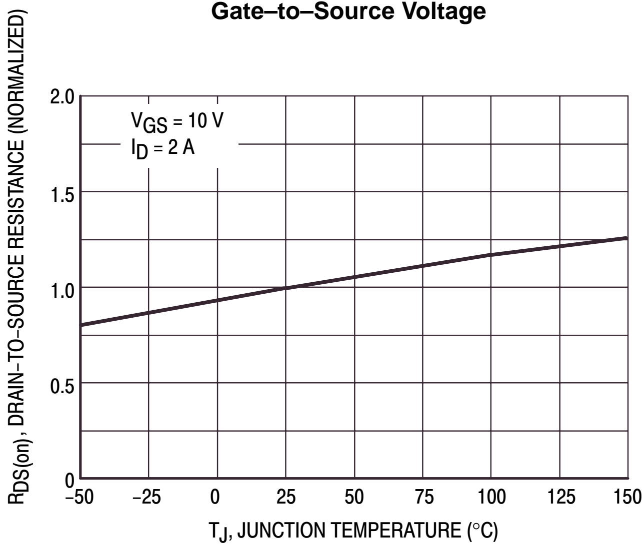



**Figure 5. On–Resistance Variation with Temperature**

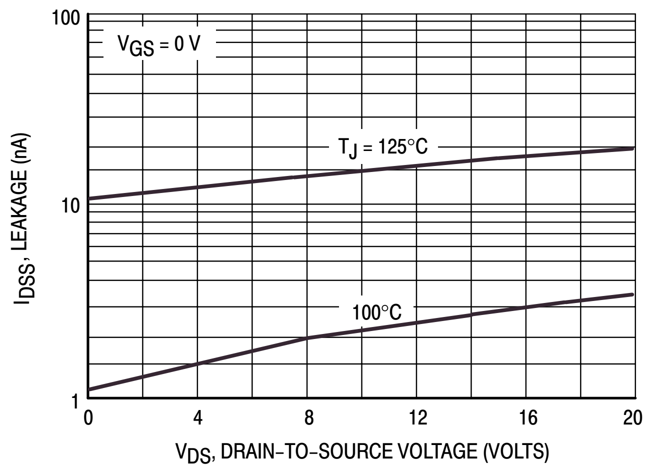



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

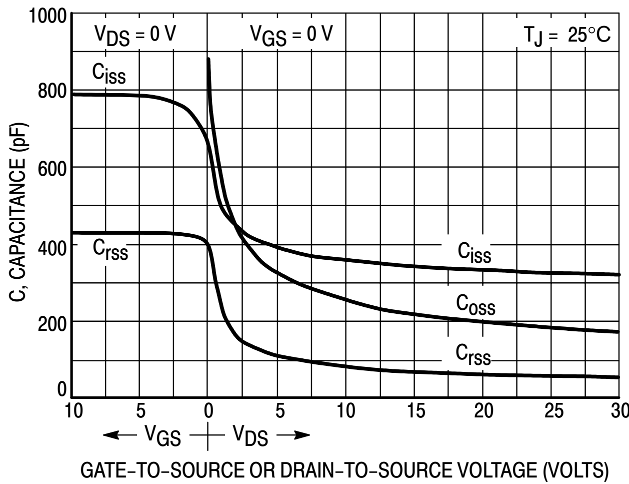



**Figure 7. Capacitance Variation**

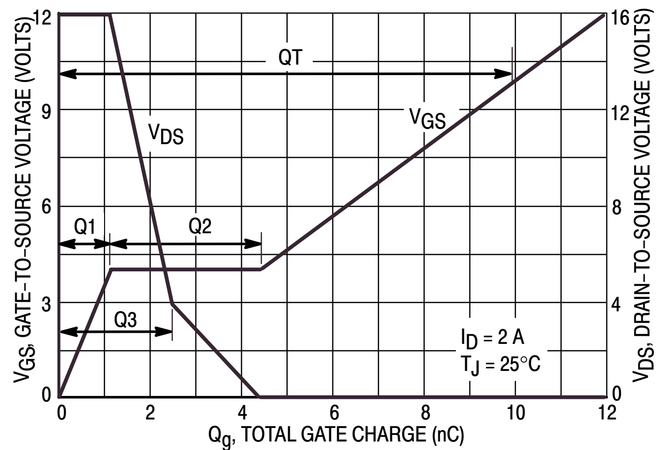



**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

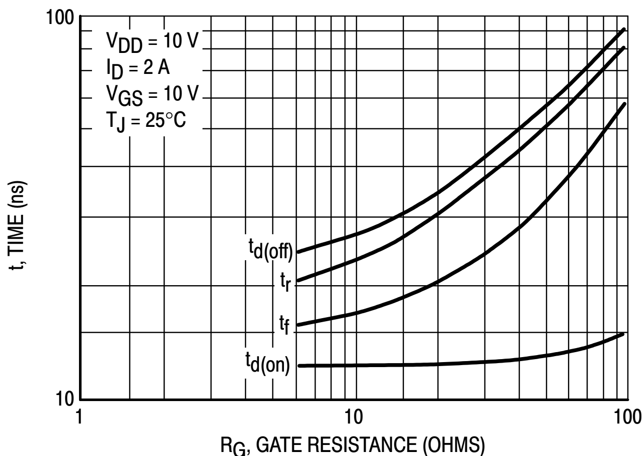



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

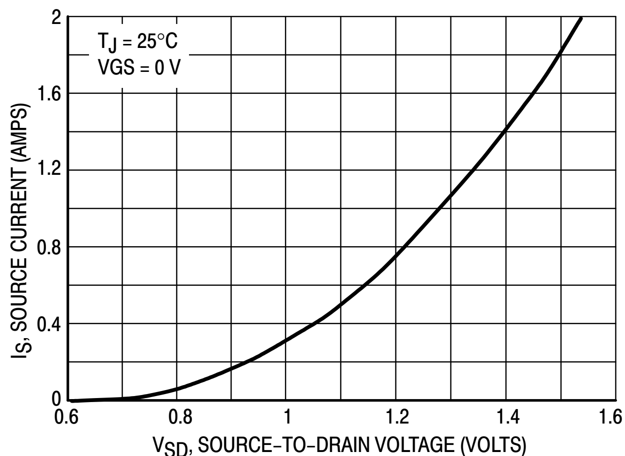



**Figure 10. Diode Forward Voltage versus Current**

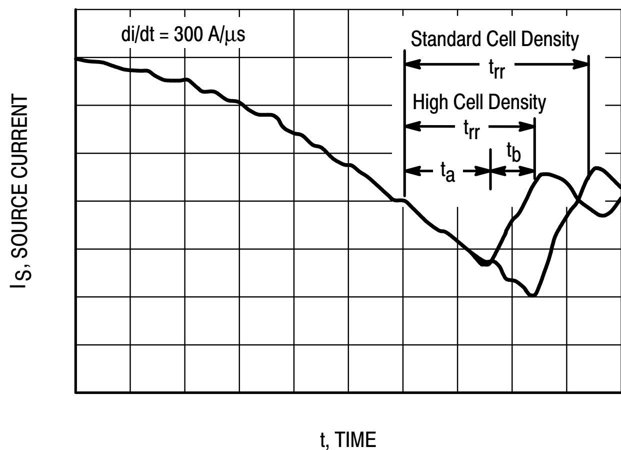



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

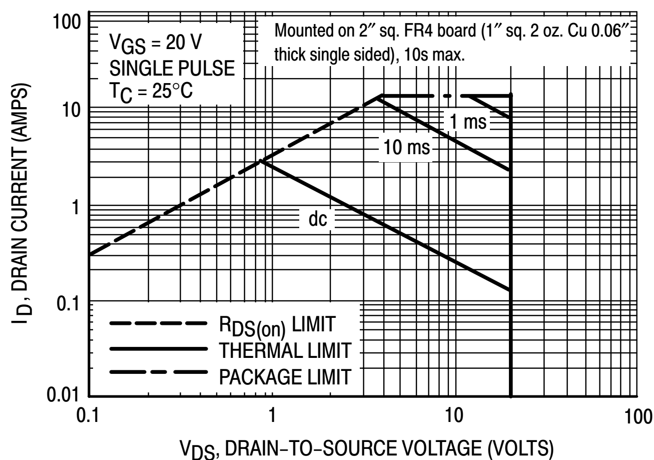



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

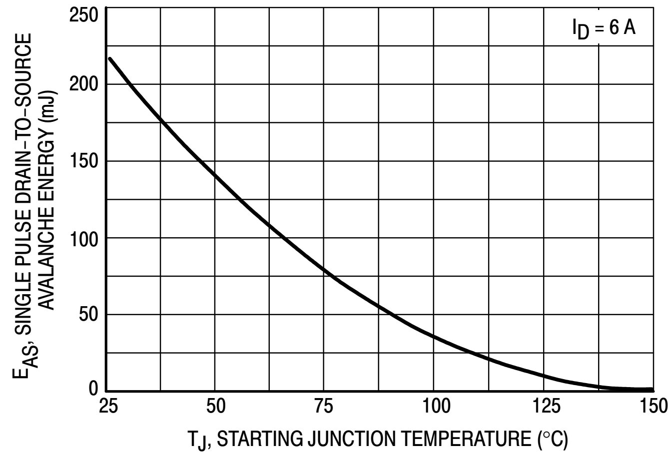



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

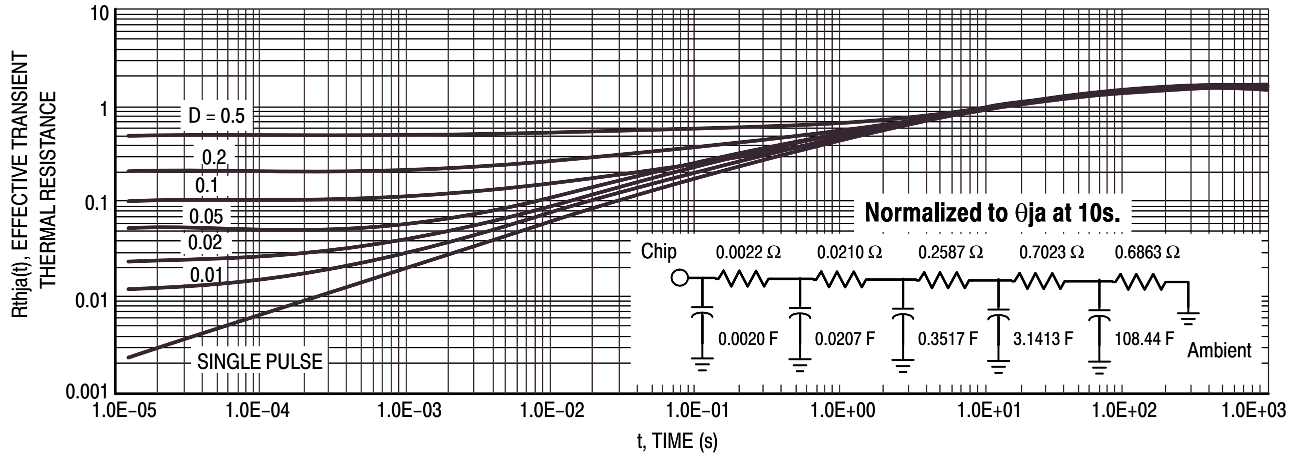



**Figure 14. Thermal Response**

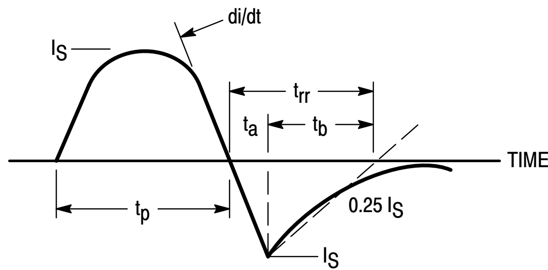
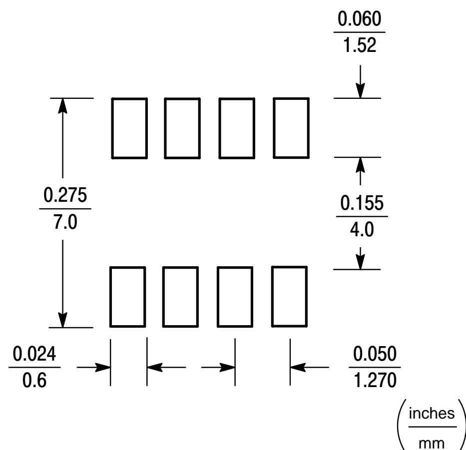



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

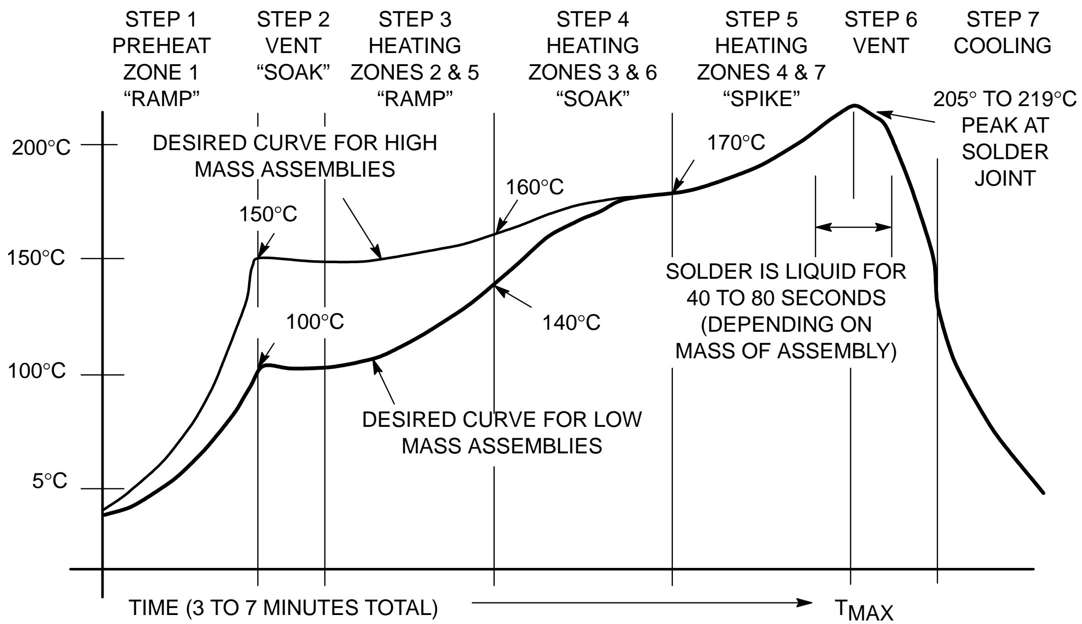



**Figure 16. Typical Solder Heating Profile**

# MMSF3300

ON Semiconductor™

http://onsemi.com

*Advance Information*

## Power MOSFET
## 11.5 Amps, 30 Volts
### N–Channel SO–8

These Power MOSFETs are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. WaveFET™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

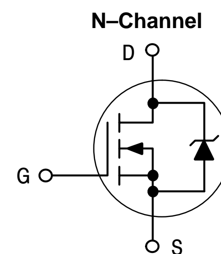
- Characterized Over a Wide Range of Power Ratings
- Ultralow $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life in Portable Applications
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Miniature SO–8 Surface Mount Package – Saves Board Space

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise specified)

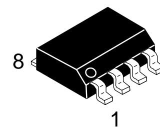
| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ±20 | Vdc |
| Gate–to–Source Operating Voltage | $V_{GS}$ | ±16 | Vdc |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, L = 18.8 mH, $I_{L(pk)}$ = 7.3 A, $V_{DS}$ = 30 Vdc) | $E_{AS}$ | 500 | mJ |

**11.5 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 12.5 mΩ**

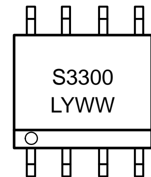
N–Channel




**MARKING DIAGRAM**

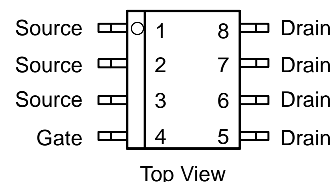



**SO–8**
**CASE 751**
**STYLE 12**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF3300R2 | SO–8 | 2500 Tape & Reel |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**POWER RATINGS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | Mounted on 1 inch square FR–4 or G10 board | $I_D$<br>$I_D$<br>$I_{DM}$ | 11.5<br>8.2<br>50 | Adc<br>Adc<br>Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor | $V_{GS}$ = 10 Vdc | $P_D$ | 2.5<br>20 | Watts<br>mW/°C |
| Thermal Resistance – Junction–to–Ambient | t ≤ 10 seconds | $R_{θJA}$ | 50 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 3.0 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | Mounted on 1 inch square FR–4 or G10 board | $I_D$<br>$I_D$<br>$I_{DM}$ | 9.1<br>6.5<br>50 | Adc<br>Adc<br>Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor | $V_{GS}$ = 10 Vdc | $P_D$ | 1.6<br>12.5 | Watts<br>mW/°C |
| Thermal Resistance – Junction–to–Ambient | Steady State | $R_{θJA}$ | 80 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 2.0 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | Mounted on minimum recommended FR–4 or G10 board | $I_D$<br>$I_D$<br>$I_{DM}$ | 9.1<br>6.5<br>50 | Adc<br>Adc<br>Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor | $V_{GS}$ = 10 Vdc | $P_D$ | 1.6<br>12.5 | Watts<br>mW/°C |
| Thermal Resistance – Junction–to–Ambient | t ≤ 10 seconds | $R_{θJA}$ | 80 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 2.0 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse (tp ≤ 10 μs) | Mounted on minimum recommended FR–4 or G10 board | $I_D$<br>$I_D$<br>$I_{DM}$ | 6.7<br>4.7<br>50 | Adc<br>Adc<br>Adc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor | $V_{GS}$ = 10 Vdc | $P_D$ | 0.8<br>6.7 | Watts<br>mW/°C |
| Thermal Resistance – Junction–to–Ambient | Steady State | $R_{θJA}$ | 150 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 1.0 | Adc |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 24 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | 0.004 | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | 0.5 | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.9 | – | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.4 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 10 | 12.5 | mΩ |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | | – | 16 | 20 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 3.0 | 18 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1700 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 600 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 200 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 21 | 40 | ns |
| Rise Time | | $t_r$ | – | 45 | 90 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 40 | 80 | |
| Fall Time | | $t_f$ | – | 40 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 12 | 25 | ns |
| Rise Time | | $t_r$ | – | 12 | 25 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 55 | 110 | |
| Fall Time | | $t_f$ | – | 39 | 80 | |
| Gate Charge | ($V_{DS}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 45 | 60 | nC |
| | | $Q_1$ | – | 5.1 | – | |
| | | $Q_2$ | – | 14 | – | |
| | | $Q_3$ | – | 13 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.78 | 1.1 | Vdc |
| | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.60 | – | |
| Reverse Recovery Time | ($I_S$ = 3.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 40 | – | ns |
| | | $t_a$ | – | 21 | – | |
| | | $t_b$ | – | 19 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.043 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

## TYPICAL ELECTRICAL CHARACTERISTICS

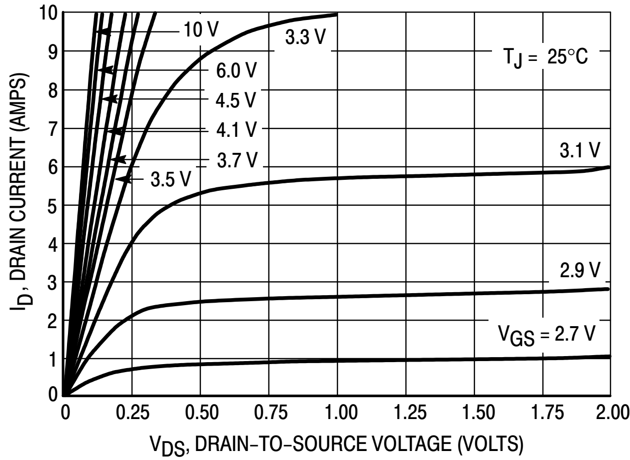



**Figure 1. On–Region Characteristics**

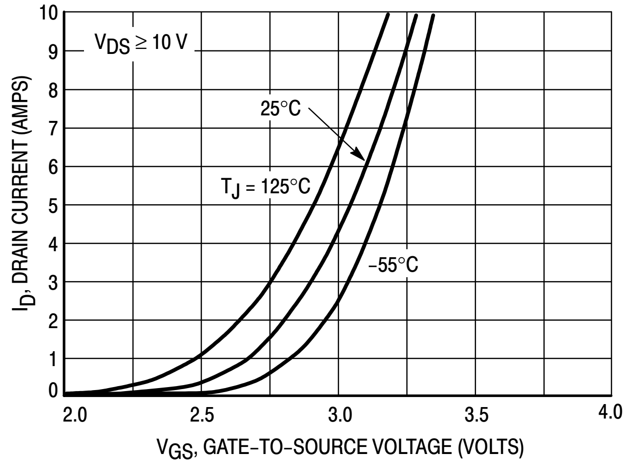



**Figure 2. Transfer Characteristics**

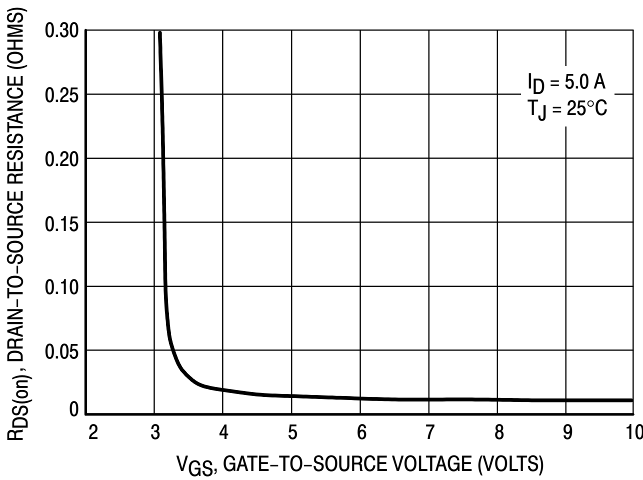



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

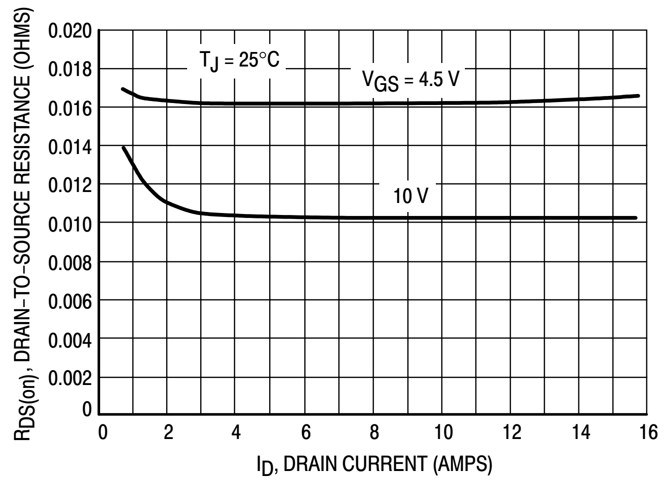



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

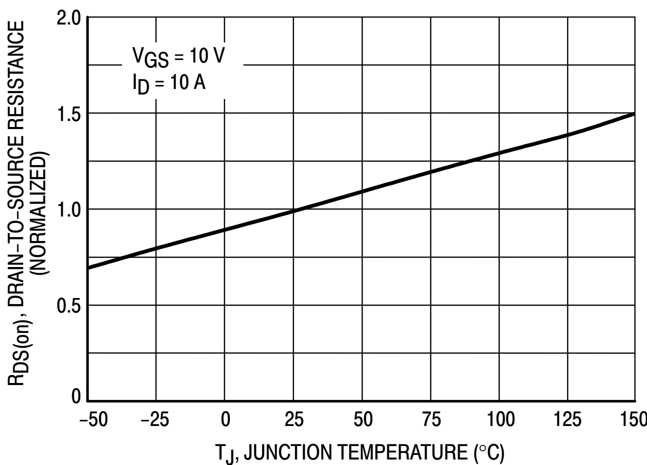



**Figure 5. On–Resistance Variation with Temperature**

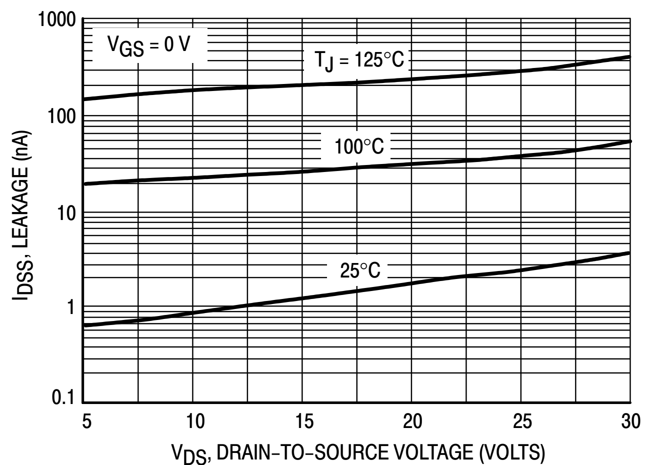



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

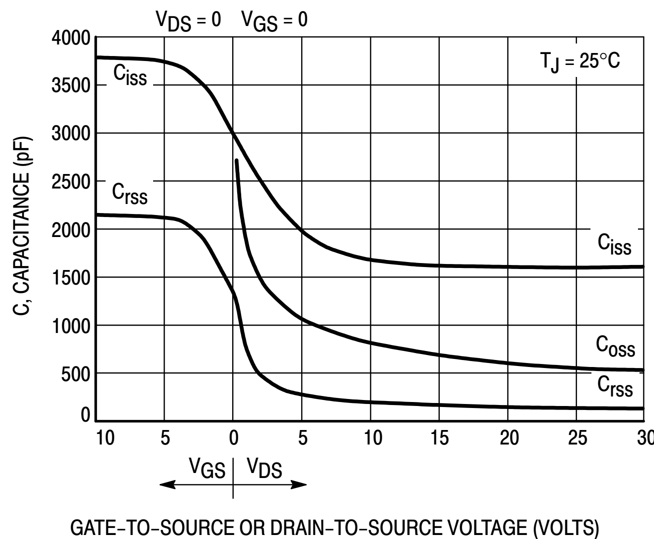



**Figure 7. Capacitance Variation**

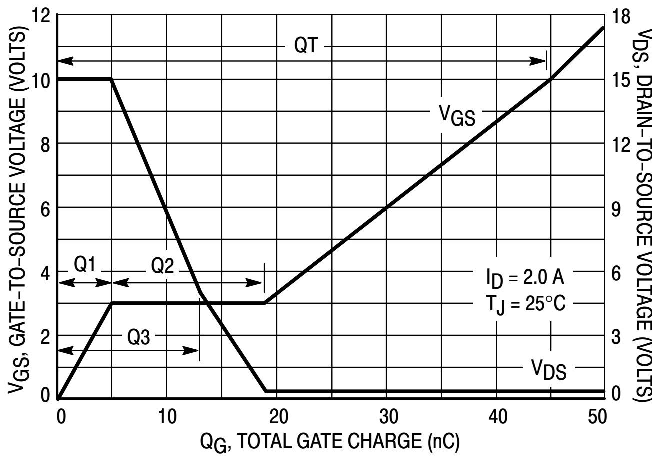



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

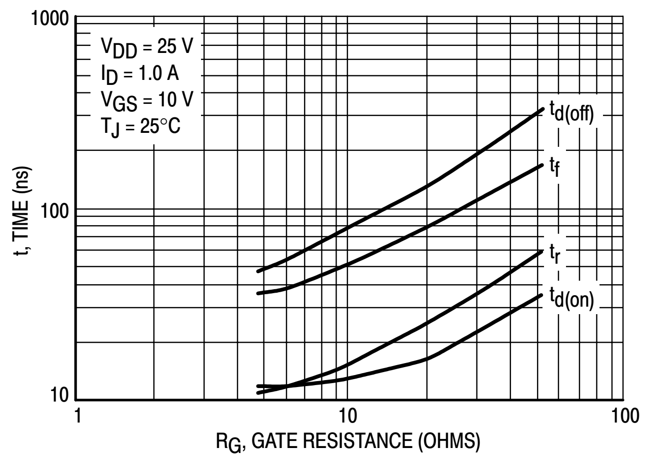



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 16. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

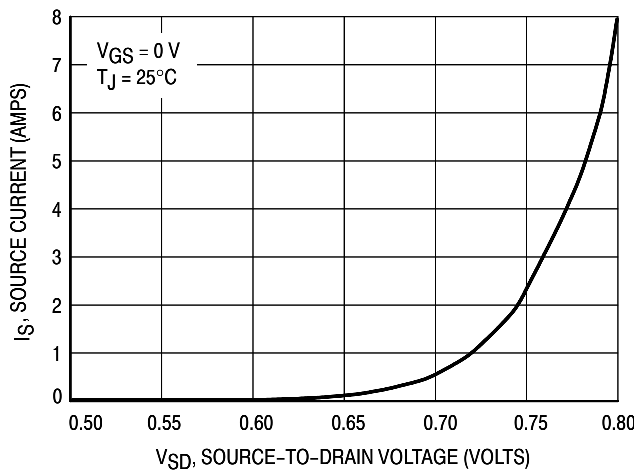



**Figure 10. Diode Forward Voltage versus Current**

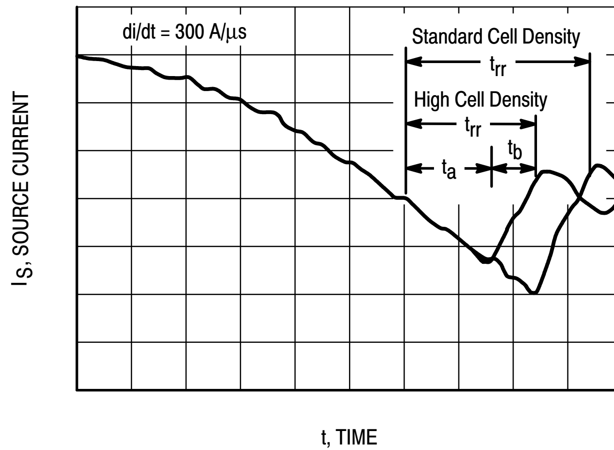



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

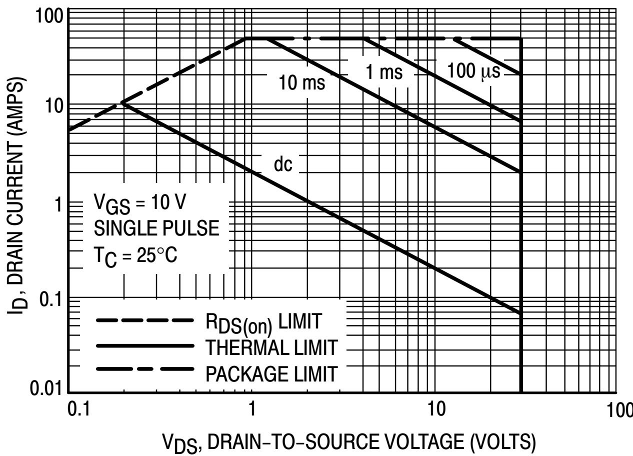



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

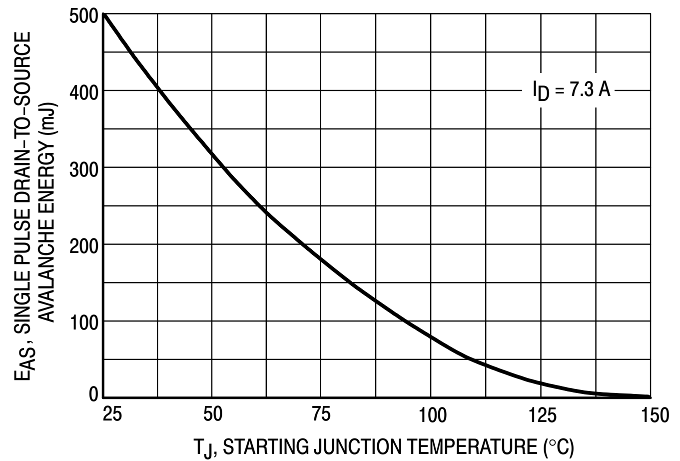



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

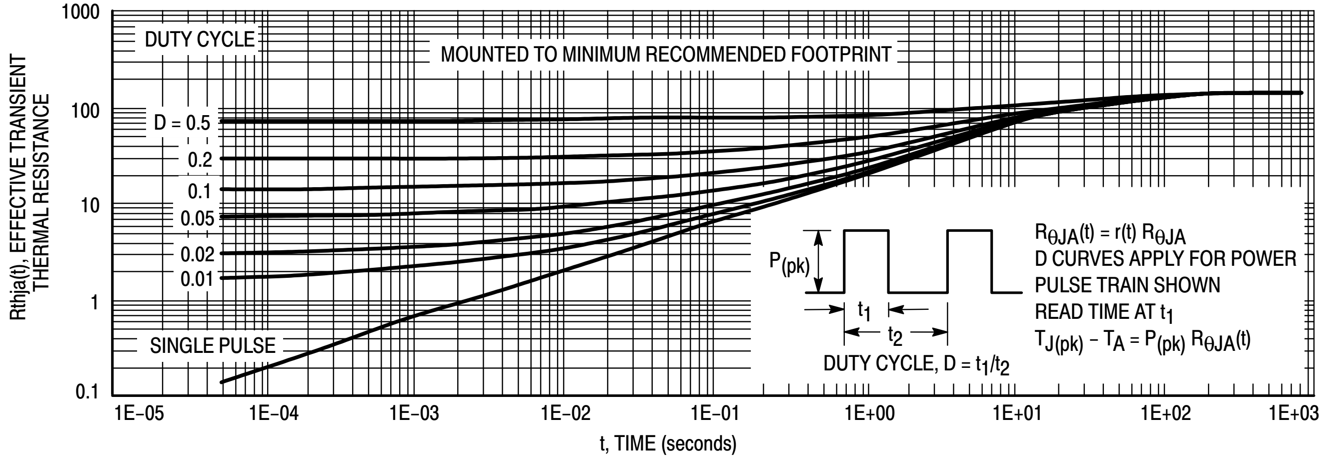
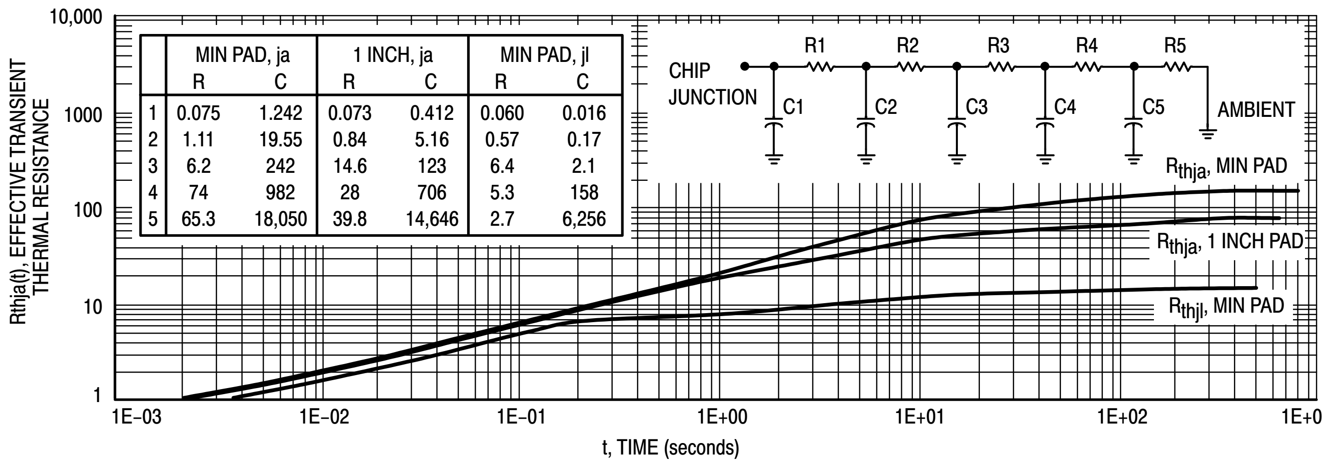



**Figure 14. Thermal Response – Various Duty Cycles**



| | MIN PAD, ja R | MIN PAD, ja C | 1 INCH, ja R | 1 INCH, ja C | MIN PAD, jl R | MIN PAD, jl C |
|---|---|---|---|---|---|---|
| 1 | 0.075 | 1.242 | 0.073 | 0.412 | 0.060 | 0.016 |
| 2 | 1.11 | 19.55 | 0.84 | 5.16 | 0.57 | 0.17 |
| 3 | 6.2 | 242 | 14.6 | 123 | 6.4 | 2.1 |
| 4 | 74 | 982 | 28 | 706 | 5.3 | 158 |
| 5 | 65.3 | 18,050 | 39.8 | 14,646 | 2.7 | 6,256 |



**Figure 15. Thermal Response – Various Mounting/Measurement Conditions**

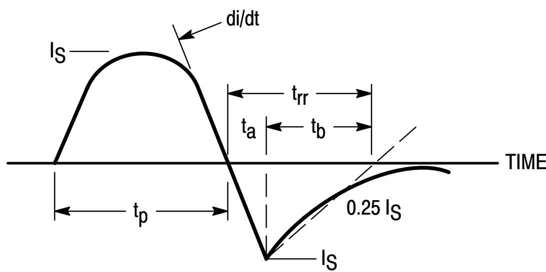



**Figure 16. Diode Reverse Recovery Waveform**

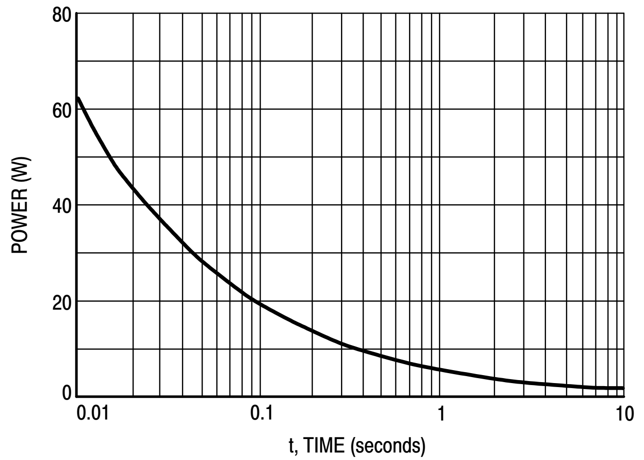
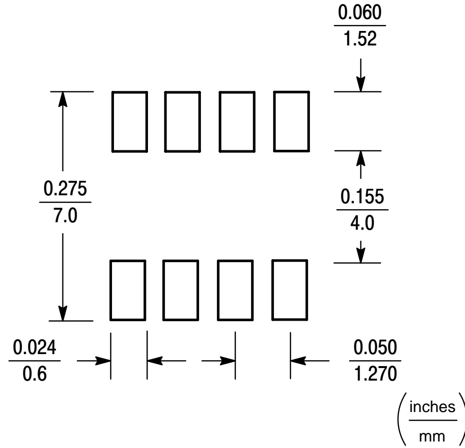



**Figure 17. Single Pulse Power**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

*Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

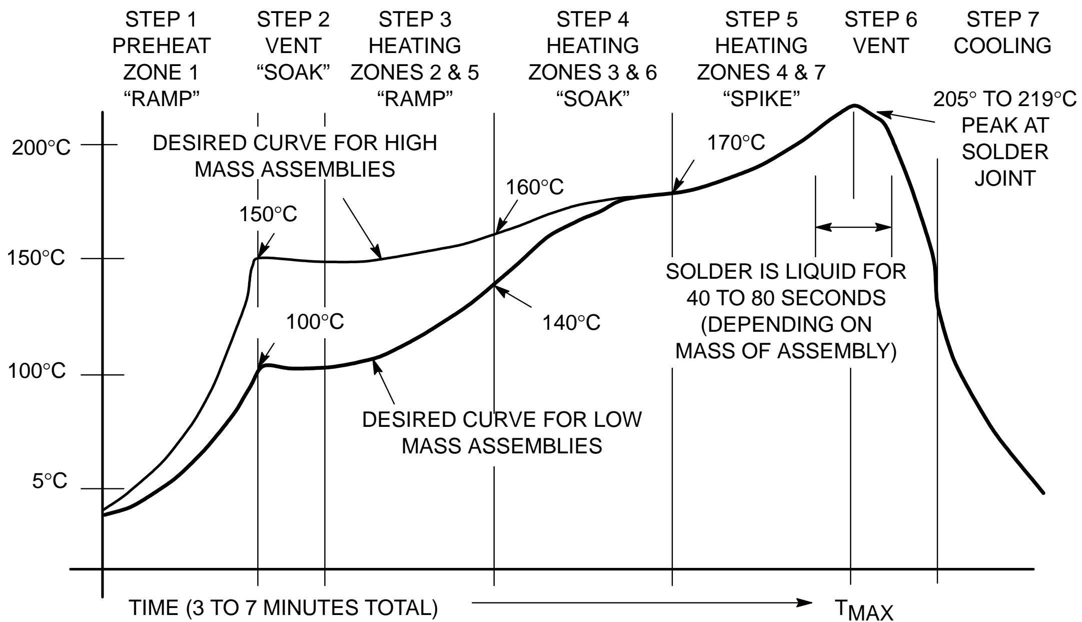



**Figure 18. Typical Solder Heating Profile**

# MMSF3P02HD

Preferred Device

## Power MOSFET 3 Amps, 20 Volts

### P–Channel SO–8

**ON Semiconductor™**

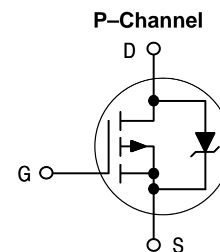
http://onsemi.com

**3 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 75 mΩ**

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

P–Channel

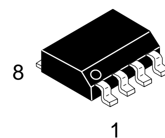



**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) (Note 1.)

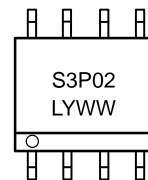
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5.6<br>3.6<br>30 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 9.0 Apk, L = 14 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 567 | mJ |
| Thermal Resistance – Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Negative sign for P–Channel device omitted for clarity.
2. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

MARKING DIAGRAM

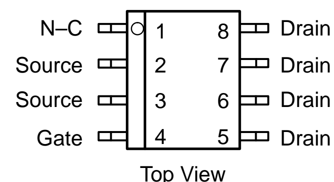



SO–8
CASE 751
STYLE 13




L = Location Code
Y = Year
WW = Work Week

PIN ASSIGNMENT




ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| MMSF3P02HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (Note 3.)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>20<br>– | <br>–<br>24 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.5 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>0.06<br>0.08 | <br>0.075<br>0.095 | Ohm |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 1.5 Adc) | | $g_{FS}$ | 3.0 | 7.2 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1010 | 1400 | pF |
| Output Capacitance | | $C_{oss}$ | – | 740 | 920 | |
| Transfer Capacitance | | $C_{rss}$ | – | 260 | 490 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 25 | 50 | ns |
| Rise Time | | $t_r$ | – | 135 | 270 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 54 | 108 | |
| Fall Time | | $t_f$ | – | 84 | 168 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 16 | 32 | |
| Rise Time | | $t_r$ | – | 40 | 80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 110 | 220 | |
| Fall Time | | $t_f$ | – | 97 | 194 | |
| Gate Charge<br>See Figure 8 | ($V_{DS}$ = 16 Vdc, $I_D$ = 3.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 33 | 46 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 11 | – | |
| | | $Q_3$ | – | 10 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>1.35<br>0.96 | <br>1.75<br>– | Vdc |
| Reverse Recovery Time<br>See Figure 15 | ($I_S$ = 3.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 76 | – | ns |
| | | $t_a$ | – | 32 | – | |
| | | $t_b$ | – | 44 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.133 | – | μC |

3. Negative sign for P–Channel device omitted for clarity.
4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

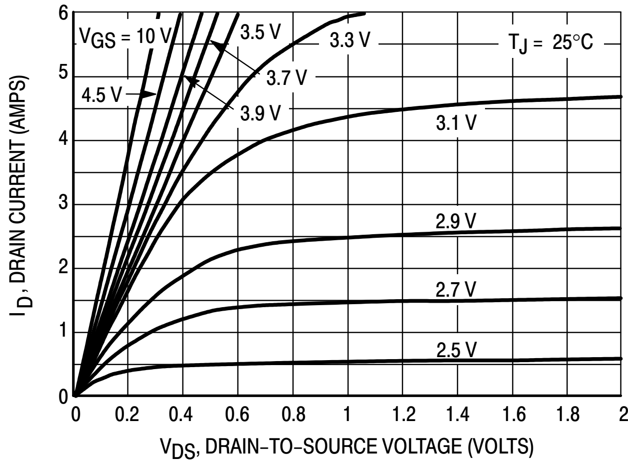



**Figure 1. On–Region Characteristics**

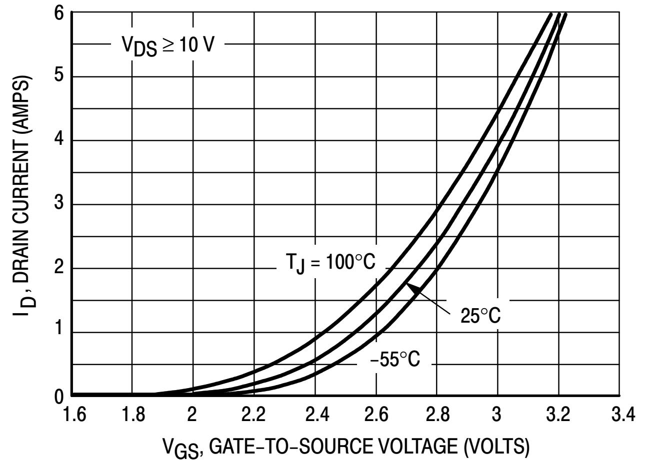



**Figure 2. Transfer Characteristics**

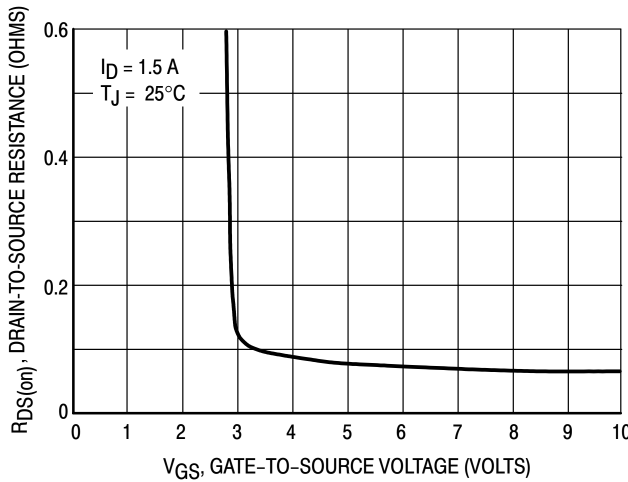



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

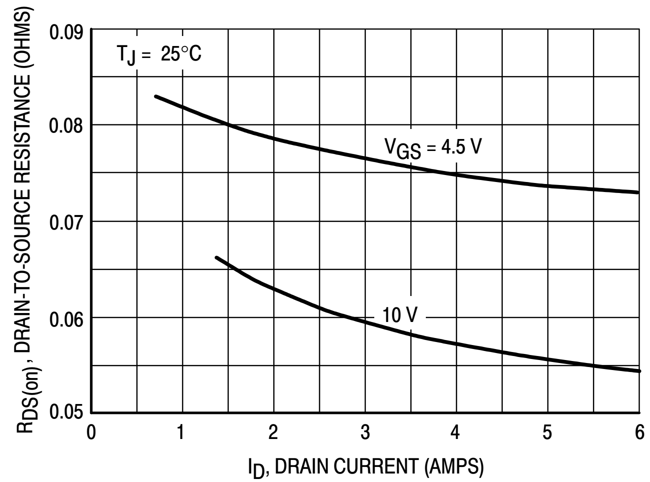



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

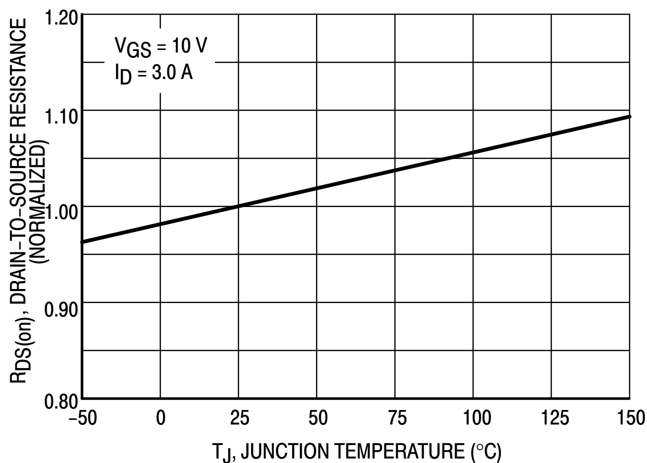



**Figure 5. On–Resistance Variation with Temperature**

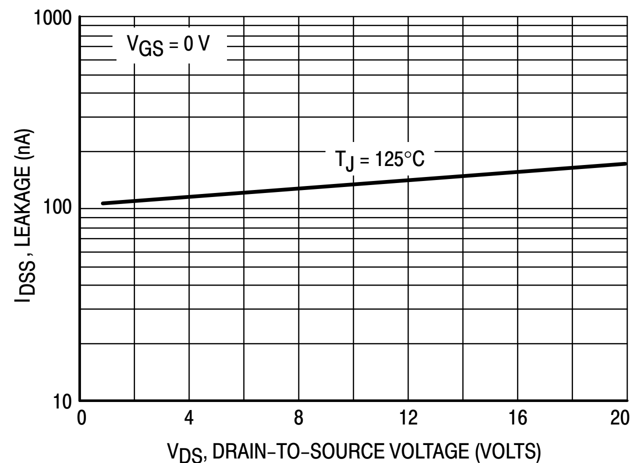



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

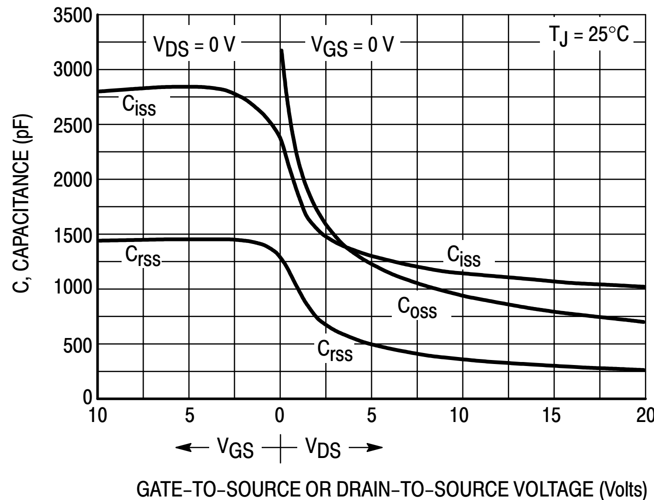



**Figure 7. Capacitance Variation**

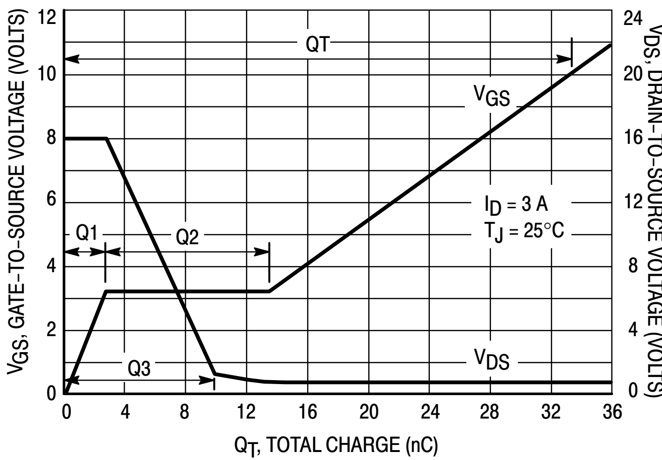



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

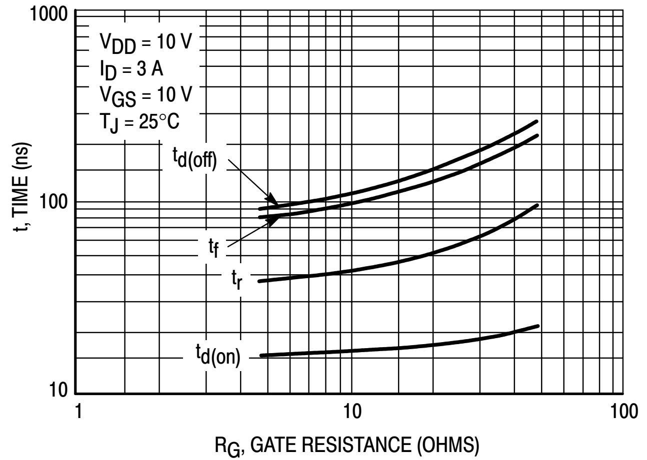



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

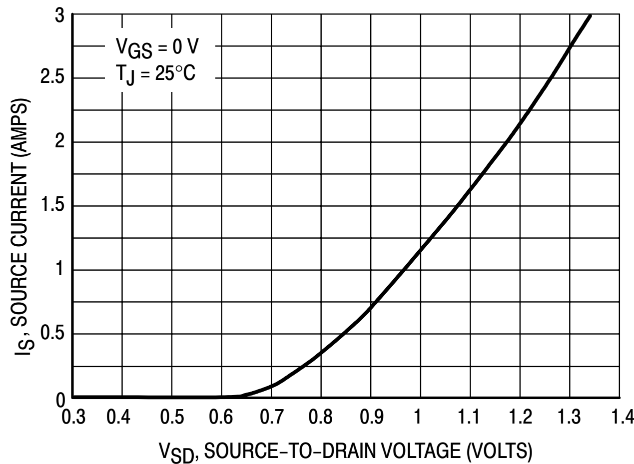



**Figure 10. Diode Forward Voltage versus Current**

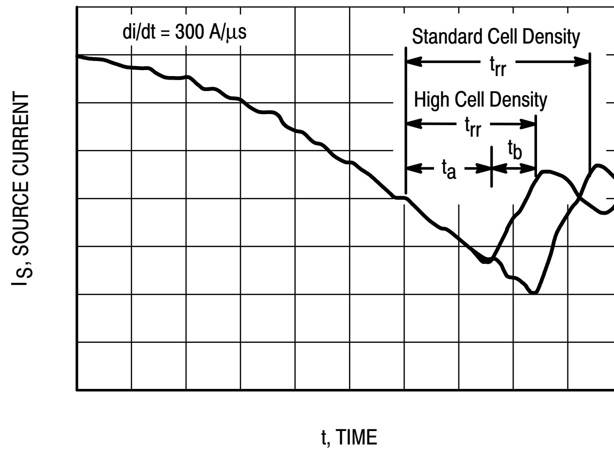



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

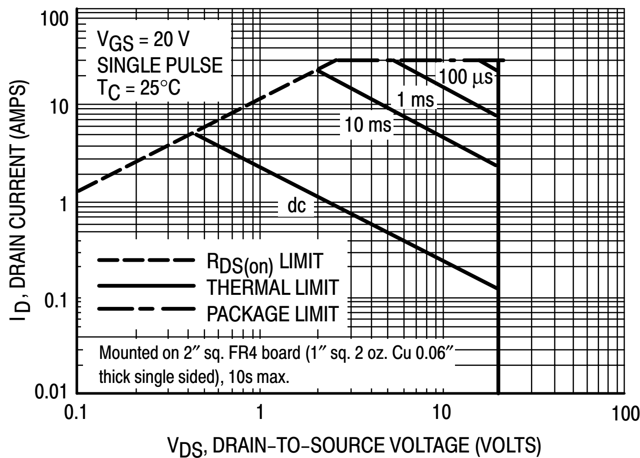



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

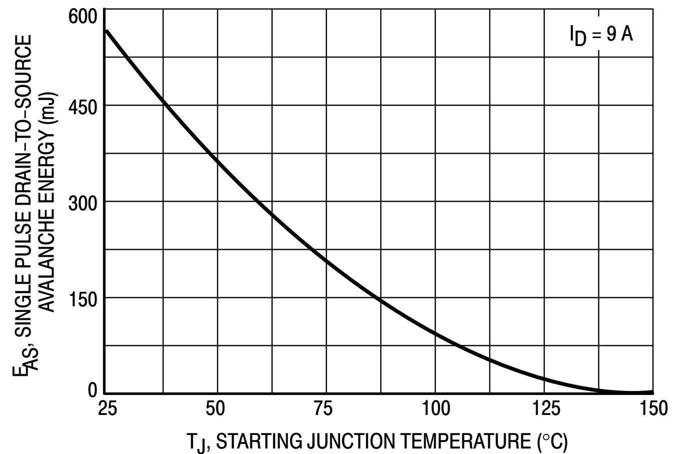



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

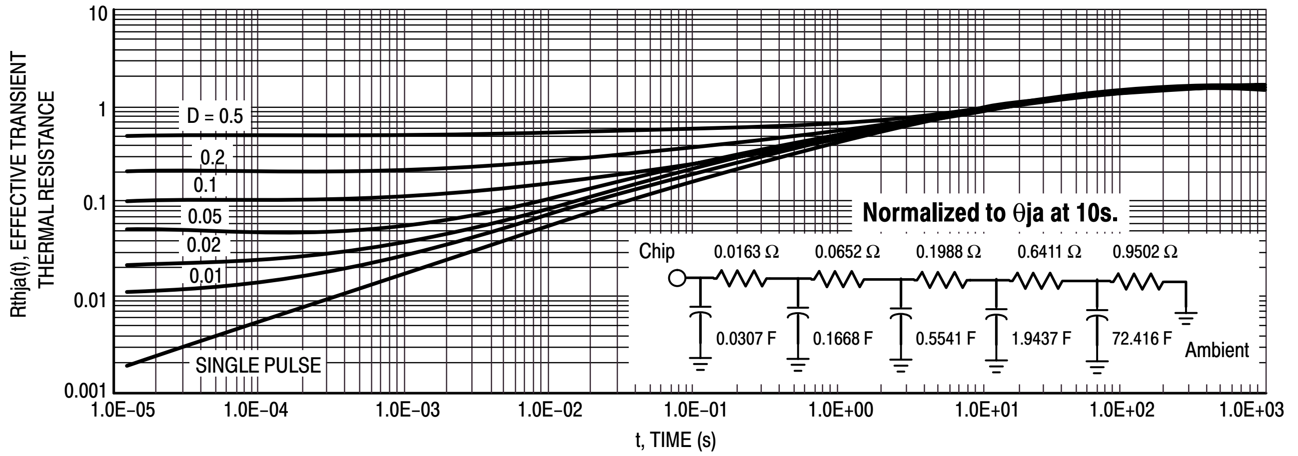



**Figure 14. Thermal Response**

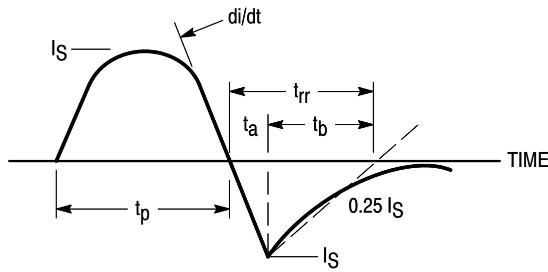
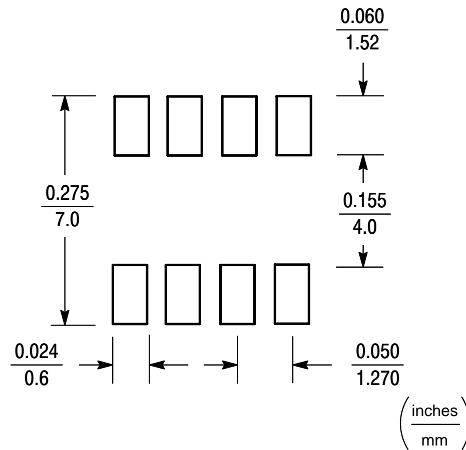



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

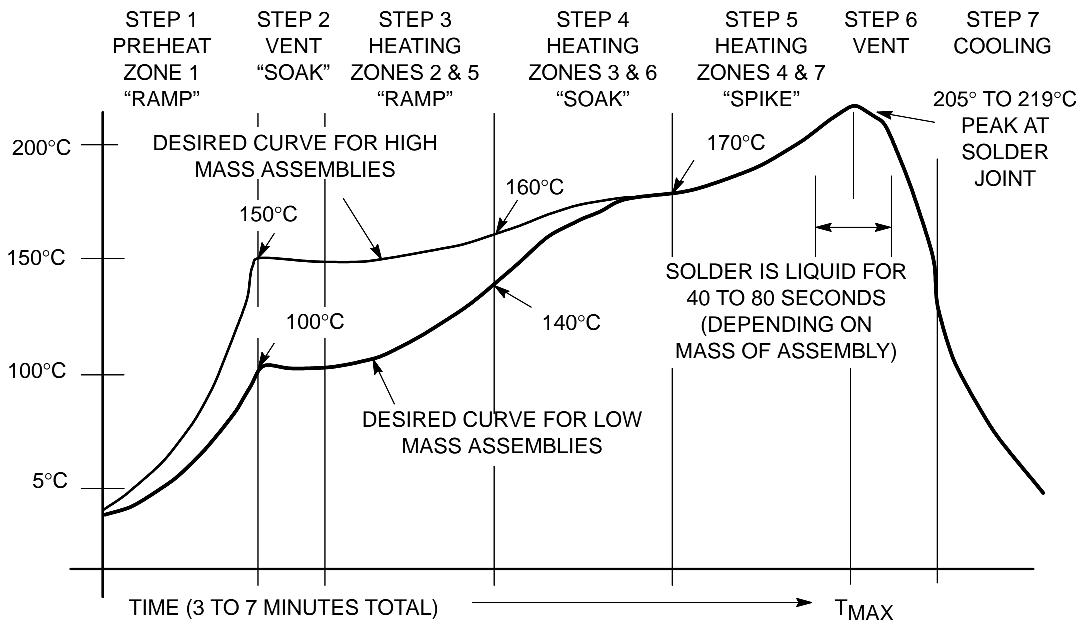



**Figure 16. Typical Solder Heating Profile**

# MMSF5N02HD

Preferred Device

# Power MOSFET 5 Amps, 20 Volts

## N–Channel SO–8

**ON Semiconductor™**

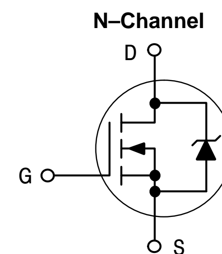
http://onsemi.com

**5 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 25 mΩ**

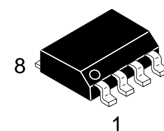
These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

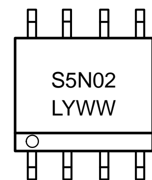
N–Channel




**MARKING DIAGRAM**




**SO–8**
**CASE 751**
**STYLE 13**



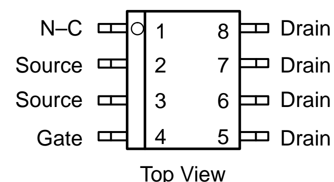

L = Location Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 8.2<br>5.6<br>41 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 20 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 6.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 675 | mJ |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF5N02HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 41 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | 0.02 | 1.0 | μAdc |
| ($V_{DS}$ = 20 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 5.0 Adc) | | $R_{DS(on)}$ | – | 0.0185 | 0.025 | Ohm |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.5 Adc) | | | – | 0.0219 | 0.040 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 3.0 | 12 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1130 | 1582 | pF |
| Output Capacitance | | $C_{oss}$ | – | 464 | 650 | |
| Transfer Capacitance | | $C_{rss}$ | – | 117 | 235 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 93 | 185 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | 70 | |
| Fall Time | | $t_f$ | – | 40 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 9.0 | – | |
| Rise Time | | $t_r$ | – | 53 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 56 | – | |
| Fall Time | | $t_f$ | – | 39 | – | |
| Gate Charge See Figure 8 | ($V_{DS}$ = 16 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 30.3 | 43 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 7.5 | – | |
| | | $Q_3$ | – | 6.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.82 | 1.0 | Vdc |
| | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.69 | – | |
| Reverse Recovery Time See Figure 15 | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 32 | – | ns |
| | | $t_a$ | – | 24 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.045 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

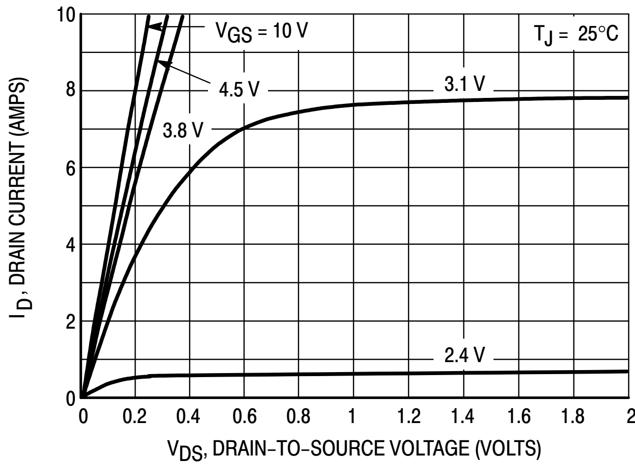



**Figure 1. On–Region Characteristics**

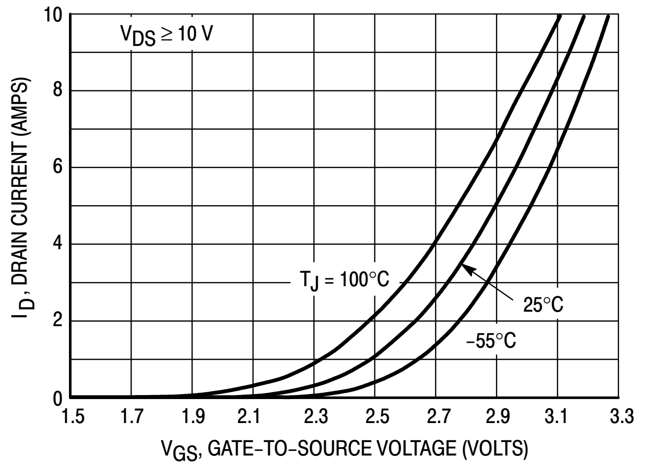



**Figure 2. Transfer Characteristics**

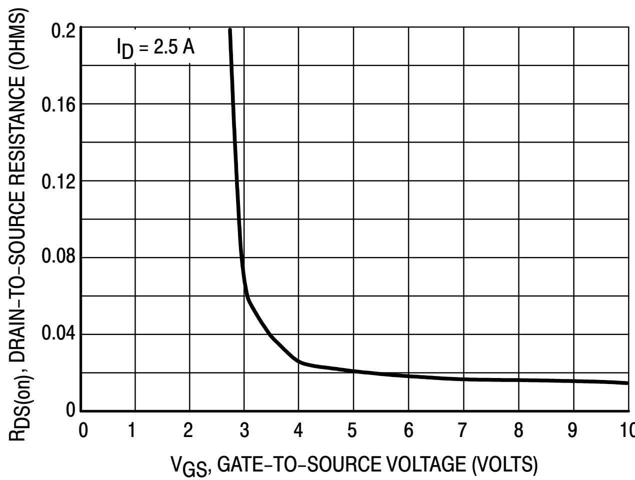



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

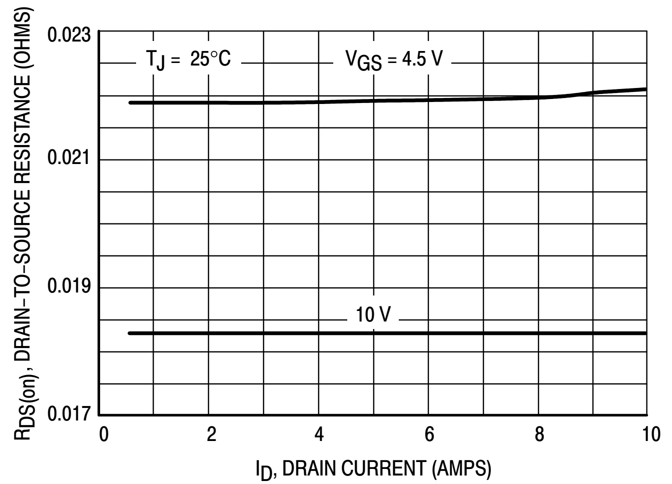



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

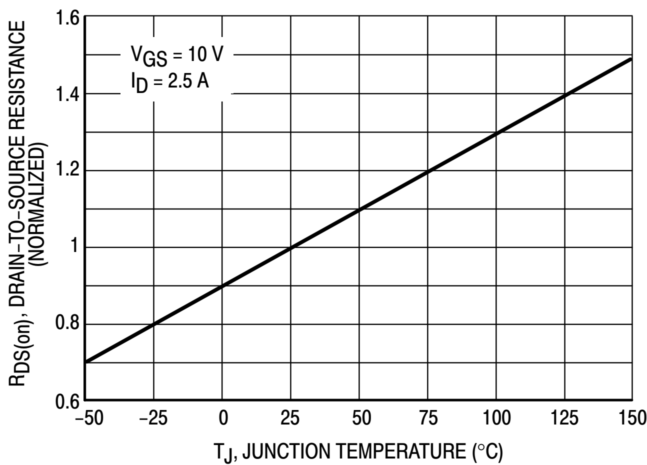



**Figure 5. On–Resistance Variation with Temperature**

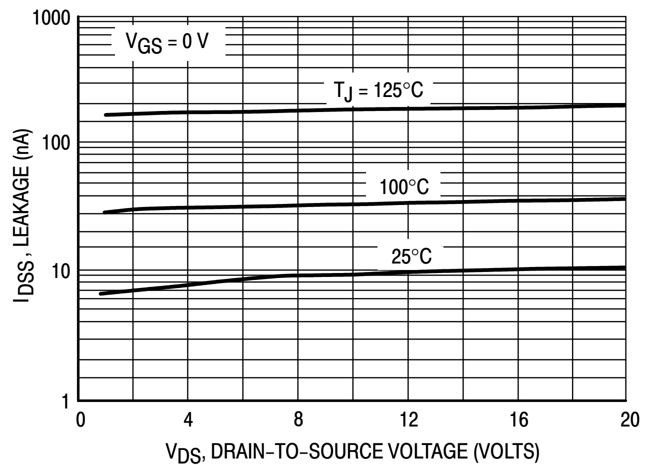



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

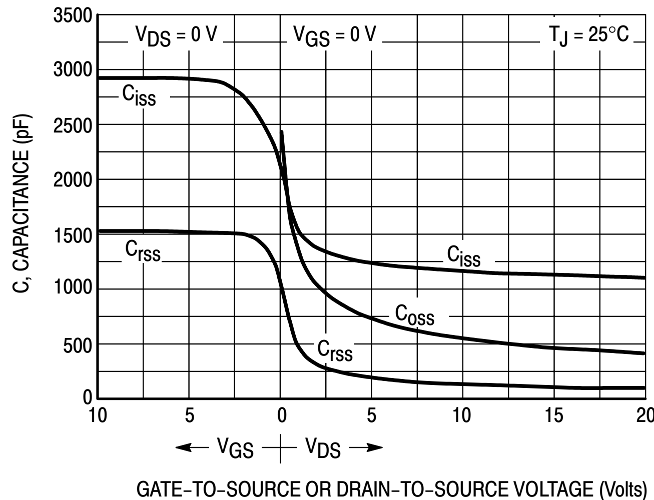



**Figure 7. Capacitance Variation**

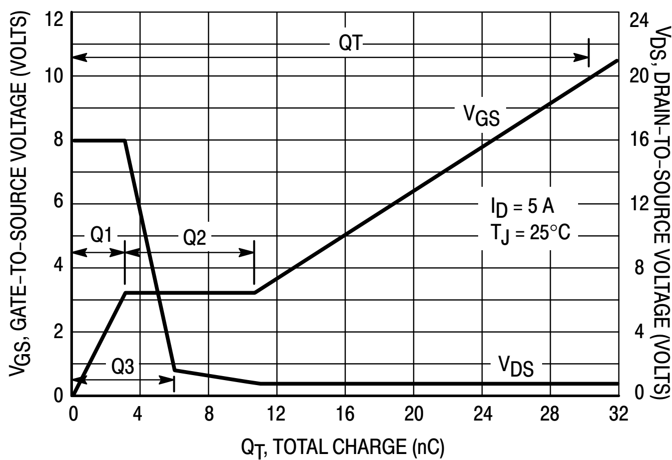



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

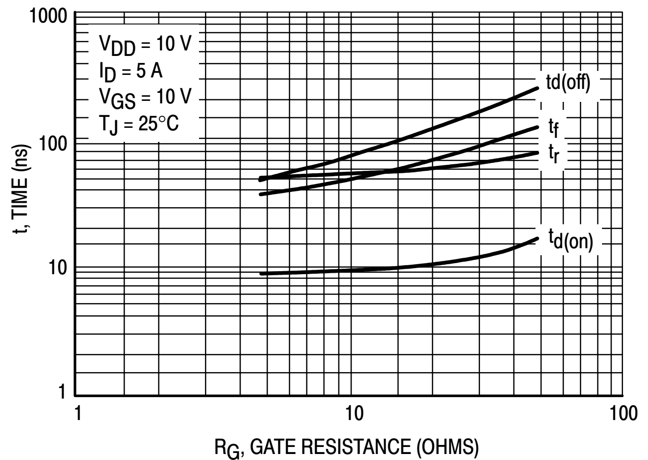



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

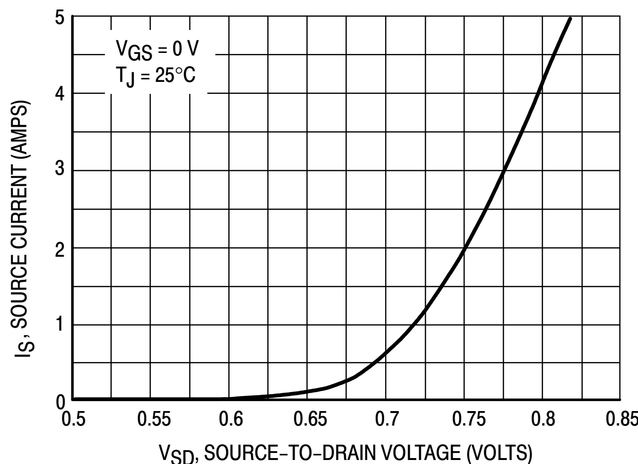



**Figure 10. Diode Forward Voltage versus Current**

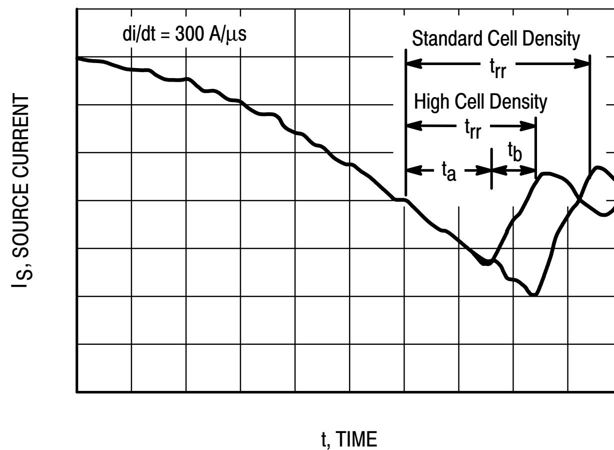



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

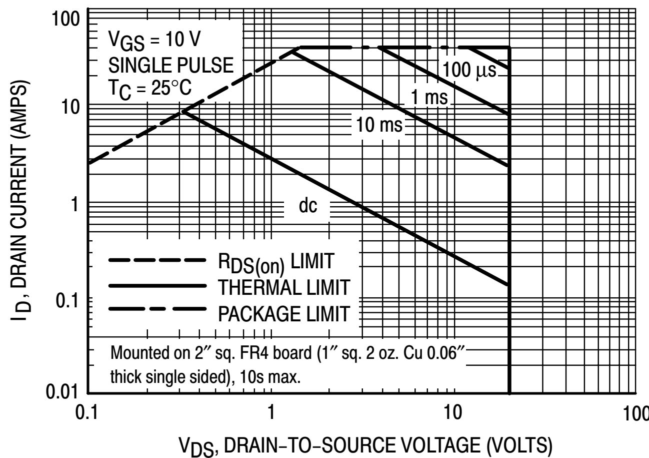



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

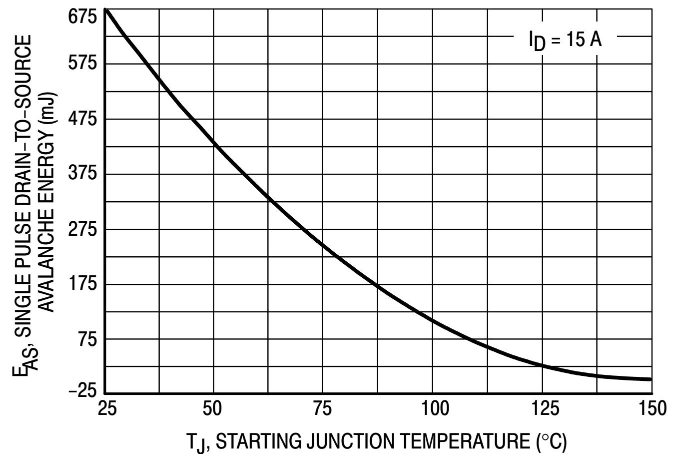



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

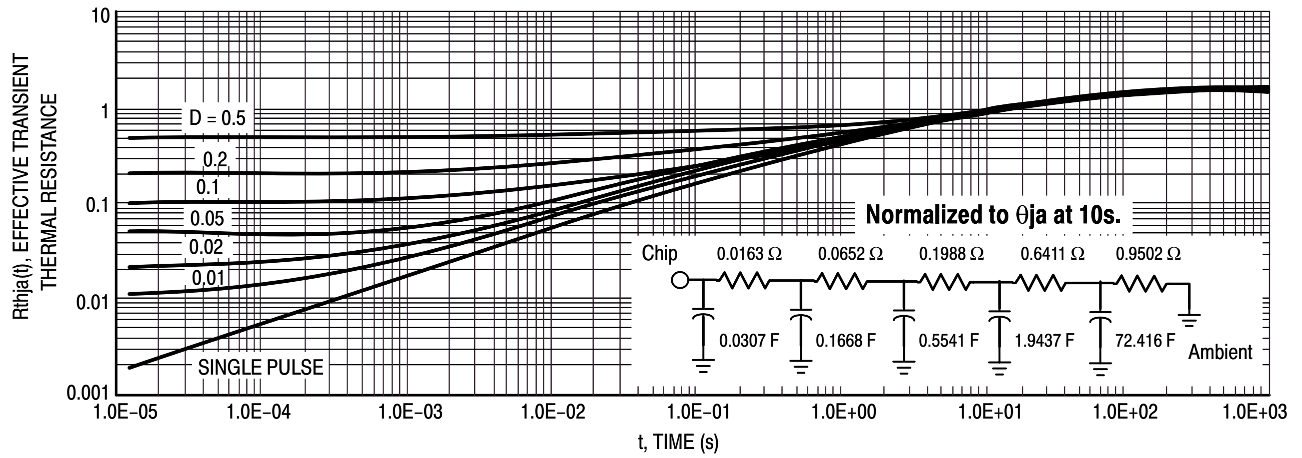



**Figure 14. Thermal Response**

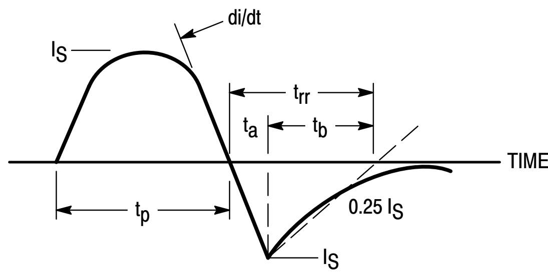
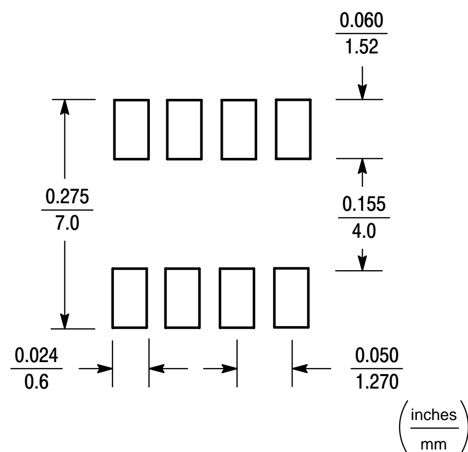



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

### TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

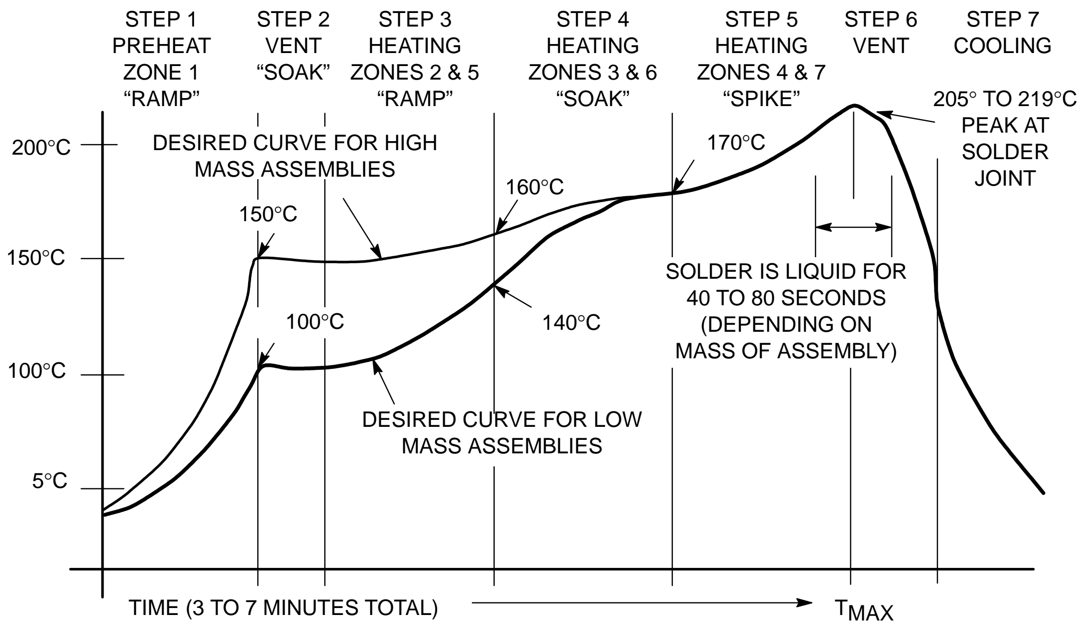



**Figure 16. Typical Solder Heating Profile**

# MMSF5N03HD

**Preferred Device**

# Power MOSFET 5 Amps, 30 Volts
## N–Channel SO–8

**ON Semiconductor™**

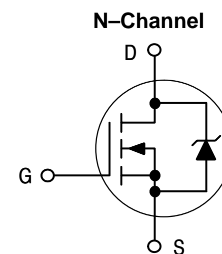
**http://onsemi.com**

**5 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

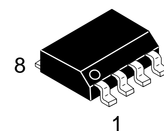
These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

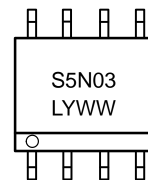
N–Channel




**MARKING DIAGRAM**

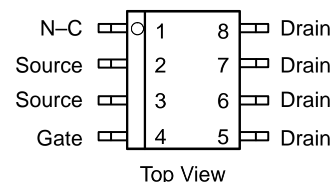



**SO–8**
**CASE 751**
**STYLE 13**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 6.5<br>4.4<br>33 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 4.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 450 | mJ |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF5N03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 30<br>– | –<br>34 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 2.0<br>5.0 | 3.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 5.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | –<br>– | 0.033<br>0.04 | 0.040<br>0.050 | Ohms |
| Forward Transconductance ($V_{DS}$ = 3 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 3.0 | 8.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1207 | 1680 | pF |
| Output Capacitance | | $C_{oss}$ | – | 354 | 490 | |
| Transfer Capacitance | | $C_{rss}$ | – | 62 | 120 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 20 | 40 | ns |
| Rise Time | | $t_r$ | – | 108 | 216 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 36 | 72 | |
| Fall Time | | $t_f$ | – | 37 | 74 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 22 | |
| Rise Time | | $t_r$ | – | 36 | 72 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 68 | 136 | |
| Fall Time | | $t_f$ | – | 38 | 76 | |
| Gate Charge<br>See Figure 8 | ($V_{DS}$ = 24 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 15.2 | 21 | nC |
| | | $Q_1$ | – | 3.4 | – | |
| | | $Q_2$ | – | 6.6 | – | |
| | | $Q_3$ | – | 5.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.88<br>0.77 | 1.3<br>– | Vdc |
| Reverse Recovery Time<br>See Figure 15 | ($I_S$ = 5.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 33 | – | ns |
| | | $t_a$ | – | 21 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.037 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

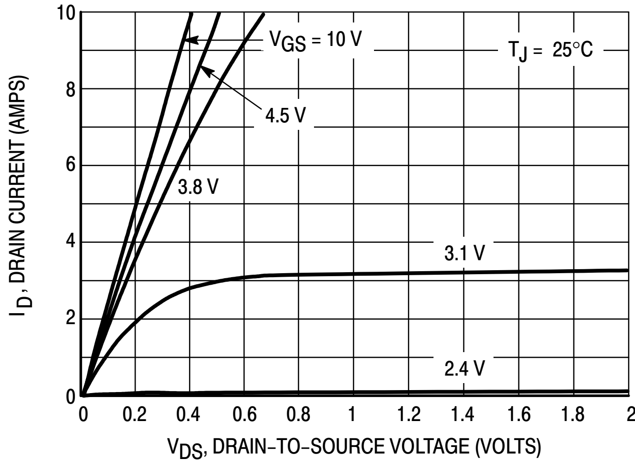



**Figure 1. On–Region Characteristics**

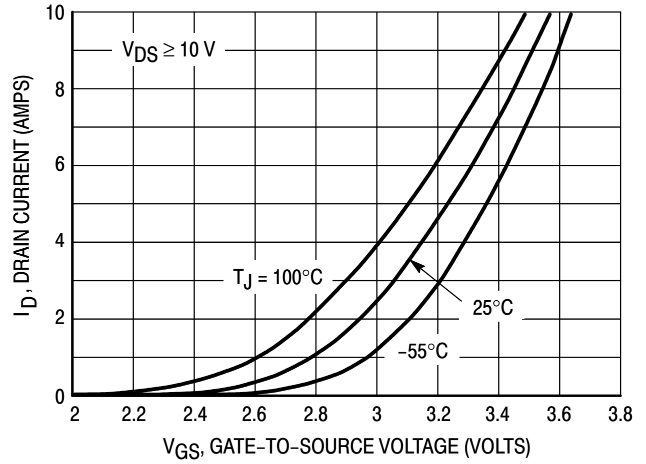



**Figure 2. Transfer Characteristics**

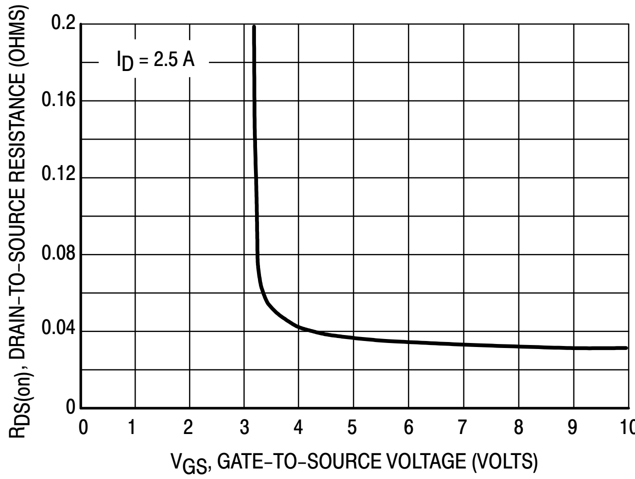



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

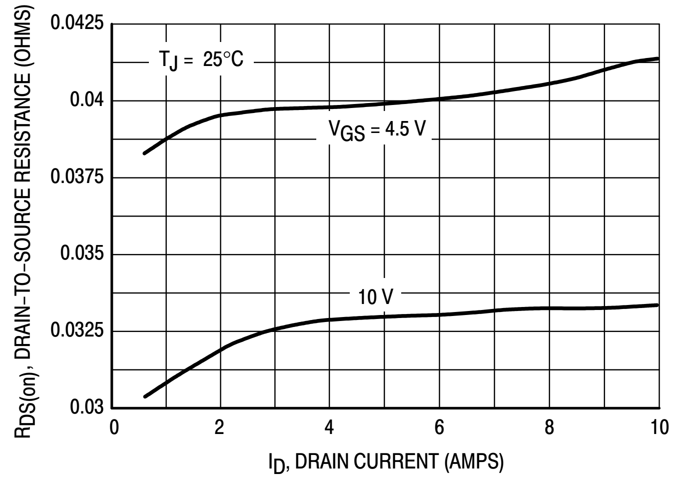



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

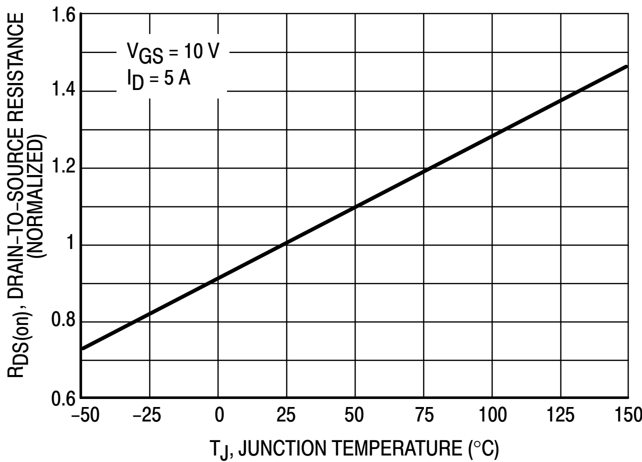



**Figure 5. On–Resistance Variation with Temperature**

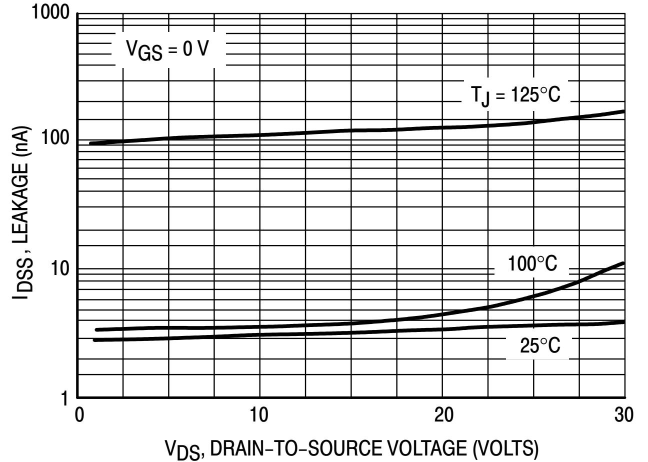



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

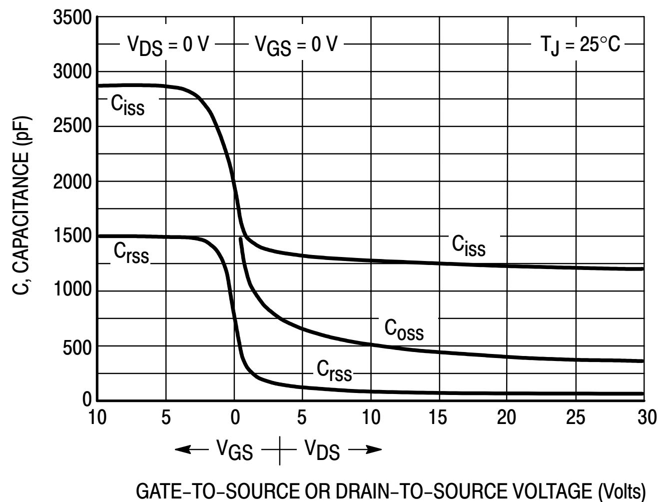



**Figure 7. Capacitance Variation**

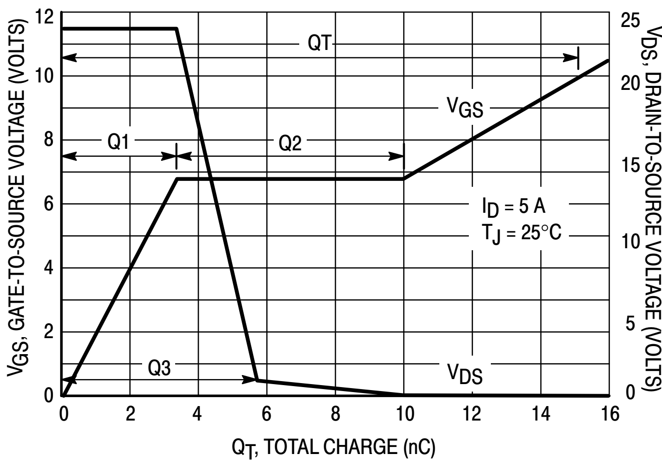



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

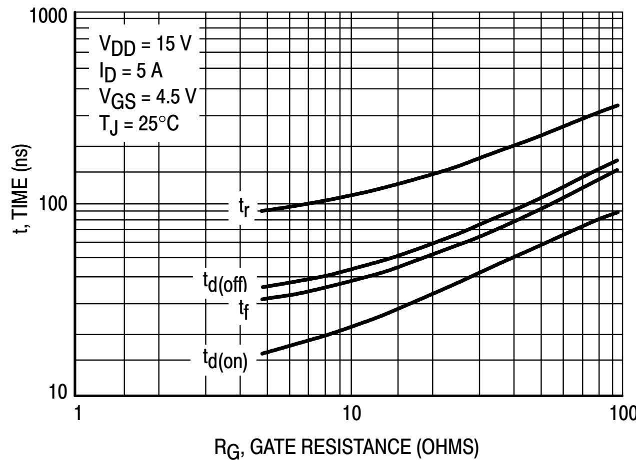



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

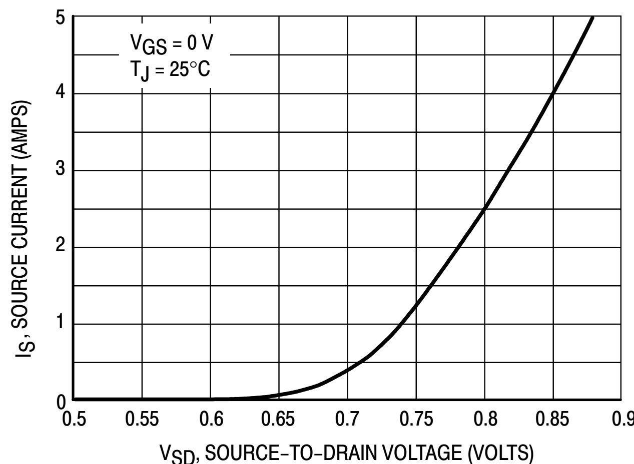



Figure 10. Diode Forward Voltage versus Current

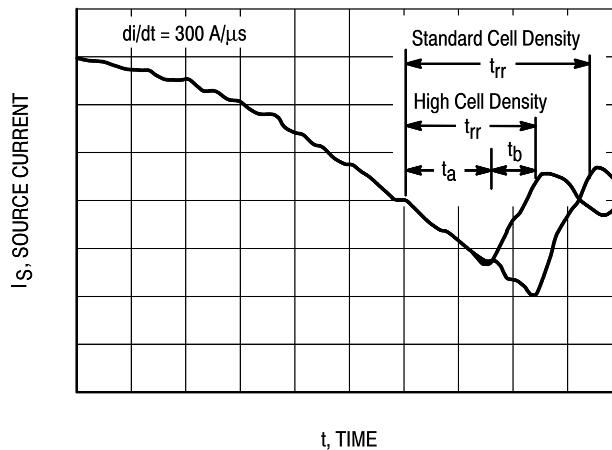



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

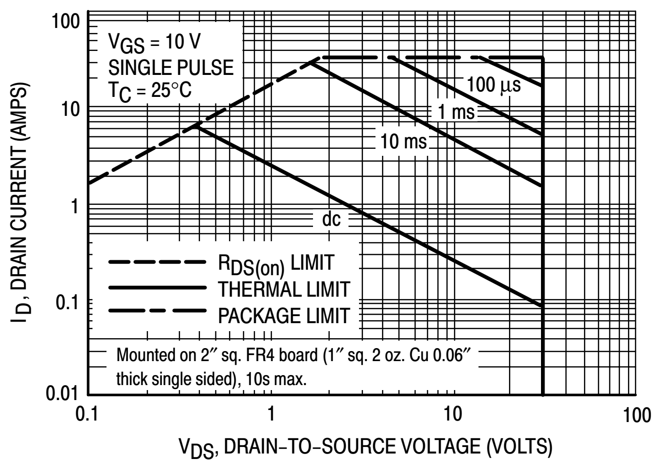



Figure 12. Maximum Rated Forward Biased Safe Operating Area

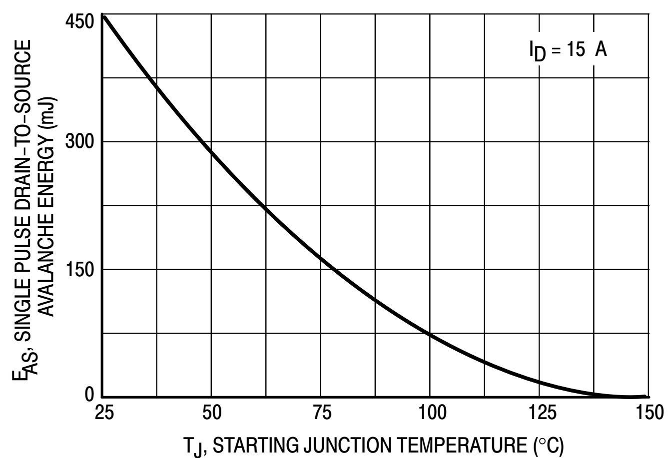



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

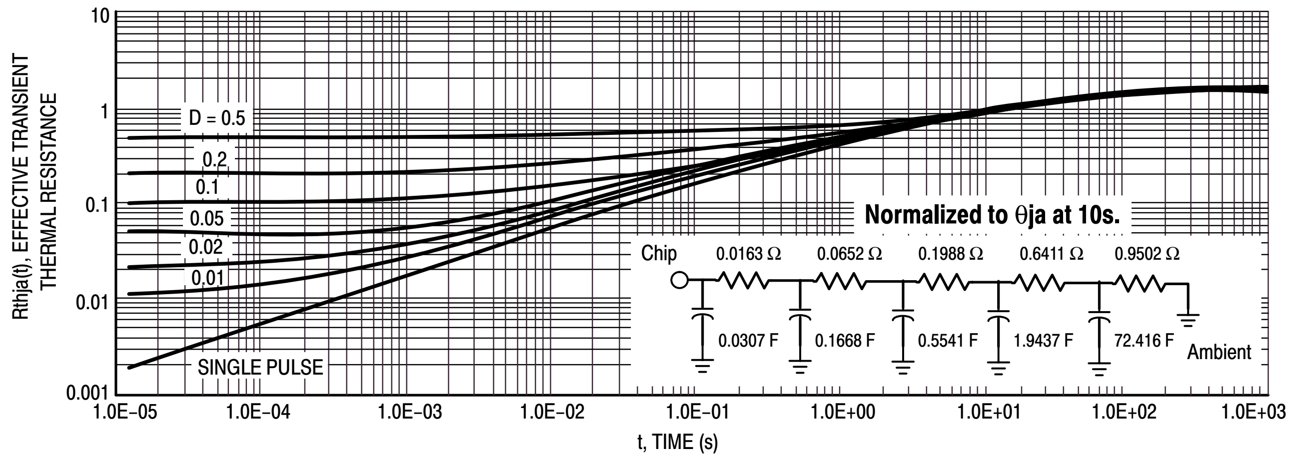



**Figure 14. Thermal Response**

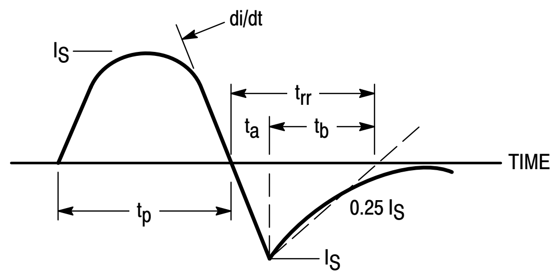
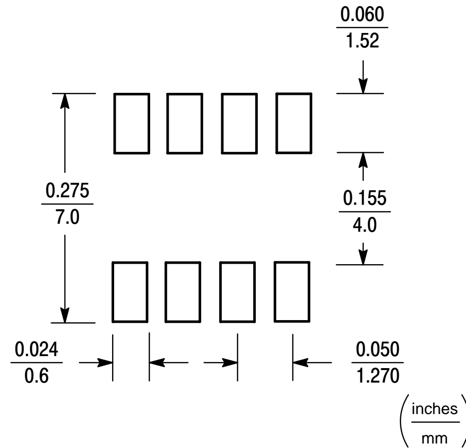



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

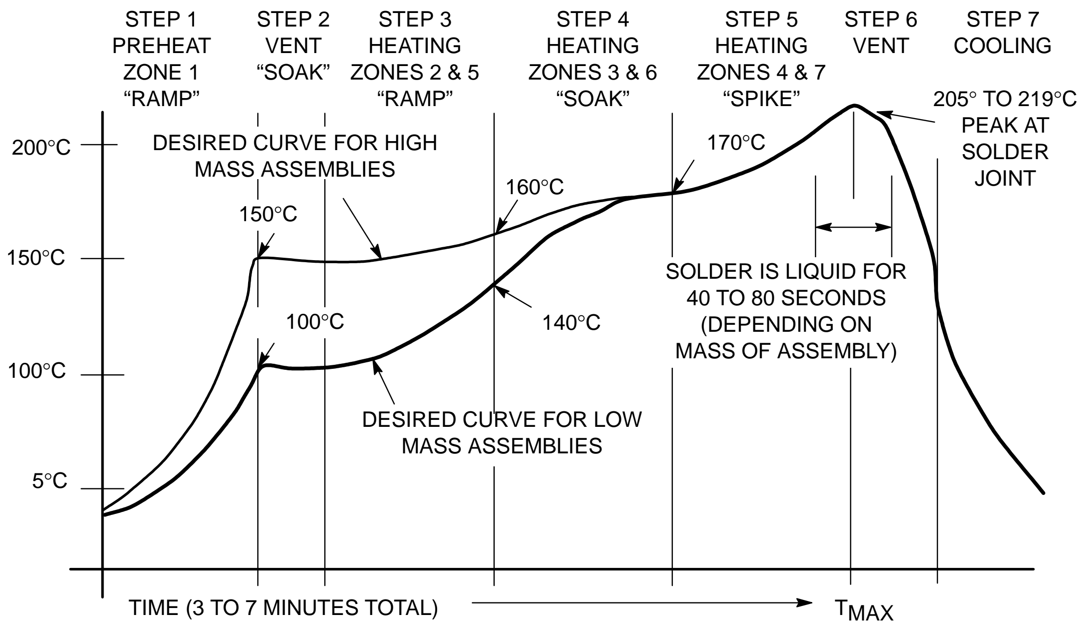



**Figure 16. Typical Solder Heating Profile**

# MMSF7N03HD

**Preferred Device**

# Power MOSFET 7 Amps, 30 Volts

## N–Channel SO–8

These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. MiniMOS™ devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for SO–8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C<br>– Continuous @ $T_A$ = 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 8.2<br>5.6<br>50 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 2.5 | Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 4.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 450 | mJ |
| Thermal Resistance – Junction to Ambient (Note 1.) | $R_{\theta JA}$ | 50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

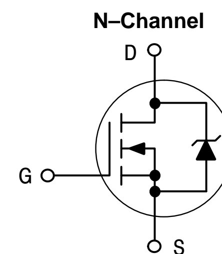
1. Mounted on 2″ square FR4 board (1″ sq. 2 oz. Cu 0.06″ thick single sided), 10 sec. max.

**ON Semiconductor™**

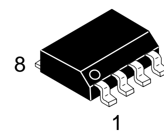
http://onsemi.com

**7 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

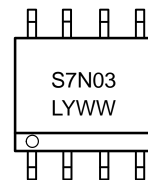
N–Channel




**MARKING DIAGRAM**

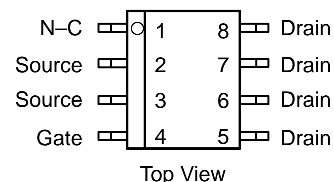



**SO–8**
**CASE 751**
**STYLE 13**




L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF7N03HDR2 | SO–8 | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 30<br>– | –<br>41 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | 0.02<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.5<br>4.0 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 7.0 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.5 Adc) | | $R_{DS(on)}$ | –<br>– | 0.023<br>0.029 | 0.028<br>0.040 | Ohms |
| Forward Transconductance ($V_{DS}$ = 3 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 3.0 | 12 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 931 | 1190 | pF |
| Output Capacitance | | $C_{oss}$ | – | 371 | 490 | |
| Transfer Capacitance | | $C_{rss}$ | – | 89 | 120 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 93 | 185 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 35 | 70 | |
| Fall Time | | $t_f$ | – | 40 | 80 | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 9.0 | – | |
| Rise Time | | $t_r$ | – | 53 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 56 | – | |
| Fall Time | | $t_f$ | – | 39 | | |
| Gate Charge<br>See Figure 8 | ($V_{DS}$ = 16 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 30 | 43 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 7.5 | – | |
| | | $Q_3$ | – | 6.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.82<br>0.69 | 1.0<br>– | Vdc |
| Reverse Recovery Time<br>See Figure 15 | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 32 | – | ns |
| | | $t_a$ | – | 24 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.045 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

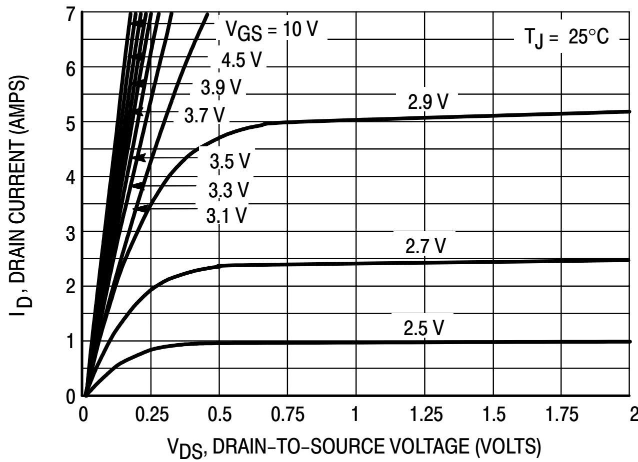



**Figure 1. On–Region Characteristics**

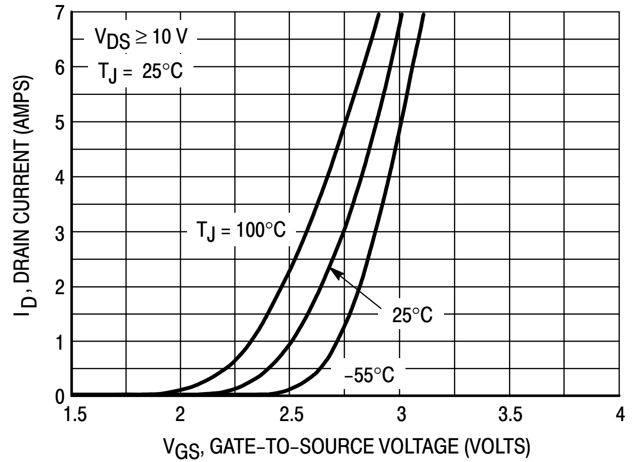



**Figure 2. Transfer Characteristics**

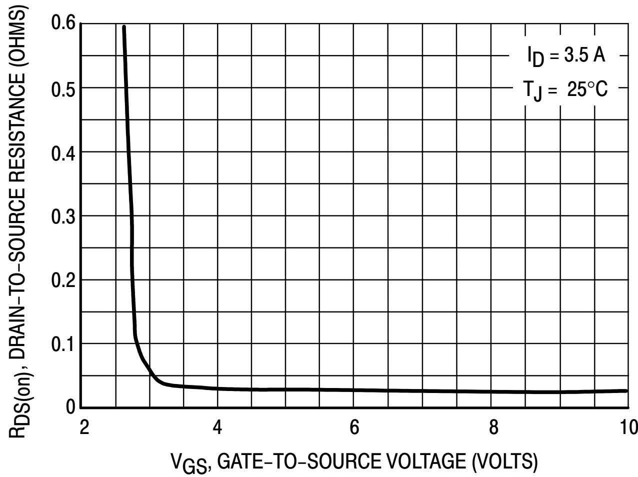



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

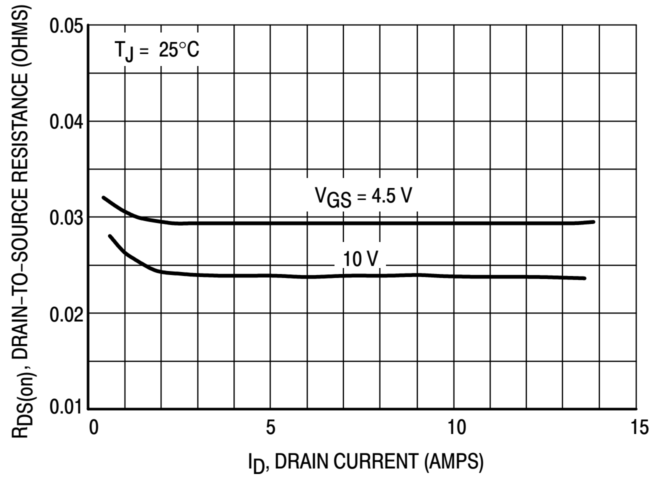



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

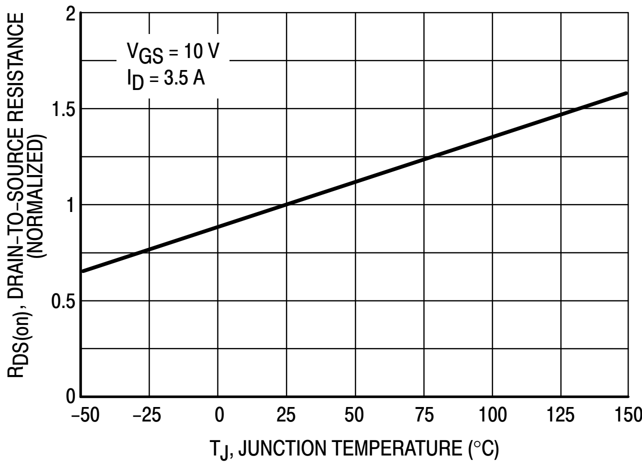



**Figure 5. On–Resistance Variation with Temperature**

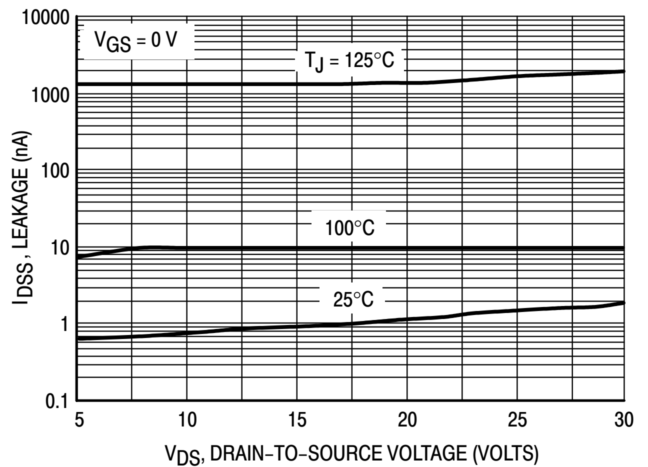



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

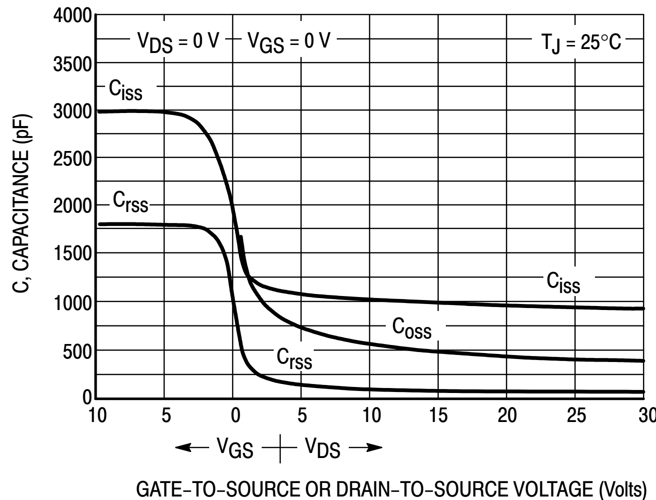



**Figure 7. Capacitance Variation**

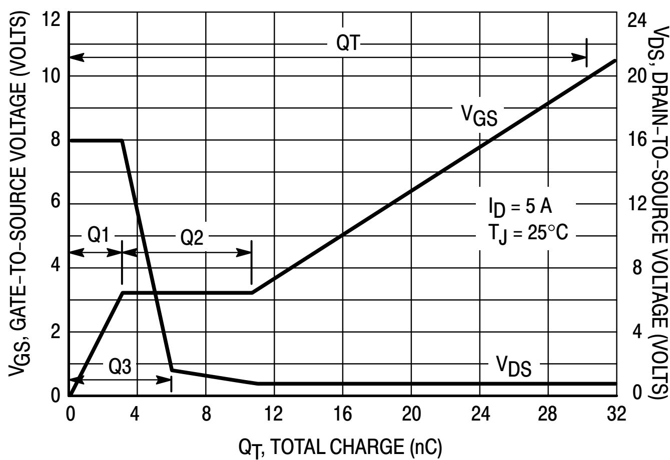
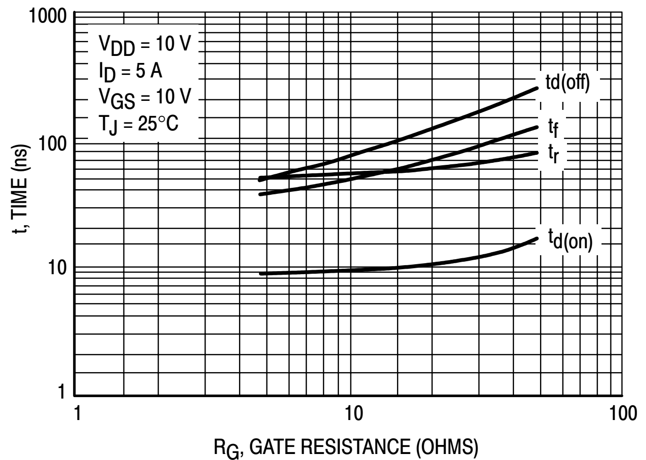



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

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The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

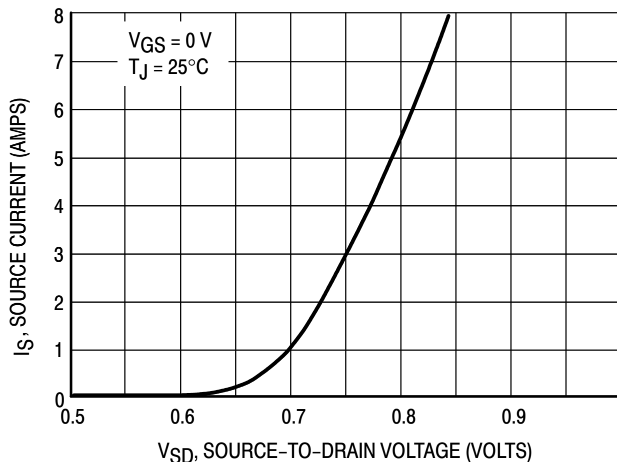



**Figure 10. Diode Forward Voltage versus Current**

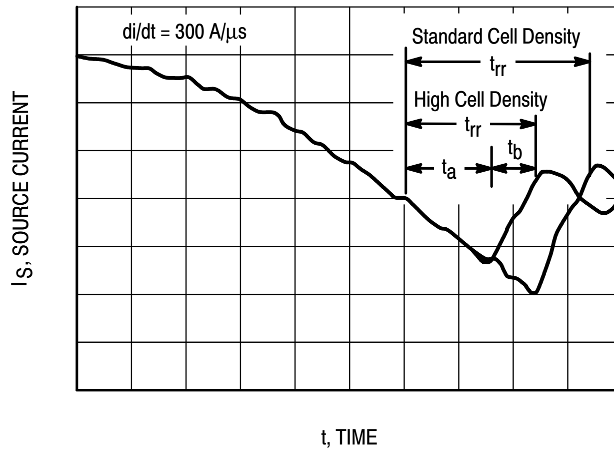



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

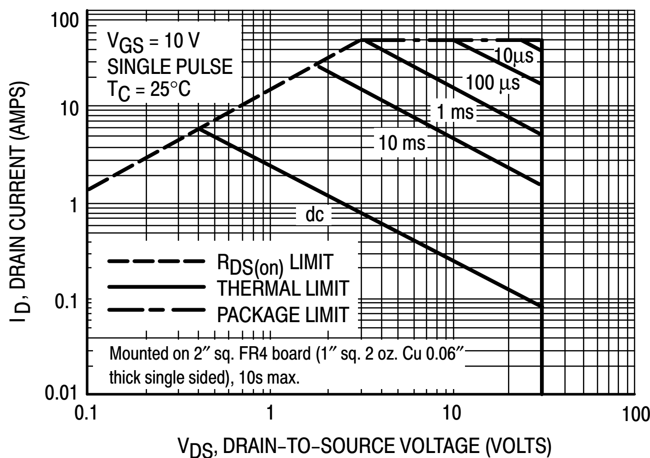



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

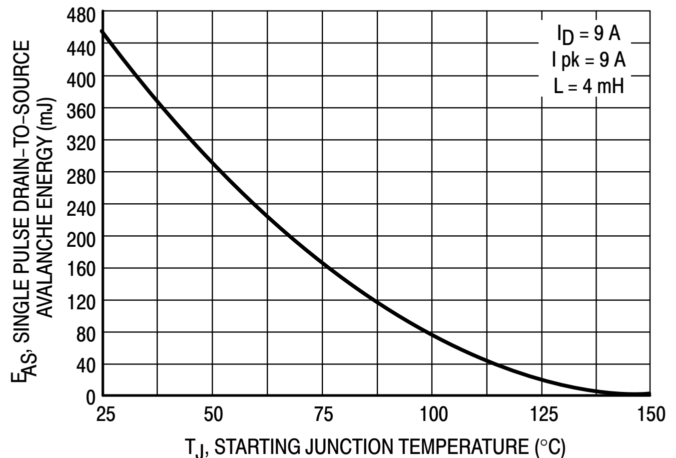



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

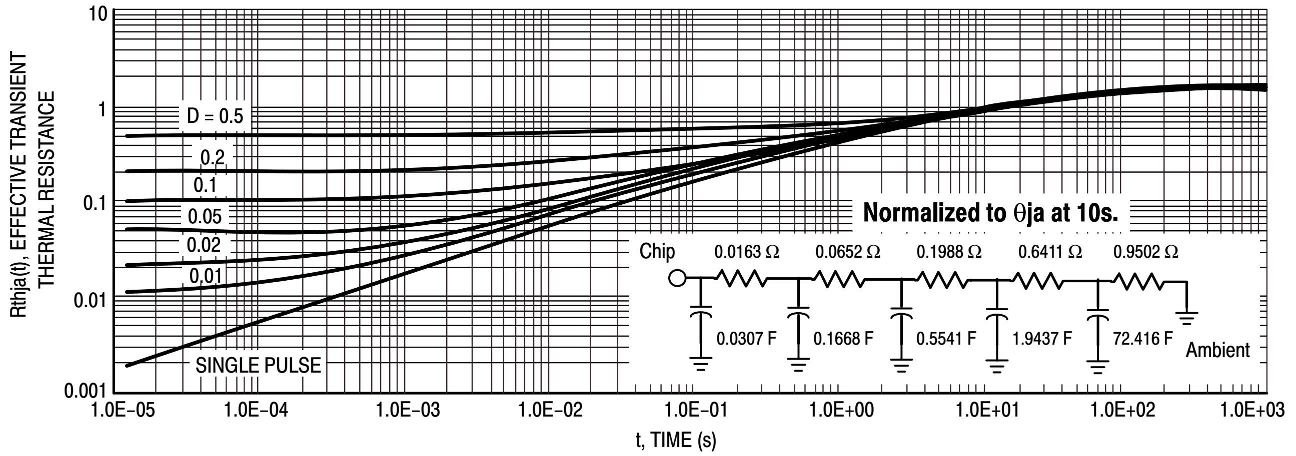



**Figure 14. Thermal Response**

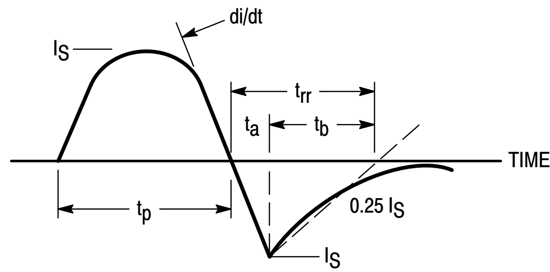
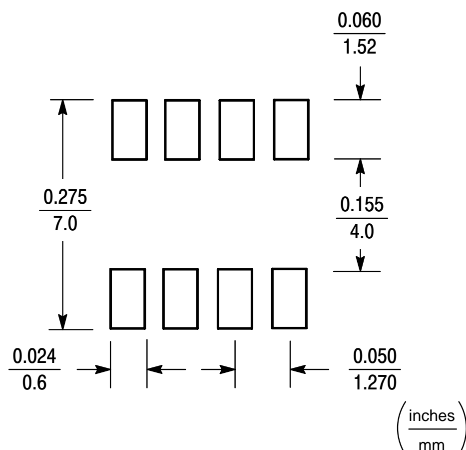



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

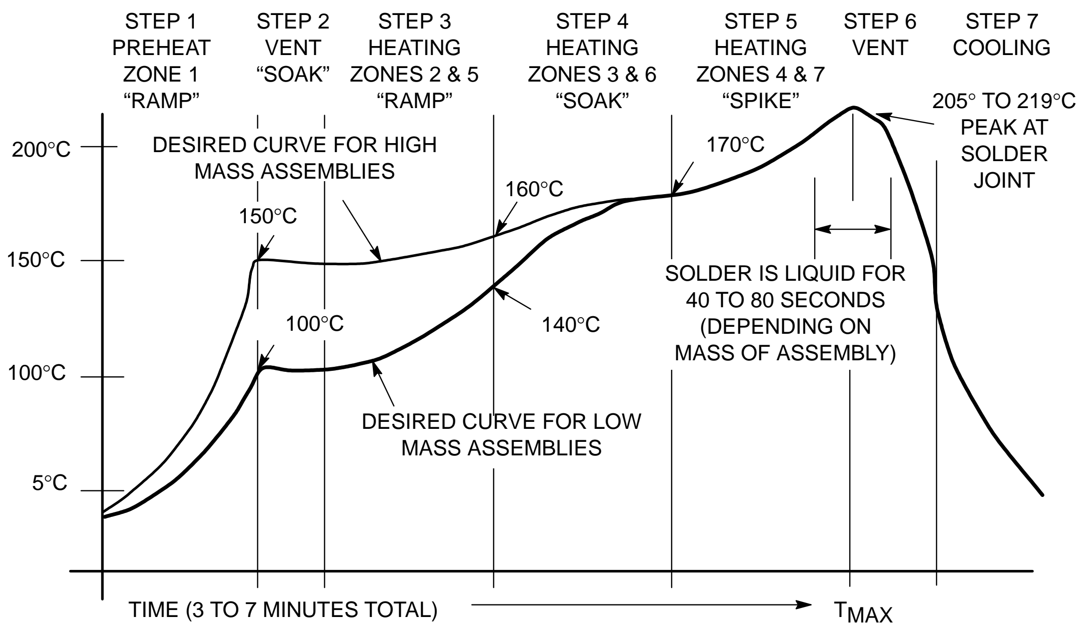



**Figure 16. Typical Solder Heating Profile**

# MMSF7N03Z

**ON Semiconductor™**

**http://onsemi.com**

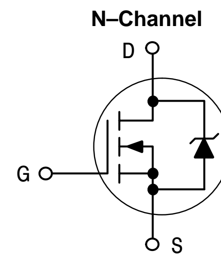
## Power MOSFET
## 7 Amps, 30 Volts
### N–Channel SO–8

EZFETs™ are an advanced series of Power MOSFETs which contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. EZFET devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

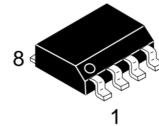
- Zener Protected Gates Provide Electrostatic Discharge Protection
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Designed to withstand 200V Machine Model and 2000V Human Body Model
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Miniature SO–8 Surface Mount Package – Saves Board Space
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for SO–8 Package Provided

**7 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 30 mΩ**

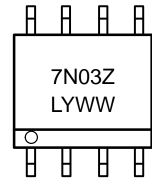
**N–Channel**




**MARKING DIAGRAM**

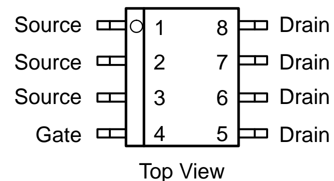



**SO–8**
**CASE 751**
**STYLE 12**




7N03Z = Device Code
L = Location Code
Y = Year
WW = Work Week

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MMSF7N03ZR2 | SO–8 | 2500 Tape & Reel |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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 15 | Vdc |
| Drain Current<br>– Continuous @ $T_A$ = 25°C (Note 1.)<br>– Continuous @ $T_A$ = 70°C (Note 1.)<br>– Pulsed Drain Current (Note 3.) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>7.5<br>5.6<br>60 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Linear Derating Factor (Note 1.) | $P_D$ | 2.5<br>20 | Watts<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Linear Derating Factor (Note 2.) | $P_D$ | 1.6<br>12 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 4.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | <br>450 | mJ |
| Thermal Resistance<br>– Junction to Ambient (Note 1.)<br>– Junction to Ambient (Note 2.) | $R_{\theta JA}$ | 50<br>80 | °C/W |

1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ 10 Seconds)
2. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ Steady State)
3. Repetitive rating; pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>35 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>0.03<br>0.15 | <br>2.0<br>10 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | 1.3 | 5.0 | µAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>2.0<br>5.5 | <br>3.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 7.5 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.8 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>22<br>30 | <br>30<br>40 | mΩ |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 3.8 Adc) (Note 4.) | | $g_{FS}$ | 4.0 | 9.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 750 | 1500 | pF |
| Output Capacitance | | $C_{oss}$ | – | 340 | 680 | |
| Transfer Capacitance | | $C_{rss}$ | – | 45 | 90 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6 Ω) (Note 4.) | $t_{d(on)}$ | – | 40 | 80 | ns |
| Rise Time | | $t_r$ | – | 90 | 180 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 470 | 940 | |
| Fall Time | | $t_f$ | – | 170 | 340 | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 4.) | $t_{d(on)}$ | – | 120 | 240 | ns |
| Rise Time | | $t_r$ | – | 350 | 700 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 430 | 860 | |
| Fall Time | | $t_f$ | – | 140 | 280 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 5.0 Adc, $V_{GS}$ = 10 Vdc) (Note 4.) | $Q_T$ | – | 34 | 48 | nC |
| | | $Q_1$ | – | 3.5 | – | |
| | | $Q_2$ | – | 9.5 | – | |
| | | $Q_3$ | – | 6.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 4.) | ($I_S$ = 7.5 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 7.5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.83<br>0.67 | <br>1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 7.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) (Note 4.) | $t_{rr}$ | – | 110 | – | ns |
| | | $t_a$ | – | 22 | – | |
| | | $t_b$ | – | 90 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.17 | – | µC |

4. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
6. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

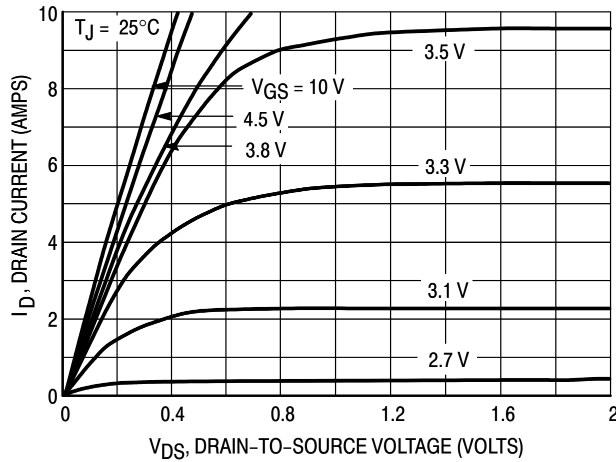



**Figure 1. On–Region Characteristics**

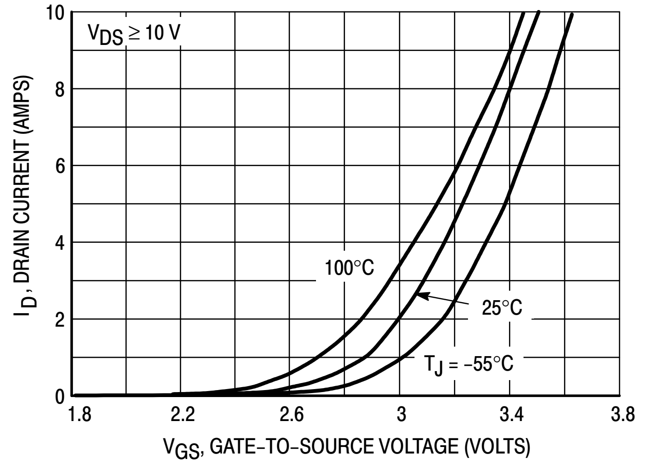



**Figure 2. Transfer Characteristics**

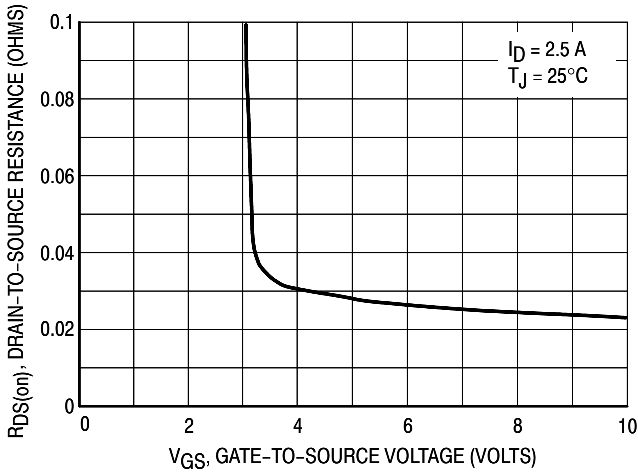



**Figure 3. On–Resistance versus Gate–to–Source Voltage**

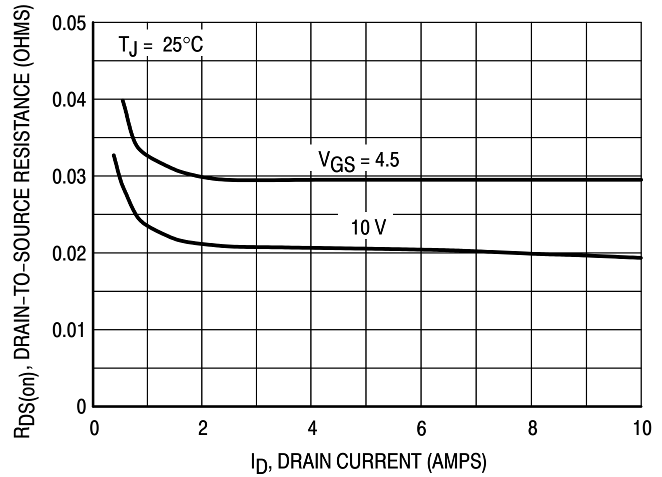



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

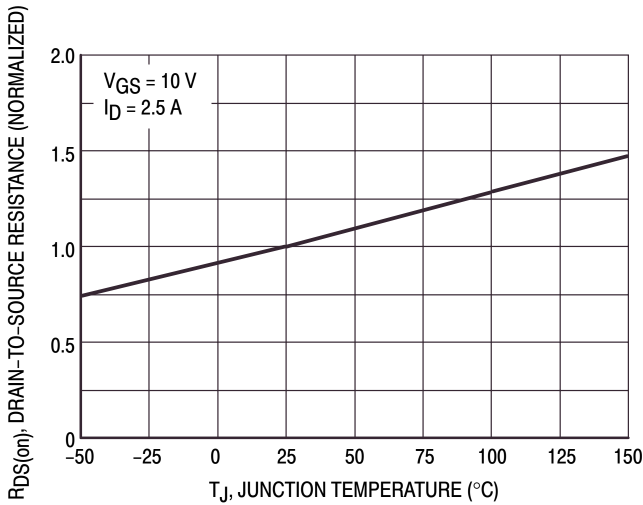



**Figure 5. On–Resistance Variation with Temperature**

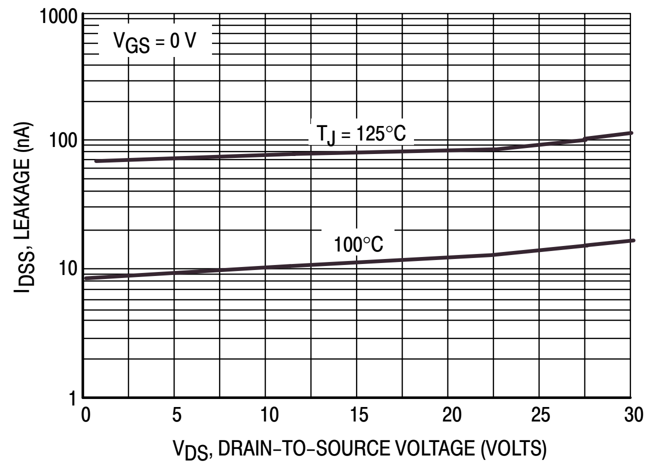



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

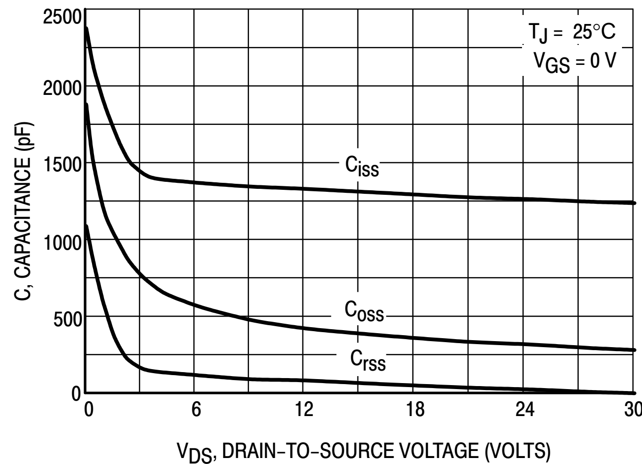



**Figure 7. Capacitance Variation**

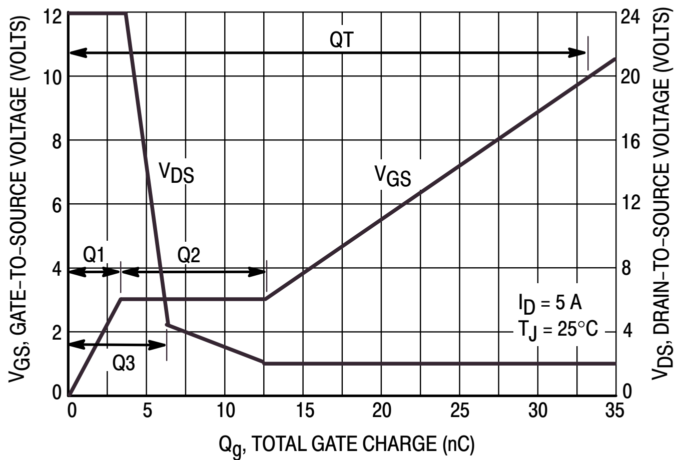



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

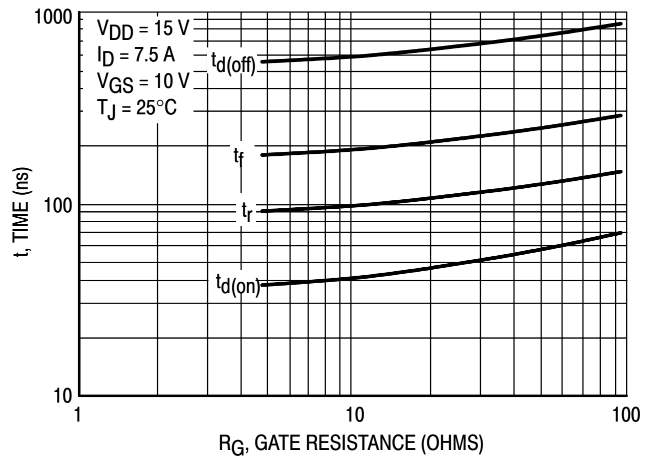



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

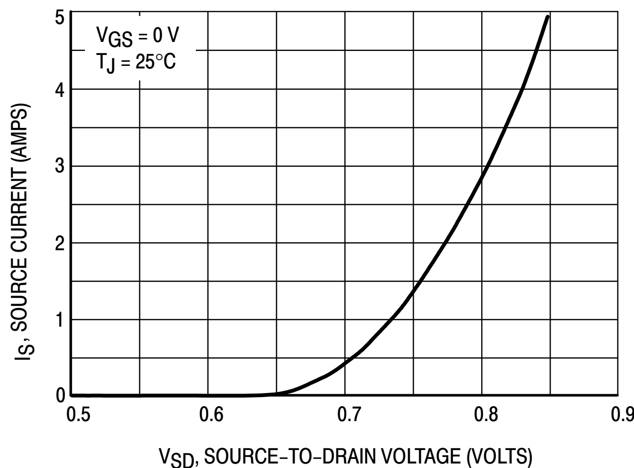



**Figure 10. Diode Forward Voltage versus Current**

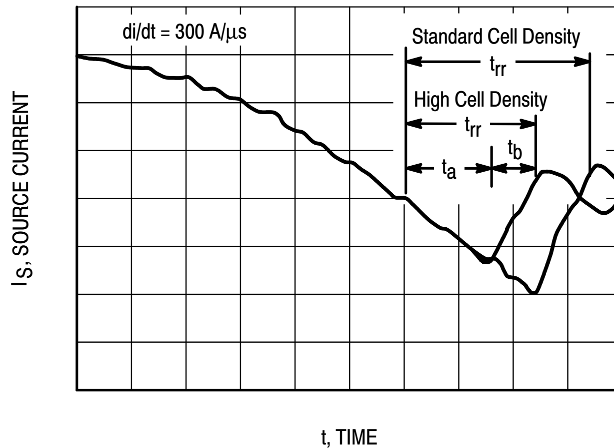



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

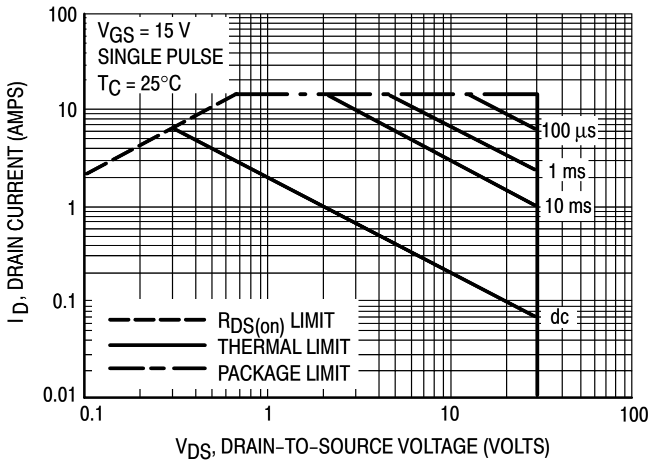



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

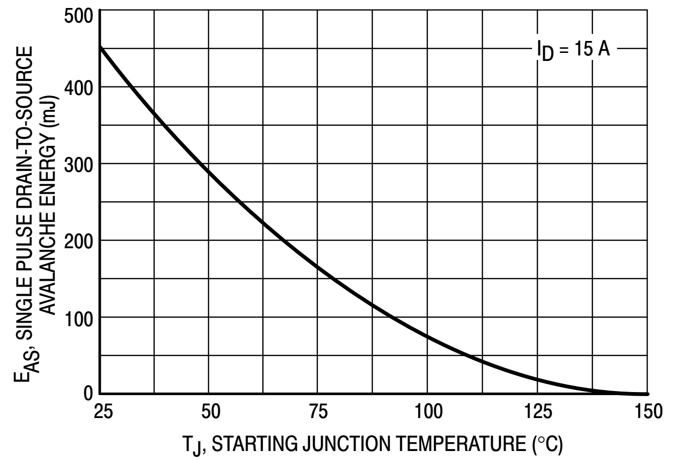



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

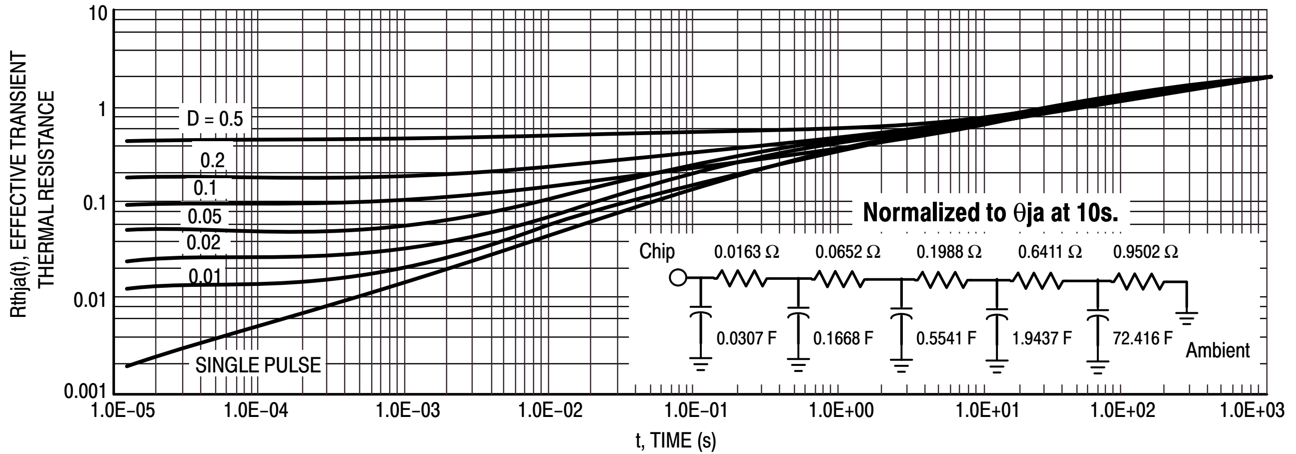



**Figure 14. Thermal Response**

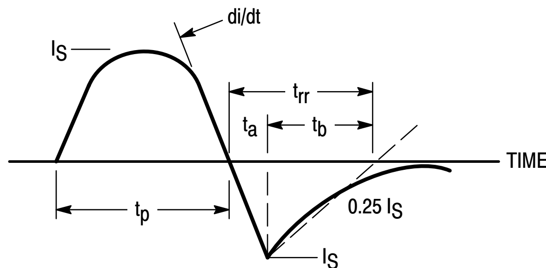
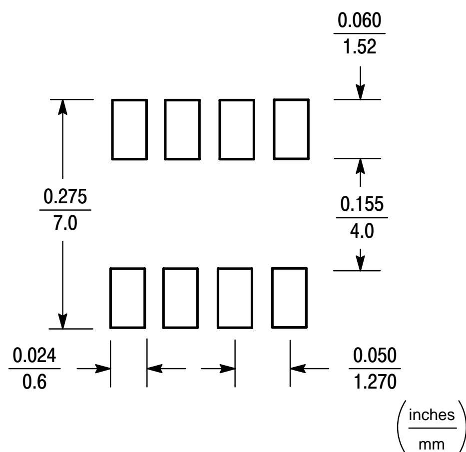



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE SO–8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## SO–8 POWER DISSIPATION

The power dissipation of the SO–8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the SO–8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 2.5 Watts.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the SO–8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

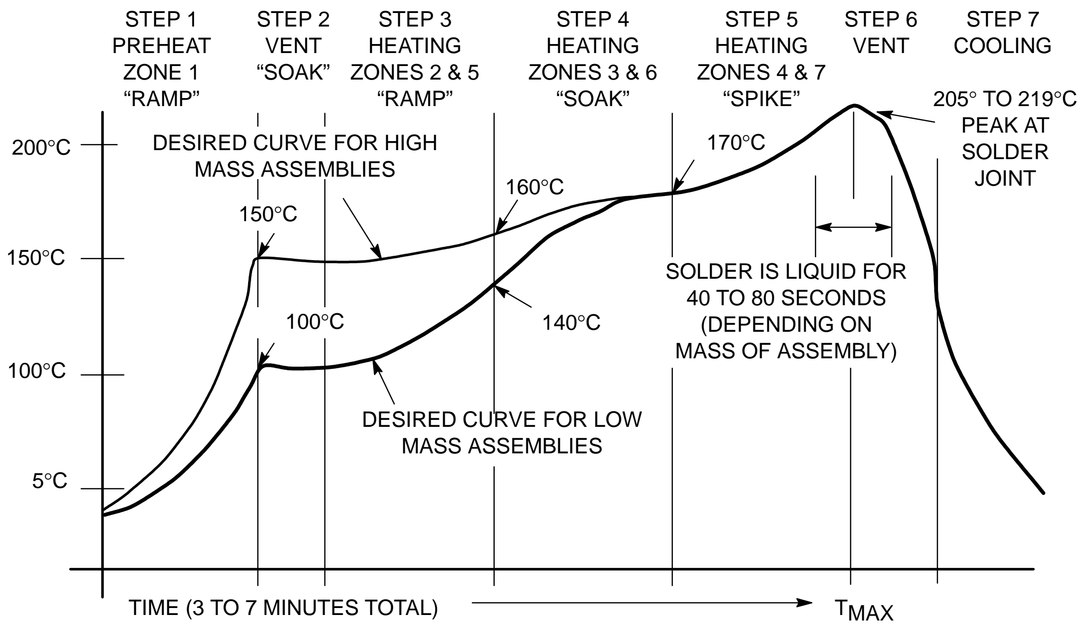



**Figure 16. Typical Solder Heating Profile**

# MPF930, MPF960, MPF990

Preferred Device

# Small Signal MOSFET 2 Amps, 35, 60, 90 Volts

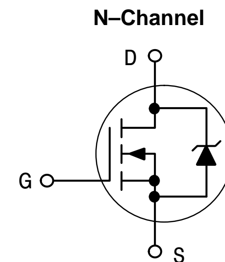
## N–Channel TO–92

ON Semiconductor

http://onsemi.com

**2 AMPERES**
**35, 60, 90 VOLTS**
**$R_{DS(on)}$ = 0.7 Ω (MPF930)**
**$R_{DS(on)}$ = 0.8 Ω (MPF960)**
**$R_{DS(on)}$ = 1.2 Ω (MPF990)**

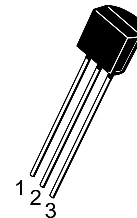
N–Channel




**MAXIMUM RATINGS**

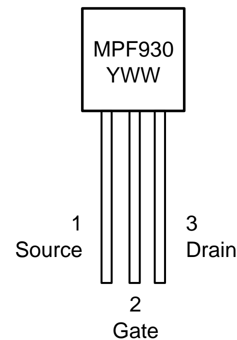
| Rating | Symbol | MPF930 | MPF960 | MPF990 | Unit |
|---|---|---|---|---|---|
| Drain–Source Voltage | $V_{DS}$ | 35 | 60 | 90 | Vdc |
| Drain–Gate Voltage | $V_{DG}$ | 35 | 60 | 90 | Vdc |
| Gate–Source Voltage – Continuous – Non–repetitive ($t_p \le 50$ μs) | $V_{GS}$ $V_{GSM}$ | | ±20 ±40 | | Vdc Vpk |
| Drain Current Continuous (Note 1.) Pulsed (Note 2.) | $I_D$ $I_{DM}$ | | 2.0 3.0 | | Adc |
| Total Device Dissipation @ $T_A$ = 25°C Derate above 25°C | $P_D$ | | 1.0 8.0 | | Watts mW/°C |
| Operating and Storage Junction Temperature Range | $T_J$, $T_{stg}$ | | –55 to 150 | | °C |
| Thermal Resistance | $\theta_{JA}$ | | 125 | | °C/W |

1. The Power Dissipation of the package may result in a lower continuous drain current.
2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.




**TO–92**
**CASE 29**
**Style 22**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 763 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 3

Publication Order Number:
MPF930/D

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 10 µAdc) | MPF930 | $V_{(BR)DSX}$ | 35 | – | – | Vdc |
| | MPF960 | | 60 | – | – | |
| | MPF990 | | 90 | – | – | |
| Gate Reverse Current ($V_{GS}$ = 15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 50 | nAdc |
| **ON CHARACTERISTICS** (Note 3.) | | | | | | |
| Zero–Gate–Voltage Drain Current ($V_{DS}$ = Maximum Rating, $V_{GS}$ = 0) | | $I_{DSS}$ | – | – | 10 | µAdc |
| Gate Threshold Voltage ($I_D$ = 1.0 mAdc, $V_{DS}$ = $V_{GS}$) | | $V_{GS(Th)}$ | 1.0 | – | 3.5 | Vdc |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 0.5 Adc) | MPF930 | $V_{DS(on)}$ | – | 0.4 | 0.7 | Vdc |
| | MPF960 | | – | 0.6 | 0.8 | |
| | MPF990 | | – | 0.6 | 1.2 | |
| ($I_D$ = 1.0 Adc) | MPF930 | | – | 0.9 | 1.4 | |
| | MPF960 | | – | 1.2 | 1.7 | |
| | MPF990 | | – | 1.2 | 2.4 | |
| ($I_D$ = 2.0 Adc) | MPF930 | | – | 2.2 | 3.0 | |
| | MPF960 | | – | 2.8 | 3.5 | |
| | MPF990 | | – | 2.8 | 4.8 | |
| Static Drain–Source On Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1.0 Adc) | MPF930 | $r_{DS(on)}$ | – | 0.9 | 1.4 | Ω |
| | MPF960 | | – | 1.2 | 1.7 | |
| | MPF990 | | – | 1.2 | 2.0 | |
| On–State Drain Current ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 10 Vdc) | | $I_{D(on)}$ | 1.0 | 2.0 | – | Amps |
| **SMALL–SIGNAL CHARACTERISTICS** | | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{iss}$ | – | 70 | – | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{rss}$ | – | 20 | – | pF |
| Output Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | | $C_{oss}$ | – | 49 | – | pF |
| Forward Transconductance ($V_{DS}$ = 25 Vdc, $I_D$ = 0.5 Adc) | | $g_{fs}$ | 200 | 380 | – | mmhos |
| **SWITCHING CHARACTERISTICS** | | | | | | |
| Turn–On Time | | $t_{on}$ | – | 7.0 | 15 | ns |
| Turn–Off Time | | $t_{off}$ | – | 7.0 | 15 | ns |

3. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2.0%.

## RESISTIVE SWITCHING

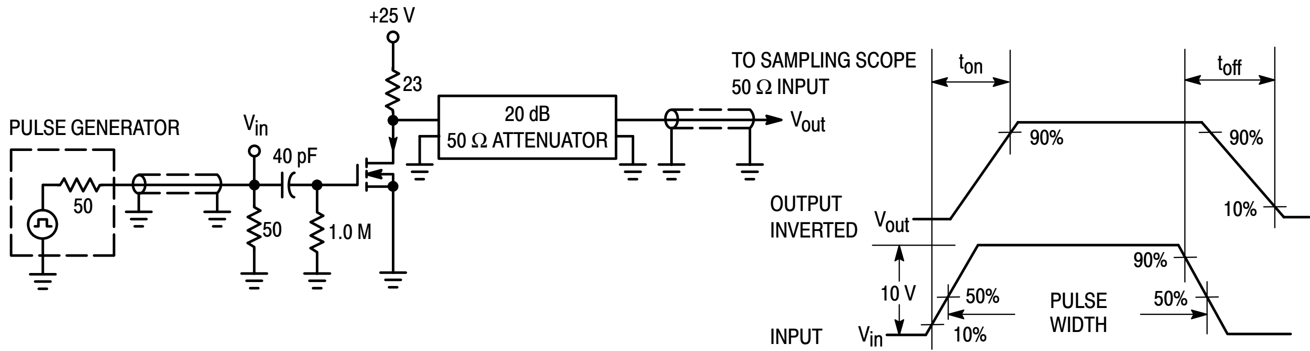



**Figure 1. Switching Test Circuit**

**Figure 2. Switching Waveforms**

## ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| MPF930 | TO–92 | 1000 Unit/Box |
| MPF930RLRE | TO–92 | 2000 Tape & Reel |
| MPF930A | TO–92 | 1000 Unit/Box |
| MPF930ARLRE | TO–92 | 2000 Tape & Reel |
| MPF960 | TO–92 | 1000 Unit/Box |
| MPF960RLRA | TO–92 | 2000 Tape & Reel |
| MPF990 | TO–92 | 1000 Unit/Box |
| MPF990RLRA | TO–92 | 2000 Tape & Reel |
| MPF990RLRP | TO–92 | 2000 Ammo Pack |

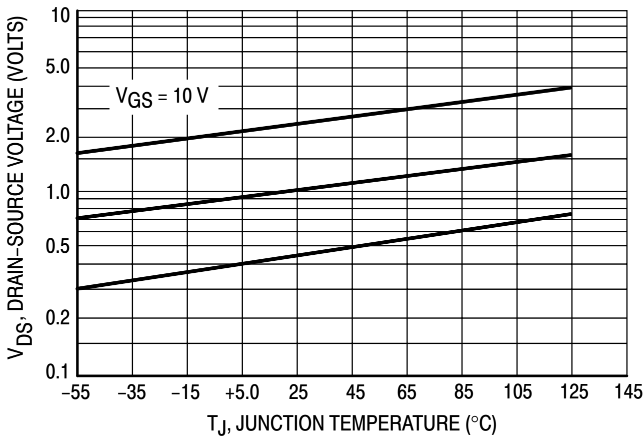



**Figure 3. On Voltage versus Temperature**

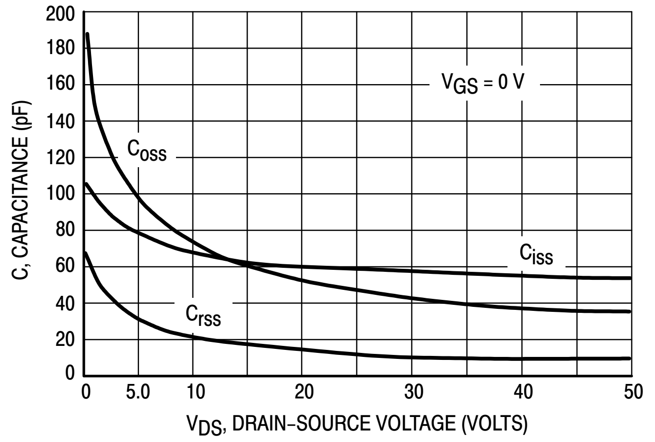



**Figure 4. Capacitance Variation**

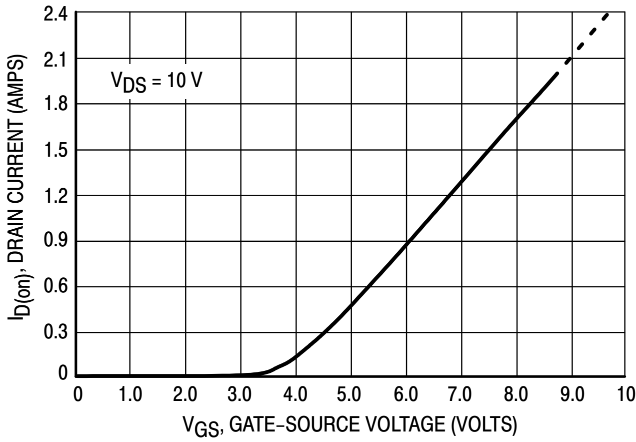



**Figure 5. Transfer Characteristic**

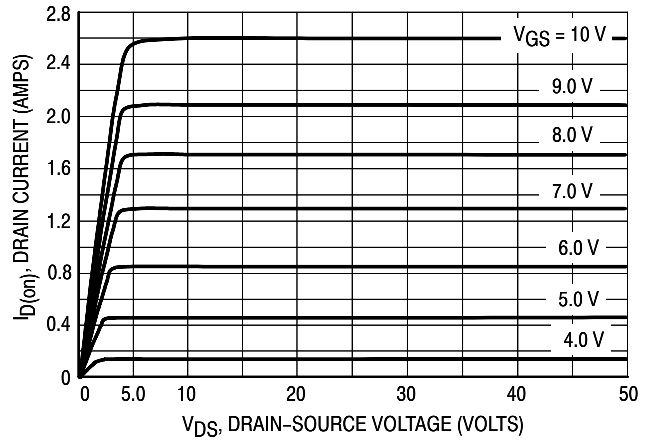



**Figure 6. Output Characteristic**

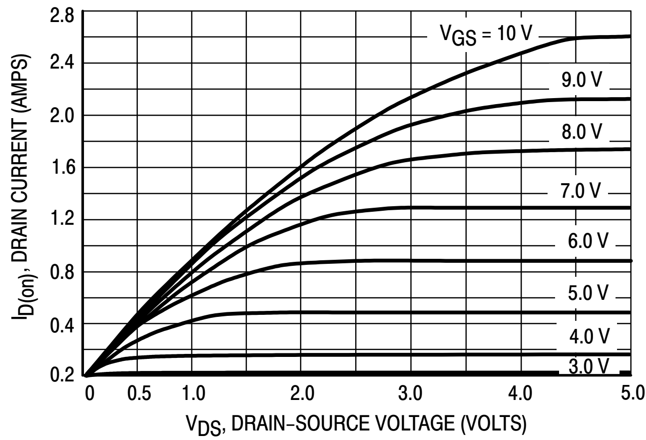



**Figure 7. Saturation Characteristic**

# MTB1306

**Preferred Device**

# Power MOSFET 75 Amps, 30 Volts, Logic Level

## N–Channel D2PAK

**ON Semiconductor™**

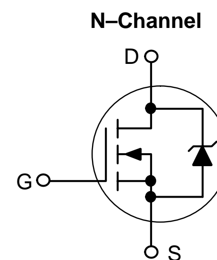
**http://onsemi.com**

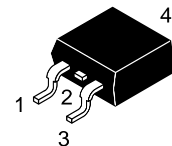
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**75 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 6.5 mΩ**

**N–Channel**



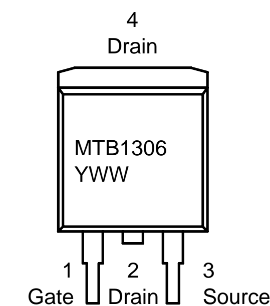

**D2PAK**
**CASE 418B**
**STYLE 2**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage – Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±20 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>59<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 150<br>1.2<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 75 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 280 | mJ |
| Thermal Resistance – Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 0.8<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5.0 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB1306 = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB1306 | D2PAK | 50 Units/Rail |
| MTB1306T4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 38 Adc) | | $R_{DS(on)}$ | – | 5.8 | 6.5 | mΩ |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 38 Adc) | | | – | 7.4 | 8.5 | |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 75 Adc) | | $V_{DS(on)}$ | – | 0.44 | 0.5 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 38 Adc, $T_J$ = 150°C) | | | – | – | 0.38 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 15 | 55 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2560 | 3584 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1305 | 1827 | |
| Transfer Capacitance | | $C_{rss}$ | – | 386 | 772 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | – | 17 | 35 | ns |
| Rise Time | | $t_r$ | – | 170 | 340 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 68 | 136 | |
| Fall Time | | $t_f$ | – | 145 | 290 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 50 | 70 | nC |
| | | $Q_1$ | – | 8.3 | – | |
| | | $Q_2$ | – | 25.3 | – | |
| | | $Q_3$ | – | 17.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.75 | 1.1 | Vdc |
| | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.64 | – | |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 84 | – | ns |
| | | $t_a$ | – | 35 | – | |
| | | $t_b$ | – | 53 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.13 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

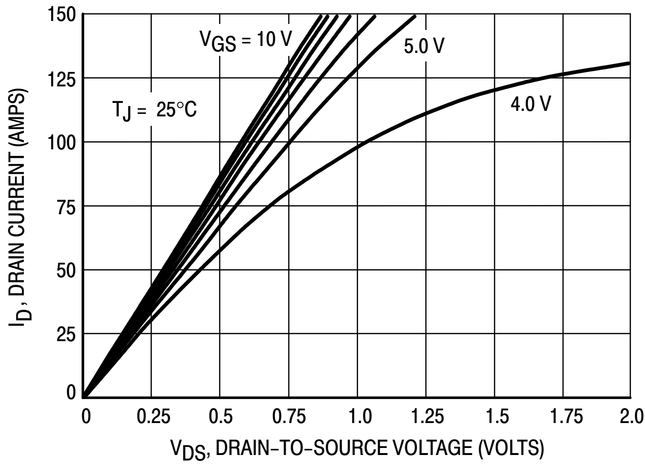


**Figure 1. On−Region Characteristics**

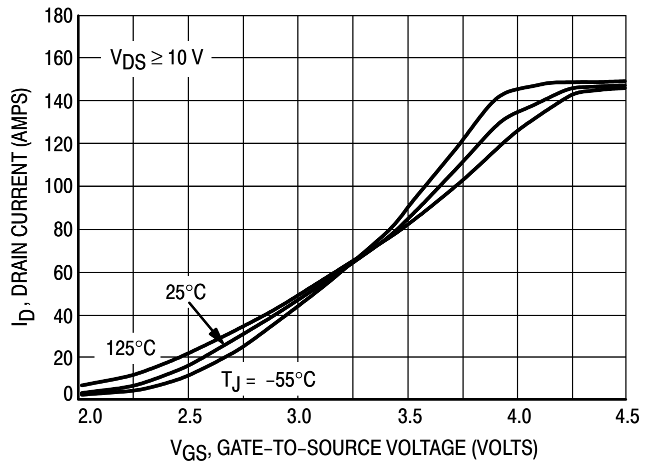


**Figure 2. Transfer Characteristics**

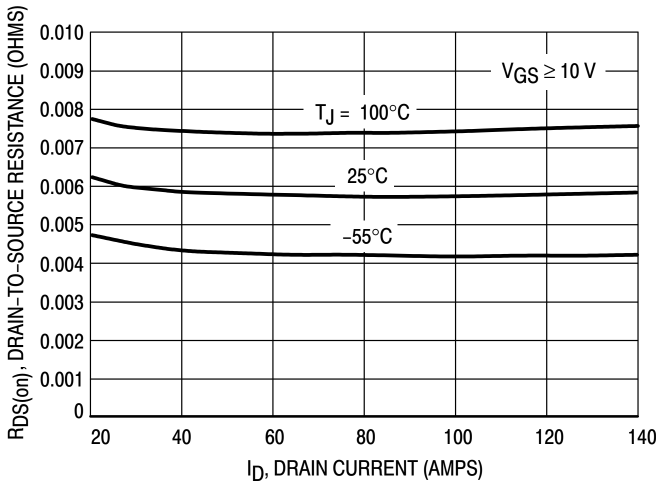


**Figure 3. On−Resistance versus Drain Current and Temperature**

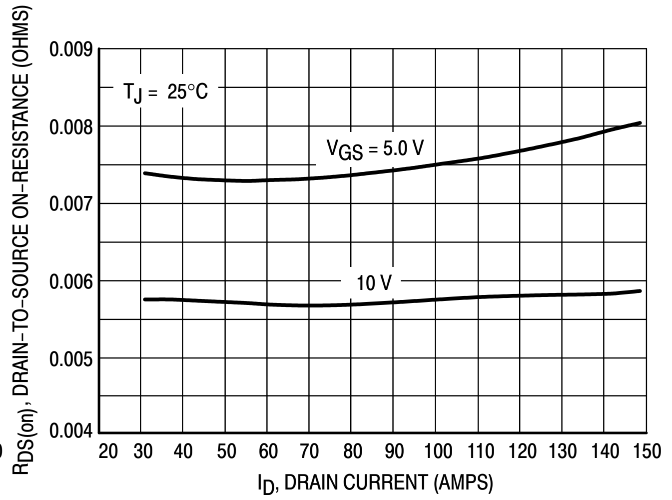


**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

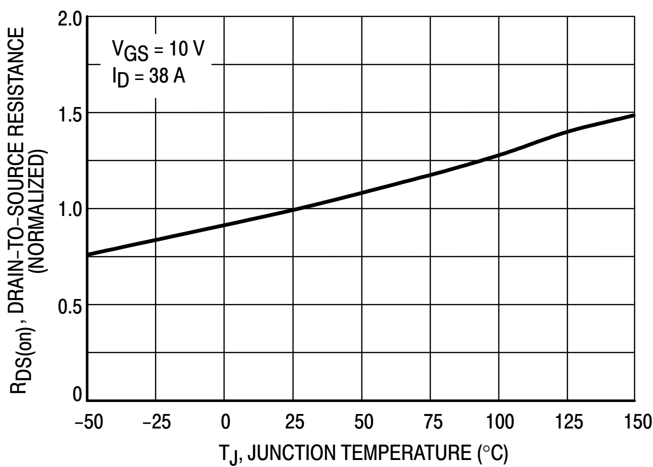


**Figure 5. On−Resistance Variation with Temperature**

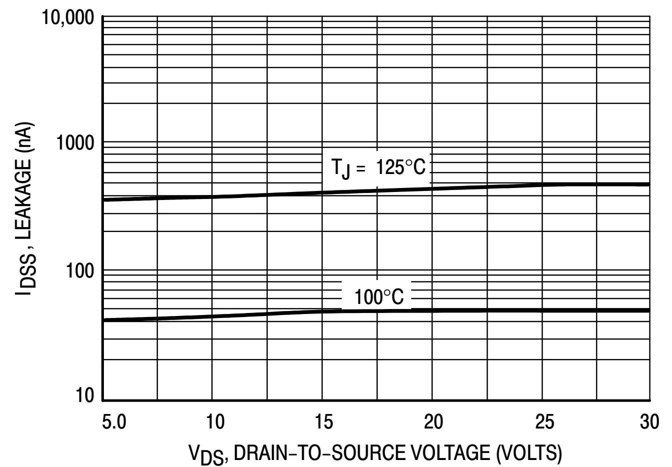


**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

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$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

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$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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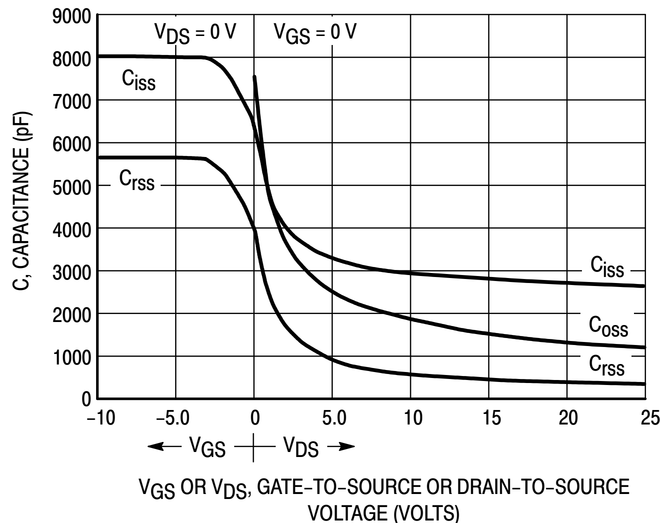



**Figure 7. Capacitance Variation**

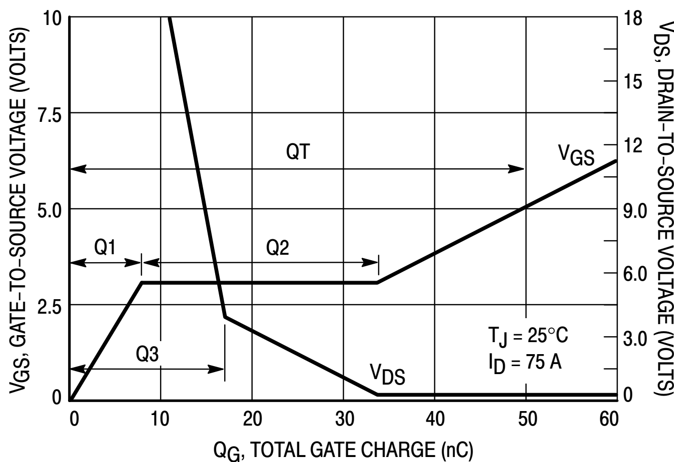



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

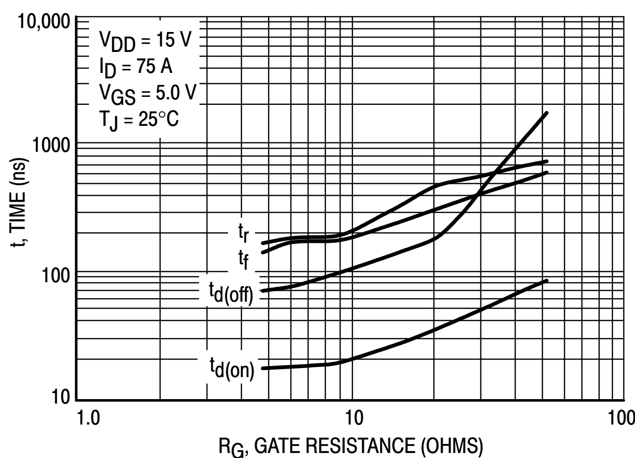



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

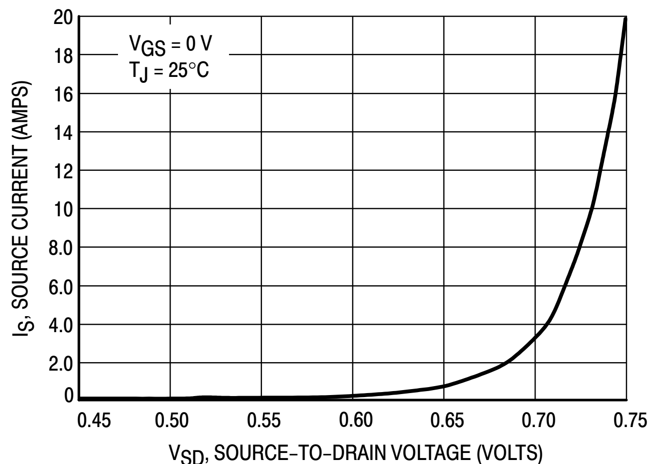



**Figure 10. Diode Forward Voltage versus Current**

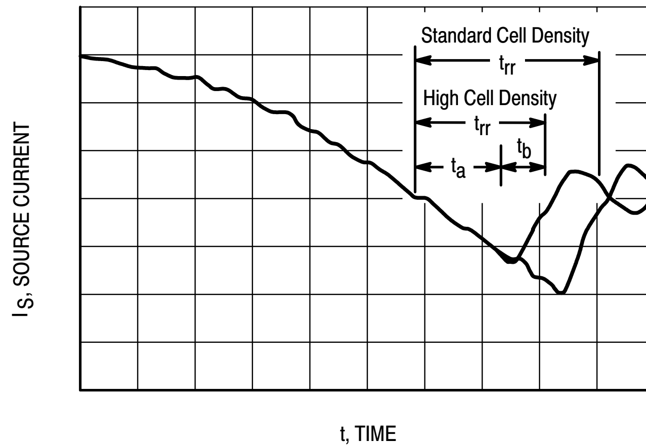



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

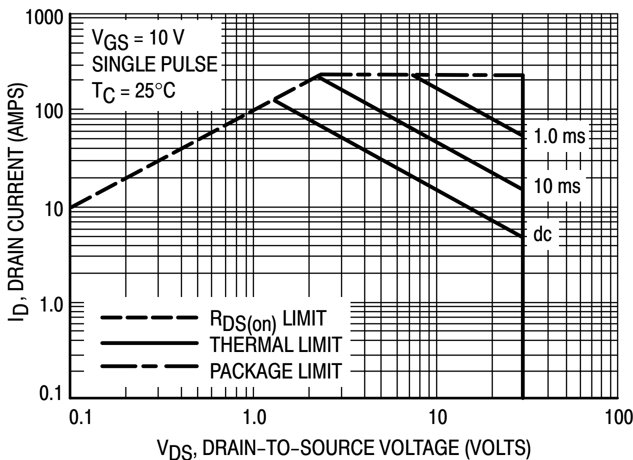



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

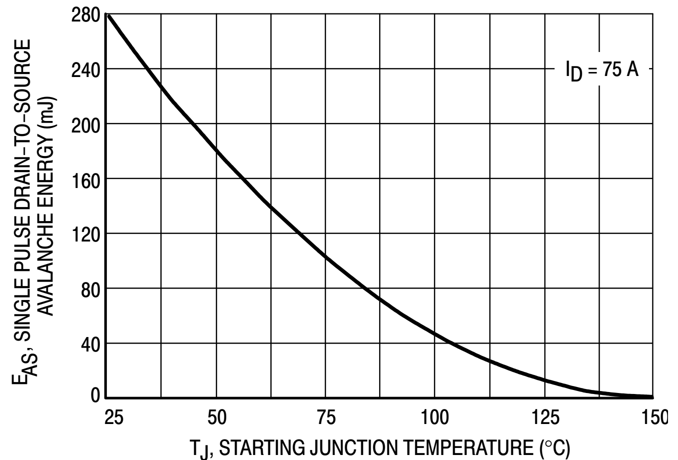



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

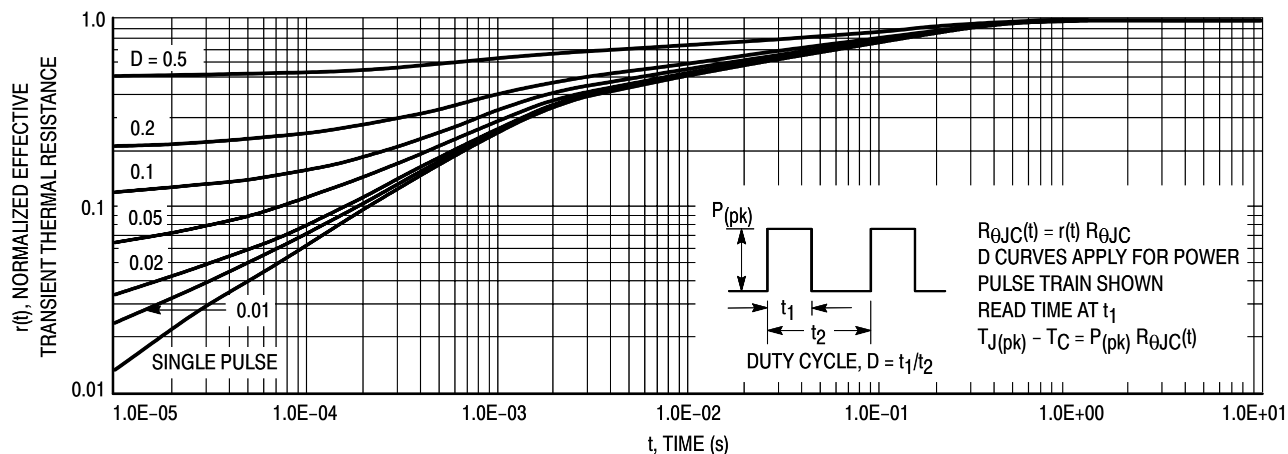



**Figure 14. Thermal Response**

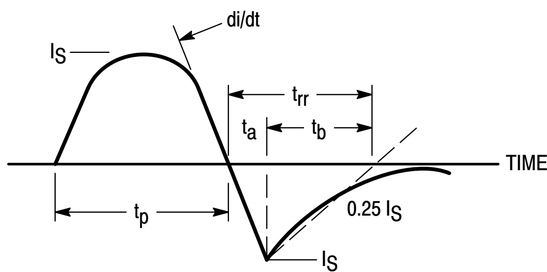



**Figure 15. Diode Reverse Recovery Waveform**

# MTB20N20E

**Preferred Device**

# Power MOSFET 20 Amps, 200 Volts

## N–Channel $D^2$PAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

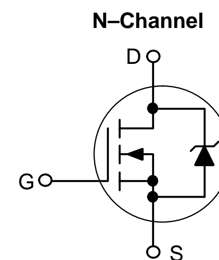
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>12<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted with the minimum recommended pad size | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 20 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 600 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

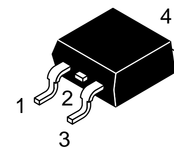
**ON Semiconductor™**

**http://onsemi.com**

**20 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 160 mΩ**

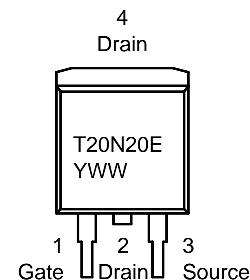
**N–Channel**




**$D^2$PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T20N20E = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB20N20E | $D^2$PAK | 50 Units/Rail |
| MTB20N20ET4 | $D^2$PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc) | | $V_{(BR)DSS}$ | 200 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 263 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | µAdc |
| ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc) | | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 7.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 0.12 | 0.16 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 20 Adc) | | $V_{DS(on)}$ | – | – | 3.84 | Vdc |
| ($I_D$ = 10 Adc, $T_J$ = 125°C) | | | – | – | 3.36 | |
| Forward Transconductance ($V_{DS}$ = 13 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 8.0 | 11 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1880 | 2700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 378 | 535 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 68 | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 17 | 40 | ns |
| Rise Time | | $t_r$ | – | 86 | 180 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | 100 | |
| Fall Time | | $t_f$ | – | 60 | 120 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 54 | 75 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 24 | – | |
| | | $Q_3$ | – | 22 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.0 | 1.35 | Vdc |
| | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.82 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 239 | – | ns |
| | | $t_a$ | – | 136 | – | |
| | | $t_b$ | – | 103 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 2.09 | – | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

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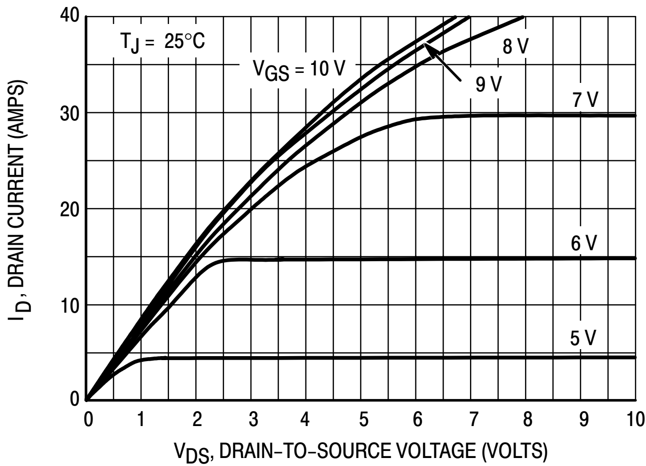


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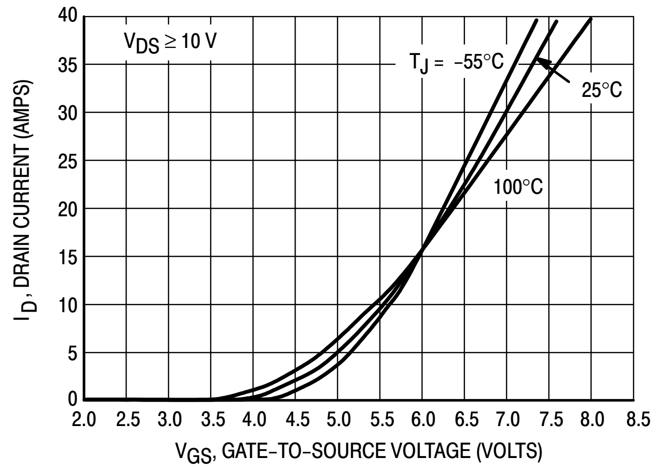


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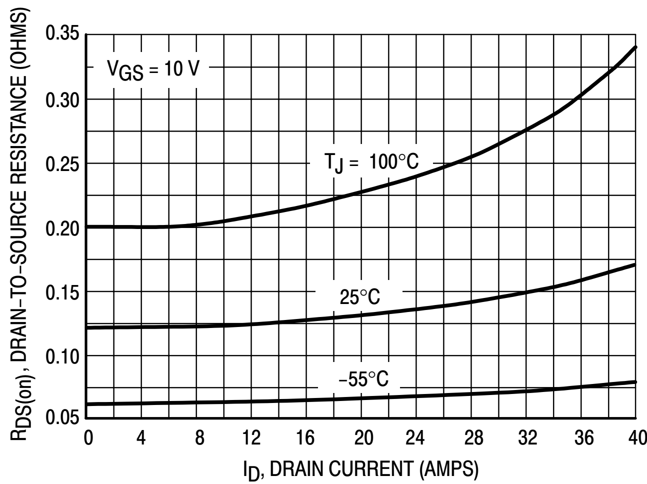


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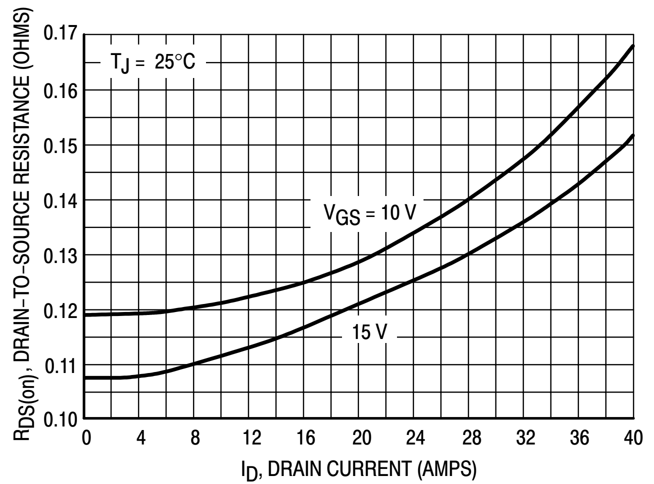


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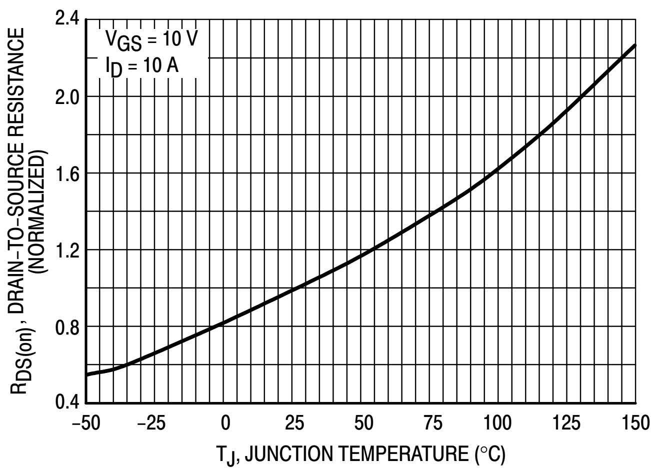


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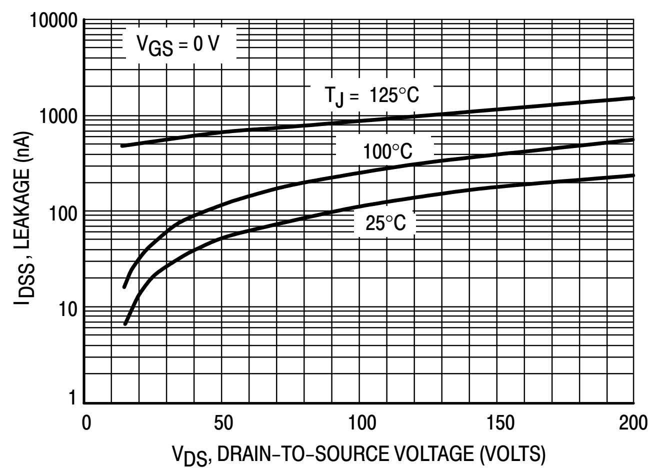


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During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
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At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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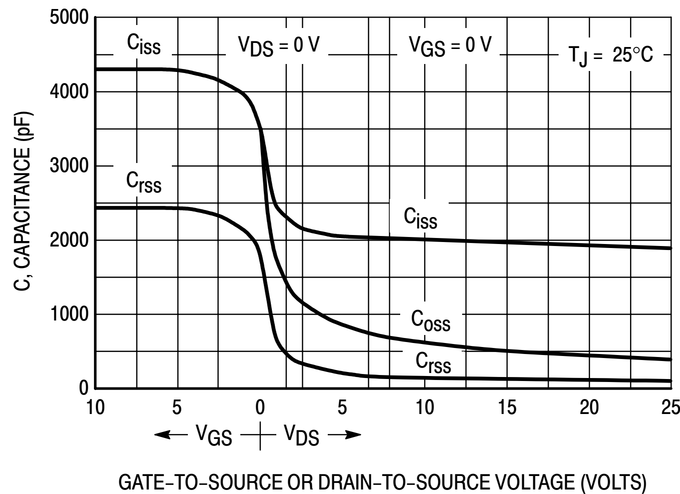


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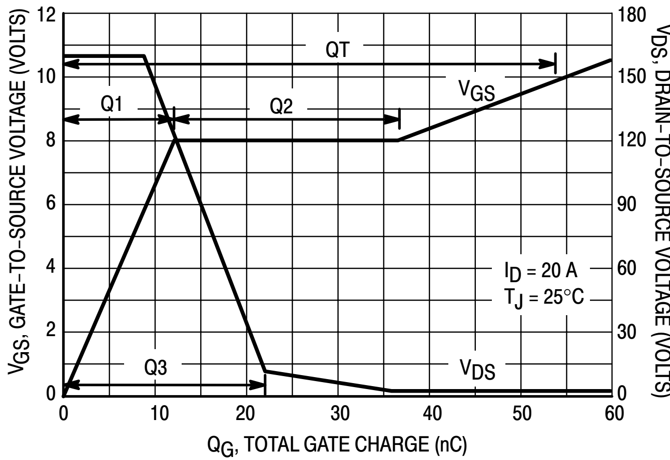



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

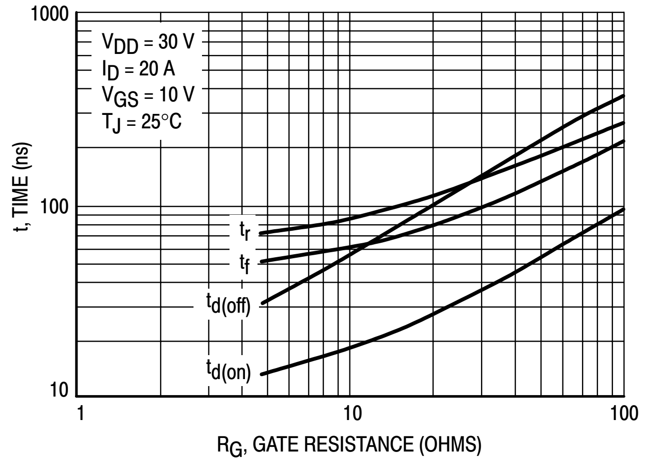



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

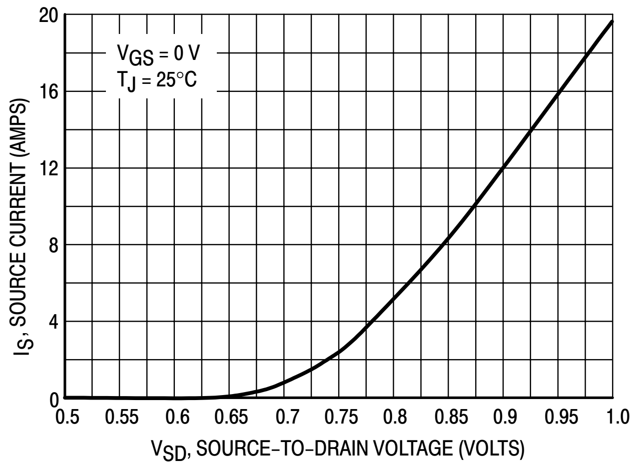



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

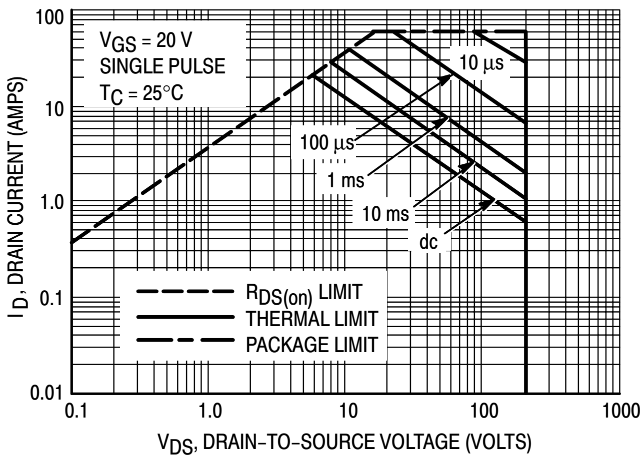



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

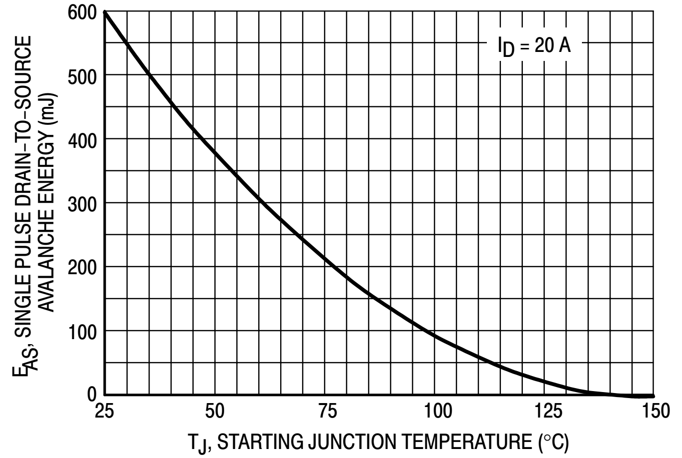



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

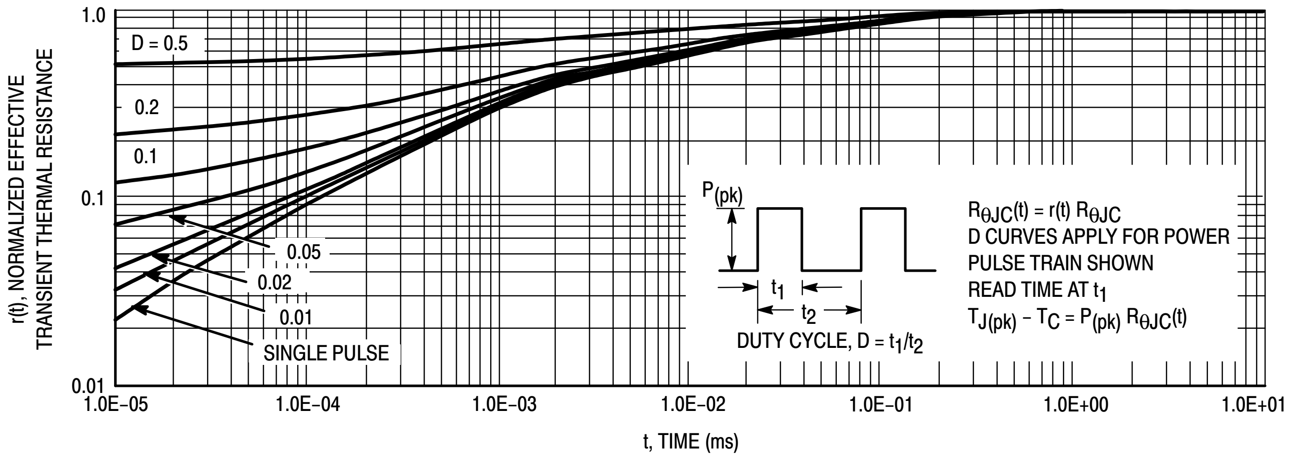



**Figure 13. Thermal Response**

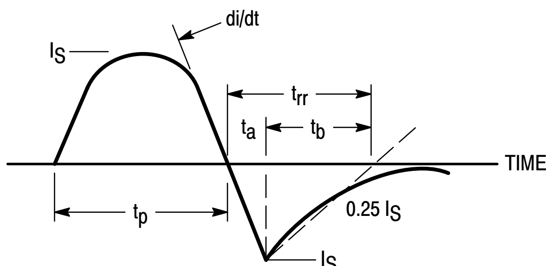



**Figure 14. Diode Reverse Recovery Waveform**

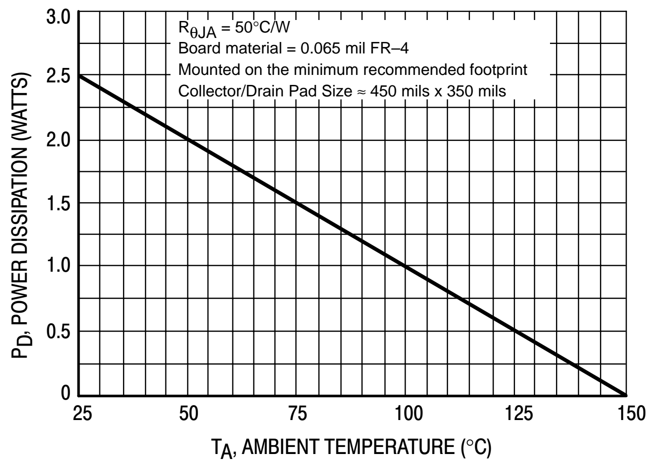
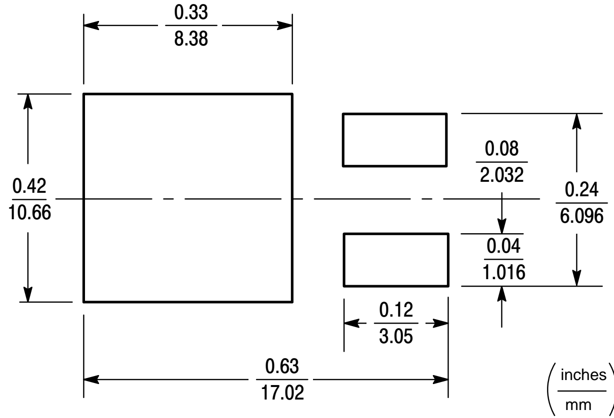



**Figure 15. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

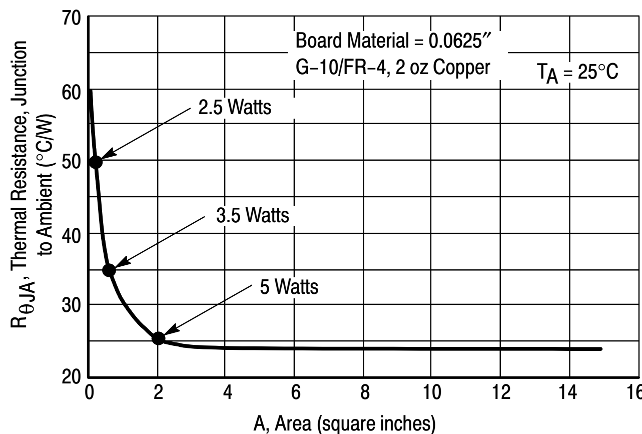



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

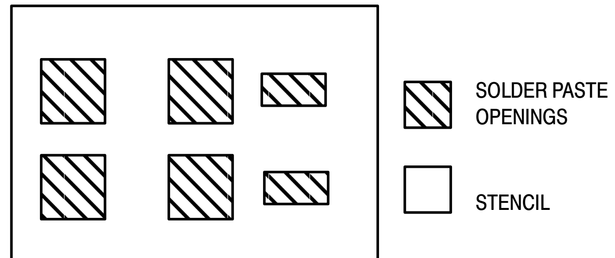



**Figure 17. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joint.

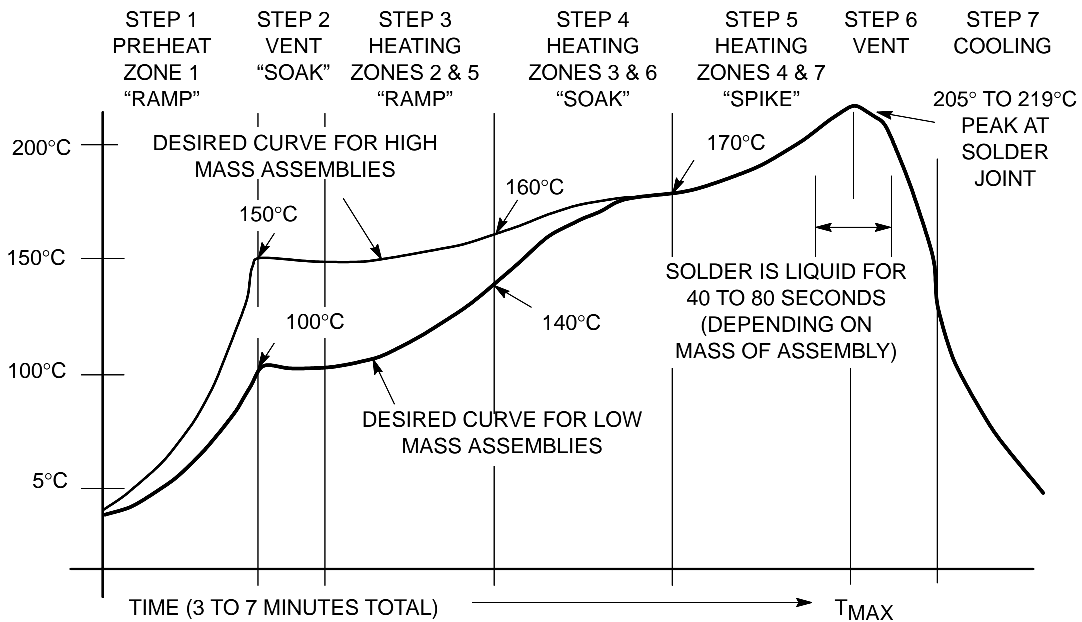



**Figure 18. Typical Solder Heating Profile**

# MTB23P06V

**Preferred Device**

# Power MOSFET 23 Amps, 60 Volts

## P–Channel $D^2PAK$

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 23<br>15<br>81 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 90<br>0.60<br>3.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 23 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 794 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

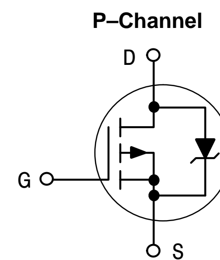
1. When surface mounted to an FR4 board using the minimum recommended pad size.

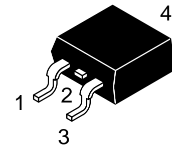
**ON Semiconductor™**

**http://onsemi.com**

**23 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

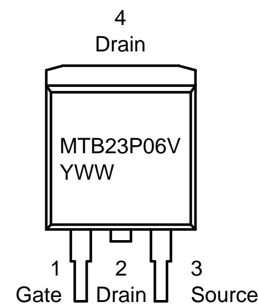
**P–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB23P06V = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB23P06V | $D^2PAK$ | 50 Units/Rail |
| MTB23P06VT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>60.5 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>5.3 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 11.5 Adc) | | $R_{DS(on)}$ | – | 0.093 | 0.12 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 23 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 11.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 2.1<br>– | 3.3<br>3.2 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 10.9 Vdc, $I_D$ = 11.5 Adc) | | $g_{FS}$ | 5.0 | 11.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1160 | 1620 | pF |
| Output Capacitance | | $C_{oss}$ | – | 380 | 530 | |
| Transfer Capacitance | | $C_{rss}$ | – | 105 | 210 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 23 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 13.8 | 30 | ns |
| Rise Time | | $t_r$ | – | 98.3 | 200 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 41 | 80 | |
| Fall Time | | $t_f$ | – | 62 | 120 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 23 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 38 | 50 | nC |
| | | $Q_1$ | – | 7.0 | – | |
| | | $Q_2$ | – | 18 | – | |
| | | $Q_3$ | – | 14 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 2.2<br>1.8 | 3.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 142 | – | ns |
| | | $t_a$ | – | 100 | – | |
| | | $t_b$ | – | 41 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.804 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

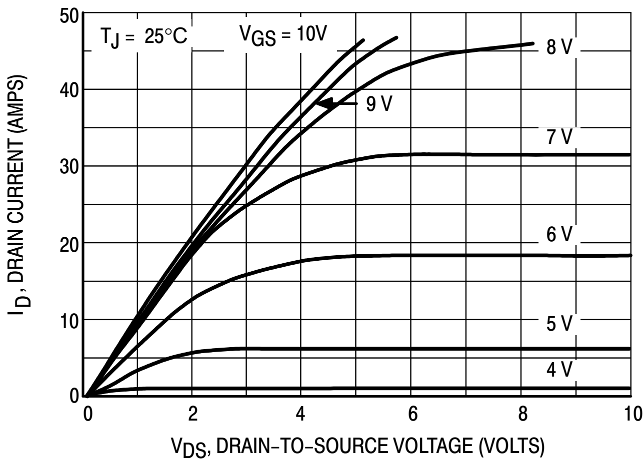



**Figure 1. On–Region Characteristics**

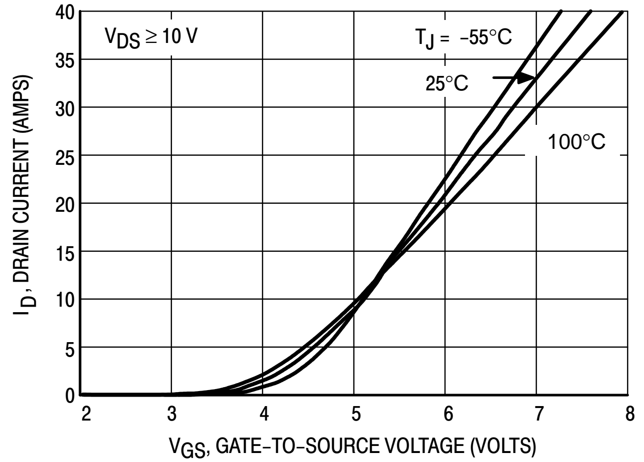



**Figure 2. Transfer Characteristics**

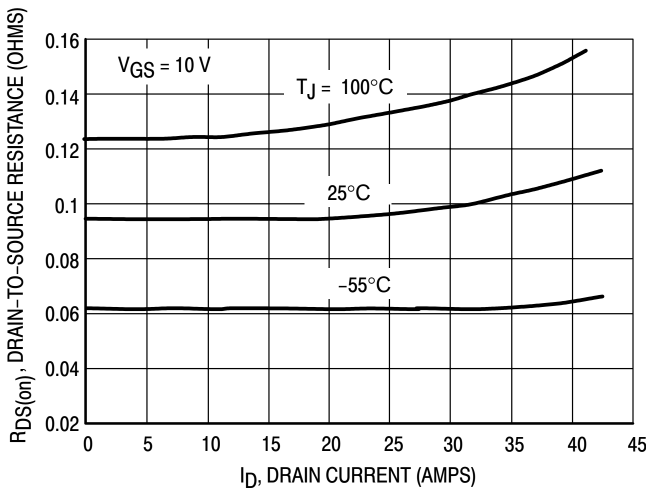



**Figure 3. On–Resistance versus Drain Current and Temperature**

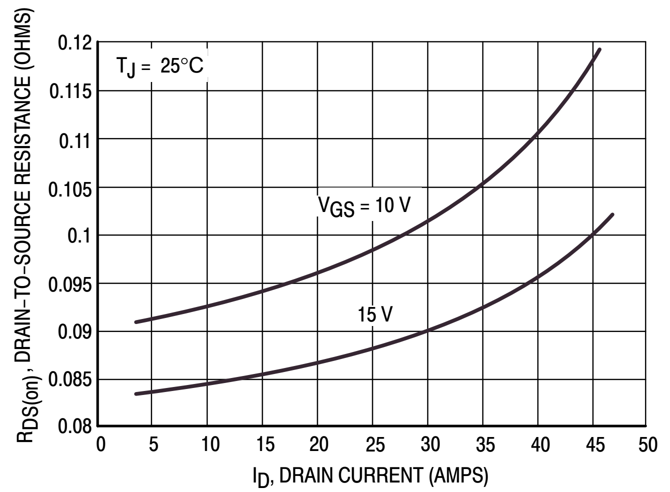



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

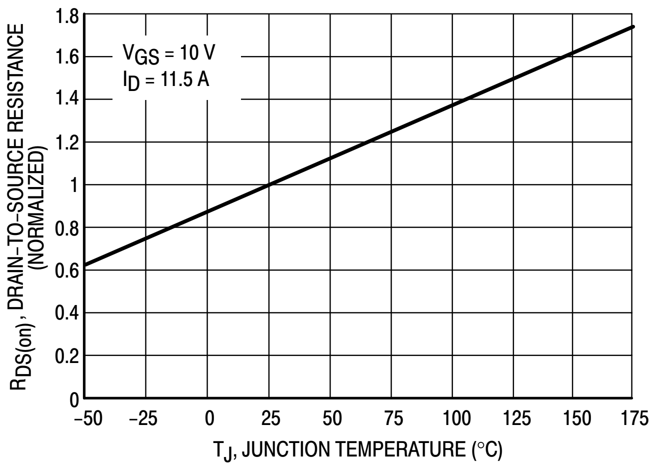



**Figure 5. On–Resistance Variation with Temperature**

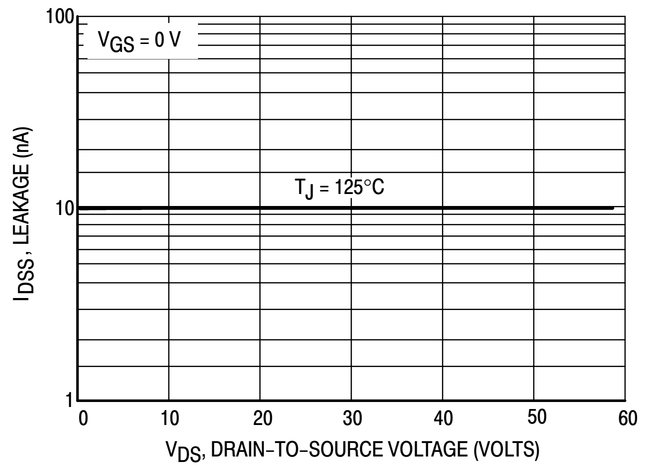



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$$t = Q/I_{G(AV)}$$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$$
$$t_f = Q_2 \times R_G/V_{GSP}$$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$$t_{d(on)} = R_G\, C_{iss}\, \mathrm{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$$
$$t_{d(off)} = R_G\, C_{iss}\, \mathrm{In}\, (V_{GG}/V_{GSP})$$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

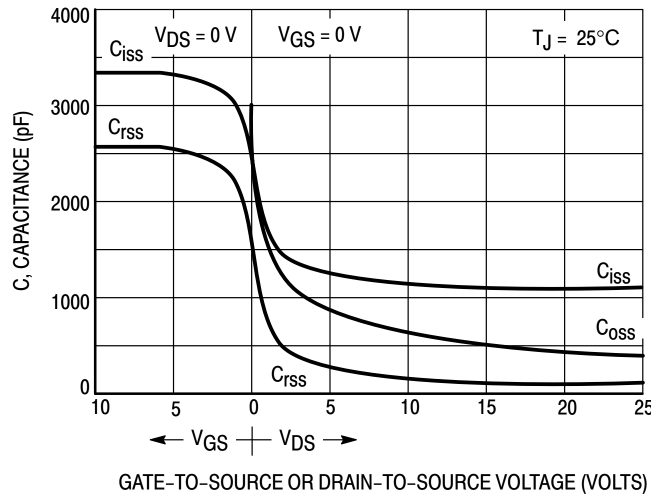



**Figure 7. Capacitance Variation**

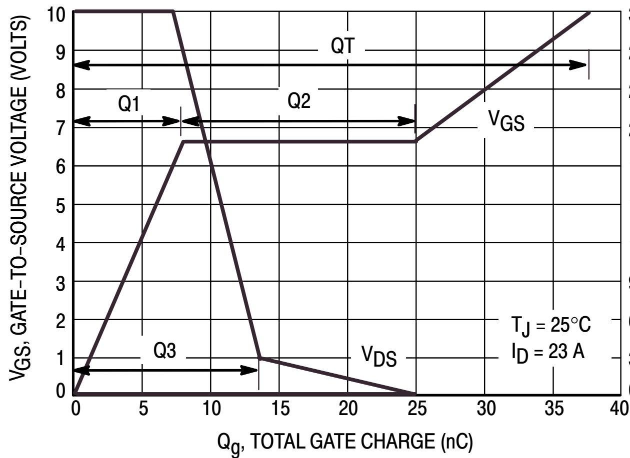



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

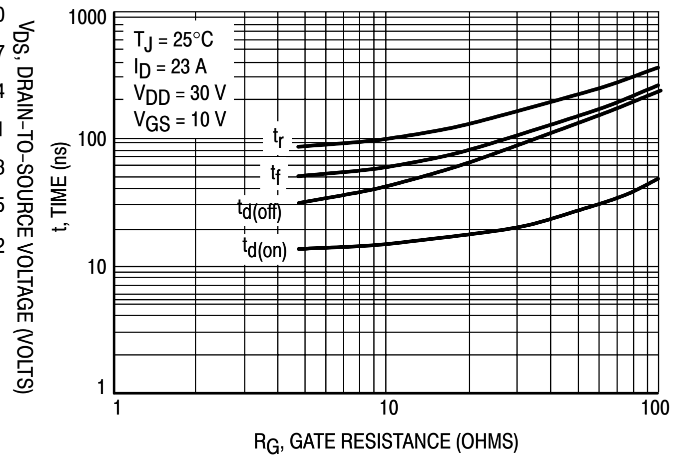



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

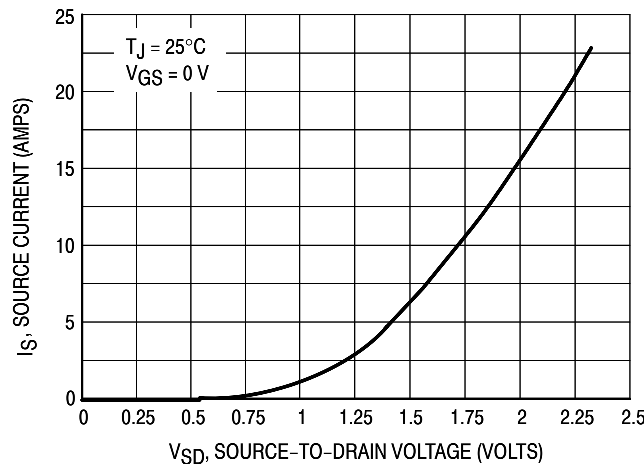



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

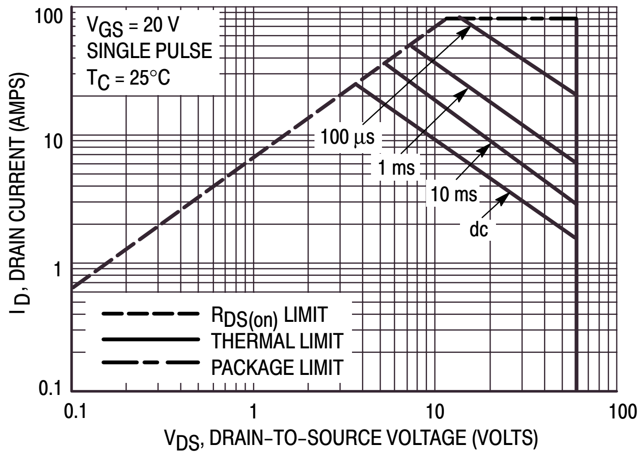



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

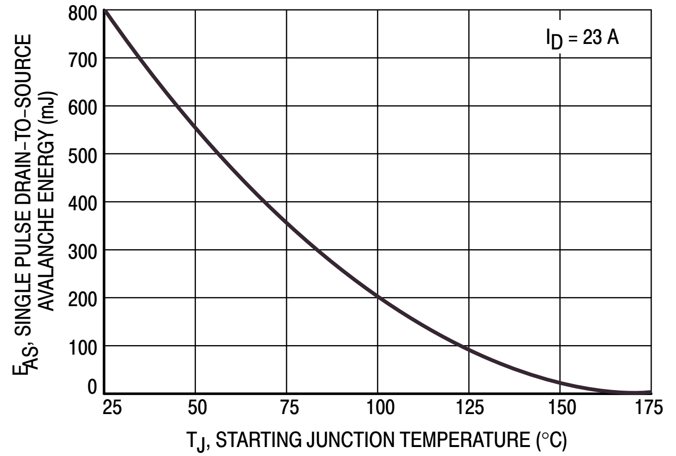



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

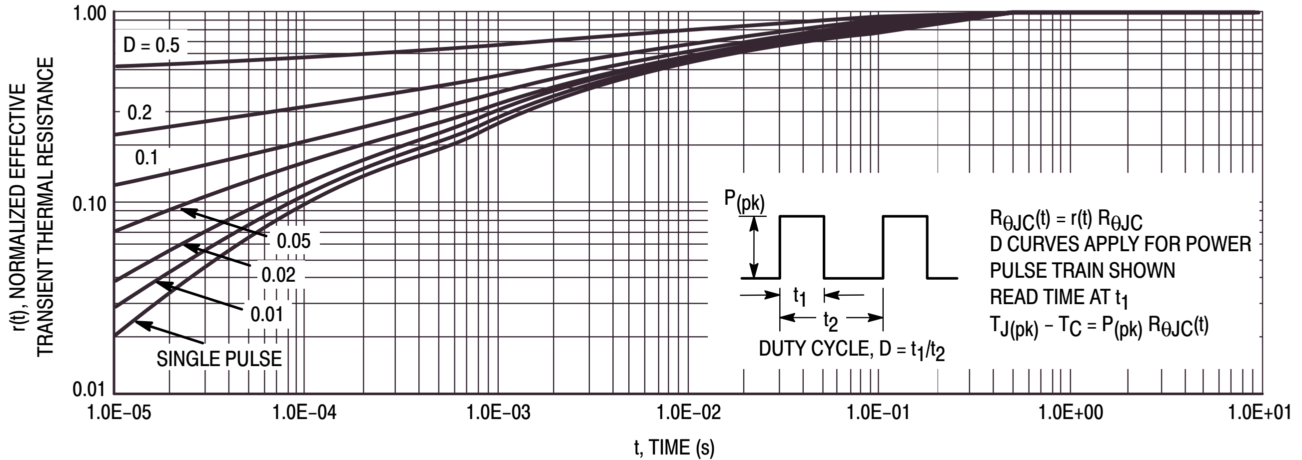



**Figure 13. Thermal Response**

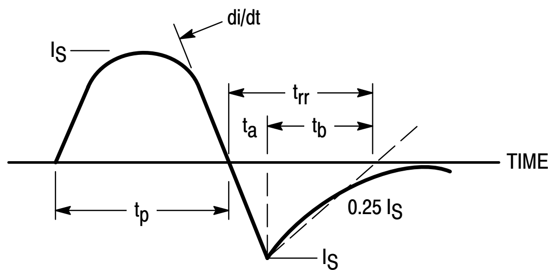



**Figure 14. Diode Reverse Recovery Waveform**

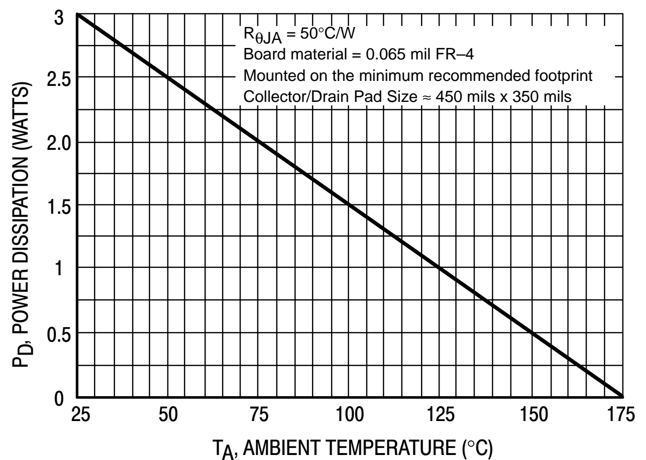
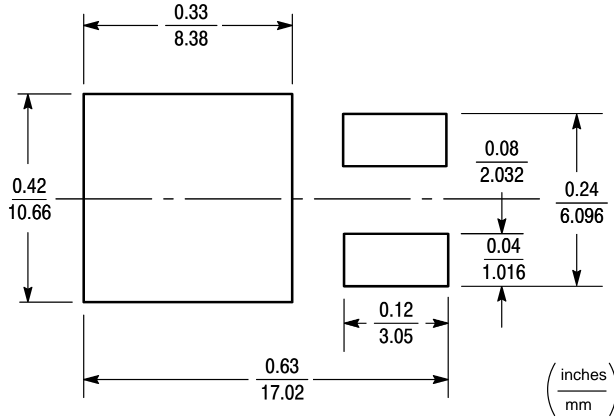



**Figure 15. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

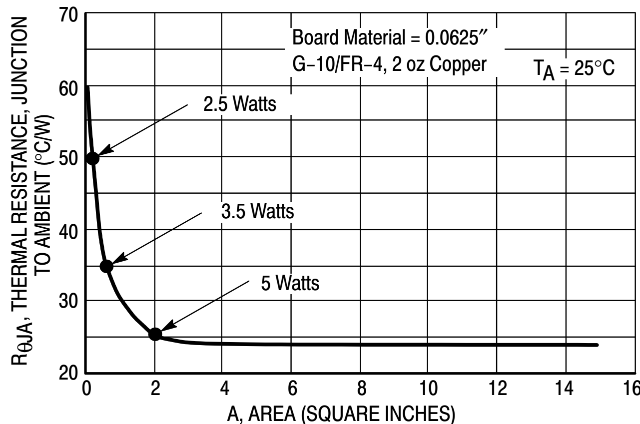



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

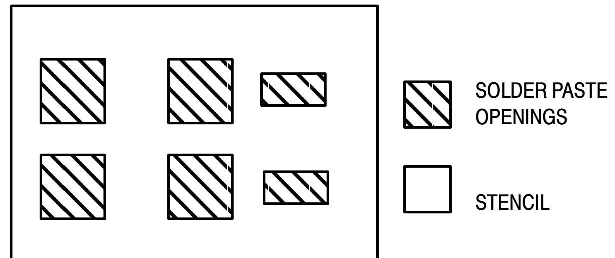



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

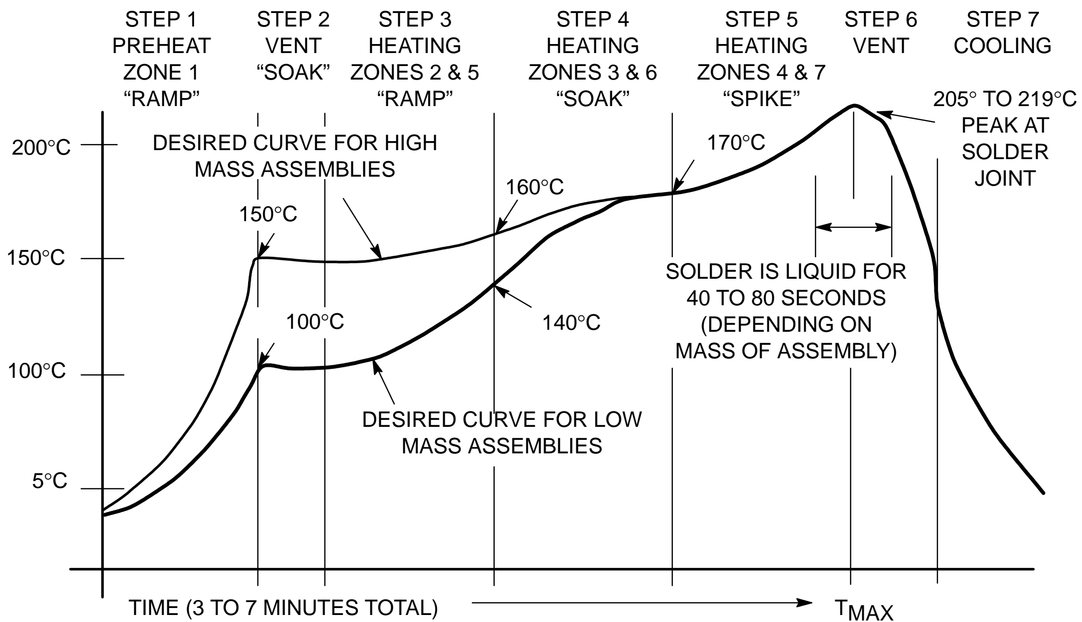



**Figure 18. Typical Solder Heating Profile**

# MTB29N15E

Preferred Device

# Power MOSFET 29 Amps, 150 Volts

## N–Channel D2PAK

**ON Semiconductor™**

http://onsemi.com

**29 AMPERES**
**150 VOLTS**
**$R_{DS(on)}$ = 70 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

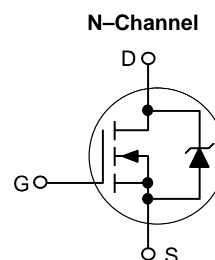
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

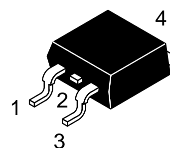
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 150 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 150 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 29<br>19<br>102 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 29 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 421 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

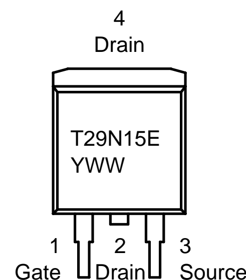
**N–Channel**




**D2PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T29N15E = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB29N15E | D2PAK | 50 Units/Rail |
| MTB29N15ET4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 150<br>– | –<br>151 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>5.4 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 14.5 Adc) | | $R_{DS(on)}$ | – | 0.054 | 0.07 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 29 Adc)<br>($I_D$ = 14.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 2.4<br>2.1 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.6 Vdc, $I_D$ = 14.5 Adc) | | $g_{FS}$ | 10 | 20 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2300 | 3220 | pF |
| Output Capacitance | | $C_{oss}$ | – | 450 | 630 | |
| Transfer Capacitance | | $C_{rss}$ | – | 130 | 260 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 75 Vdc, $I_D$ = 29 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 19 | 40 | ns |
| Rise Time | | $t_r$ | – | 95 | 190 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 90 | 180 | |
| Fall Time | | $t_f$ | – | 85 | 170 | |
| Gate Charge | ($V_{DS}$ = 120 Vdc, $I_D$ = 29 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 83 | 120 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 37 | – | |
| | | $Q_3$ | – | 23 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.92<br>0.84 | 1.3<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 174 | – | ns |
| | | $t_a$ | – | 126 | – | |
| | | $t_b$ | – | 48 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.4 | – | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | |

2. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

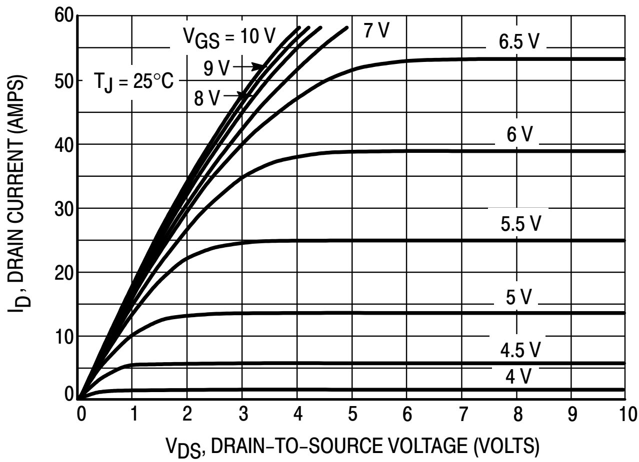



**Figure 1. On–Region Characteristics**

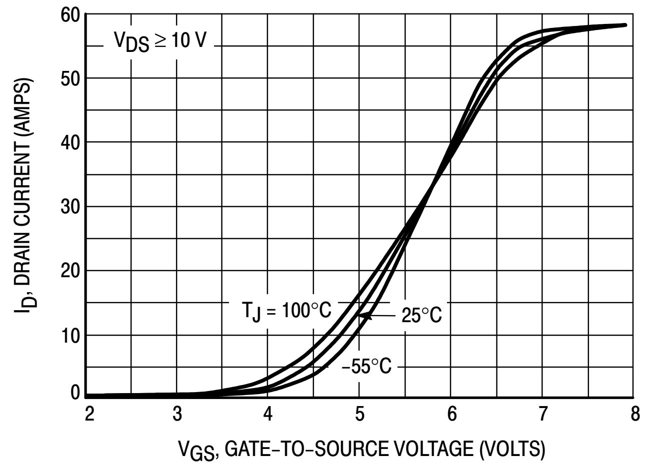



**Figure 2. Transfer Characteristics**

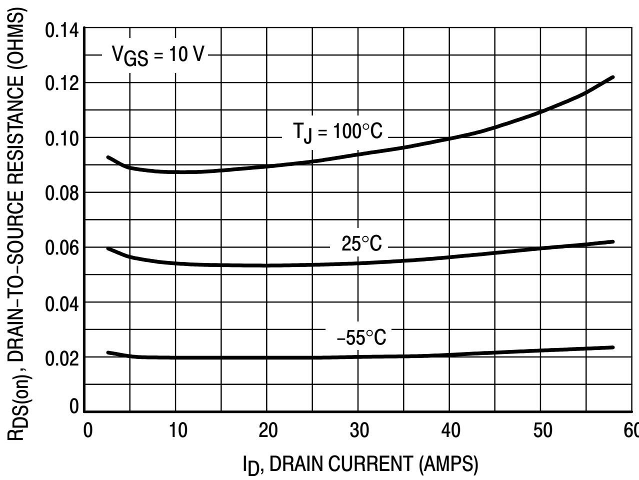



**Figure 3. On–Resistance versus Drain Current and Temperature**

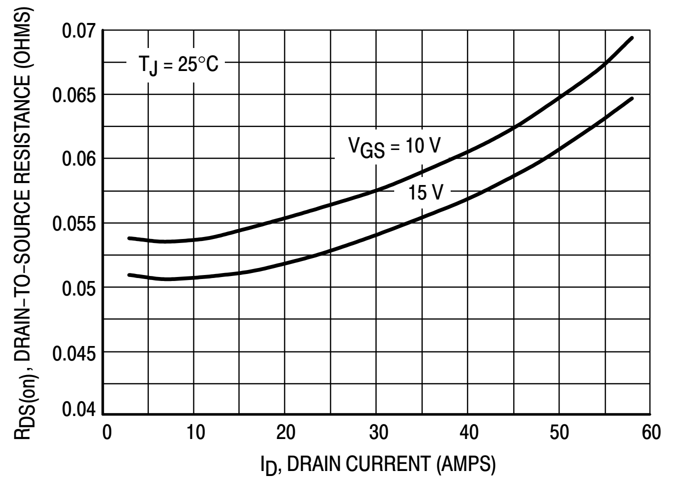



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

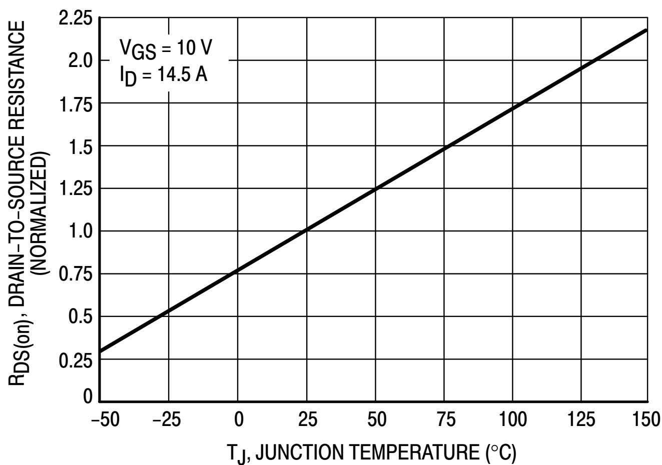



**Figure 5. On–Resistance Variation with Temperature**

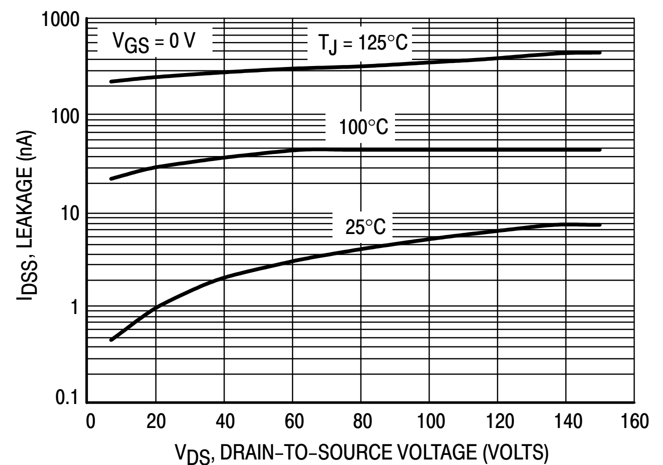



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

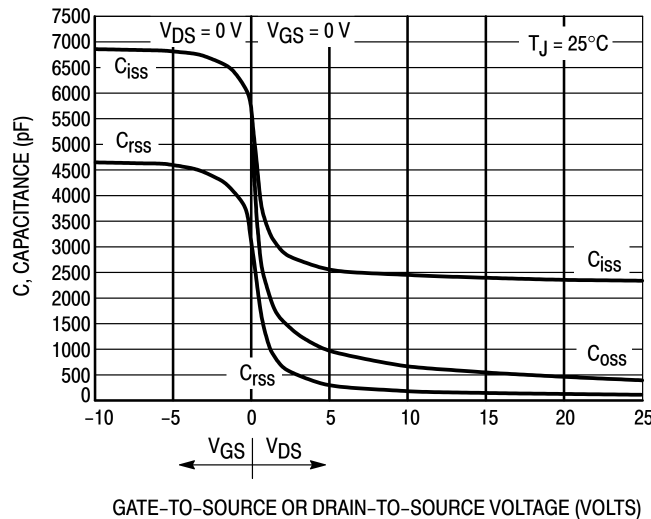



**Figure 7. Capacitance Variation**

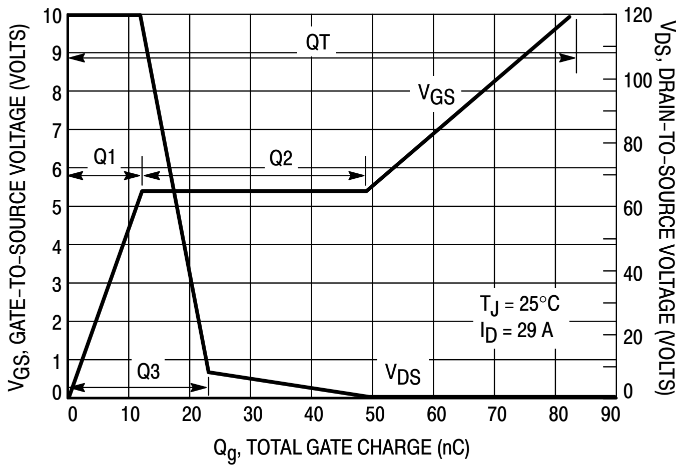



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

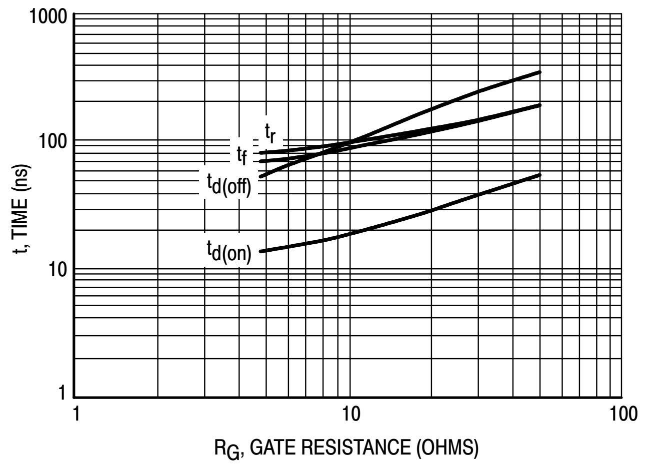



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

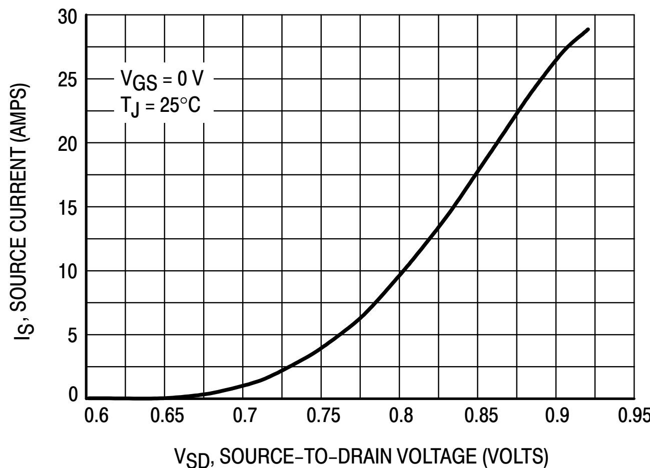



**Figure 10. Diode Forward Voltage versus Current**

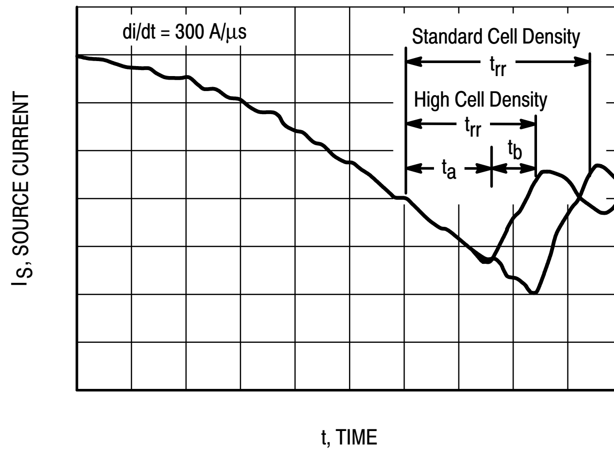



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

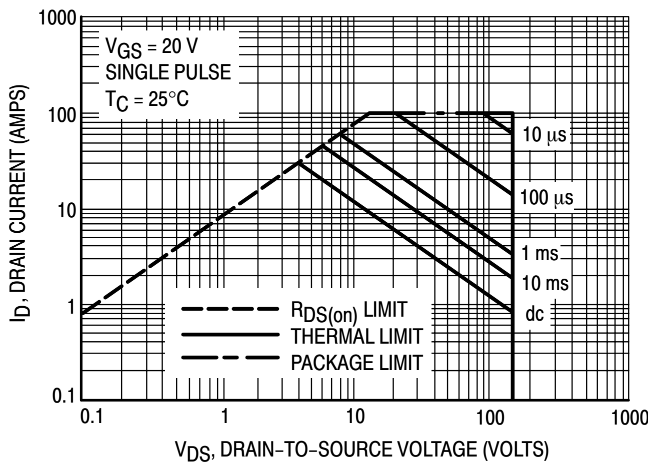



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

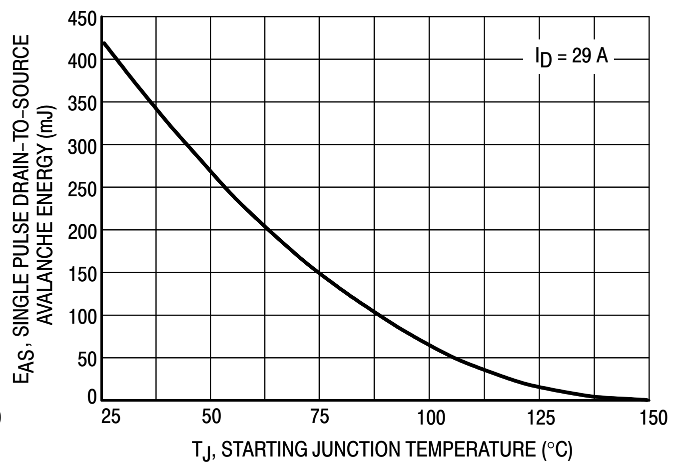



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

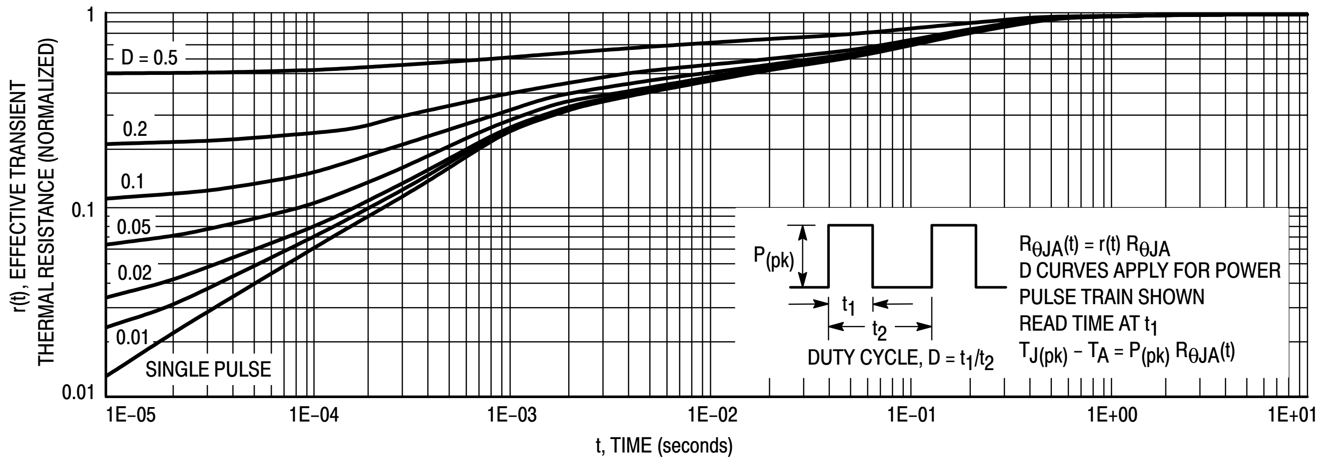



**Figure 14. Thermal Response**

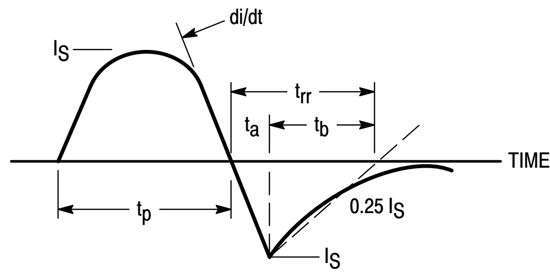



**Figure 15. Diode Reverse Recovery Waveform**

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

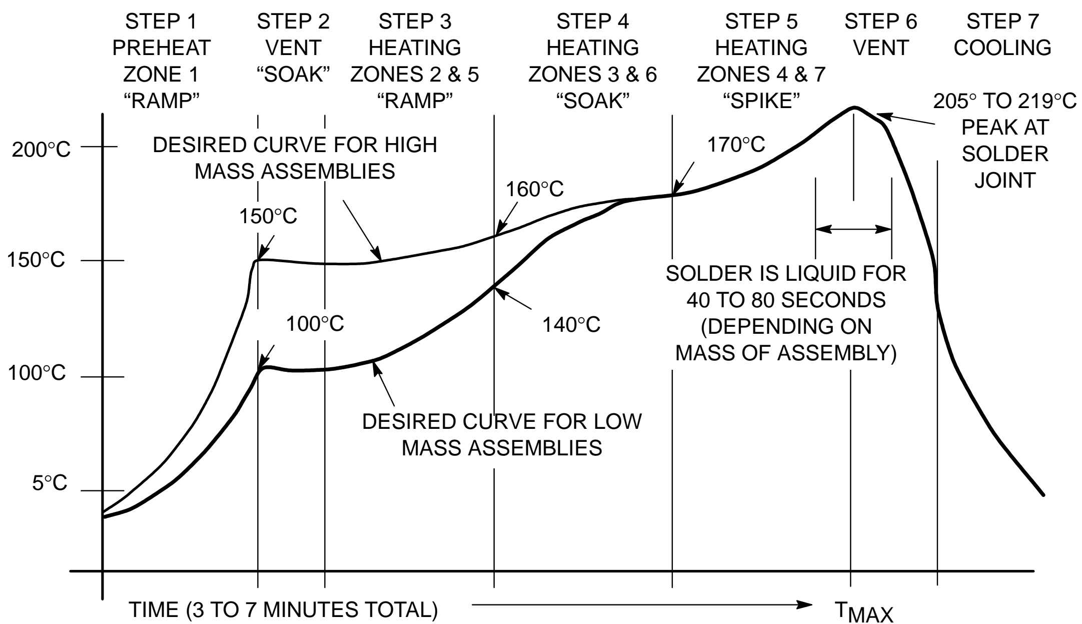



**Figure 16. Typical Solder Heating Profile**

# MTB30N06VL

**Preferred Device**

# Power MOSFET 30 Amps, 60 Volts, Logic Level

## N–Channel D2PAK

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

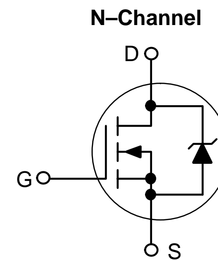
**30 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 50 mΩ**

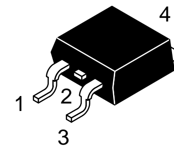
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>±20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 30<br>20<br>105 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 90<br>0.6<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 30 Apk, L = 0.342 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 154 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{θJC}$<br>$R_{θJA}$<br>$R_{θJA}$ | <br>1.67<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

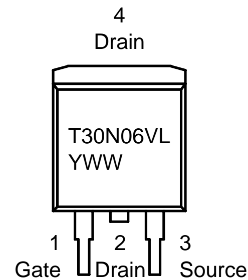
**N–Channel**




**D2PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T30N06VL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB30N06VL | D2PAK | 50 Units/Rail |
| MTB30N06VLT4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>63 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.5<br>4.0 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5 Vdc, $I_D$ = 15 Adc) | | $R_{DS(on)}$ | – | 0.033 | 0.05 | Ohms |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5 Vdc, $I_D$ = 30 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 15 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.1<br>– | 1.8<br>1.73 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.25 Vdc, $I_D$ = 15 Adc) | | $g_{FS}$ | 13 | 21 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1130 | 1580 | pF |
| Output Capacitance | | $C_{oss}$ | – | 360 | 500 | |
| Transfer Capacitance | | $C_{rss}$ | – | 95 | 190 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 30 | ns |
| Rise Time | | $t_r$ | – | 260 | 520 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 54 | 110 | |
| Fall Time | | $t_f$ | – | 108 | 220 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 27 | 40 | nC |
| | | $Q_1$ | – | 5 | – | |
| | | $Q_2$ | – | 17 | – | |
| | | $Q_3$ | – | 15 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 0.98<br>0.89 | 1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 86 | – | ns |
| | | $t_a$ | – | 49 | – | |
| | | $t_b$ | – | 37 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.228 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

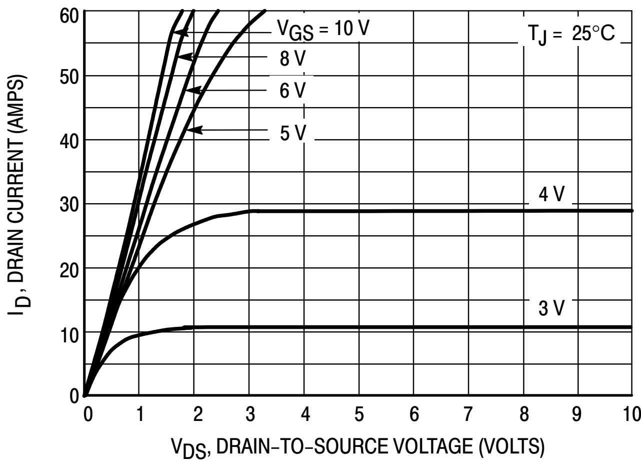



**Figure 1. On–Region Characteristics**

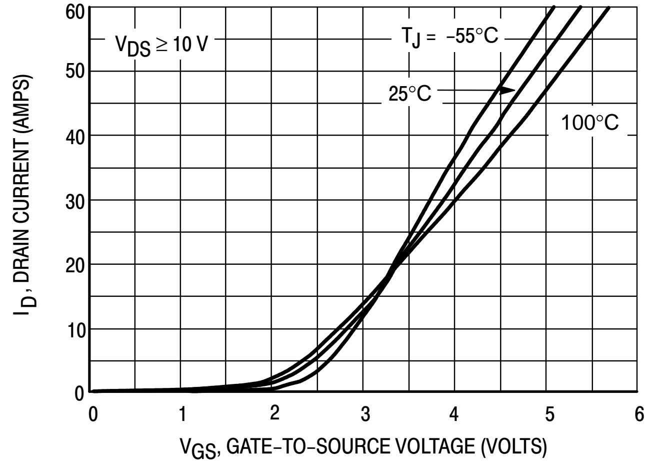



**Figure 2. Transfer Characteristics**

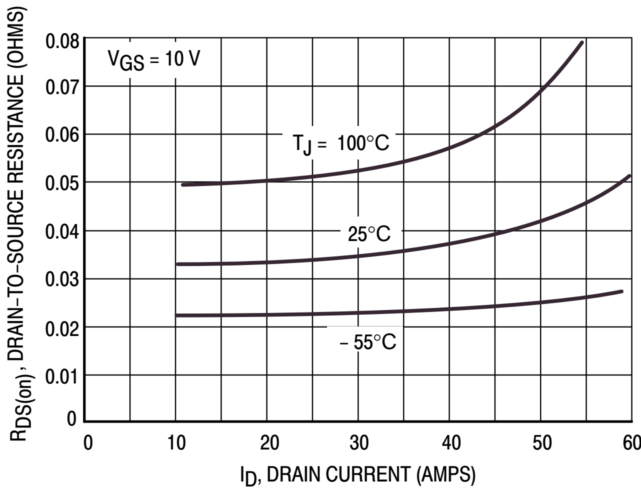



**Figure 3. On–Resistance versus Drain Current and Temperature**

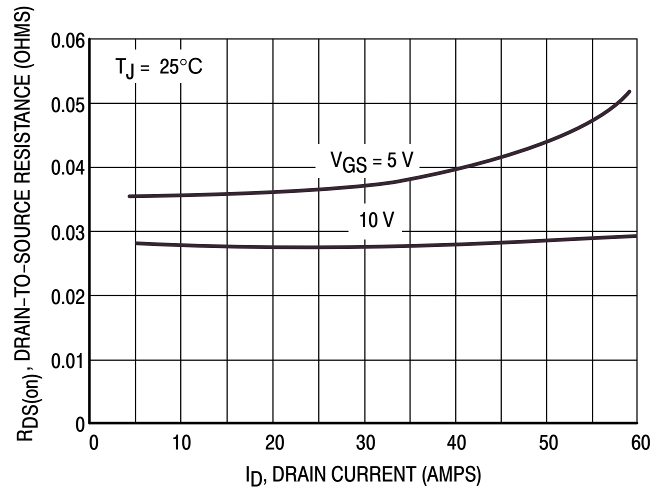



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

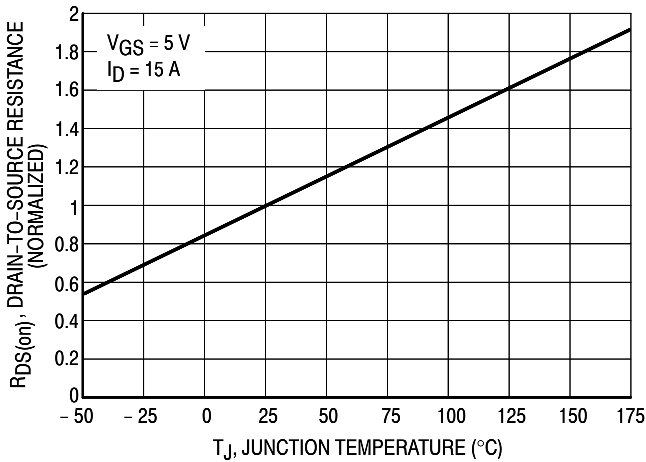



**Figure 5. On–Resistance Variation with Temperature**

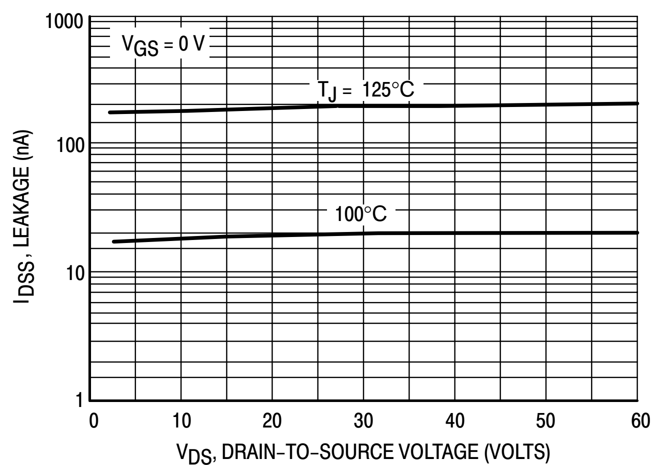



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

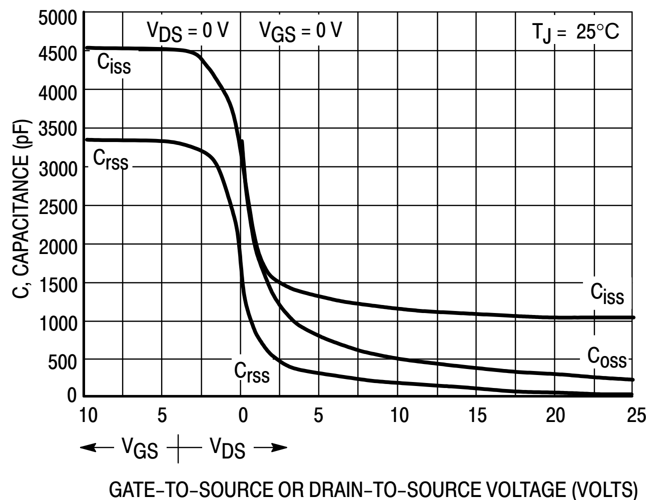



**Figure 7. Capacitance Variation**

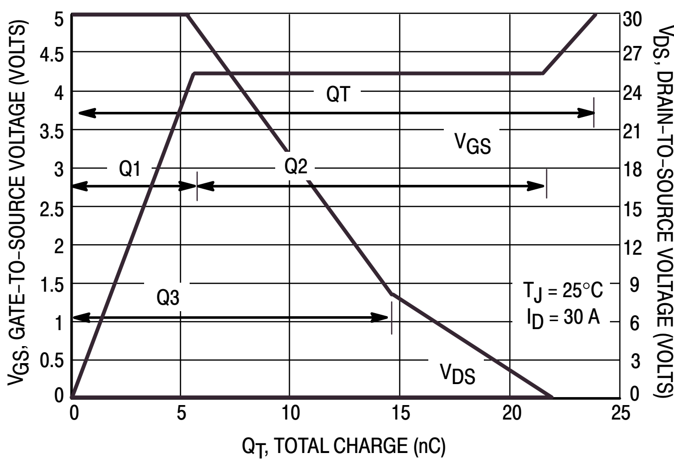



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

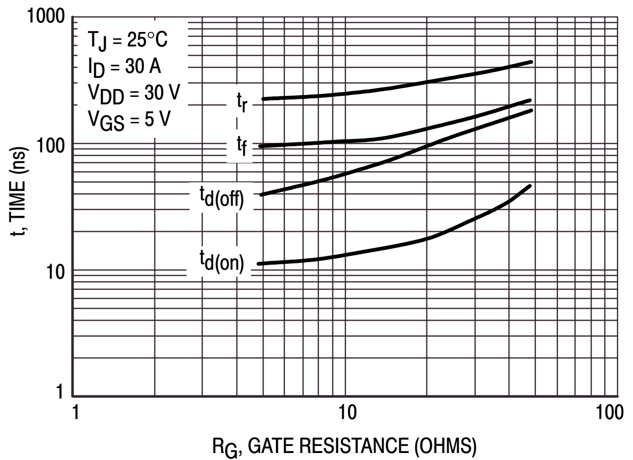



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

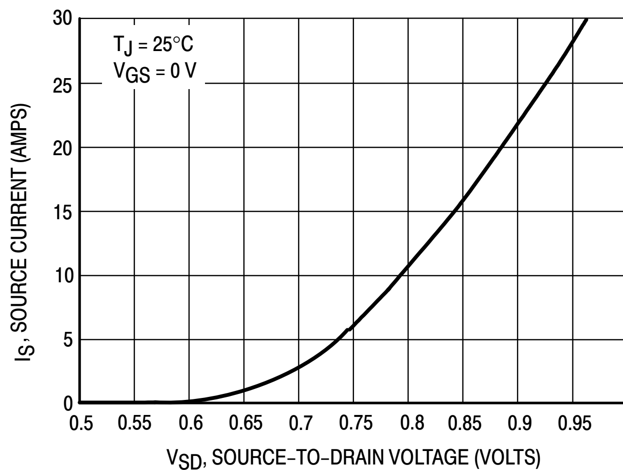



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

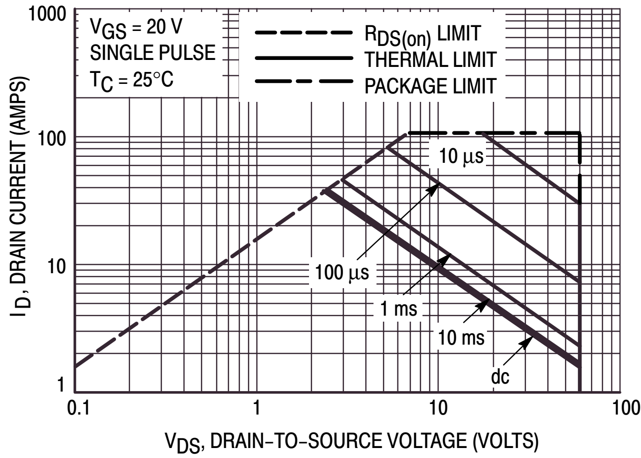



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

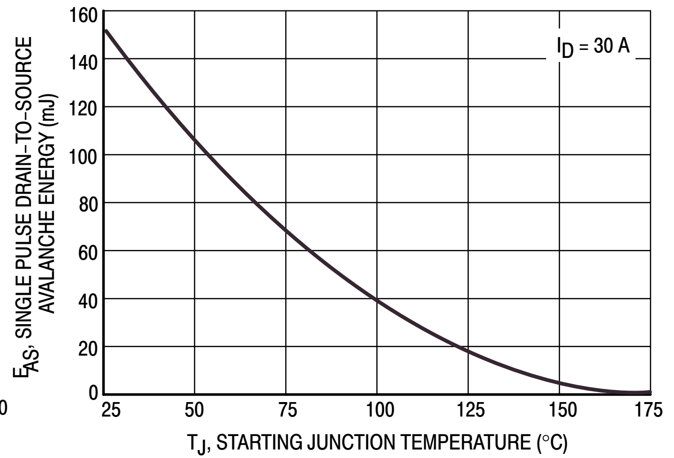



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

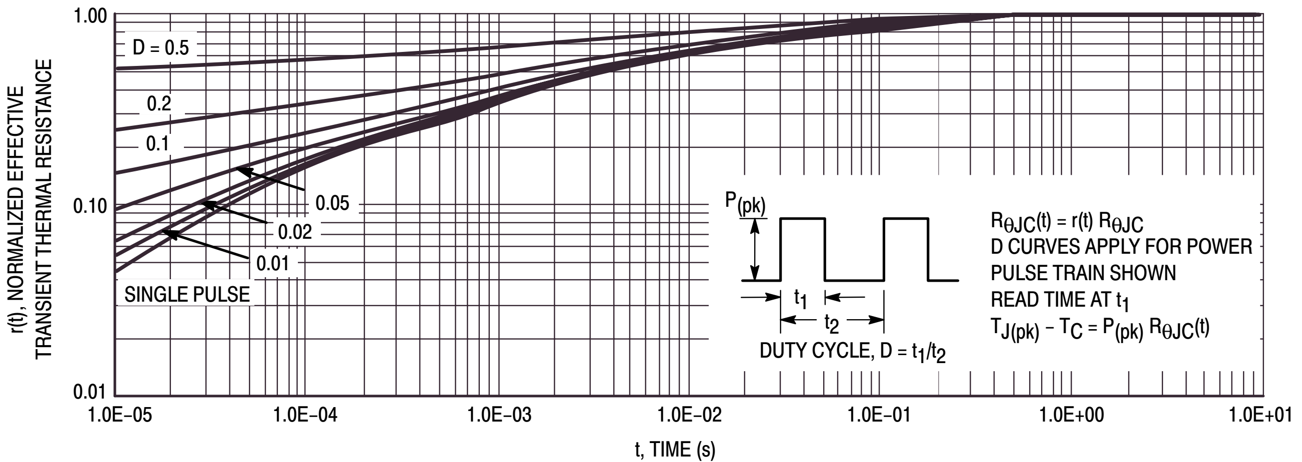



**Figure 13. Thermal Response**

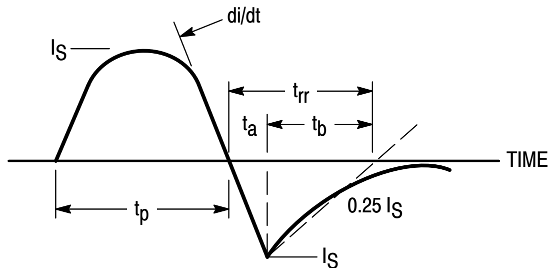



**Figure 14. Diode Reverse Recovery Waveform**

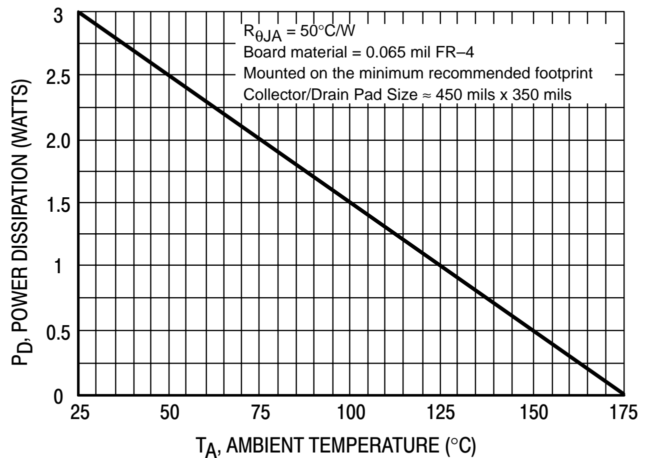
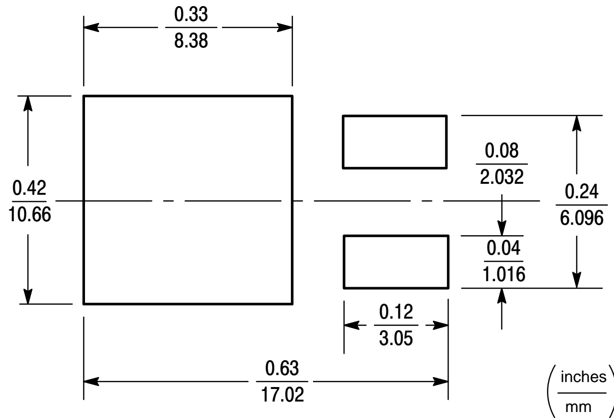



**Figure 15. D²PAK Power Derating Curve**

# INFORMATION FOR USING THE D$^2$PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D$^2$PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D$^2$PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

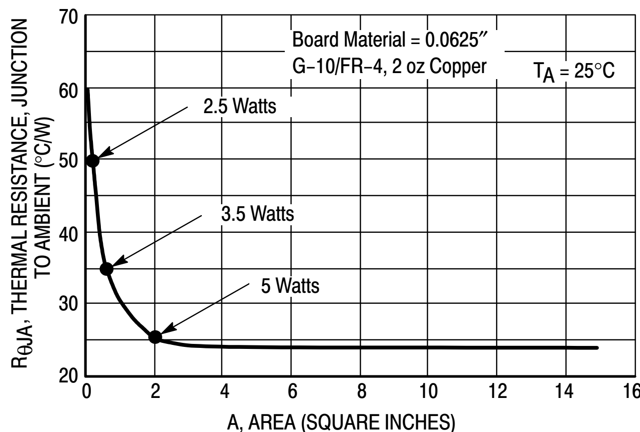



**Figure 16. Thermal Resistance versus Drain Pad Area for the D$^2$PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

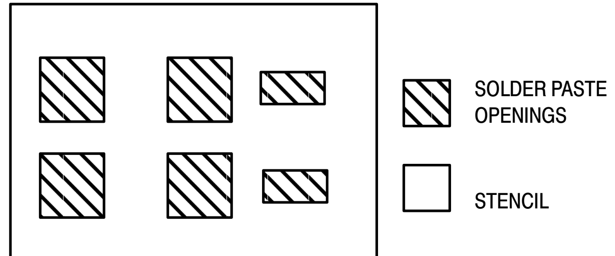



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

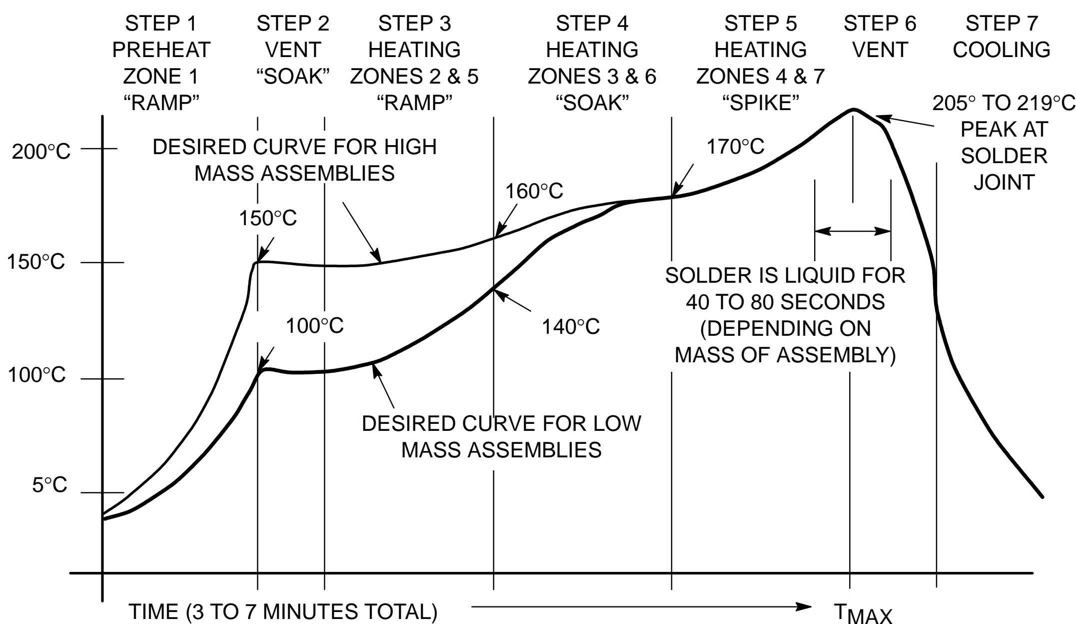



**Figure 18. Typical Solder Heating Profile**

# MTB30P06V

Preferred Device

# Power MOSFET 30 Amps, 60 Volts

## P–Channel $D^2PAK$

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 30<br>19<br>105 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>0.83<br>3.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 30 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 450 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.2<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

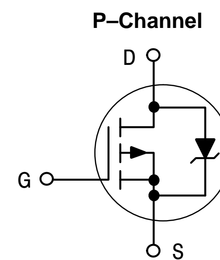
1. When surface mounted to an FR4 board using the minimum recommended pad size.

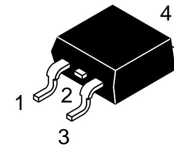
**ON Semiconductor™**

**http://onsemi.com**

**30 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 80 mΩ**

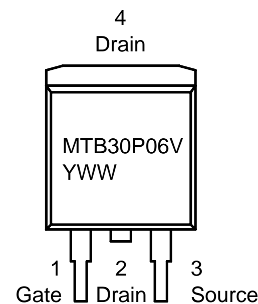
**P–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB30P06V = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB30P06V | $D^2PAK$ | 50 Units/Rail |
| MTB30P06VT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

© Semiconductor Components Industries, LLC, 2000

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | 60<br>– | –<br>62 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | 2.0<br>– | 2.6<br>5.3 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc) | $R_{DS(on)}$ | – | 0.067 | 0.08 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 30 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc, $T_J$ = 150°C) | $V_{DS(on)}$ | –<br>– | 2.0<br>– | 2.9<br>2.8 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.3 Vdc, $I_D$ = 15 Adc) | $g_{FS}$ | 5.0 | 7.9 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1562 | 2190 | pF |
| Output Capacitance | $C_{oss}$ | – | 524 | 730 | |
| Transfer Capacitance | $C_{rss}$ | – | 154 | 310 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | |
| Turn–On Delay Time ($V_{DD}$ = 30 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14.7 | 30 | ns |
| Rise Time | $t_r$ | – | 25.9 | 50 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 98 | 200 | |
| Fall Time | $t_f$ | – | 52.4 | 100 | |
| Gate Charge (See Figure 8) ($V_{DS}$ = 48 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 54 | 80 | nC |
| | $Q_1$ | – | 9.0 | – | |
| | $Q_2$ | – | 26 | – | |
| | $Q_3$ | – | 20 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 2.3<br>1.9 | 3.0<br>– | Vdc |
| Reverse Recovery Time ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 175 | – | ns |
| | $t_a$ | – | 107 | – | |
| | $t_b$ | – | 68 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.965 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

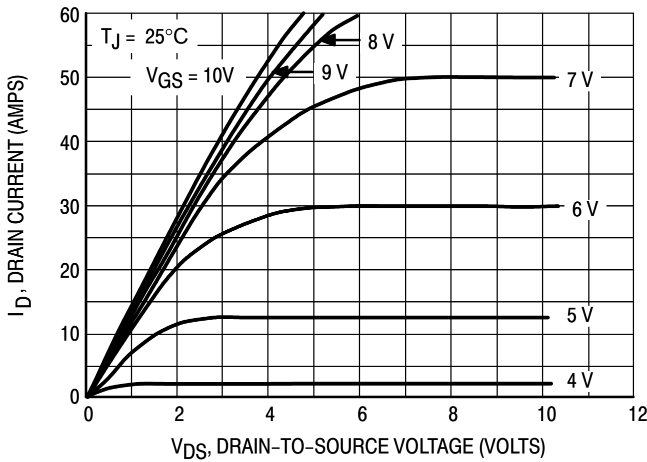



**Figure 1. On–Region Characteristics**

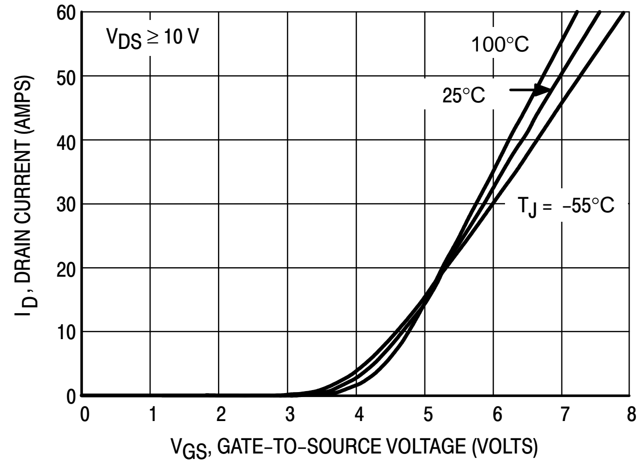



**Figure 2. Transfer Characteristics**

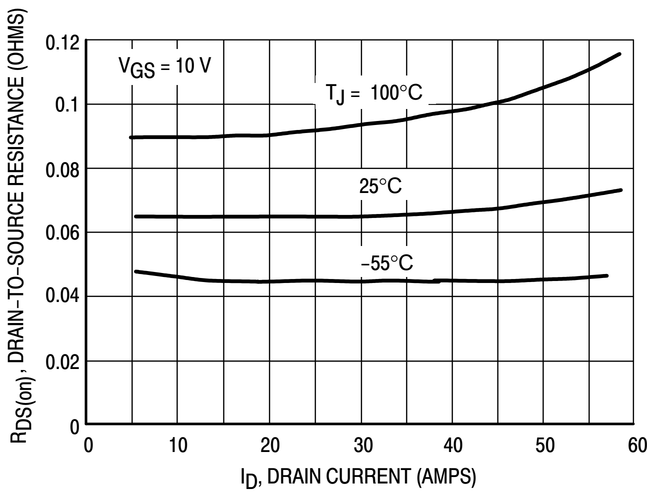



**Figure 3. On–Resistance versus Drain Current and Temperature**

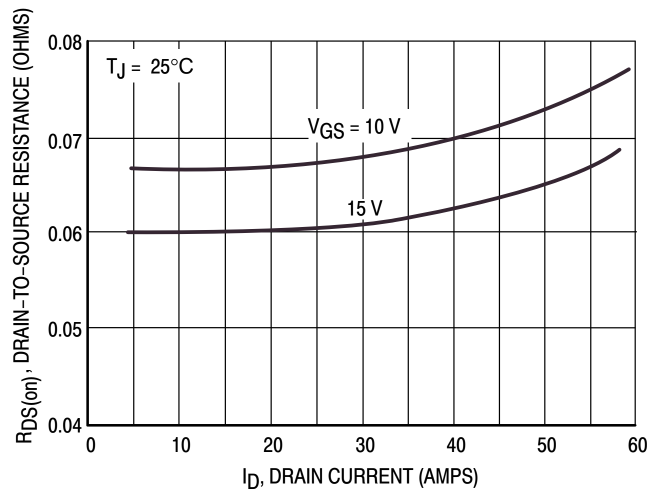



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

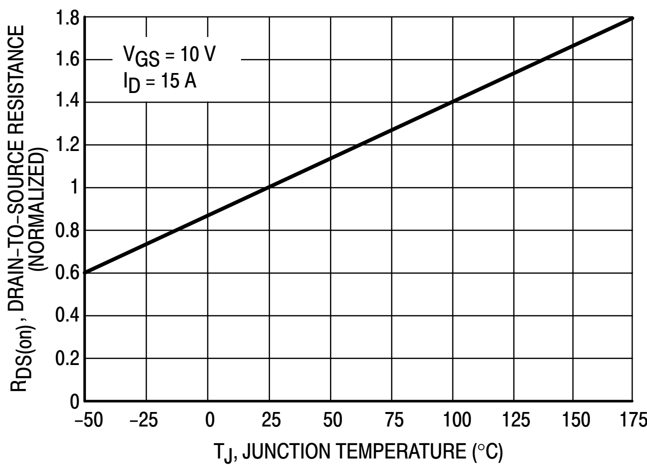



**Figure 5. On–Resistance Variation with Temperature**

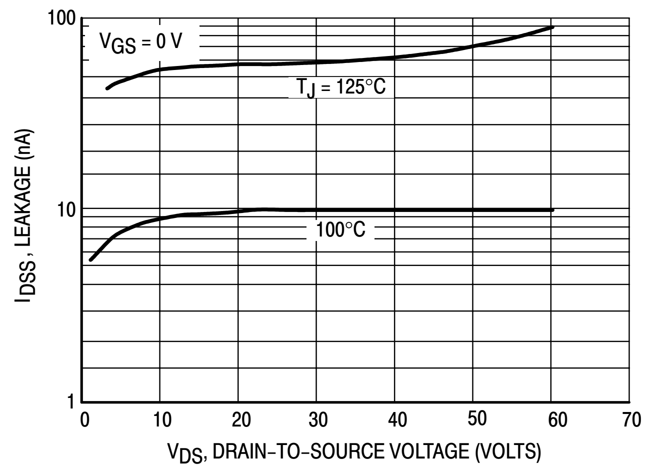



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

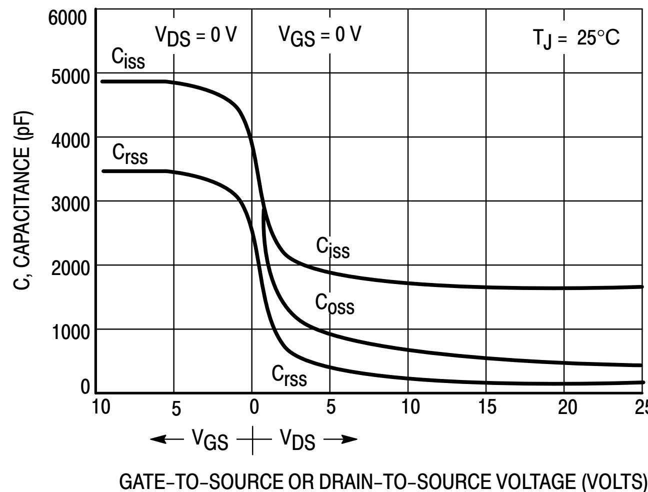



**Figure 7. Capacitance Variation**

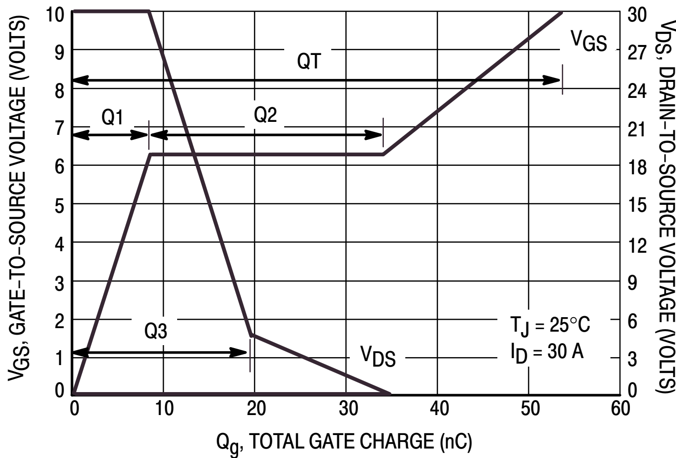



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

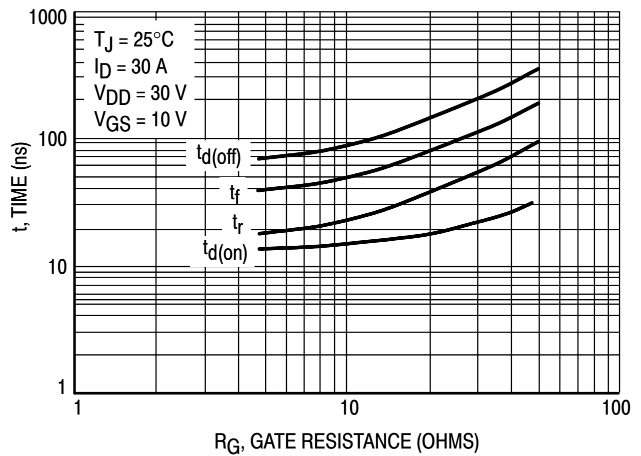



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

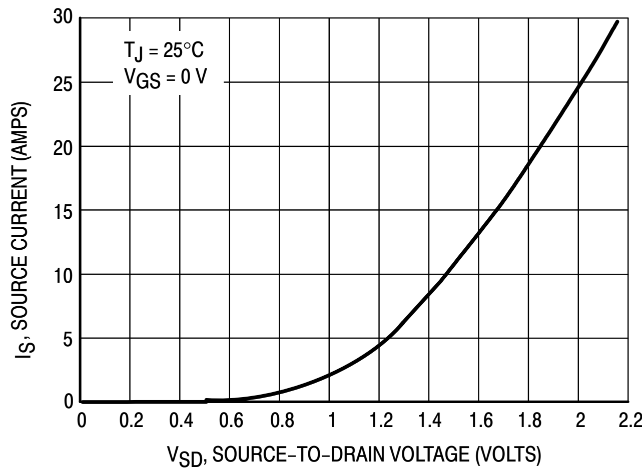



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

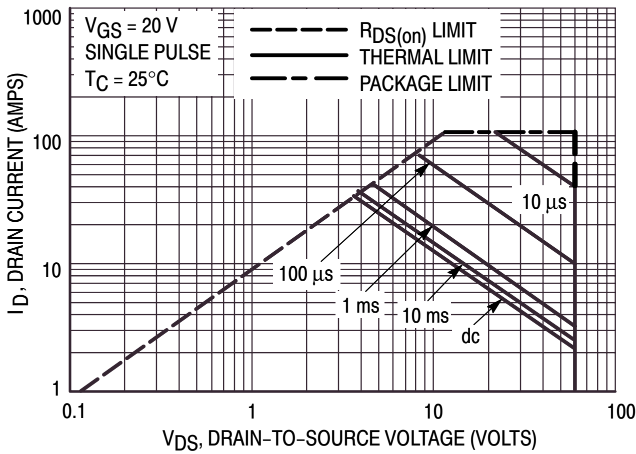



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

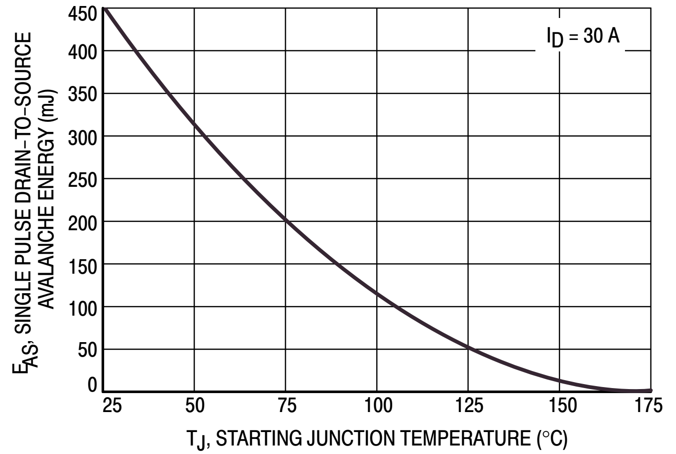



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

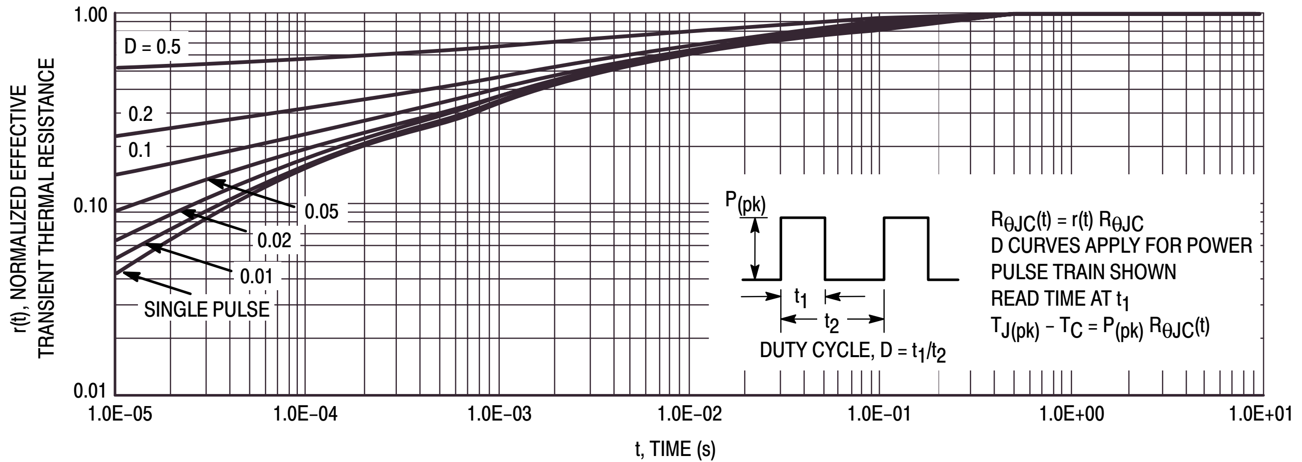



**Figure 13. Thermal Response**

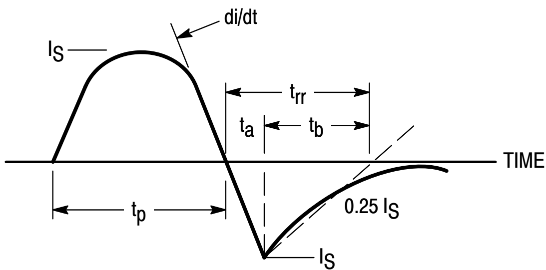



**Figure 14. Diode Reverse Recovery Waveform**

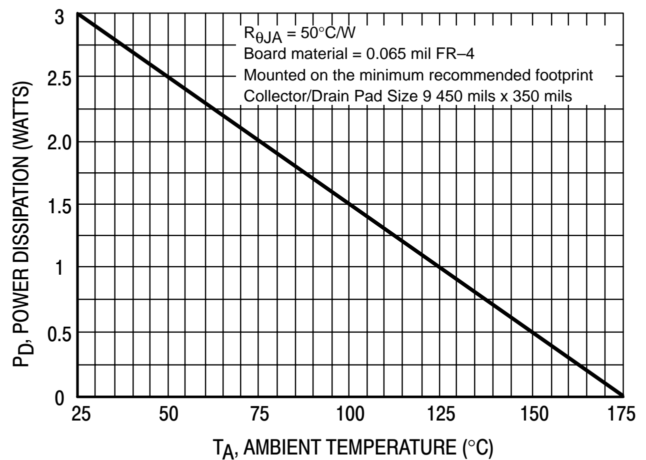
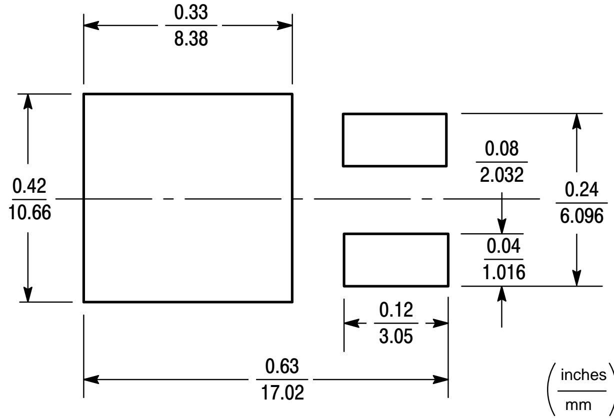



**Figure 15. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

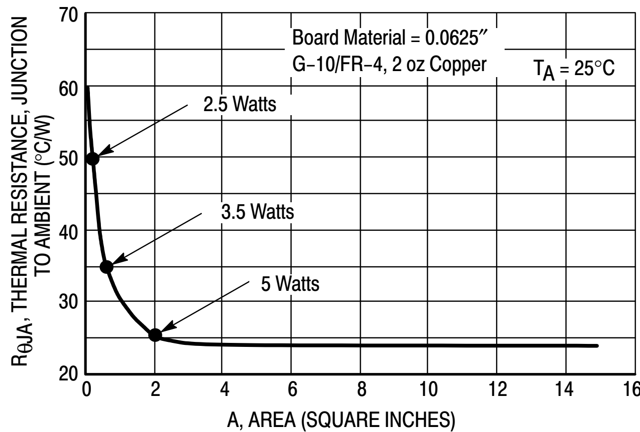



**Figure 16. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

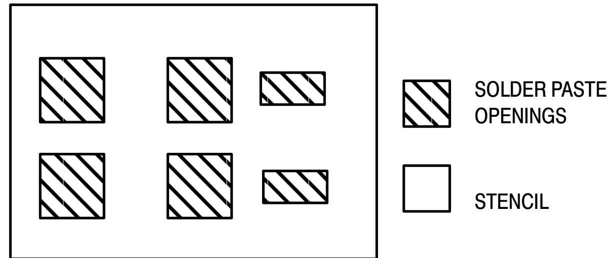



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

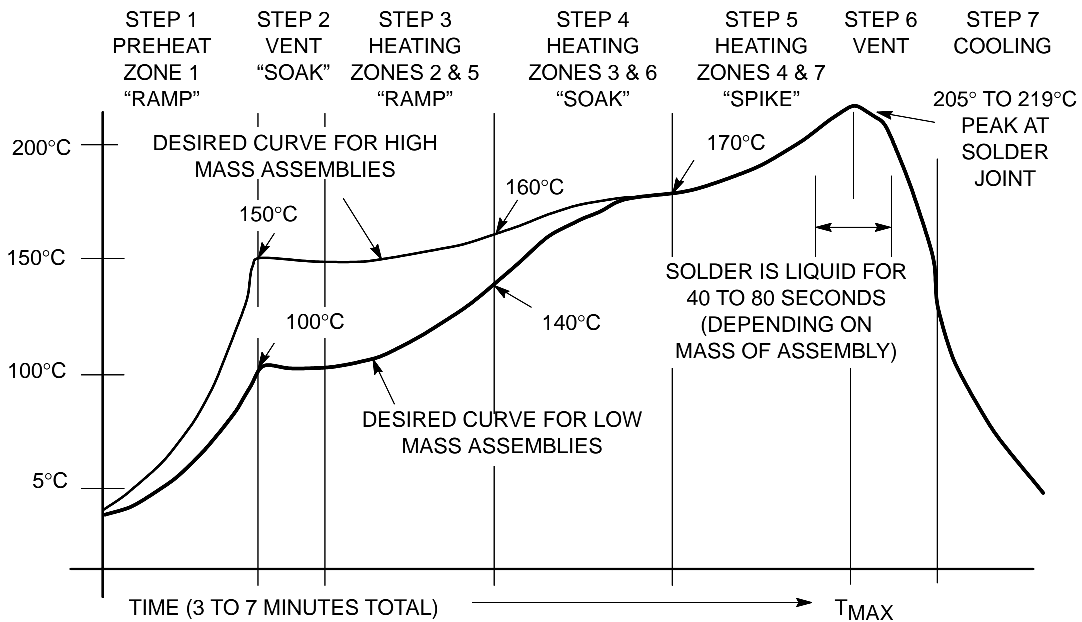



**Figure 18. Typical Solder Heating Profile**

# MTB36N06V

**Preferred Device**

# Power MOSFET 32 Amps, 60 Volts

## N–Channel $D^2PAK$

**ON Semiconductor™**

**http://onsemi.com**

**32 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

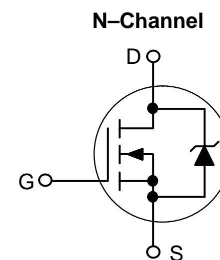
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

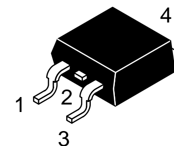
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq 50$ µs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq 10$ µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 32<br>22.6<br>112 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 90<br>0.6<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 32 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 205 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

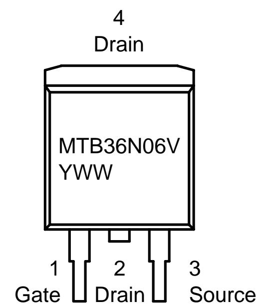
**N–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTB36N06V | = Device Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB36N06V | $D^2PAK$ | 50 Units/Rail |
| MTB36N06VT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 3

Publication Order Number:
MTB36N06V/D

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>61 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.6<br>6.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 0.034 | 0.04 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 32 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.25<br>– | 1.54<br>1.47 | Vdc |
| Forward Transconductance ($V_{DS}$ = 7.6 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | 5.0 | 7.83 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1220 | 1700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 337 | 470 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 74.8 | 150 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 30 | ns |
| Rise Time | | $t_r$ | – | 138 | 270 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 54 | 100 | |
| Fall Time | | $t_f$ | – | 91 | 180 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 39 | 50 | nC |
| | | $Q_1$ | – | 7 | – | |
| | | $Q_2$ | – | 17 | – | |
| | | $Q_3$ | – | 13 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.03<br>0.94 | 2.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 92 | – | ns |
| | | $t_a$ | – | 64 | – | |
| | | $t_b$ | – | 28 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.332 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

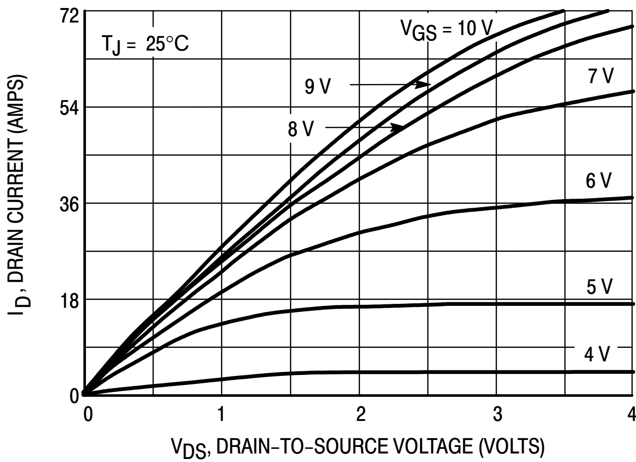



**Figure 1. On–Region Characteristics**

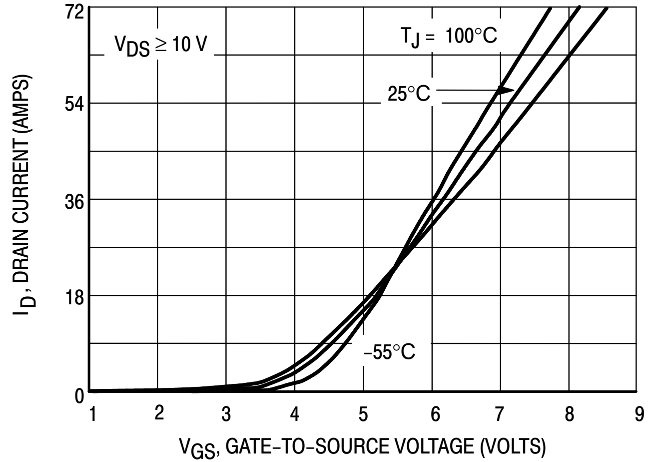



**Figure 2. Transfer Characteristics**

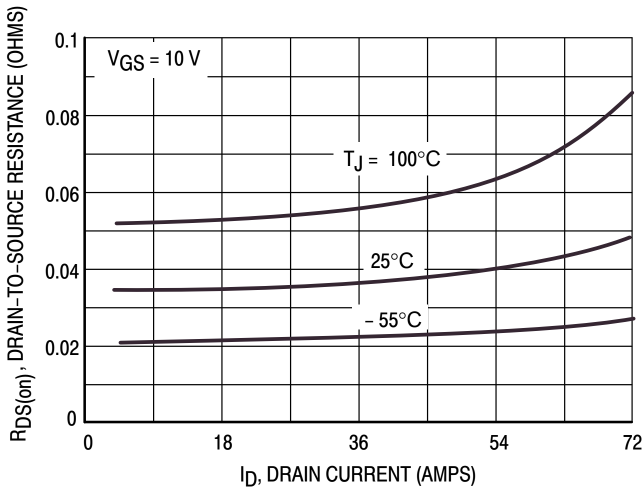



**Figure 3. On–Resistance versus Drain Current and Temperature**

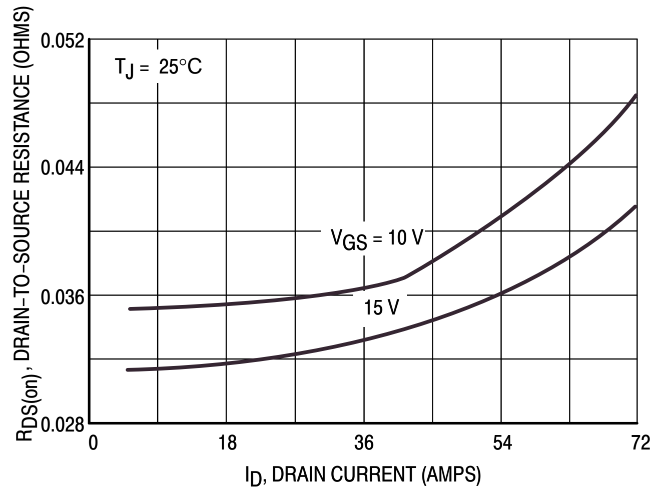



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

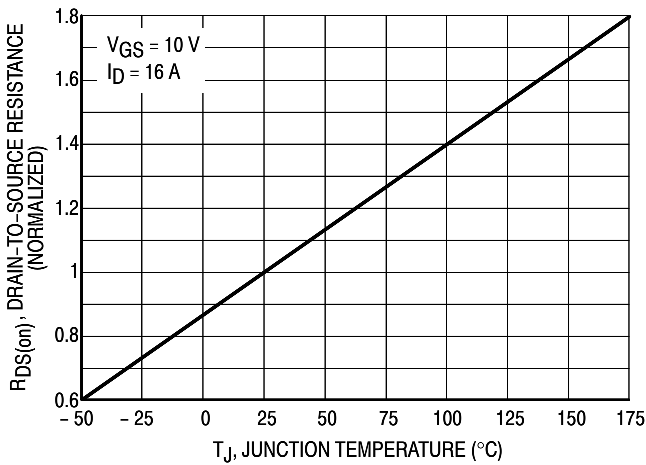



**Figure 5. On–Resistance Variation with Temperature**

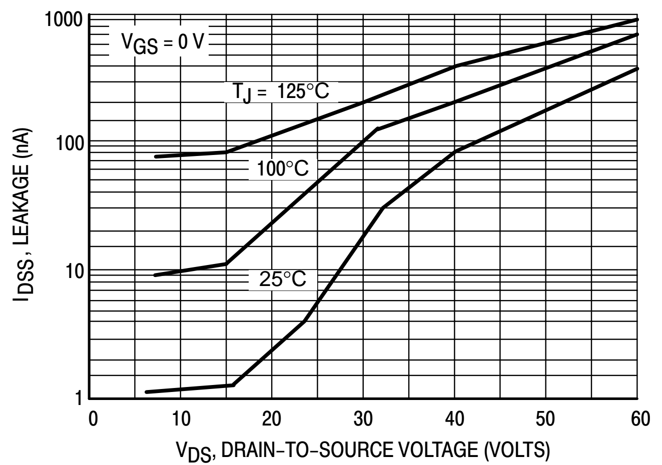



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

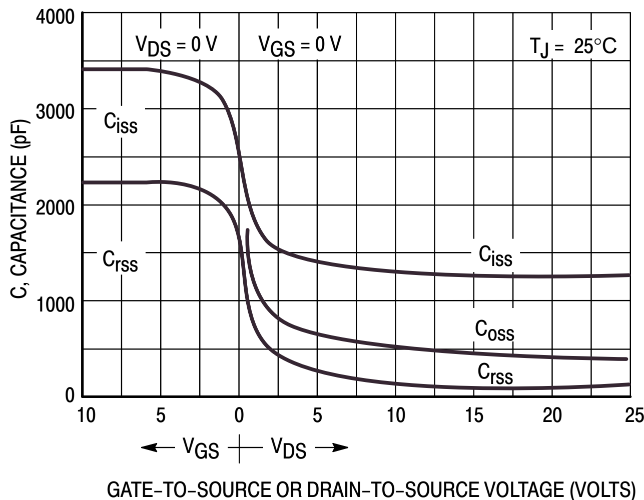



**Figure 7. Capacitance Variation**

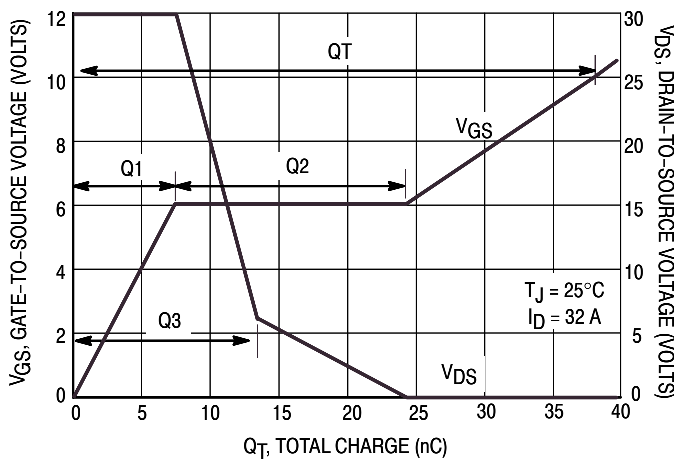



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

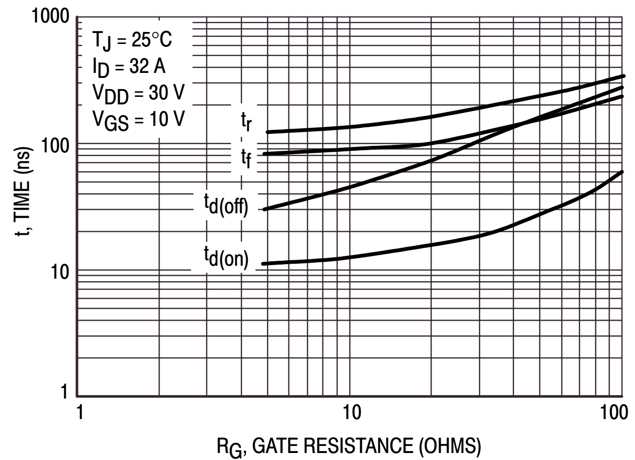



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

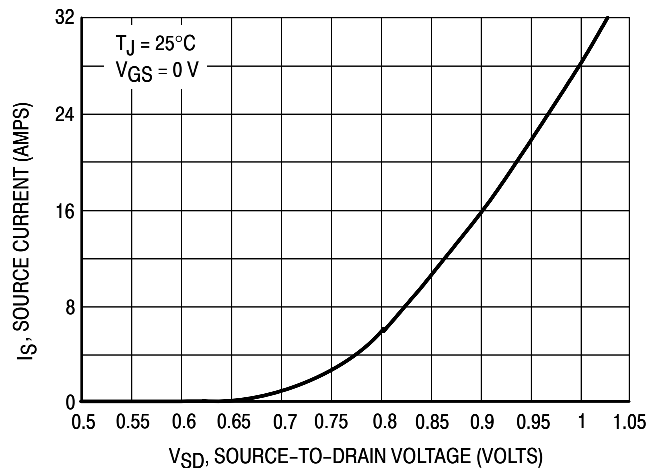



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

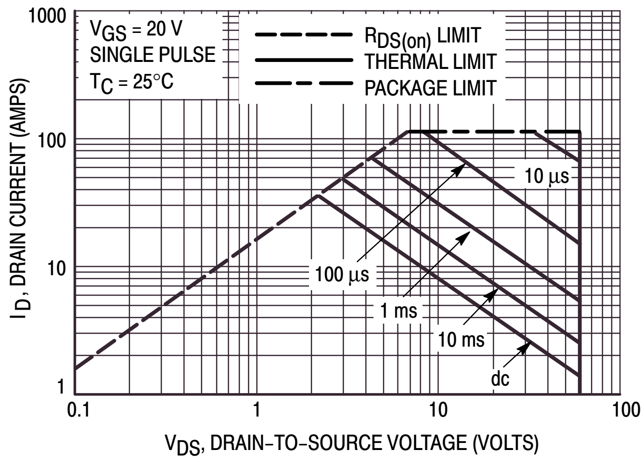



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

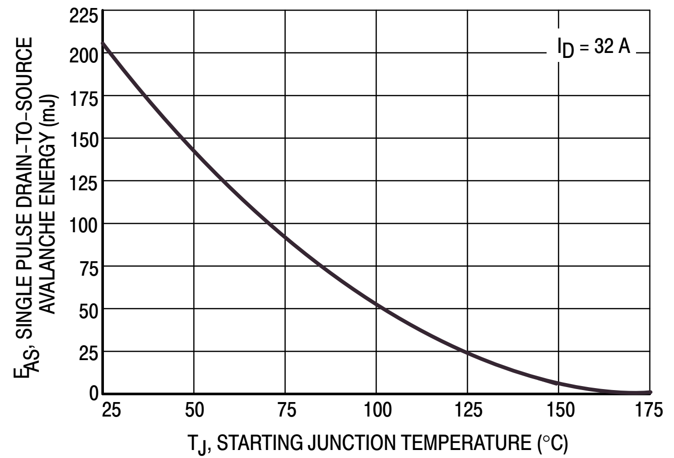



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

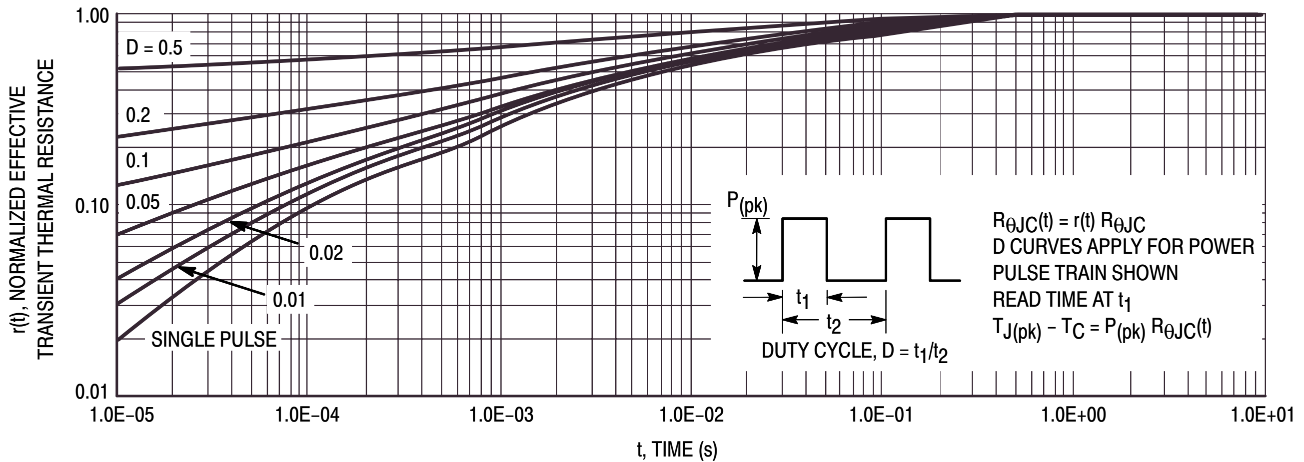



**Figure 13. Thermal Response**

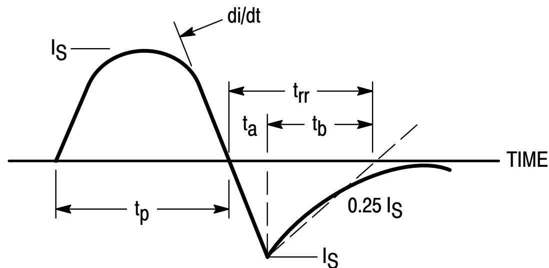



**Figure 14. Diode Reverse Recovery Waveform**

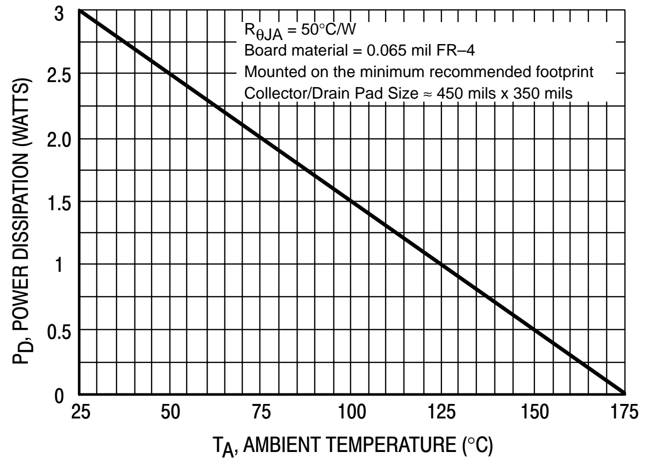
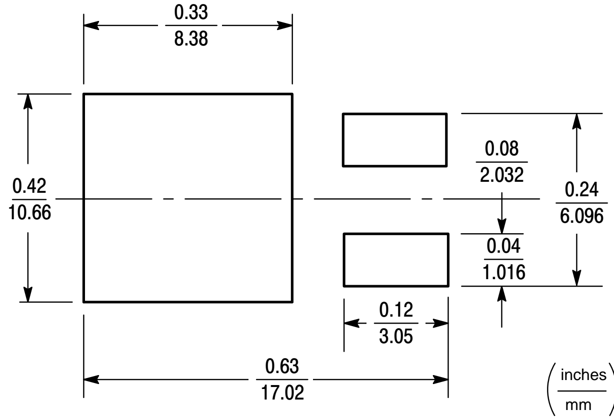



**Figure 15. D2PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

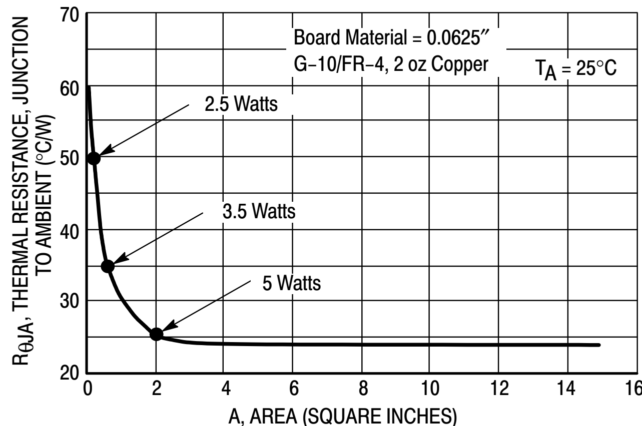



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

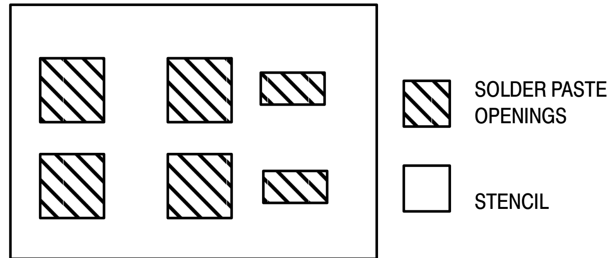



**Figure 17. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

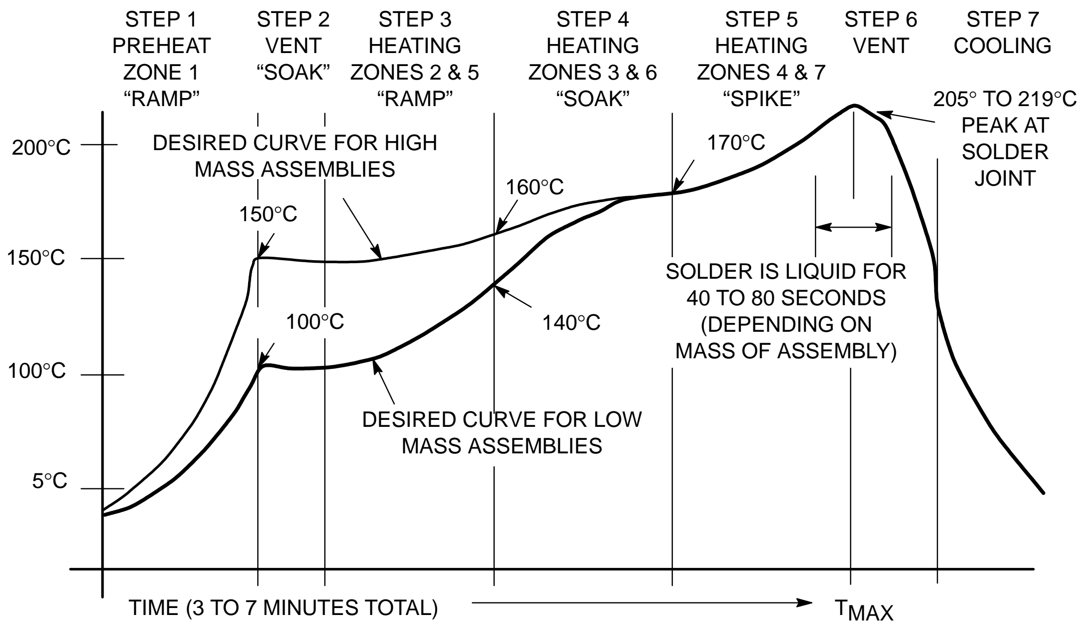



**Figure 18. Typical Solder Heating Profile**

# MTB40N10E

Preferred Device

# Power MOSFET 40 Amps, 100 Volts

## N–Channel D2PAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

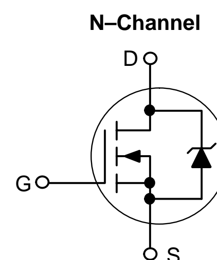
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 40<br>29<br>140 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 169<br>1.35<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 75 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 40 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 800 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>0.74<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

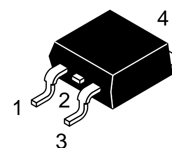
1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ON Semiconductor™**

http://onsemi.com

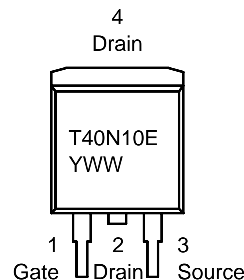
**40 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**




**D2PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T40N10E = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB40N10E | D2PAK | 50 Units/Rail |
| MTB40N10ET4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) (Cpk ≥ 2.0) (Note 4.) | | $V_{(BR)DSS}$ | <br>100<br>– | <br>–<br>112 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.9<br>6.7 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc) (Cpk ≥ 2.0) (Note 4.) | | $R_{DS(on)}$ | – | 0.033 | 0.04 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 40 Adc)<br>($I_D$ = 20 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.9<br>1.7 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.4 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 21 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2305 | 3230 | pF |
| Output Capacitance | | $C_{oss}$ | – | 620 | 1240 | |
| Transfer Capacitance | | $C_{rss}$ | – | 205 | 290 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 50 Vdc, $I_D$ = 40 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 19 | 40 | ns |
| Rise Time | | $t_r$ | – | 165 | 330 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 75 | 150 | |
| Fall Time | | $t_f$ | – | 97 | 190 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 40 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 80 | 110 | nC |
| | | $Q_1$ | – | 15 | – | |
| | | $Q_2$ | – | 40 | – | |
| | | $Q_3$ | – | 29 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.96<br>0.88 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 14) | ($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 152 | – | ns |
| | | $t_a$ | – | 117 | – | |
| | | $t_b$ | – | 35 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.0 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $Cpk = \left|\frac{\text{Max limit} - \text{Typ}}{3 \times \text{sigma}}\right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

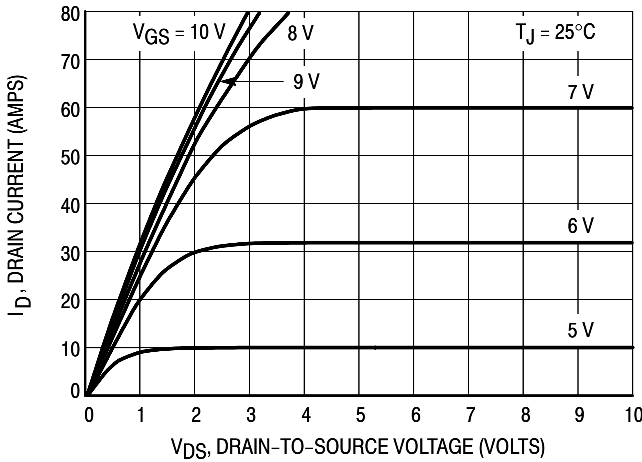



**Figure 1. On−Region Characteristics**

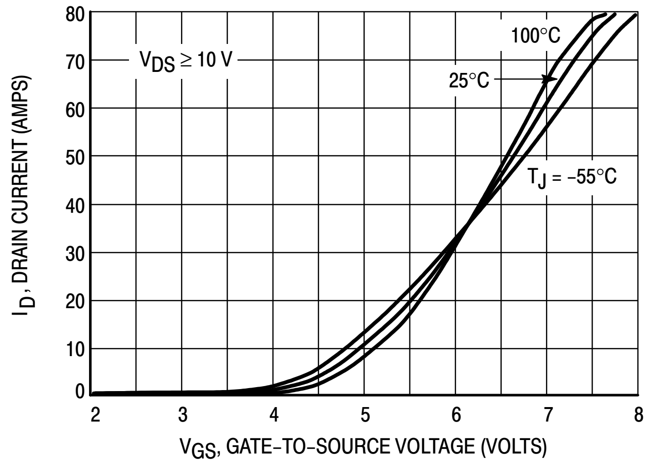



**Figure 2. Transfer Characteristics**

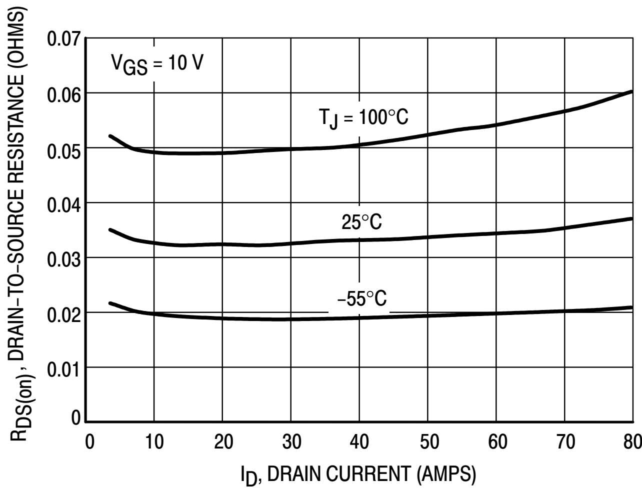



**Figure 3. On−Resistance versus Drain Current and Temperature**

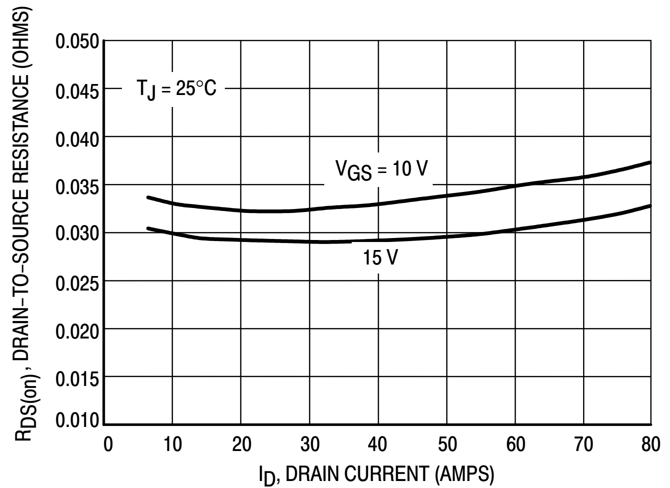



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

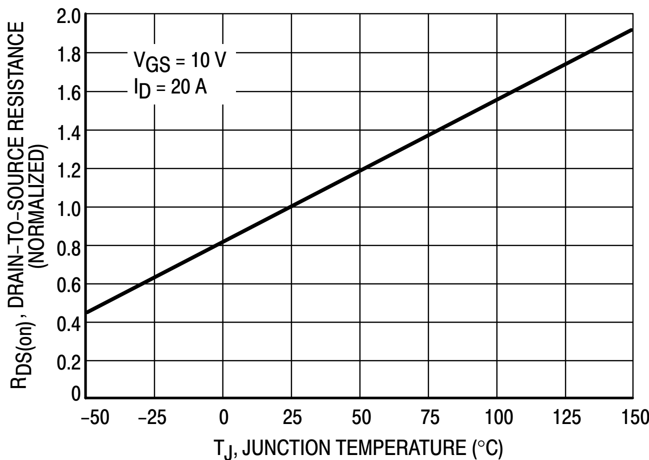



**Figure 5. On−Resistance Variation with Temperature**

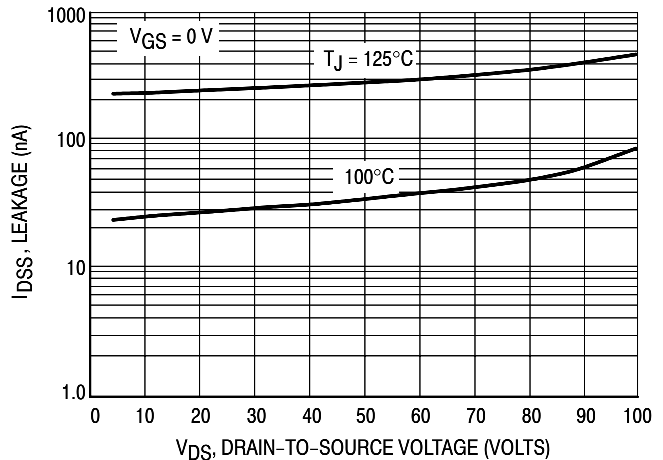



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

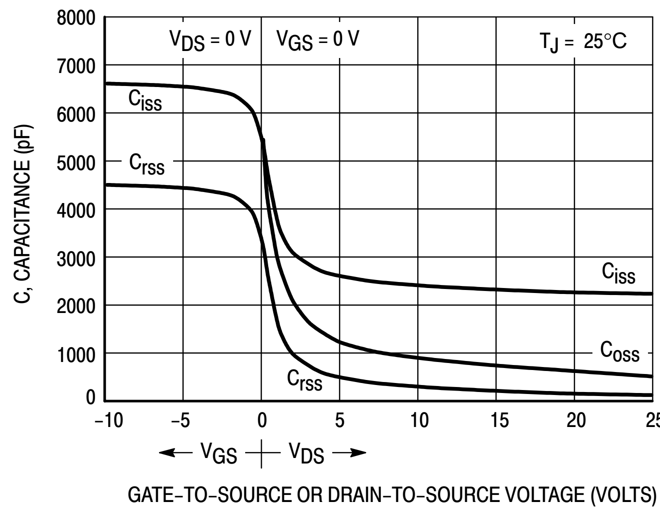



**Figure 7. Capacitance Variation**

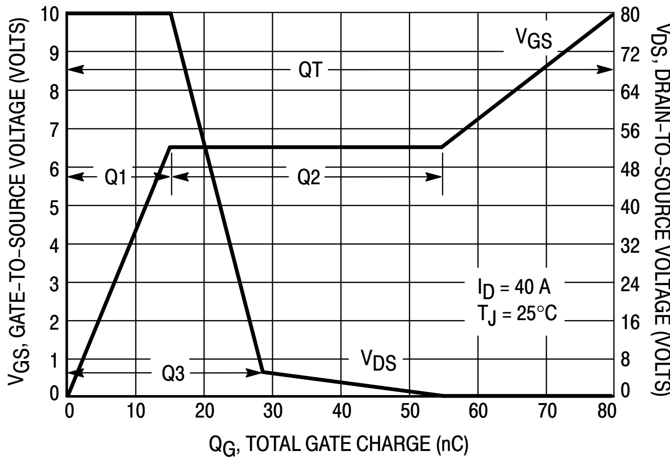



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

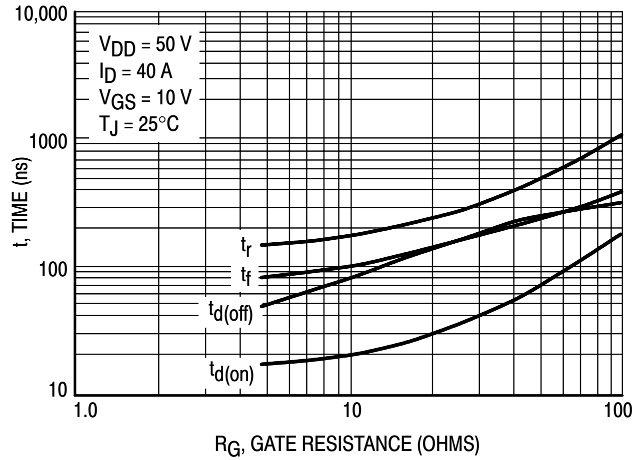



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

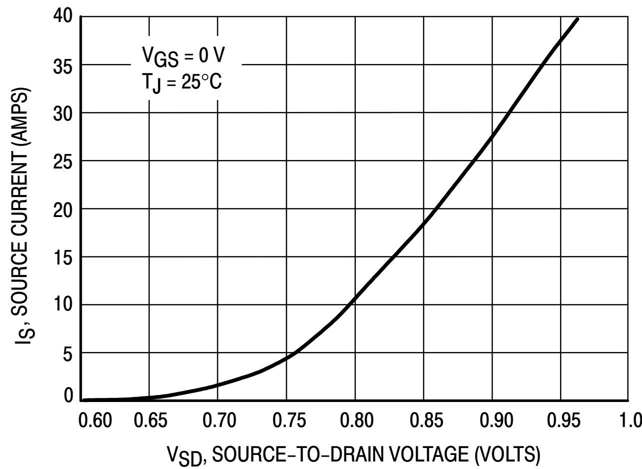



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

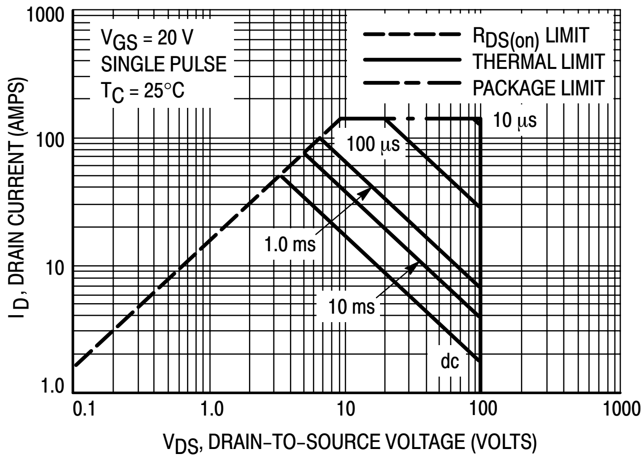



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

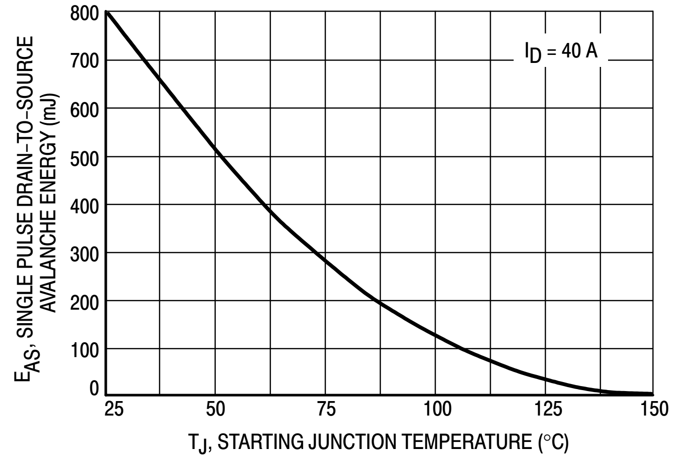



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

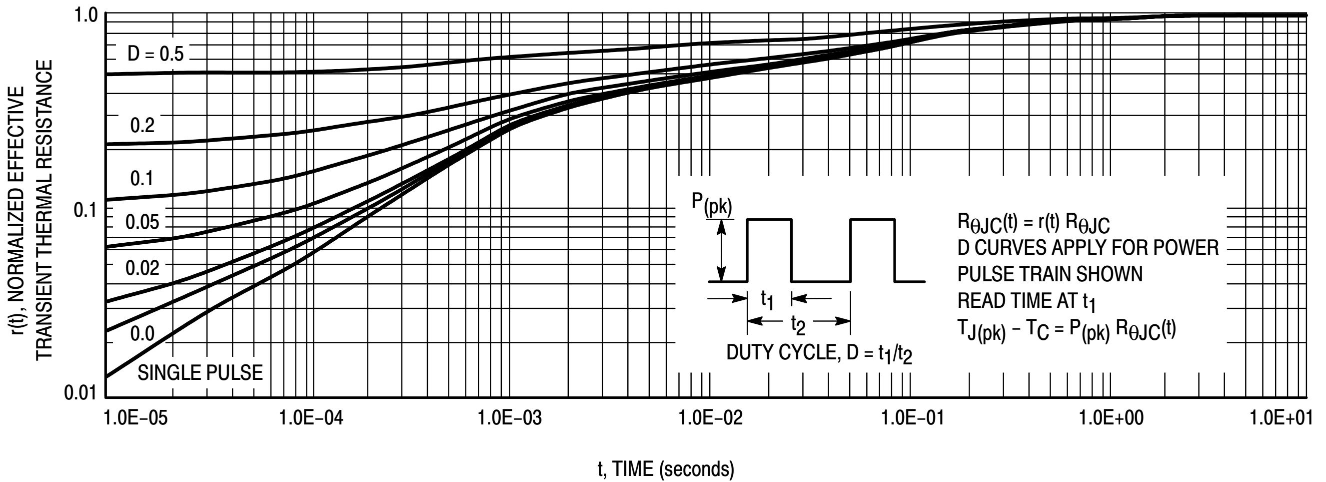



**Figure 13. Thermal Response**

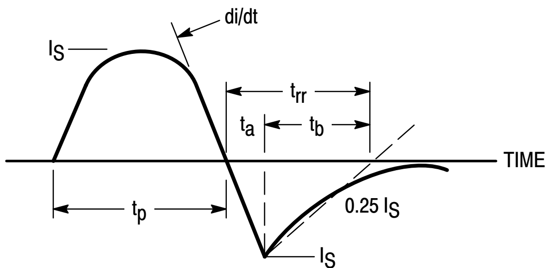



**Figure 14. Diode Reverse Recovery Waveform**

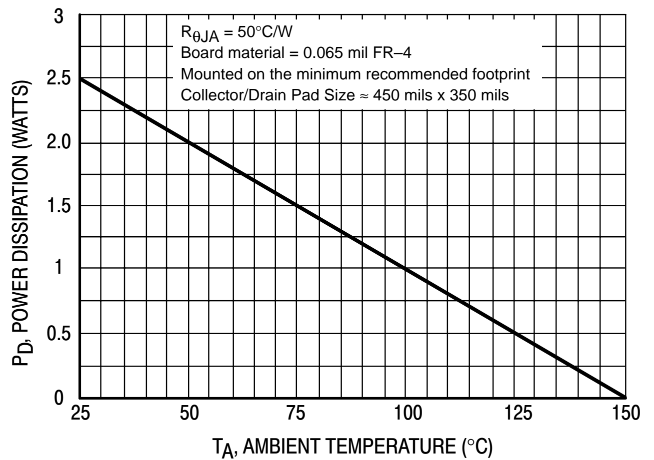
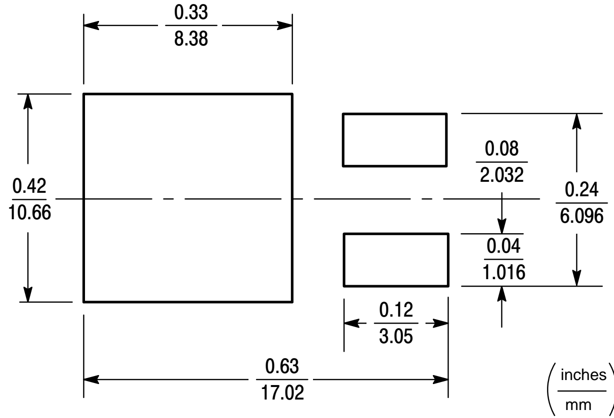



**Figure 15. $D^2PAK$ Power Derating Curve**

# INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

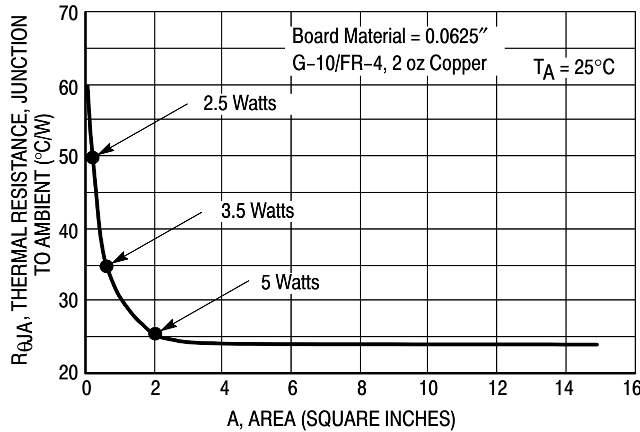



**Figure 16. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

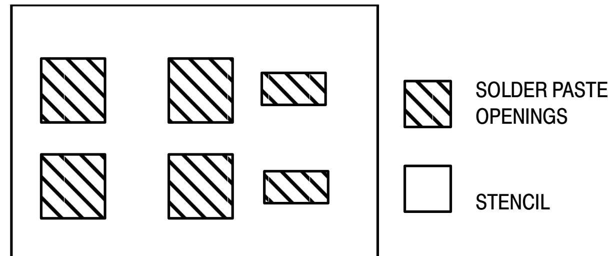



**Figure 17. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

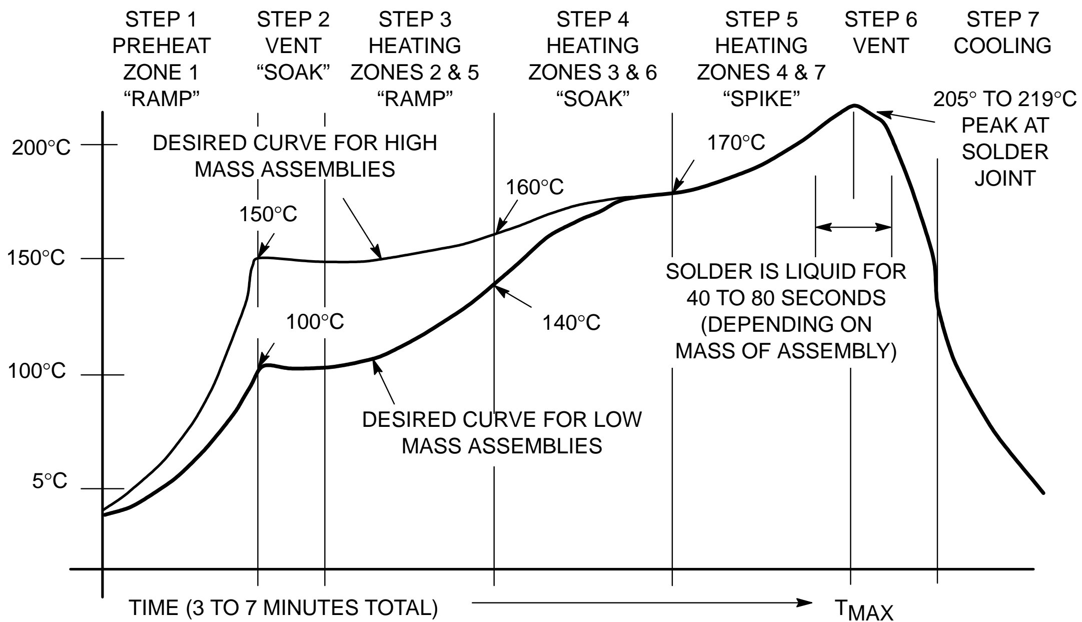



**Figure 18. Typical Solder Heating Profile**

# MTB50N06V

**Preferred Device**

# Power MOSFET 42 Amps, 60 Volts
## N–Channel D2PAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 42<br>30<br>147 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>0.83<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 42 Apk, L = 0.454 μH, $R_G$ = 25 Ω) | $E_{AS}$ | 400 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.2<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

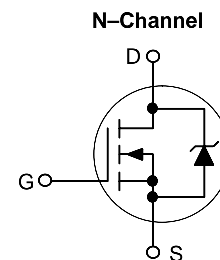
1. When surface mounted to an FR4 board using the minimum recommended pad size.

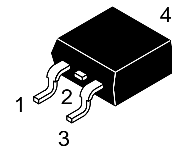
**ON Semiconductor™**

**http://onsemi.com**

**42 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

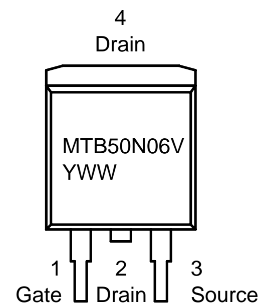
**N–Channel**




**D2PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTB50N06V | = Device Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB50N06V | D2PAK | 50 Units/Rail |
| MTB50N06VT4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>69 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>3.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 21 Adc) | | $R_{DS(on)}$ | – | 0.025 | 0.028 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 42 Adc)<br>($I_D$ = 21 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.4<br>– | 1.7<br>1.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.25 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 16 | 23 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1644 | 2320 | pF |
| Output Capacitance | | $C_{oss}$ | – | 465 | 660 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 112 | 230 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 20 | ns |
| Rise Time | | $t_r$ | – | 122 | 250 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 64 | 110 | |
| Fall Time | | $t_f$ | – | 54 | 90 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 47 | 70 | nC |
| | | $Q_1$ | – | 9 | – | |
| | | $Q_2$ | – | 21 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.06<br>0.99 | 2.5<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 84 | – | ns |
| | | $t_a$ | – | 73 | – | |
| | | $t_b$ | – | 11 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.28 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

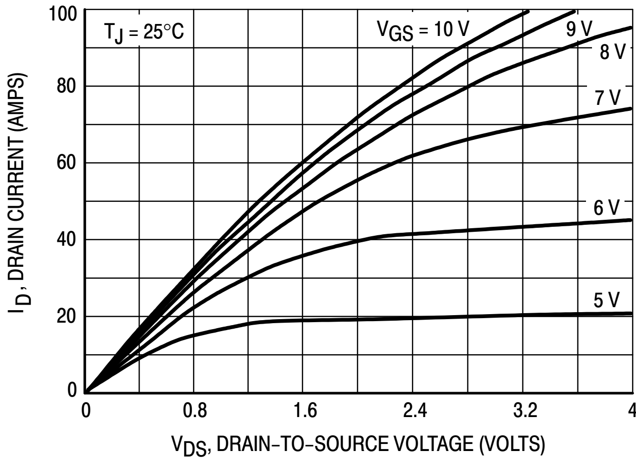



**Figure 1. On–Region Characteristics**

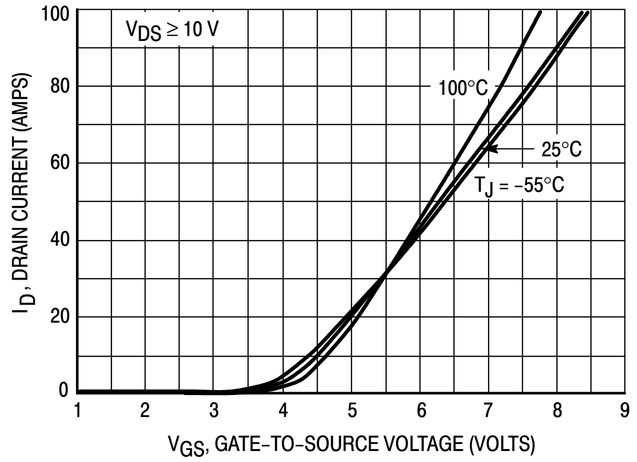



**Figure 2. Transfer Characteristics**

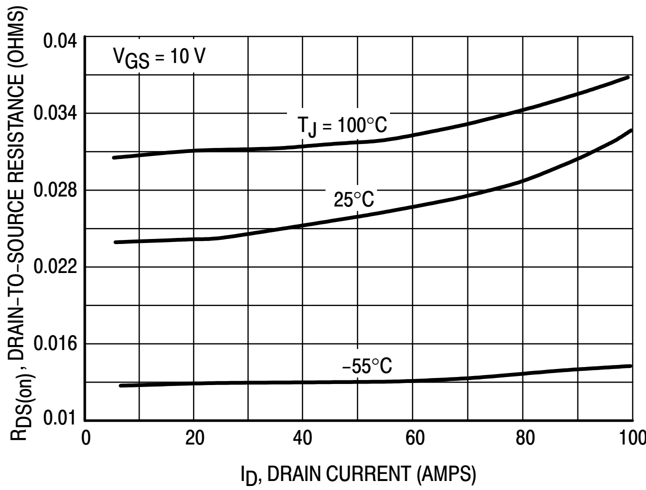



**Figure 3. On–Resistance versus Drain Current and Temperature**

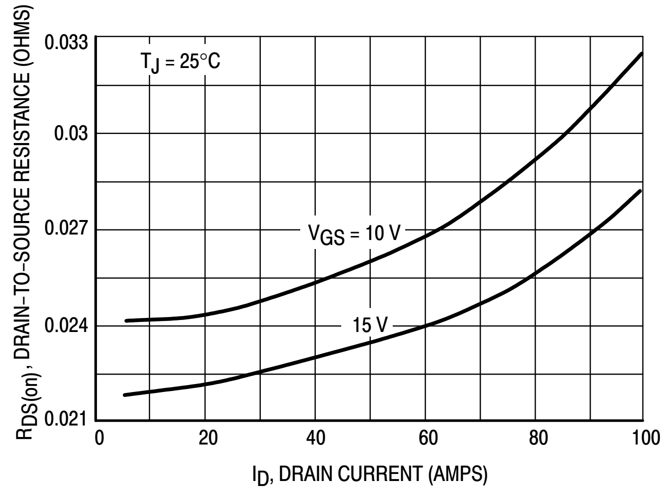



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

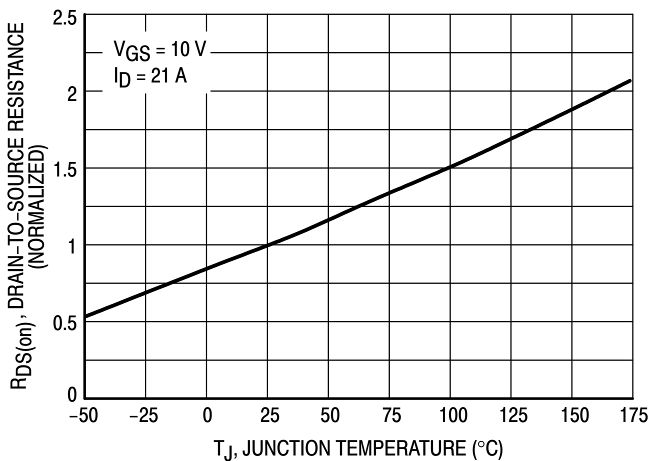



**Figure 5. On–Resistance Variation with Temperature**

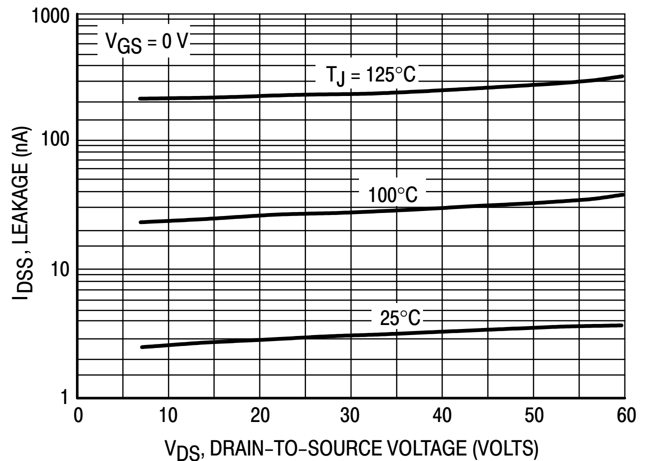



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

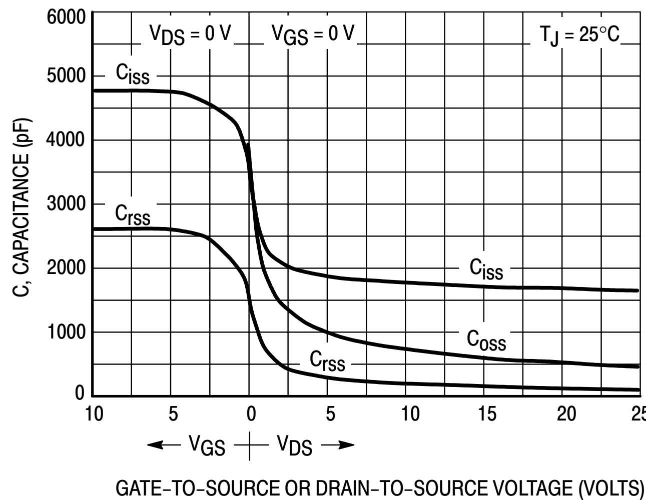



**Figure 7. Capacitance Variation**

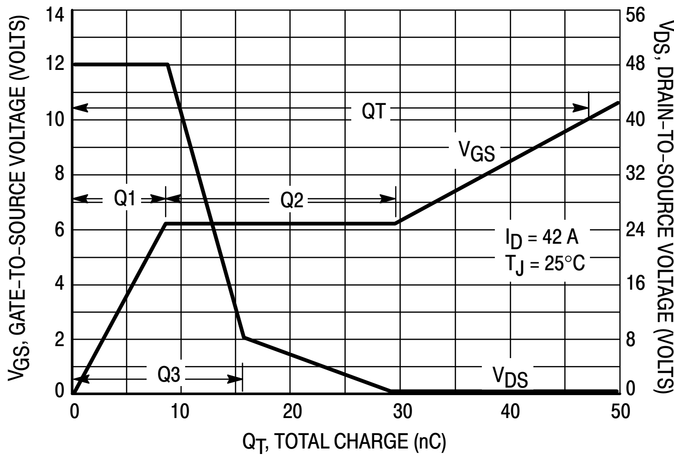



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

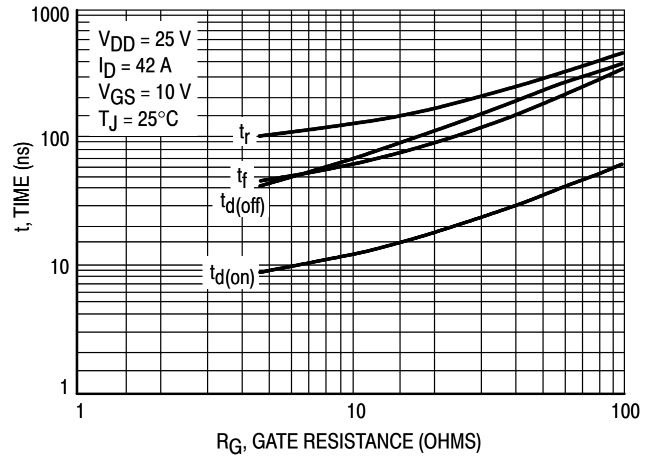



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

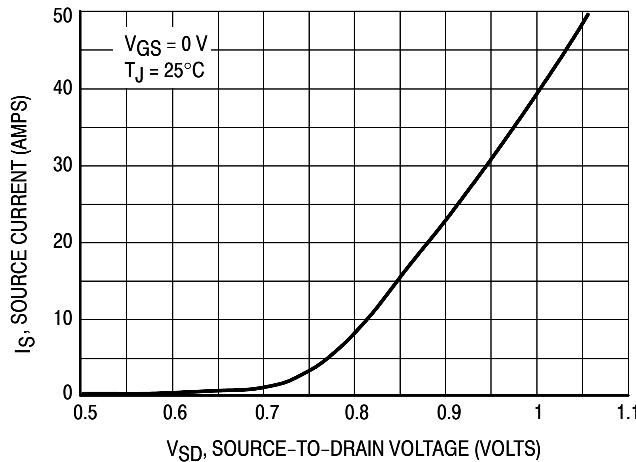



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

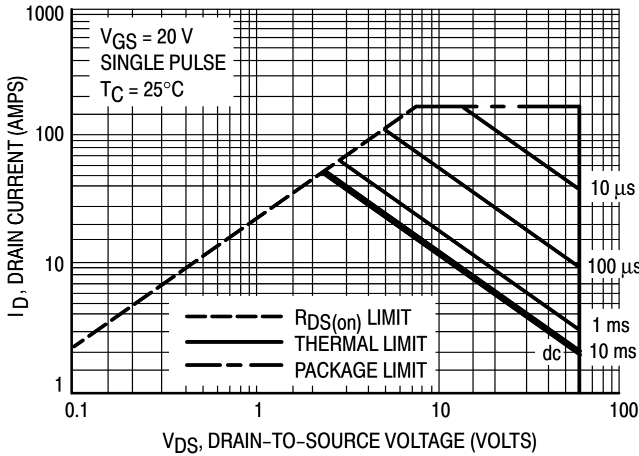



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

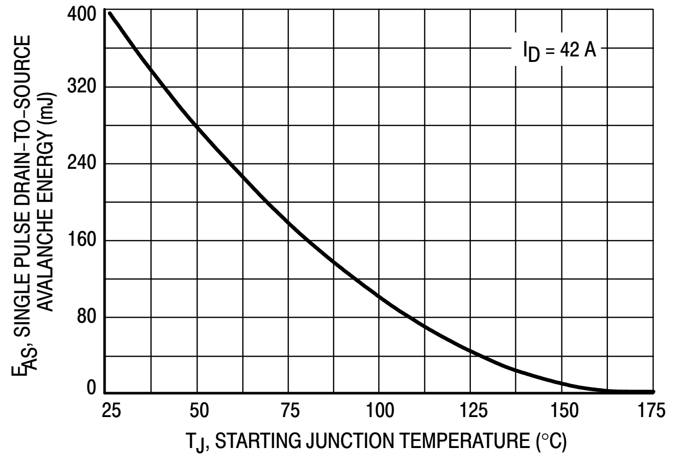



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

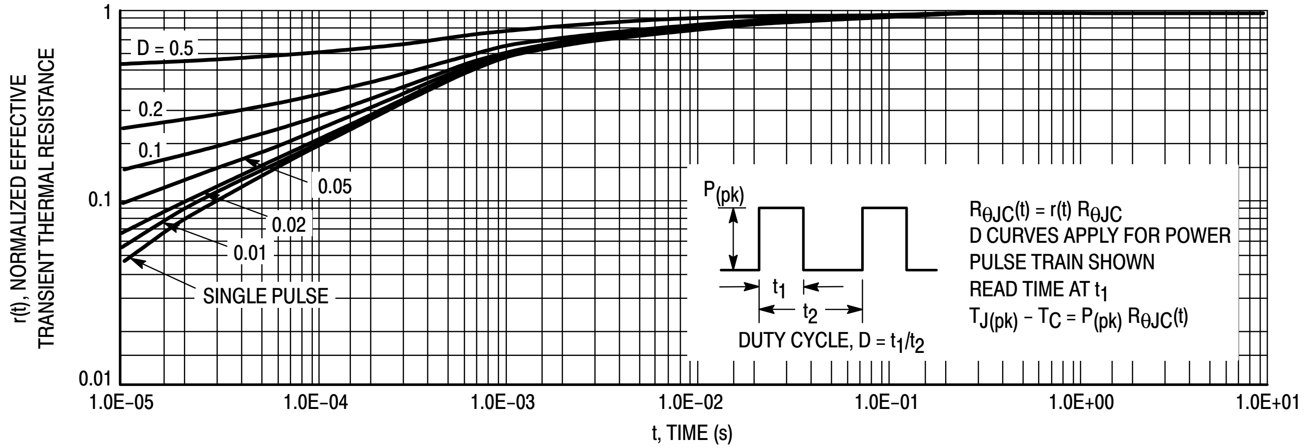



**Figure 13. Thermal Response**

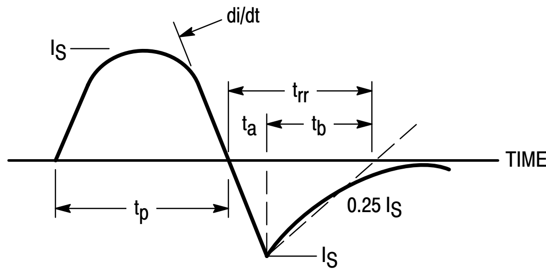



**Figure 14. Diode Reverse Recovery Waveform**

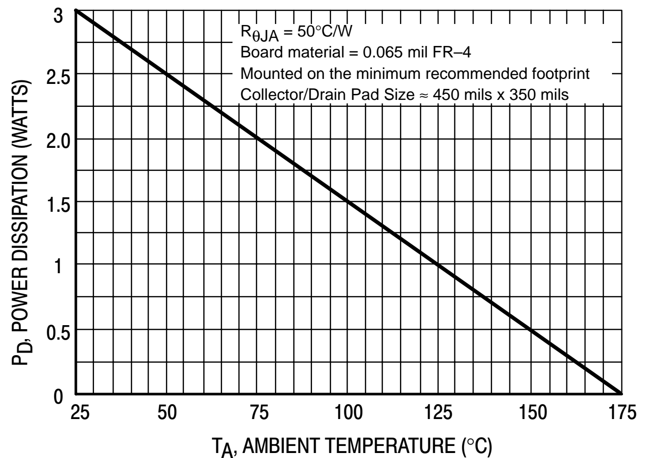
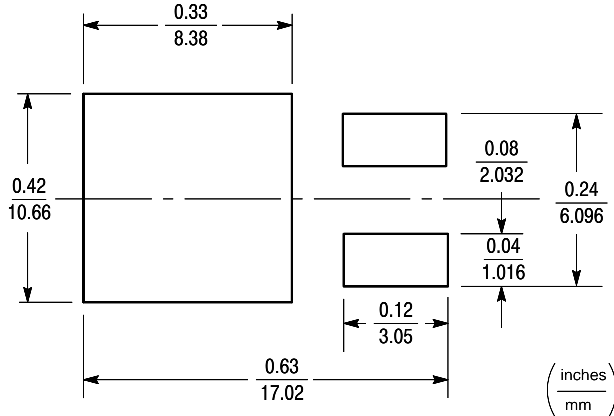



**Figure 15. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a $D^2PAK$ device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the $D^2PAK$ package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

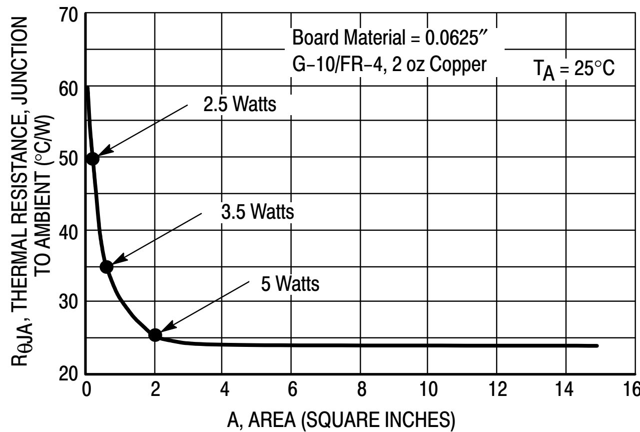



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

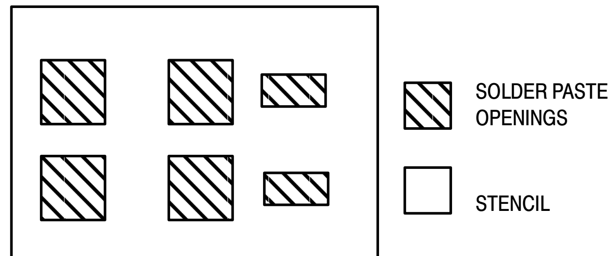



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

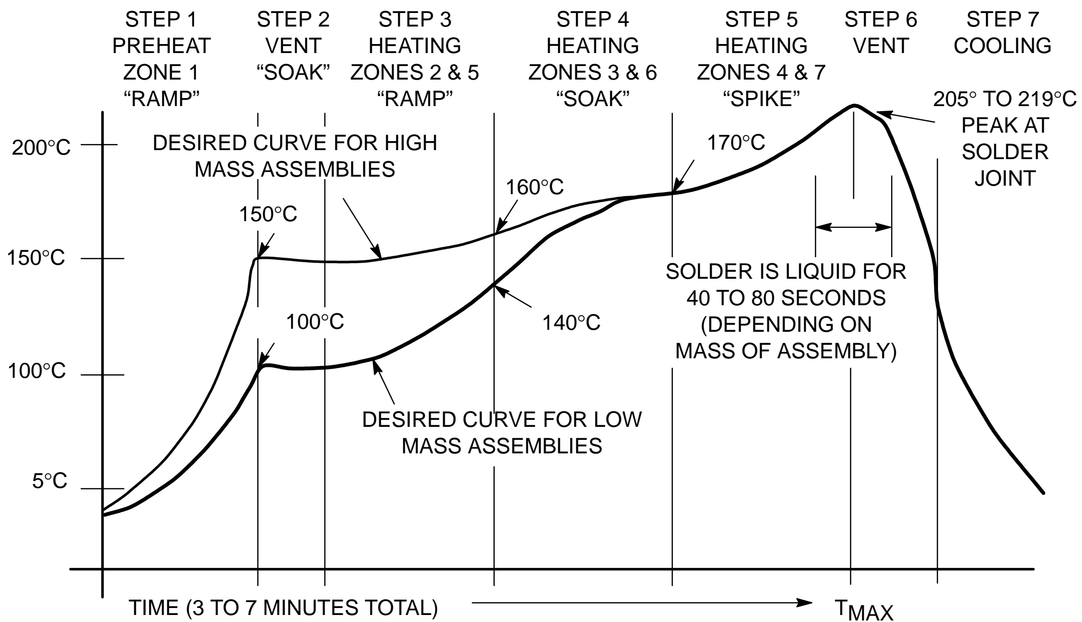



**Figure 18. Typical Solder Heating Profile**

# MTB50N06VL

**Preferred Device**

# Power MOSFET 42 Amps, 60 Volts, Logic Level

## N–Channel $D^2PAK$

**ON Semiconductor™**

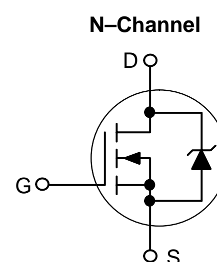
**http://onsemi.com**

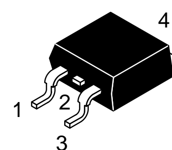
**42 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 32 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**N–Channel**



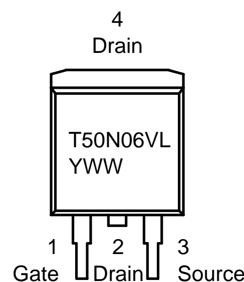

**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>±20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 42<br>30<br>147 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>0.83<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 42 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 265 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.2<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**MARKING DIAGRAM & PIN ASSIGNMENT**




T50N06VL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB50N06VL | $D^2PAK$ | 50 Units/Rail |
| MTB50N06VLT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = .25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>64 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.4<br>4.3 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5 Vdc, $I_D$ = 21 Adc) | | $R_{DS(on)}$ | – | 0.025 | 0.032 | Ohms |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5 Vdc, $I_D$ = 42 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 21 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.2<br>– | 1.6<br>1.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 28 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1570 | 2200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 508 | 710 | |
| Transfer Capacitance | | $C_{rss}$ | – | 135 | 270 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 16 | 30 | ns |
| Rise Time | | $t_r$ | – | 355 | 701 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 80 | 160 | |
| Fall Time | | $t_f$ | – | 160 | 320 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 40 | 60 | nC |
| | | $Q_1$ | – | 11 | – | |
| | | $Q_2$ | – | 20 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.03<br>0.94 | 2.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 91.1 | – | ns |
| | | $t_a$ | – | 63.8 | – | |
| | | $t_b$ | – | 27.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.299 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

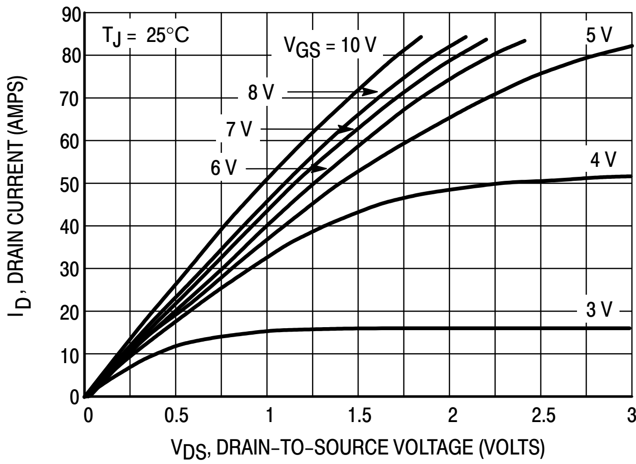



**Figure 1. On–Region Characteristics**

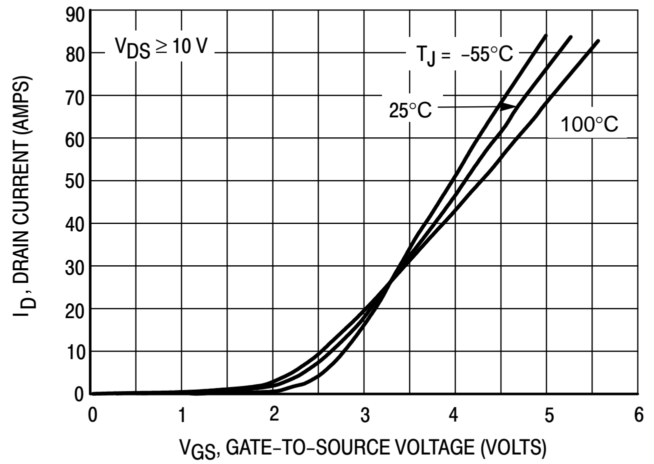



**Figure 2. Transfer Characteristics**

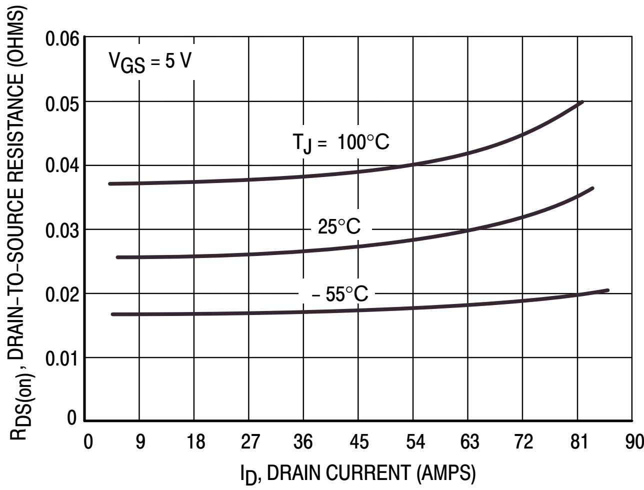



**Figure 3. On–Resistance versus Drain Current and Temperature**

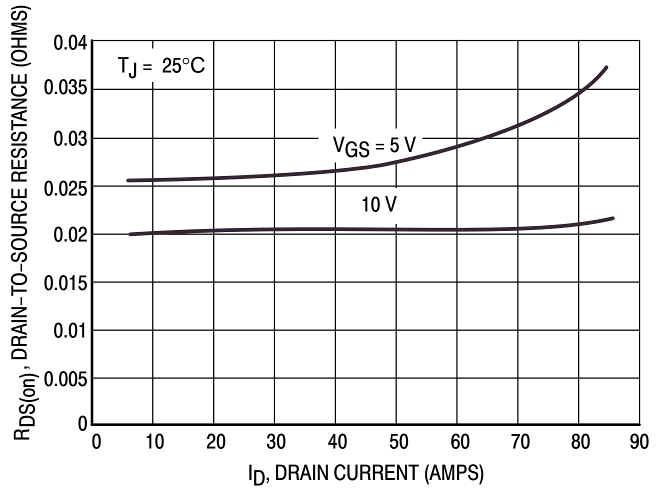



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

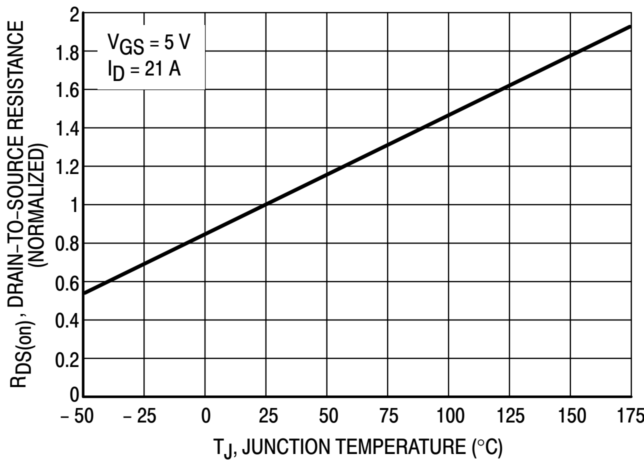



**Figure 5. On–Resistance Variation with Temperature**

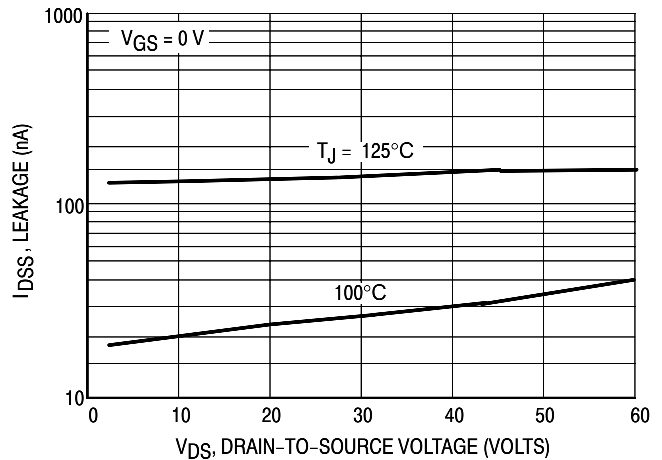



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

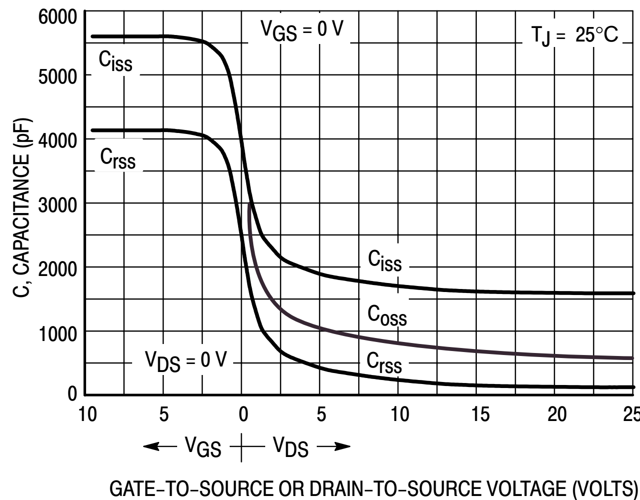



**Figure 7. Capacitance Variation**

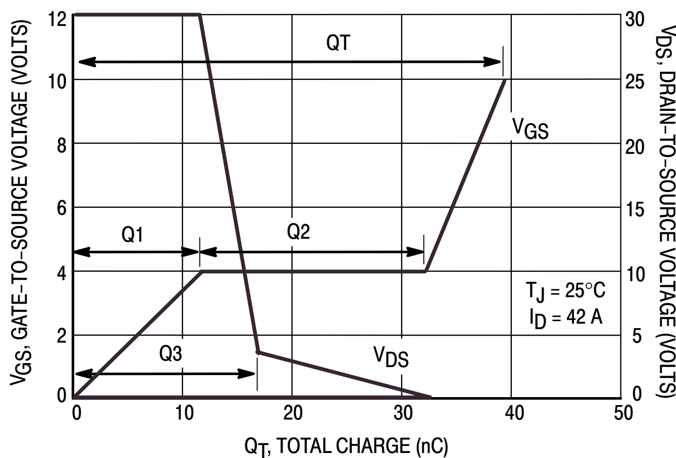



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

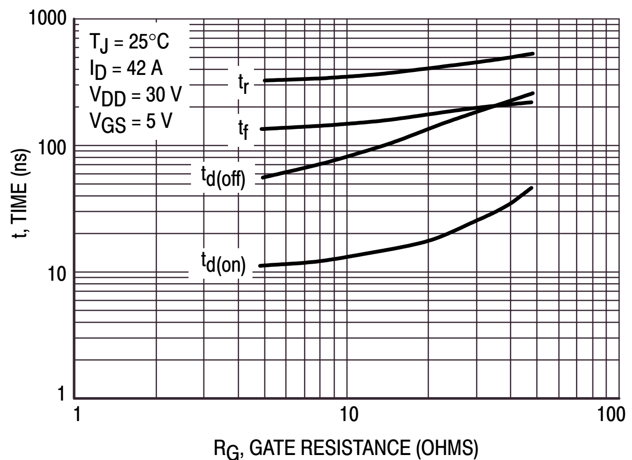



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

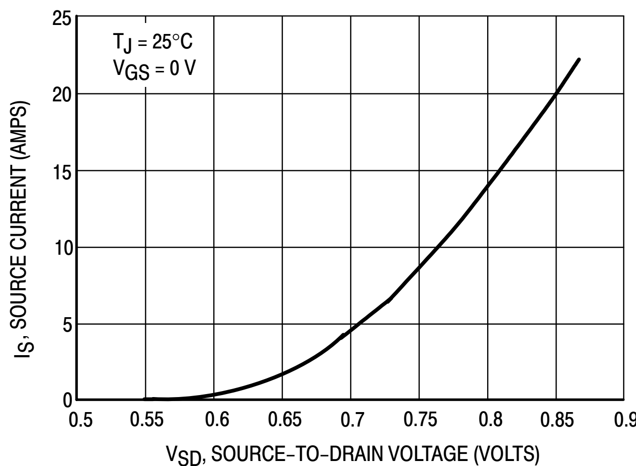



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

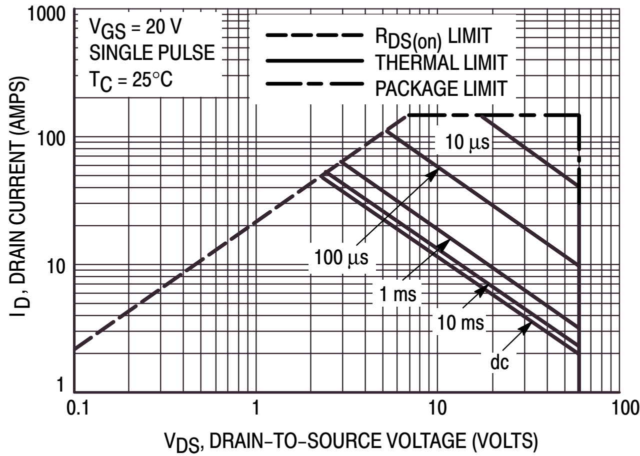



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

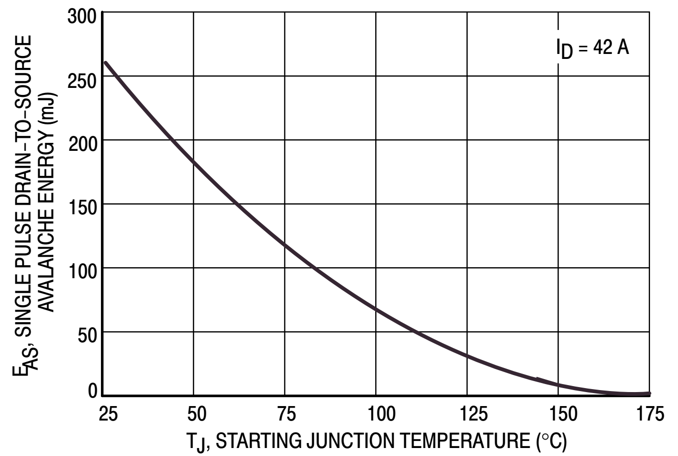



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

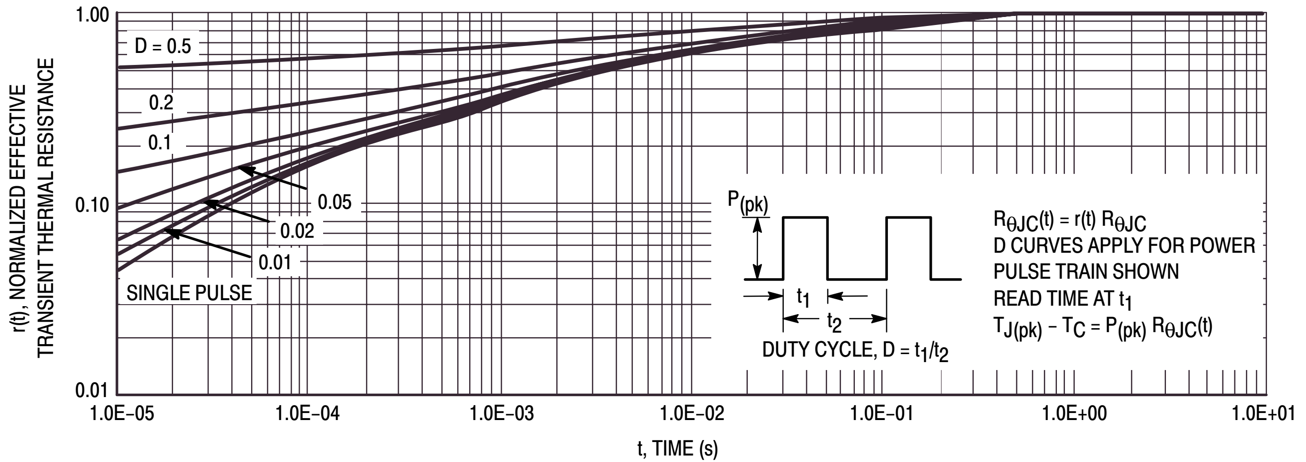



**Figure 13. Thermal Response**

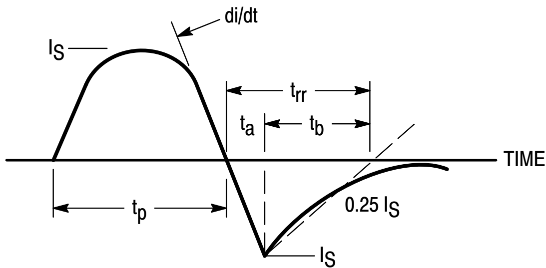



**Figure 14. Diode Reverse Recovery Waveform**

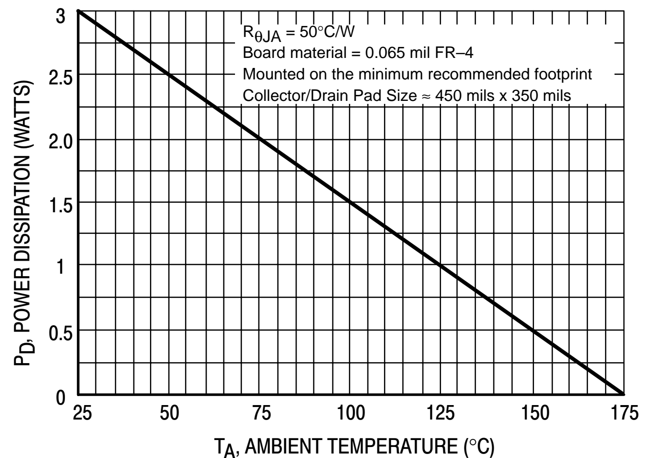
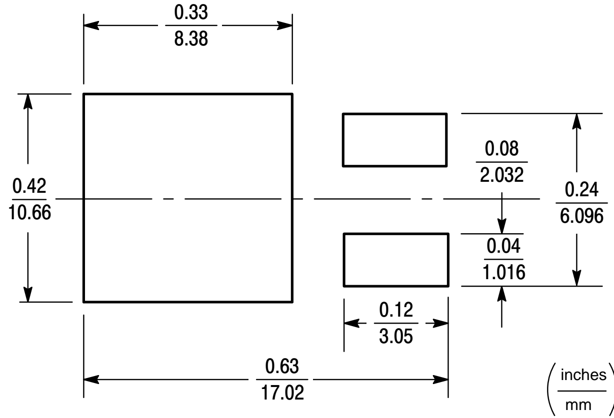



**Figure 15. D2PAK Power Derating Curve**

# INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

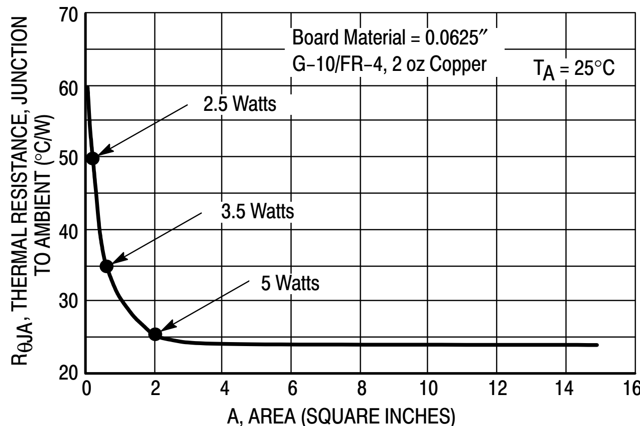



**Figure 16. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

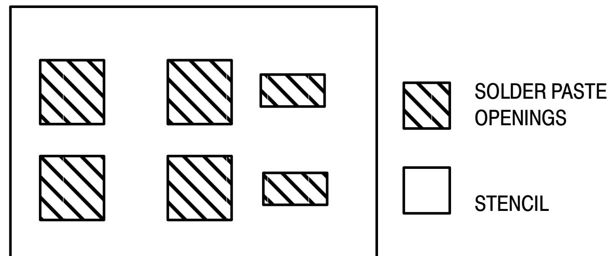



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

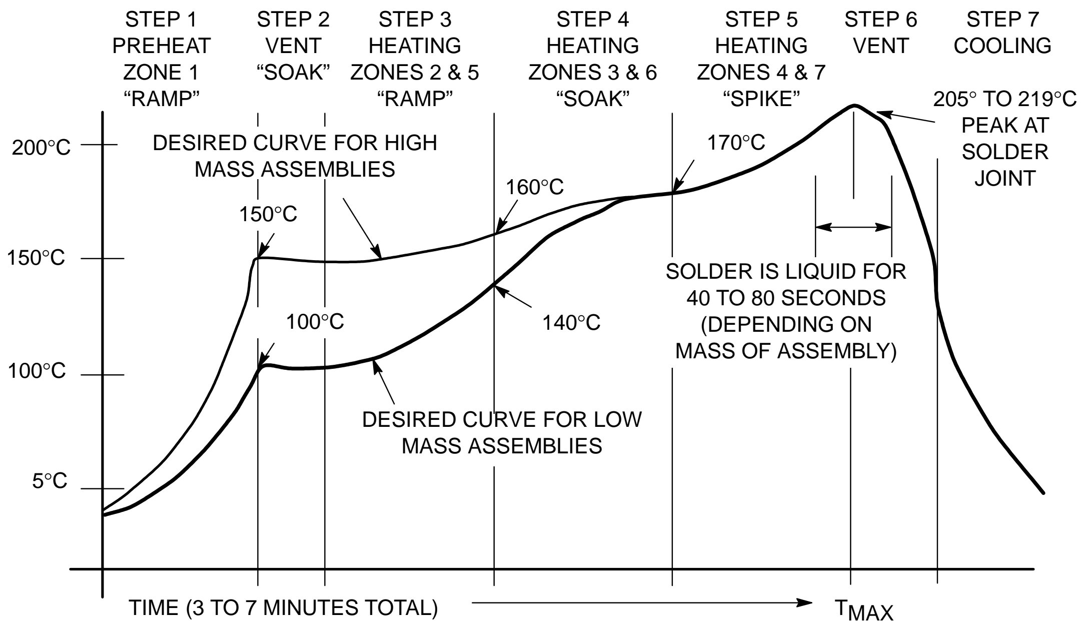



**Figure 18. Typical Solder Heating Profile**

# MTB50P03HDL

**Preferred Device**

# Power MOSFET 50 Amps, 30 Volts, Logic Level

## P–Channel $D^2PAK$

**ON Semiconductor**™

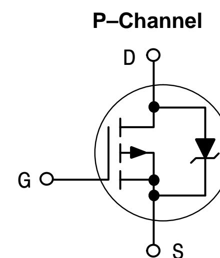
**http://onsemi.com**

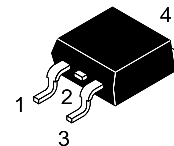
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**50 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 25 mΩ**

**P–Channel**



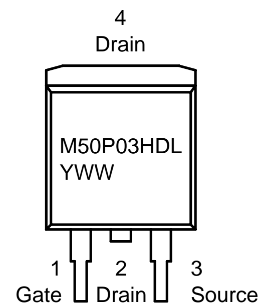




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 50<br>31<br>150 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C, when mounted with the minimum recommended pad size | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 50 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 1250 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




M50P03HDL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB50P03HDL | $D^2PAK$ | 50 Units/Rail |
| MTB50P03HDLT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>26 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 25 Adc) | $R_{DS(on)}$ | – | 20.9 | 25 | mOhm |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 50 Adc)<br>($I_D$ = 25 Adc, $T_J$ =125°C) | $V_{DS(on)}$ | <br>–<br>– | <br>0.83<br>– | <br>1.5<br>1.3 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 5.0 Vdc, $I_D$ = 25 Adc) | $g_{FS}$ | 15 | 20 | – | mhos |

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3500 | 4900 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1550 | 2170 | |
| Transfer Capacitance | | $C_{rss}$ | – | 550 | 770 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$= 15 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 22 | 30 | ns |
| Rise Time | | $t_r$ | – | 340 | 466 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 90 | 117 | |
| Fall Time | | $t_f$ | – | 218 | 300 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 24 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 74 | 100 | nC |
| | | $Q_1$ | – | 13.6 | – | |
| | | $Q_2$ | – | 44.8 | – | |
| | | $Q_3$ | – | 35 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 50 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 50 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 2.39<br>1.84 | 3.0<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 15) | ($I_S$ = 50 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 106 | – | ns |
| | | $t_a$ | – | 58 | – | |
| | | $t_b$ | – | 48 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.246 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

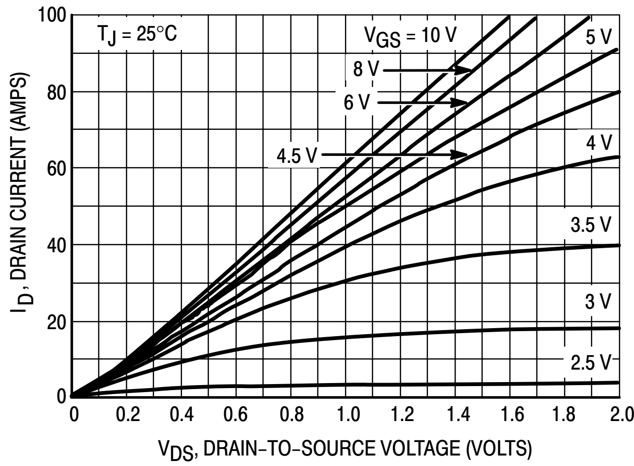



**Figure 1. On–Region Characteristics**

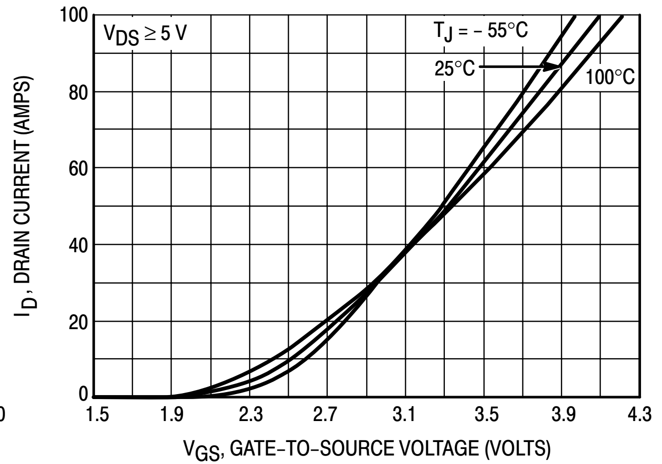



**Figure 2. Transfer Characteristics**

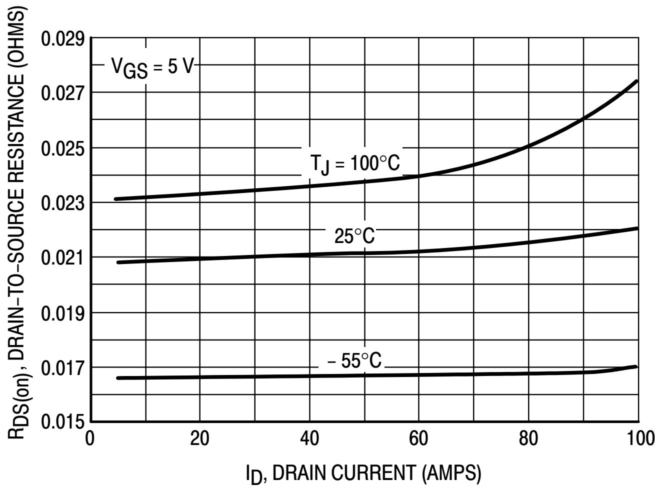



**Figure 3. On–Resistance versus Drain Current and Temperature**

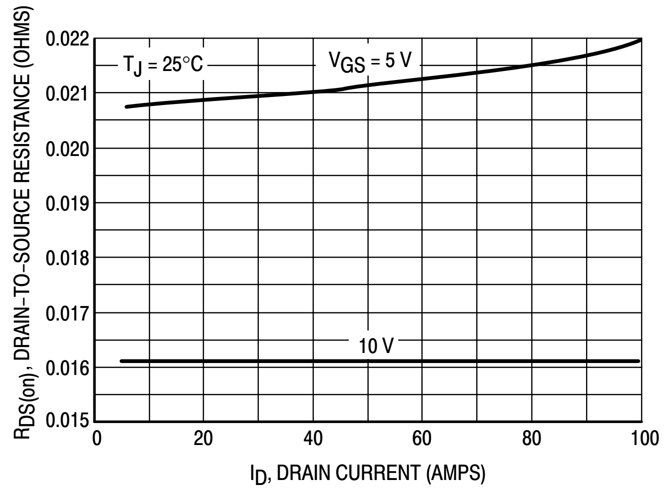



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

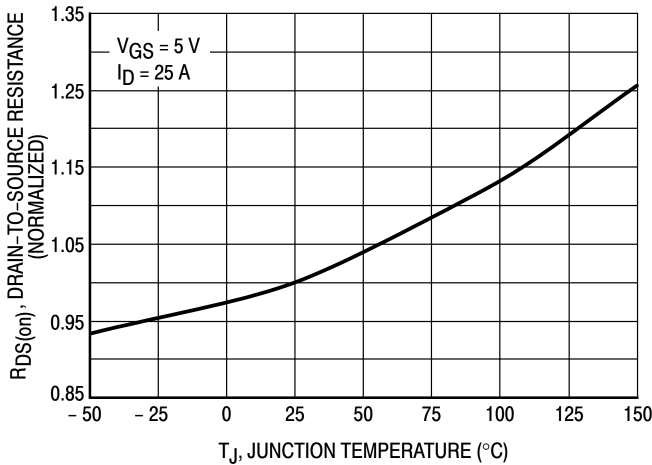



**Figure 5. On–Resistance Variation with Temperature**

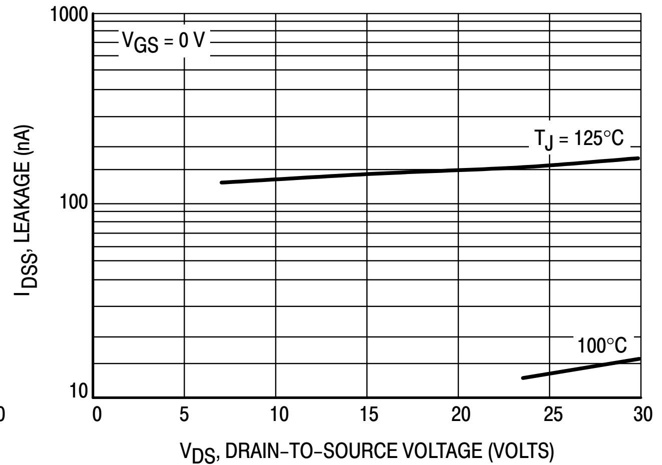



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

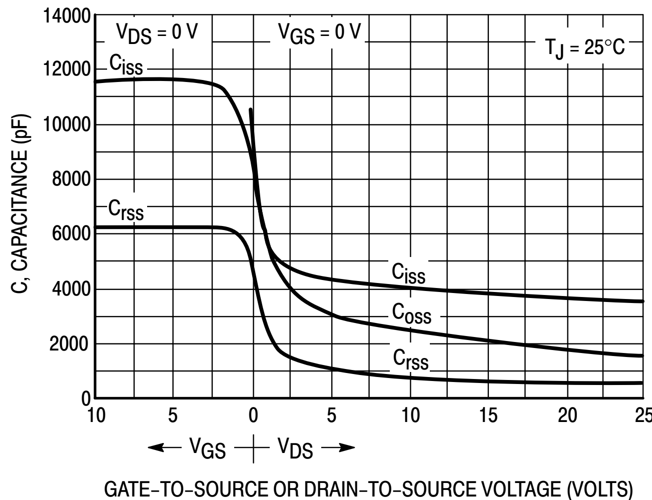



**Figure 7. Capacitance Variation**

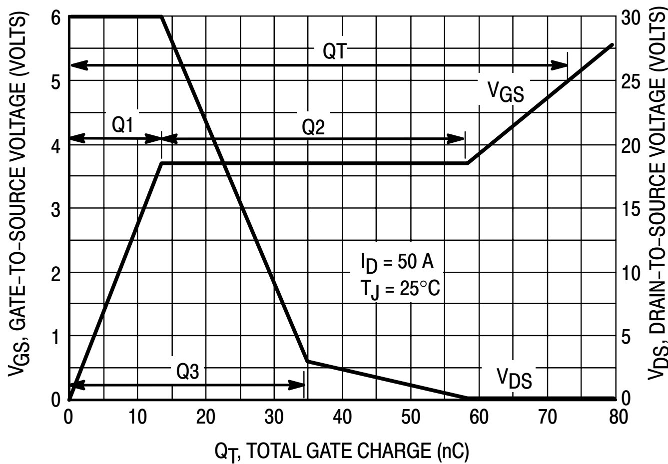



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

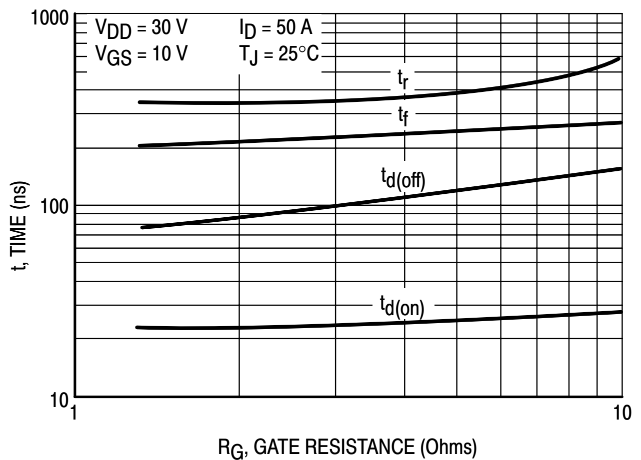



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

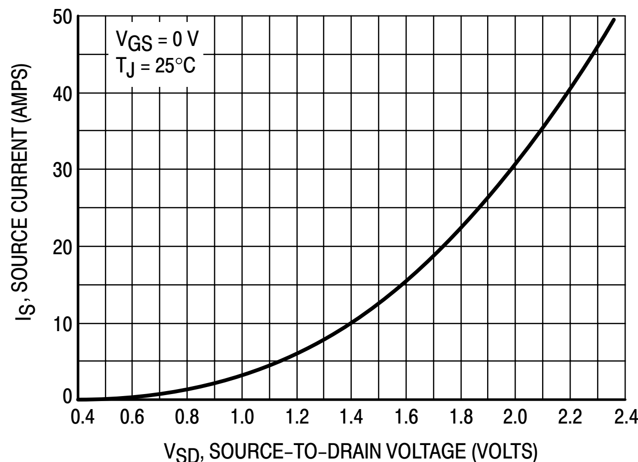



**Figure 10. Diode Forward Voltage versus Current**

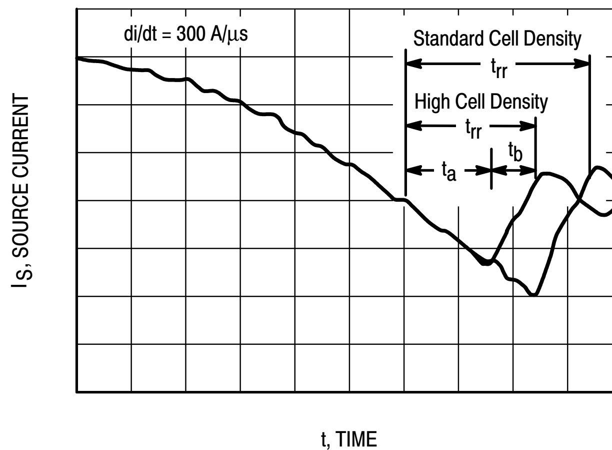



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

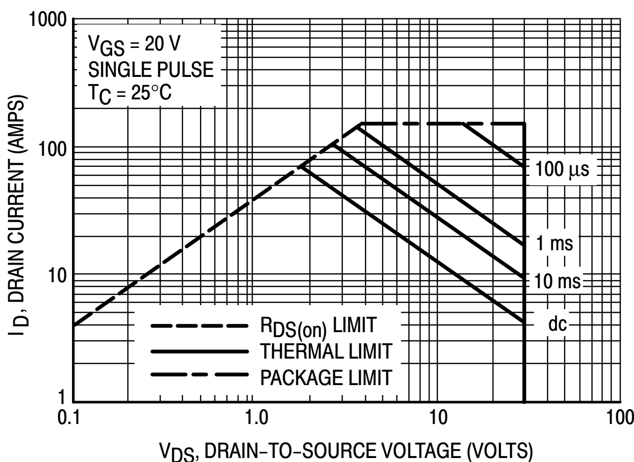



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

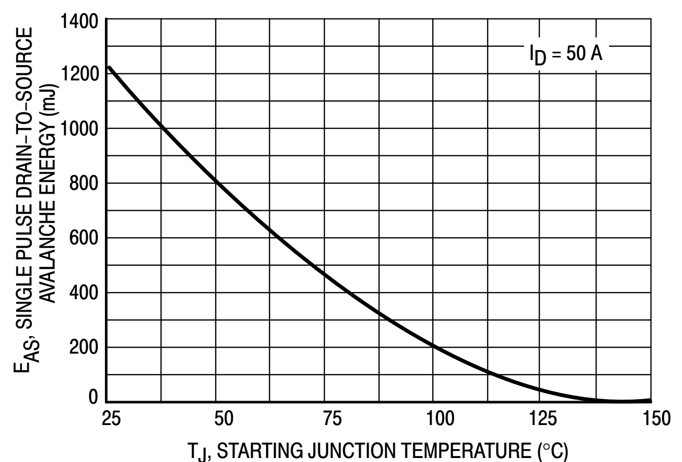



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

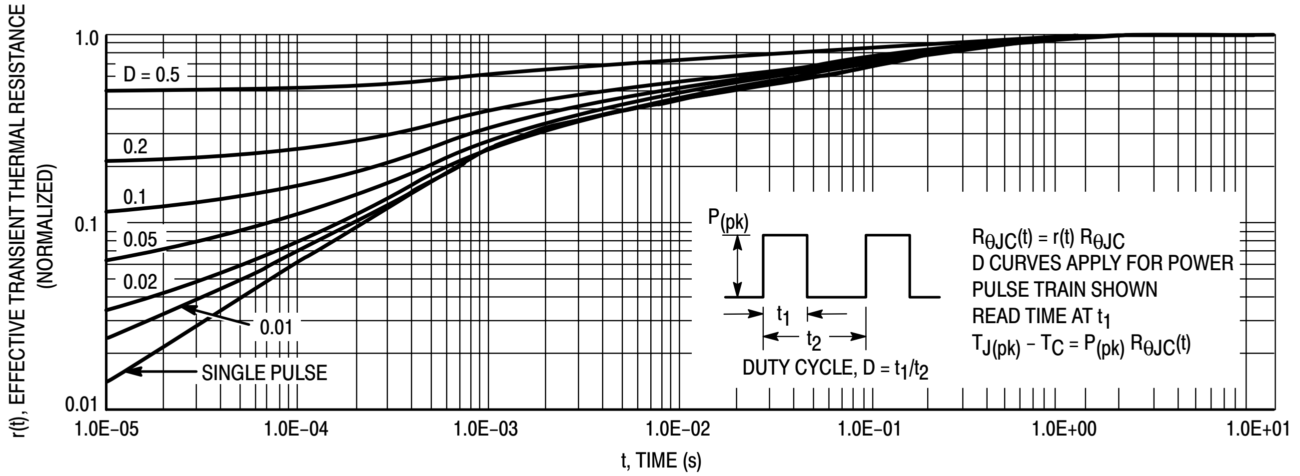



**Figure 14. Thermal Response**

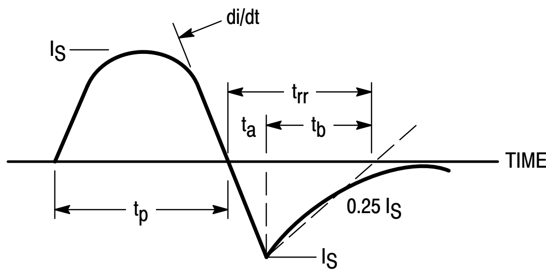



**Figure 15. Diode Reverse Recovery Waveform**

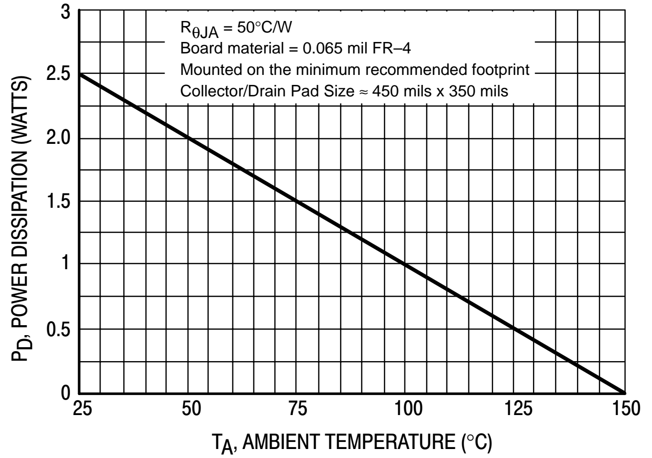
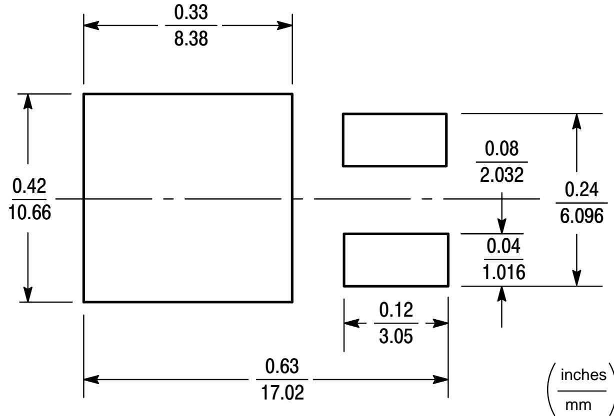



**Figure 16. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

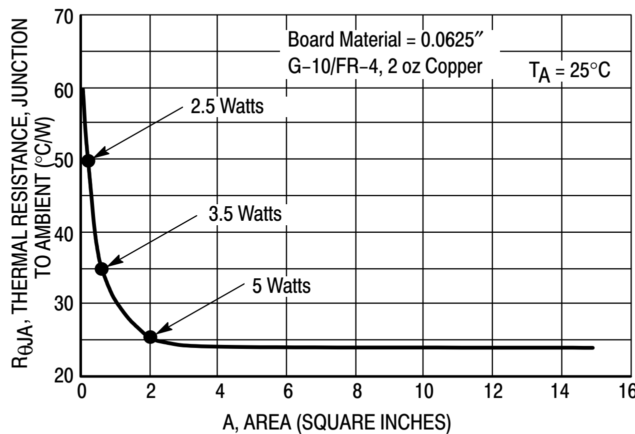



**Figure 17. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D$^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 18 shows a typical stencil for the DPAK and D$^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

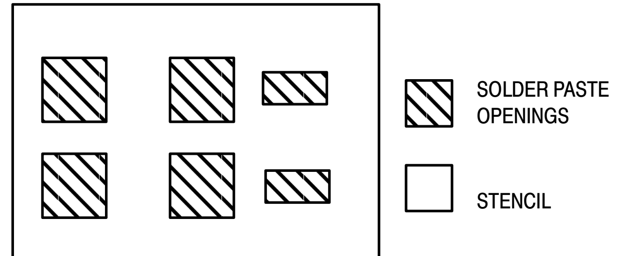



**Figure 18. Typical Stencil for DPAK and D$^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D$^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 19 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

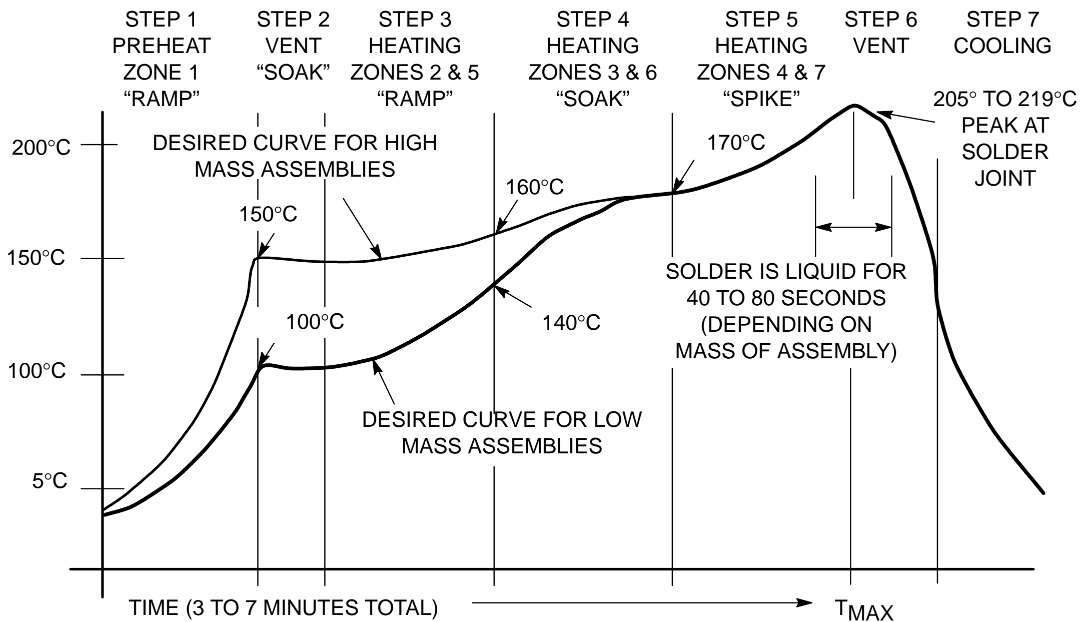



**Figure 19. Typical Solder Heating Profile**

# MTB52N06V

**Preferred Device**

# Power MOSFET 52 Amps, 60 Volts

## N–Channel $D^2PAK$

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 52<br>41<br>182 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 188<br>1.25<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 52 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 406 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>0.8<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

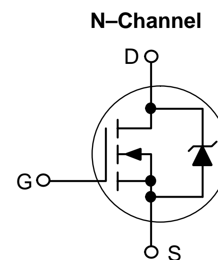
1. When surface mounted to an FR4 board using the minimum recommended pad size.

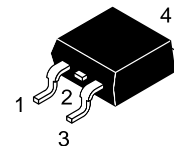
**ON Semiconductor™**

**http://onsemi.com**

**52 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 22 mΩ**

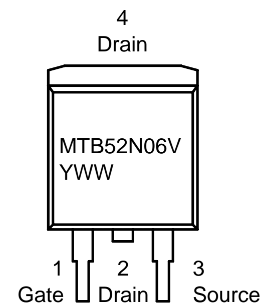
**N–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB52N06V = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB52N06V | $D^2PAK$ | 50 Units/Rail |
| MTB52N06VT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 4

Publication Order Number:
MTB52N06V/D

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>66 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.7<br>6.4 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 26 Adc) | | $R_{DS(on)}$ | – | 0.019 | 0.022 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 52 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 26 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.4<br>1.2 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.3 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 24 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1900 | 2660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 580 | 810 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 150 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 20 | ns |
| Rise Time | | $t_r$ | – | 298 | 600 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 70 | 140 | |
| Fall Time | | $t_f$ | – | 110 | 220 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 125 | 175 | nC |
| | | $Q_1$ | – | 10 | – | |
| | | $Q_2$ | – | 30 | – | |
| | | $Q_3$ | – | 40 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>–<br>– | <br>1.0<br>0.98 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 14) | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 100 | – | ns |
| | | $t_a$ | – | 80 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.341 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

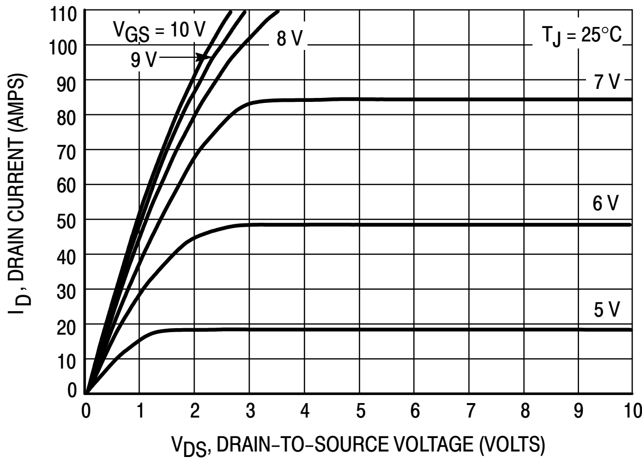



**Figure 1. On−Region Characteristics**

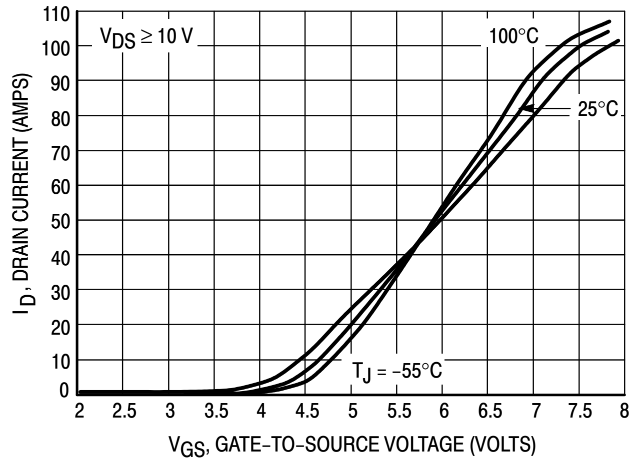



**Figure 2. Transfer Characteristics**

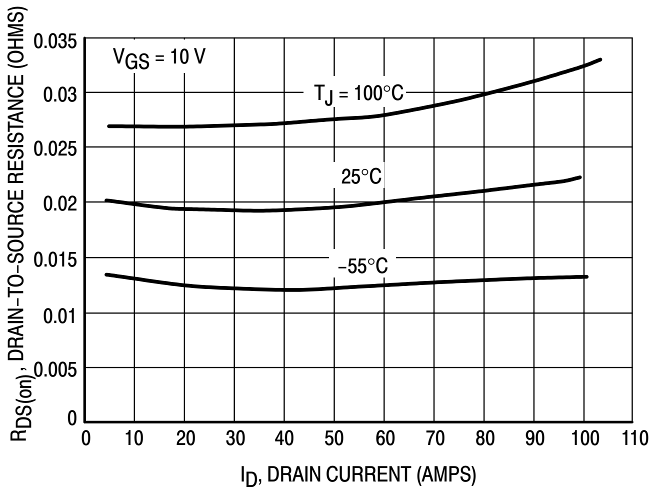



**Figure 3. On−Resistance versus Drain Current and Temperature**

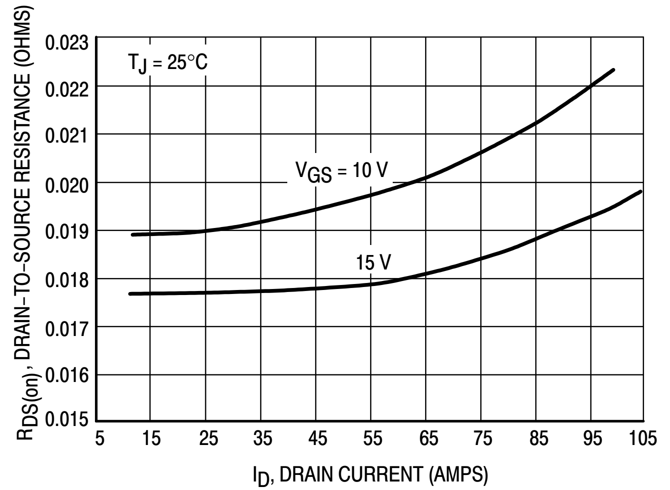



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

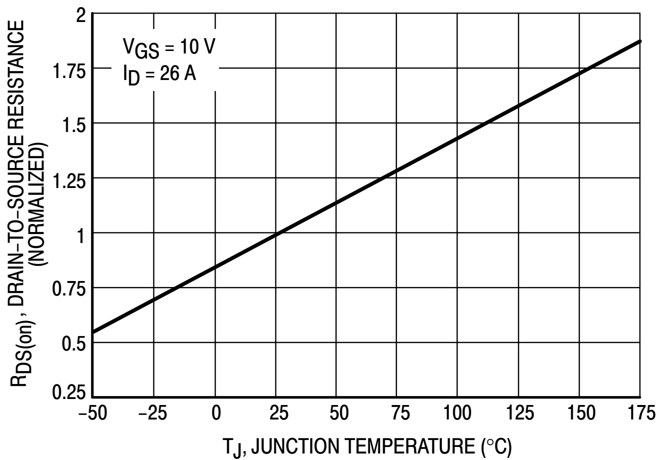



**Figure 5. On−Resistance Variation with Temperature**

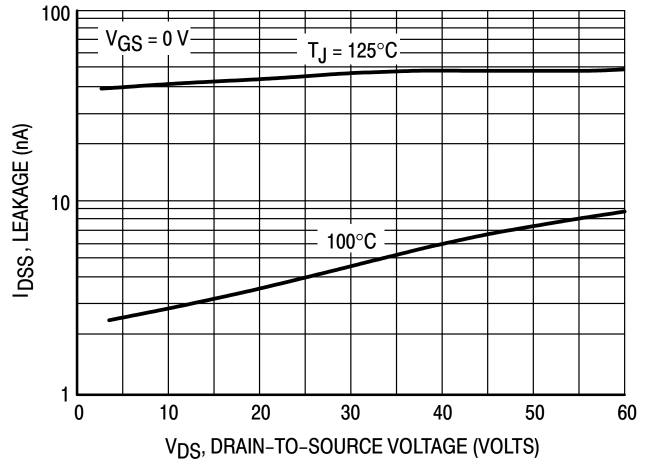



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \text{In} \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \text{In} \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

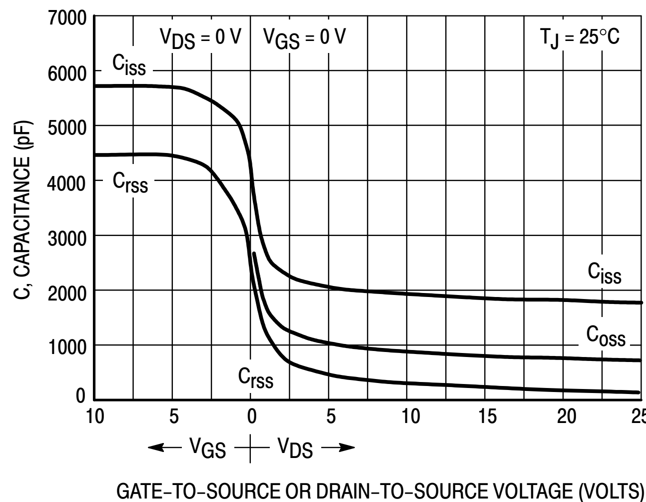



**Figure 7. Capacitance Variation**

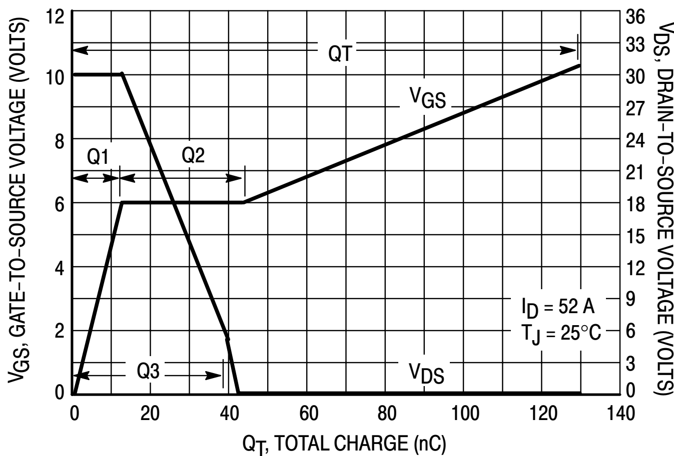



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

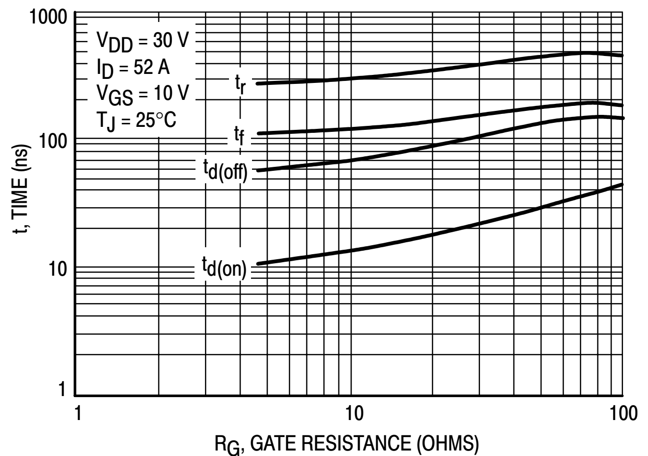



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

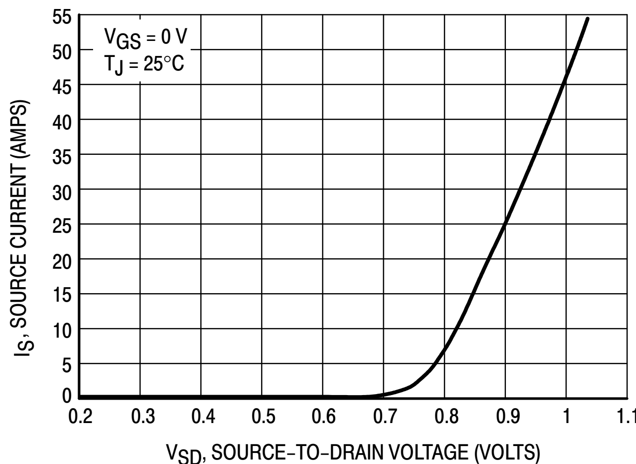



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

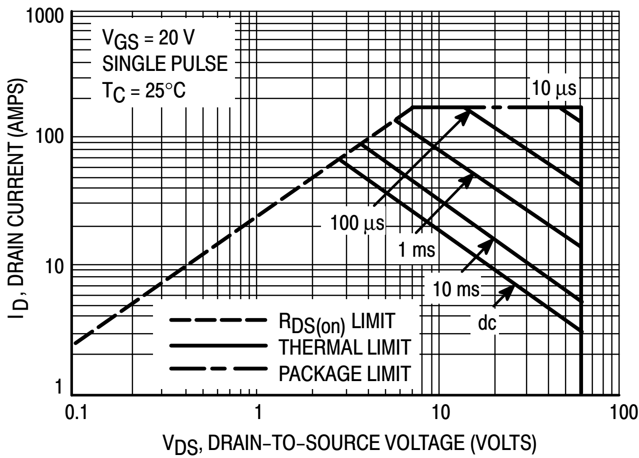



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

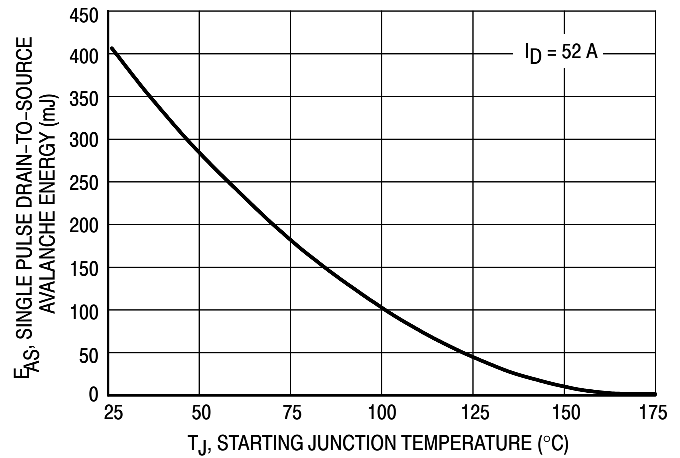



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

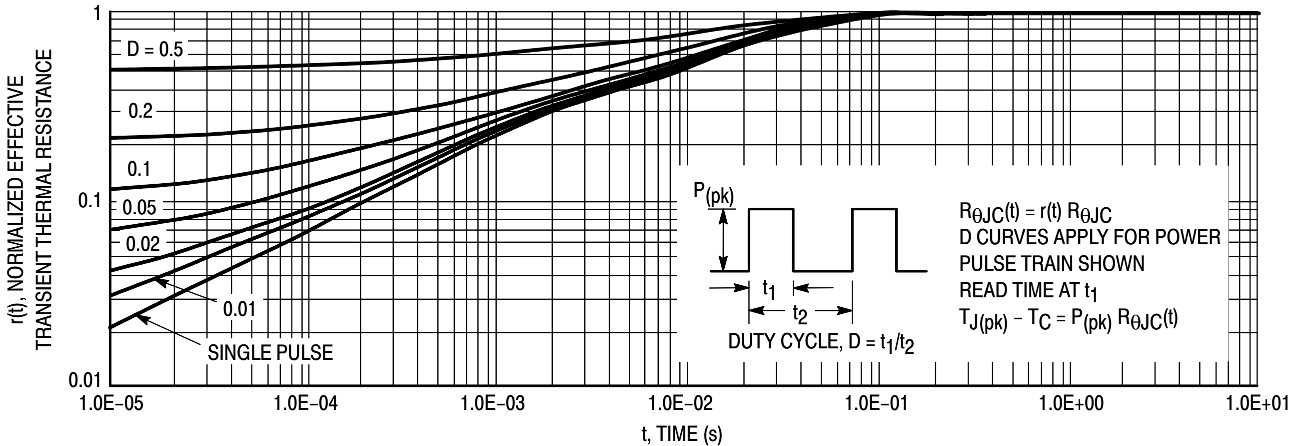



**Figure 13. Thermal Response**

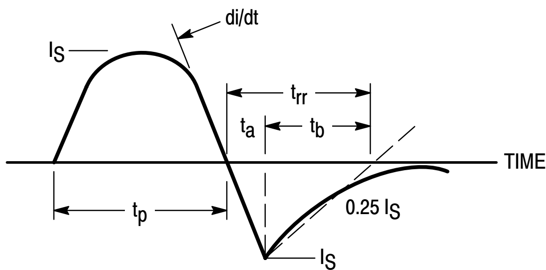



**Figure 14. Diode Reverse Recovery Waveform**

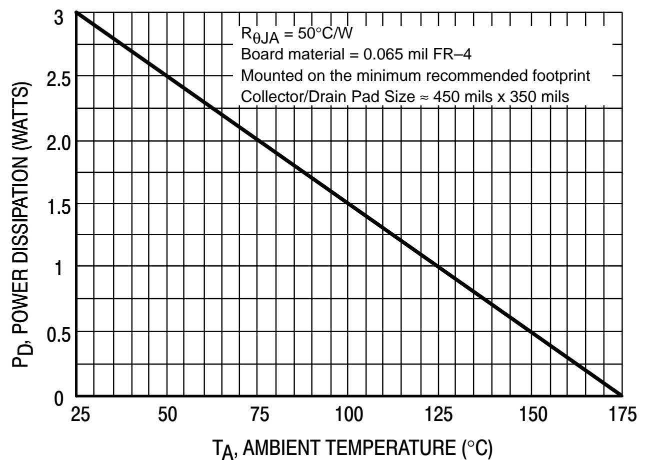
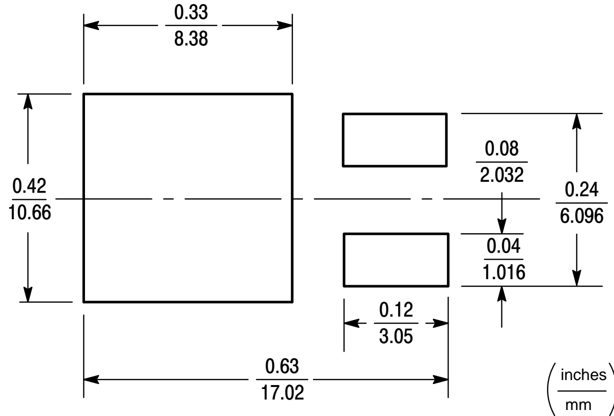



**Figure 15. $D^2$PAK Power Derating Curve**

# INFORMATION FOR USING THE D$^2$PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D$^2$PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D$^2$PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

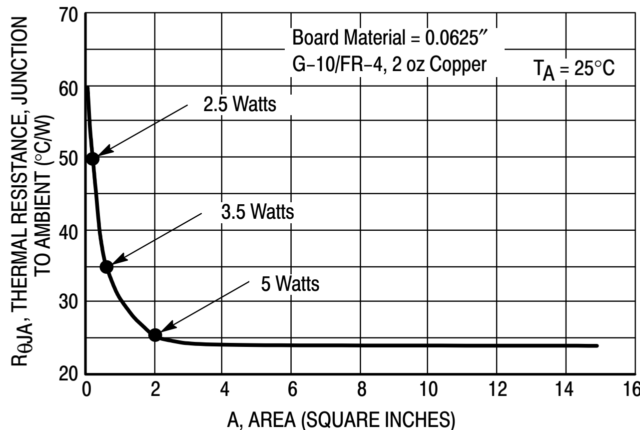



**Figure 16. Thermal Resistance versus Drain Pad Area for the D$^2$PAK Package (Typical)**

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

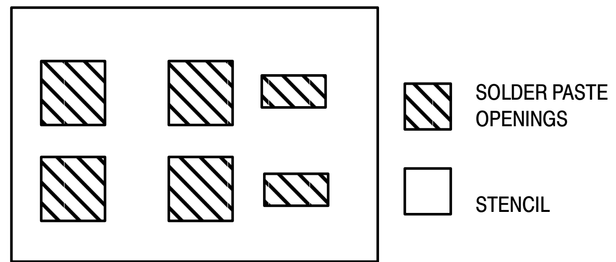



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

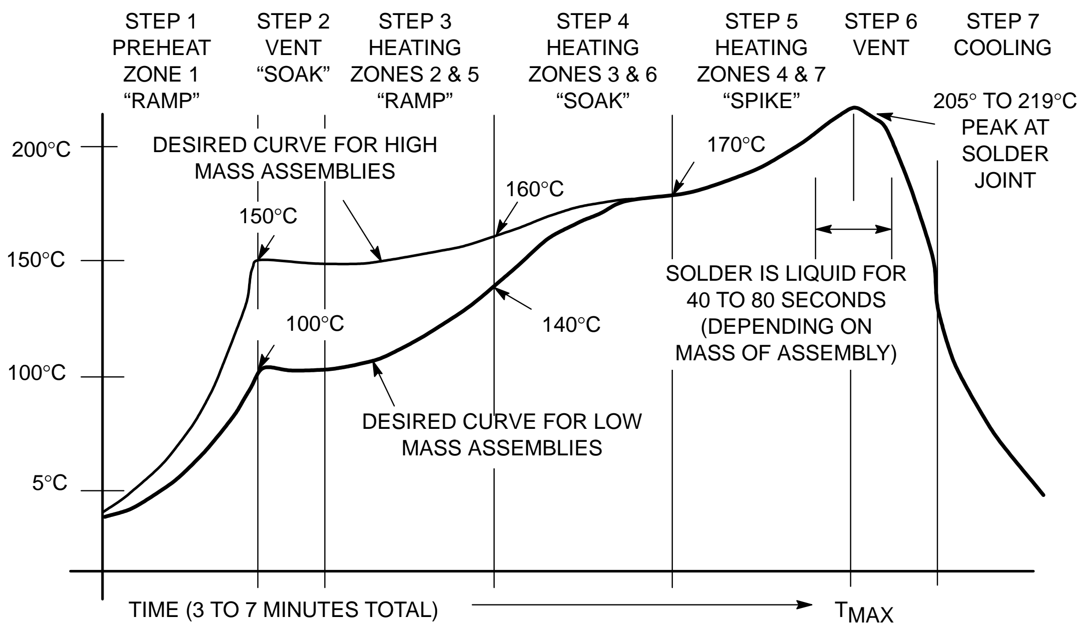



**Figure 18. Typical Solder Heating Profile**

# MTB52N06VL

Preferred Device

# Power MOSFET
# 52 Amps, 60 Volts, Logic Level
## N–Channel $D^2PAK$

ON Semiconductor™

http://onsemi.com

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

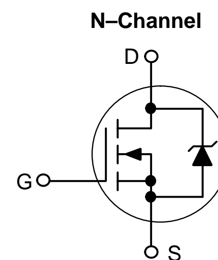
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

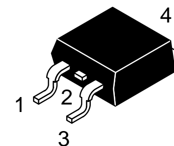
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>±25 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>52<br>41<br>182 | <br>Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 188<br>1.25<br>3.0 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 52 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 406 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>0.8<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**52 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 25 mΩ**

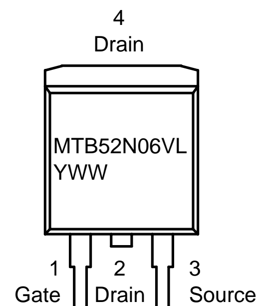
N–Channel




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB52N06VL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB52N06VL | $D^2PAK$ | 50 Units/Rail |
| MTB52N06VLT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = .25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>65 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.5 | <br>2.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 26 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.022 | <br>0.025 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5 Vdc, $I_D$ = 52 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 26 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.6<br>1.4 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.3 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 30 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1900 | 2660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 550 | 770 | |
| Transfer Capacitance | | $C_{rss}$ | – | 170 | 340 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 500 | 1000 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 100 | 200 | |
| Fall Time | | $t_f$ | – | 200 | 400 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 62 | 90 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 31 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | $V_{SD}$ | <br>–<br>– | <br>1.03<br>0.9 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 104 | – | ns |
| | | $t_a$ | – | 63 | – | |
| | | $t_b$ | – | 41 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.28 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

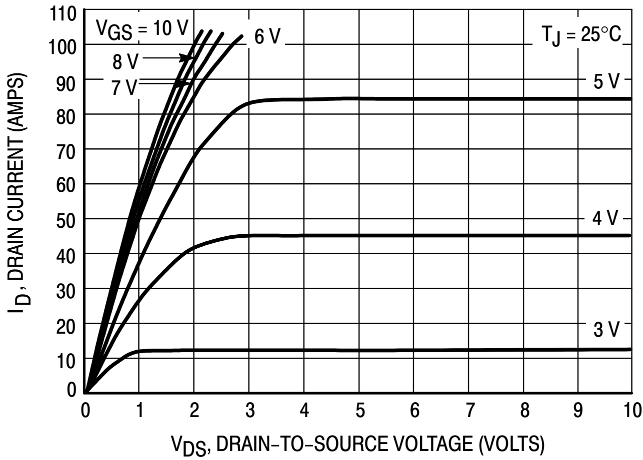



**Figure 1. On–Region Characteristics**

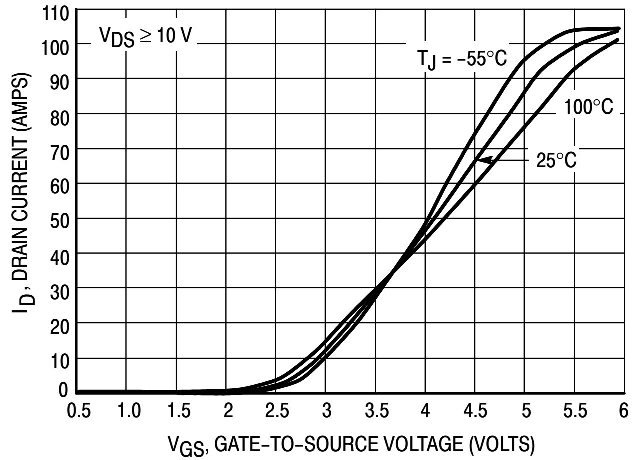



**Figure 2. Transfer Characteristics**

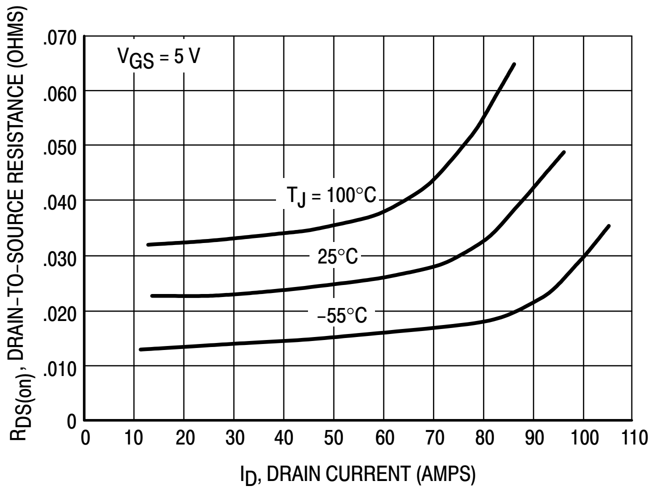



**Figure 3. On–Resistance versus Drain Current and Temperature**

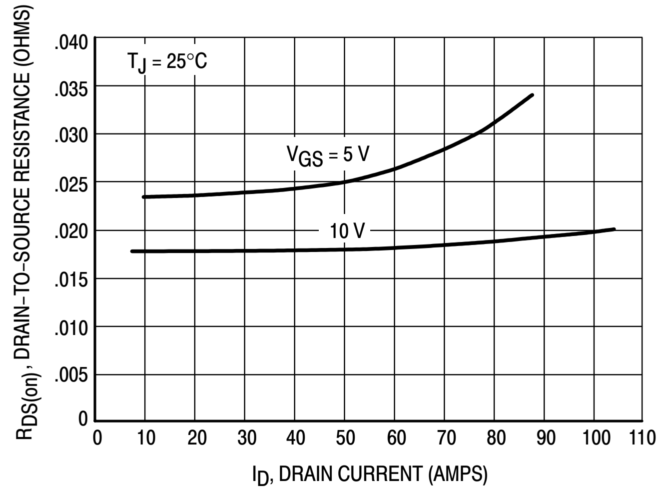



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

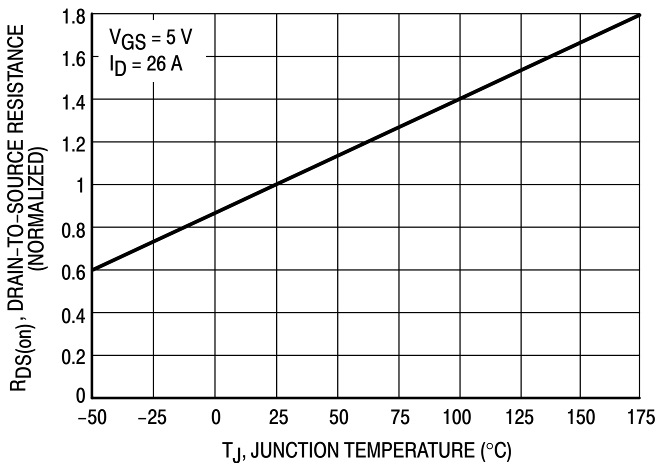



**Figure 5. On–Resistance Variation with Temperature**

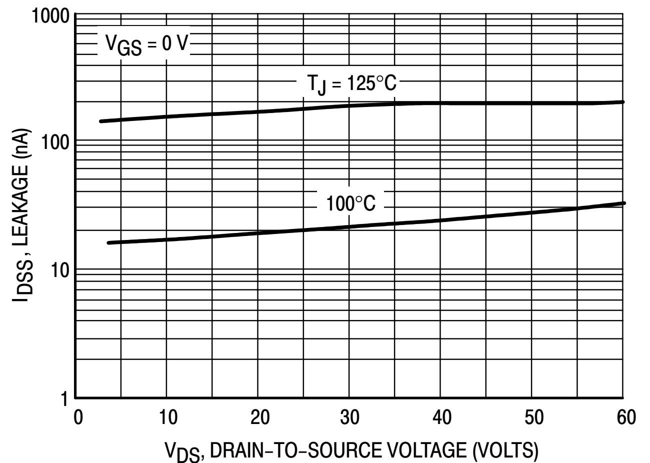



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

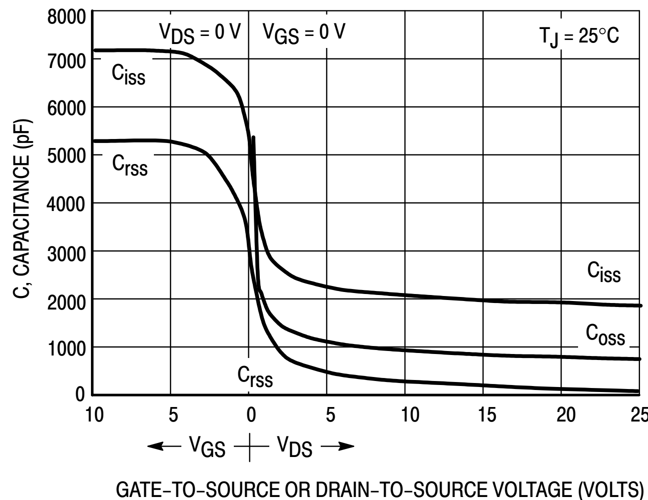



**Figure 7. Capacitance Variation**

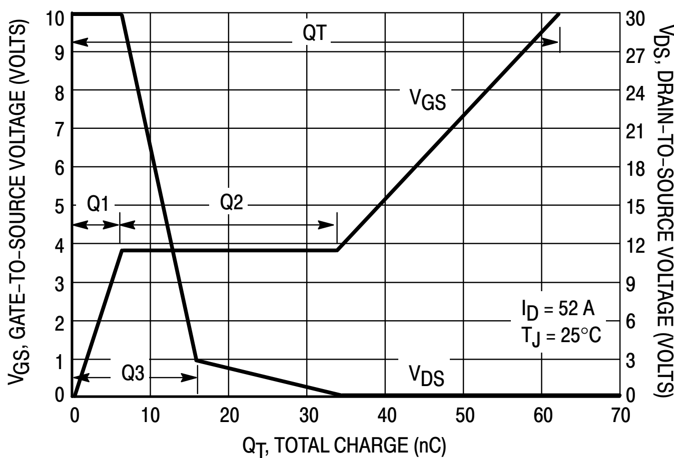



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

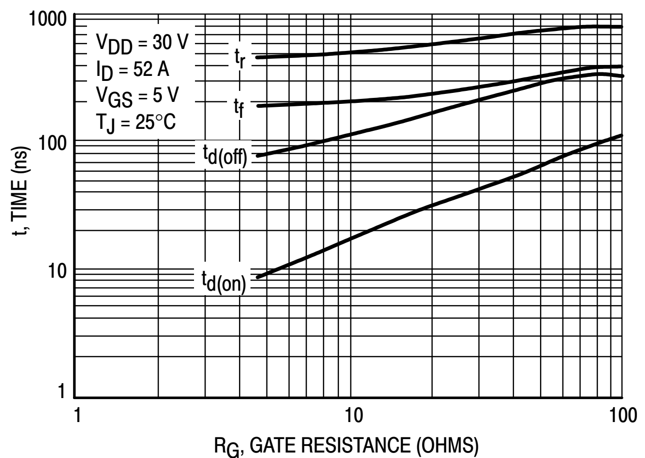



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

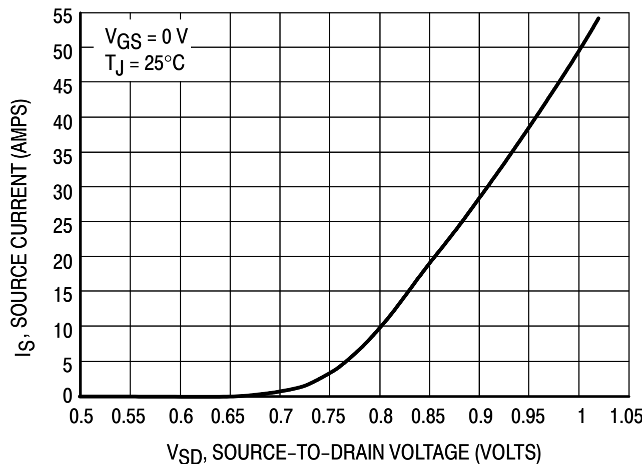



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

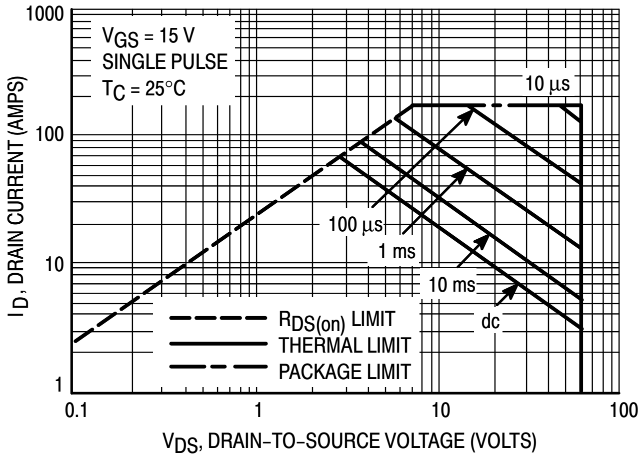



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

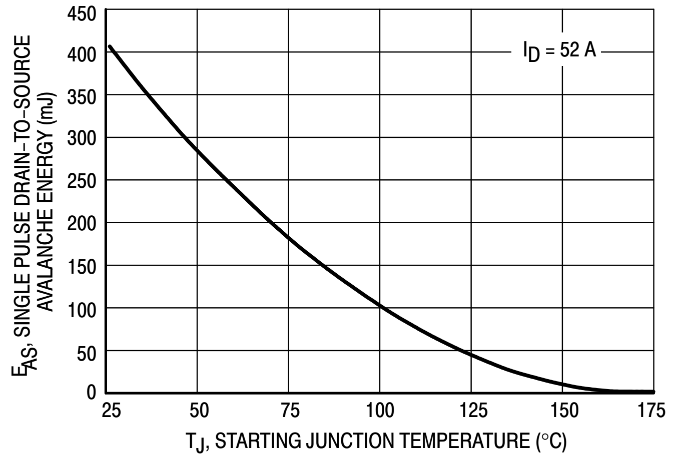



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

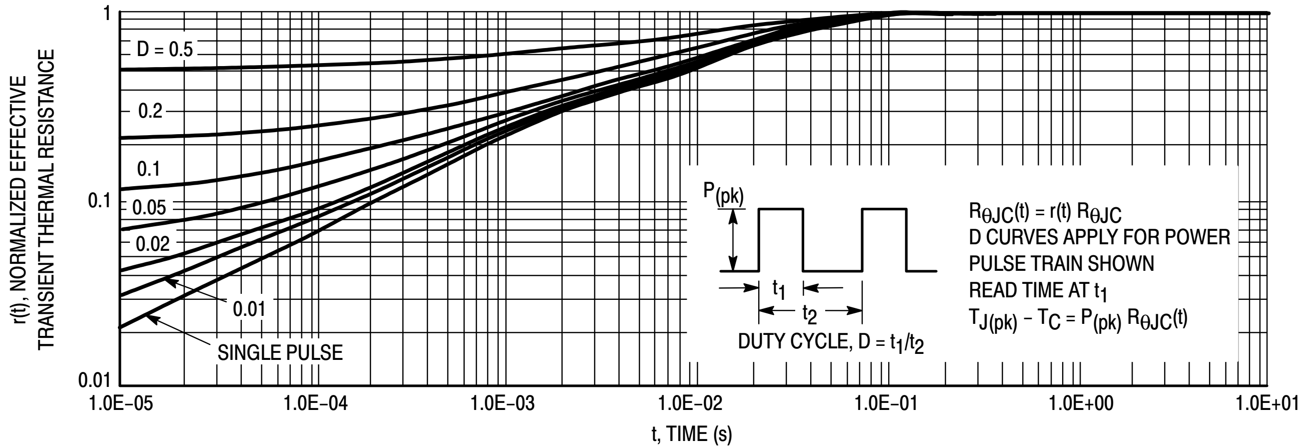



**Figure 13. Thermal Response**

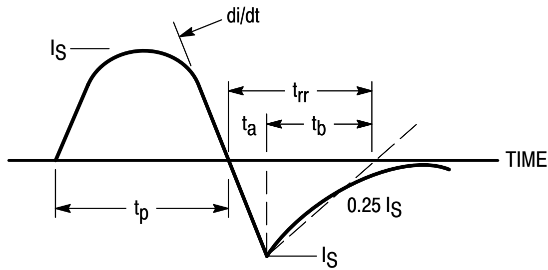



**Figure 14. Diode Reverse Recovery Waveform**

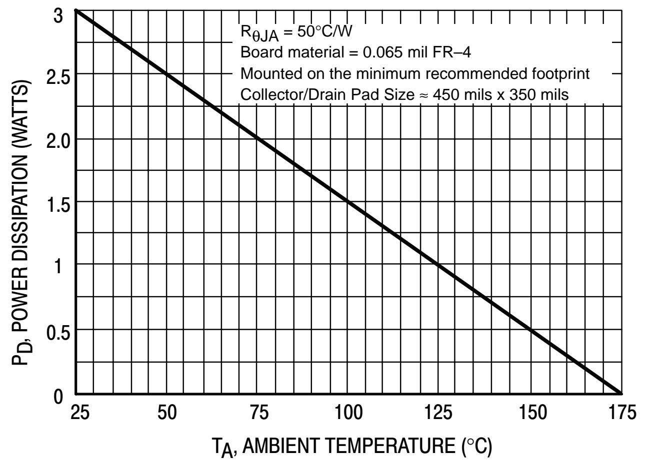
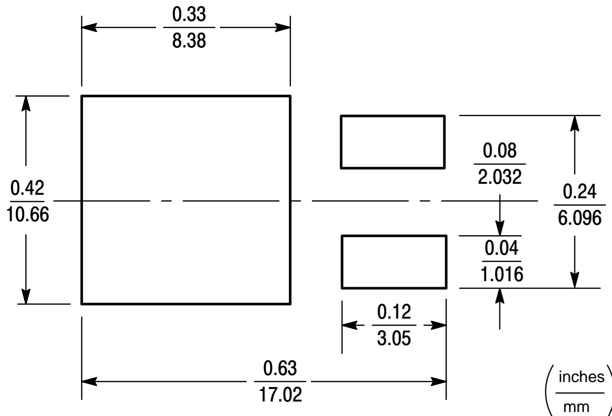



**Figure 15. D²PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{50°C/W} = 3.0 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 3.0 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

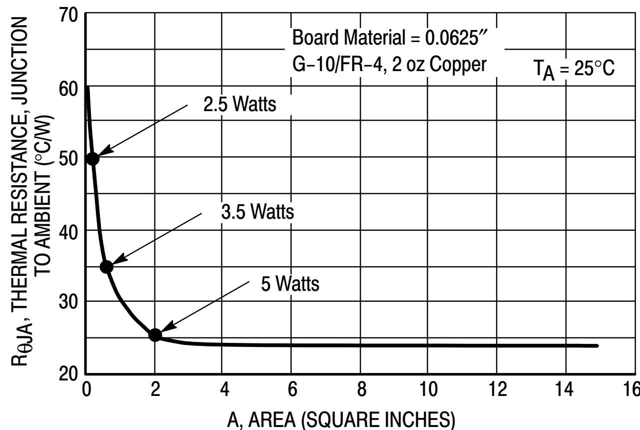



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

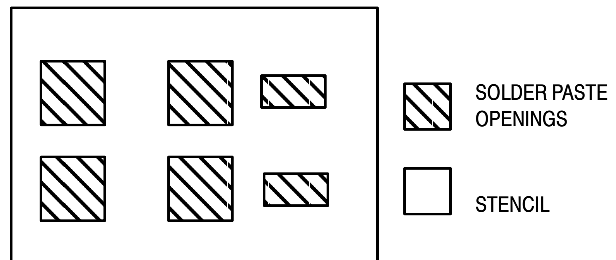



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

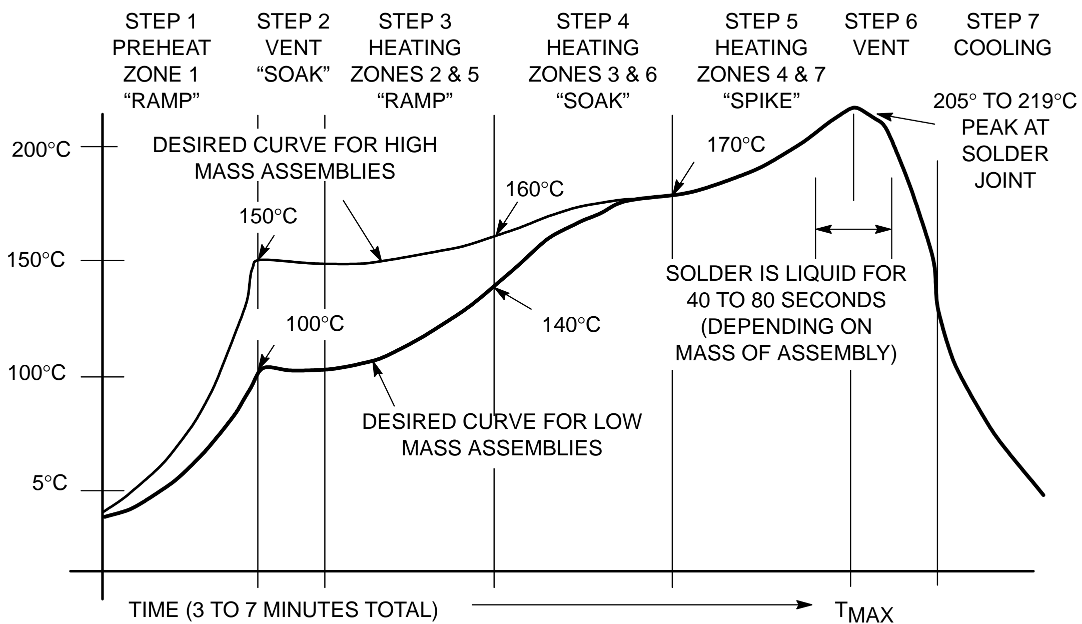



**Figure 18. Typical Solder Heating Profile**

# MTB55N06Z

**Preferred Device**

# Power MOSFET 55 Amps, 60 Volts

## N–Channel D2PAK

This Power MOSFET is designed to withstand high energy in the avalanche mode and switch efficiently. This high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Low Stored Gate Charge for Efficient Switching
- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor–Absorbs High Energy in the Avalanche Mode
- ESD Protected. Designed to Typically Withstand 400 V Machine Model and 4000 V Human Body Model.

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous @ $T_C$ = 25°C<br>– Continuous @ $T_C$ = 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>55<br>35.5<br>165 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 113<br>0.91<br>2.5 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{DS}$ = 60 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 55 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 454 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.1<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

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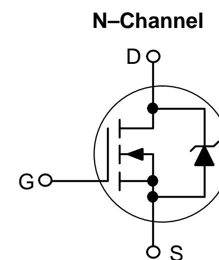
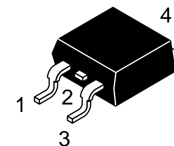
**55 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 18 mΩ**

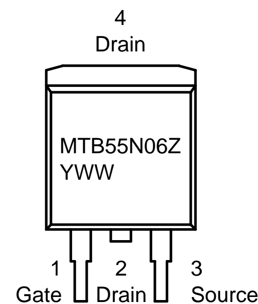
**N–Channel**




**D2PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB55N06Z = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB55N06Z | D2PAK | 50 Units/Rail |
| MTB55N06ZT4 | D2PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>53 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>6.0 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 27.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>14 | <br>18 | mΩ |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 55 Adc)<br>($I_D$ = 27.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.825<br>0.74 | <br>1.2<br>1.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 4.0 Vdc, $I_D$ = 27.5 Adc) | | $g_{FS}$ | 12 | 15 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1390 | 1950 | pF |
| Output Capacitance | | $C_{oss}$ | – | 520 | 730 | |
| Transfer Capacitance | | $C_{rss}$ | – | 119 | 238 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 55 Adc, $V_{GS(on)}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 27 | 54 | ns |
| Rise Time | | $t_r$ | – | 157 | 314 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 116 | 232 | |
| Fall Time | | $t_f$ | – | 126 | 252 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 55 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 40 | 56 | nC |
| | | $Q_1$ | – | 7.0 | – | |
| | | $Q_2$ | – | 18 | – | |
| | | $Q_3$ | – | 15 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.93<br>0.82 | <br>1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 57 | – | ns |
| | | $t_a$ | – | 32 | – | |
| | | $t_b$ | – | 25 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.11 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

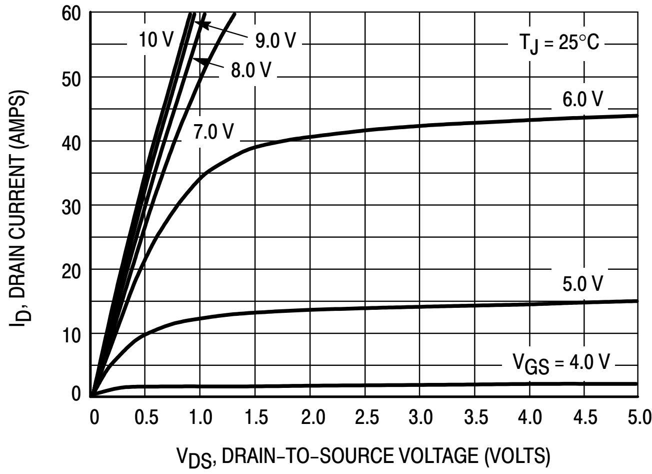


**Figure 1. On–Region Characteristics**

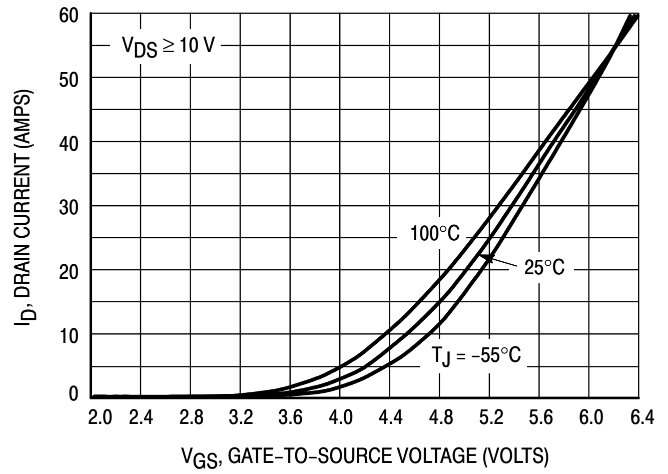


**Figure 2. Transfer Characteristics**

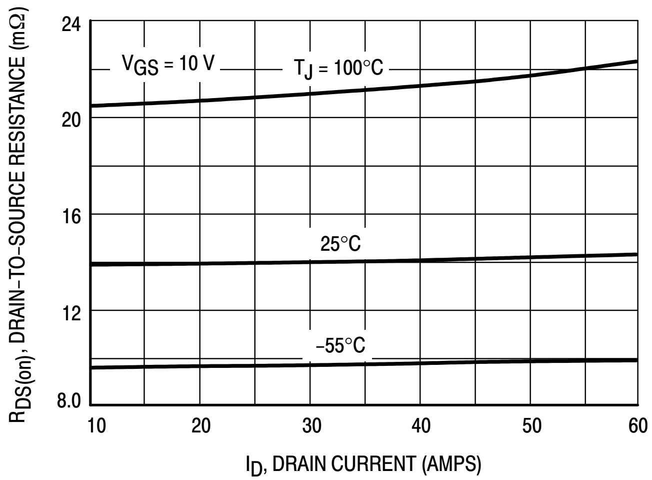


**Figure 3. On–Resistance versus Drain Current and Temperature**

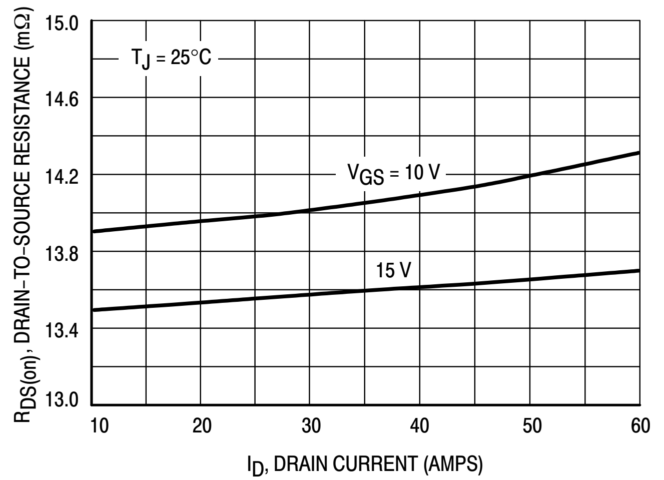


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

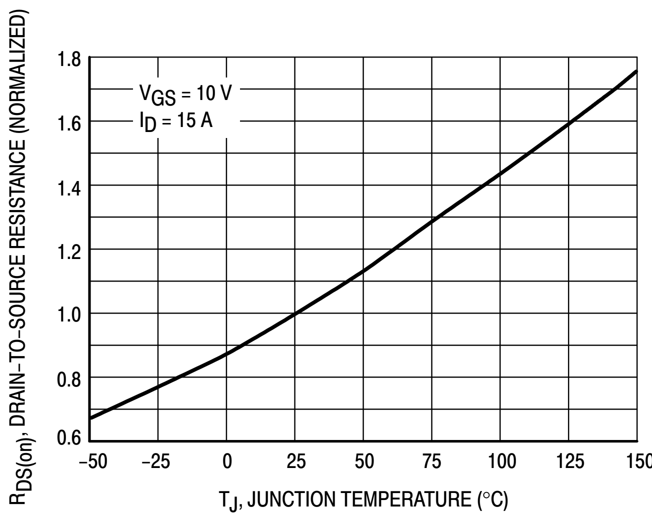


**Figure 5. On–Resistance Variation with Temperature**

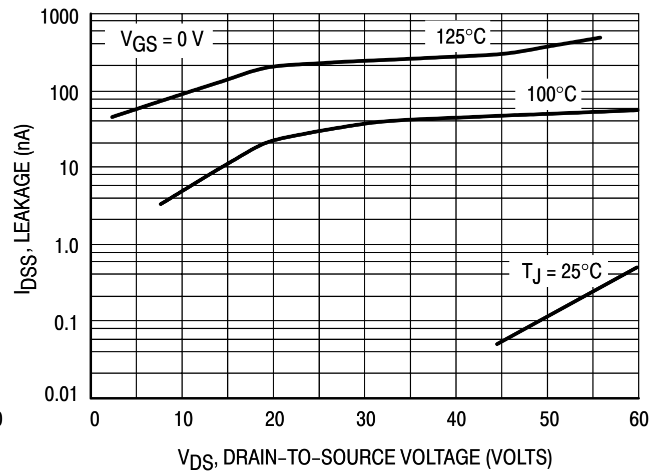


**Figure 6. Drain–to–Source Leakage Current versus Voltage**

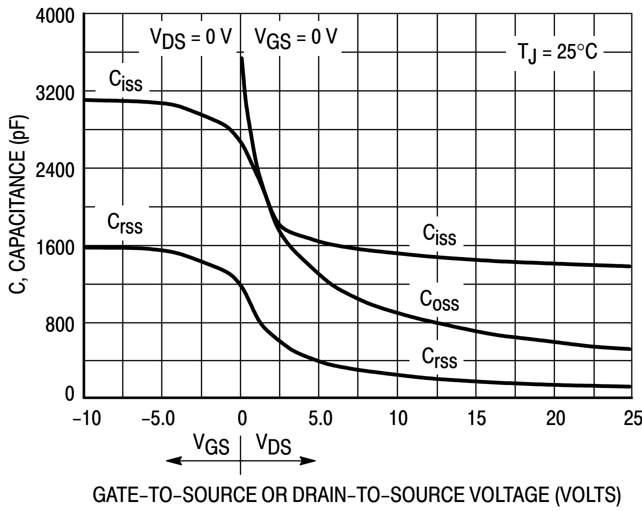


**Figure 7. Capacitance Variation**

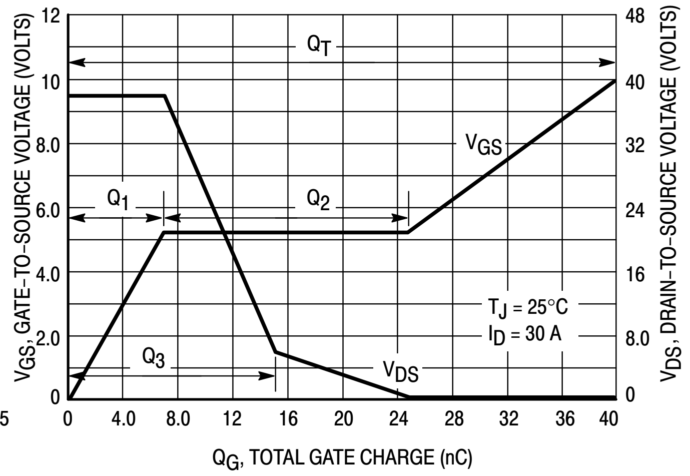


**Figure 8. Gate–to–Source and Drain–to–Source Voltage versus Total Charge**

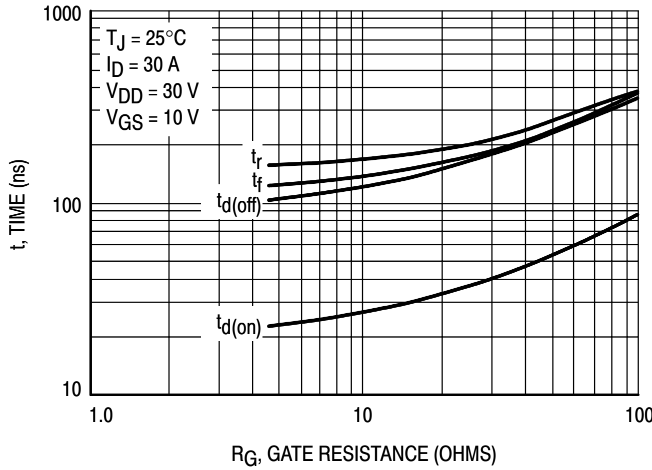


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

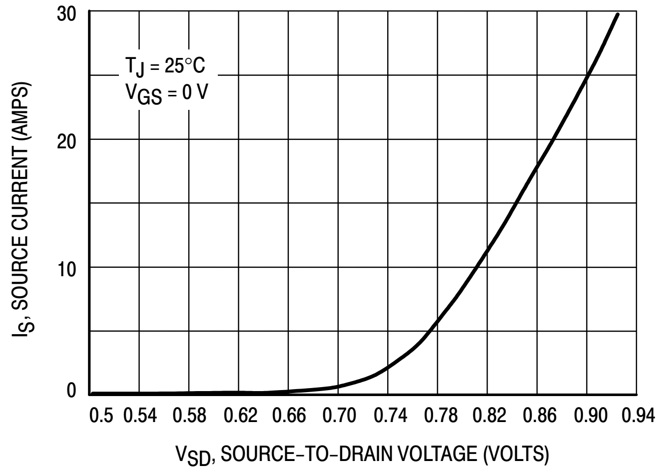


**Figure 10. Diode Forward Voltage versus Current**

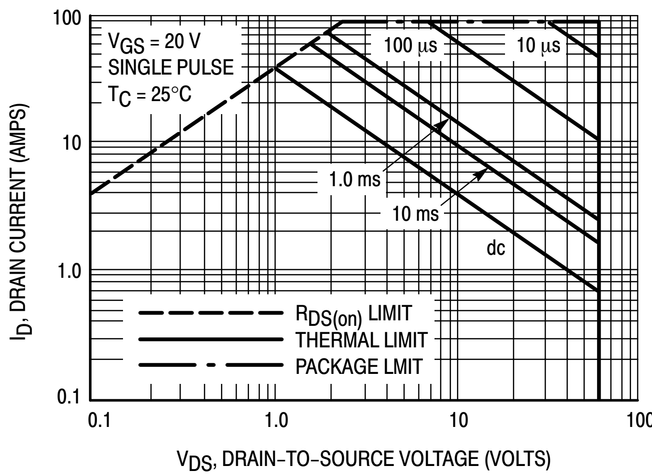


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

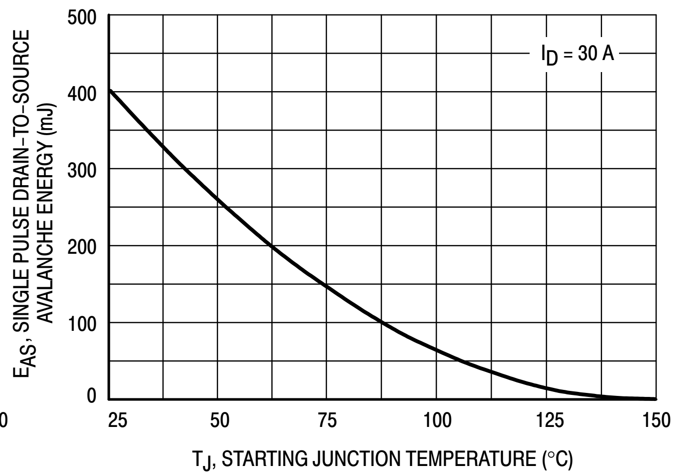


**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

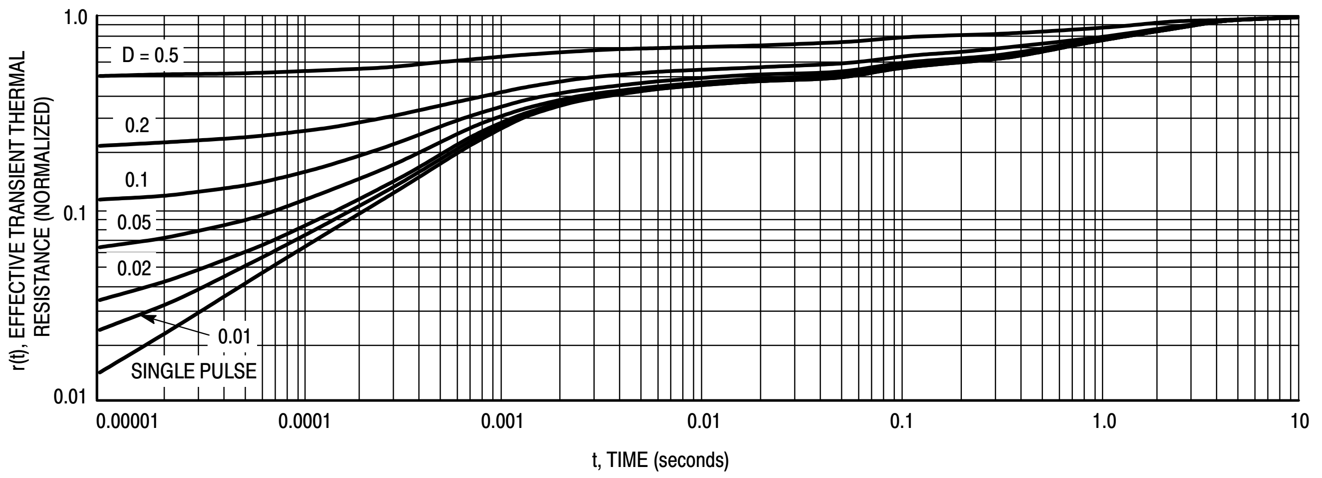


Figure 13. Thermal Response

# MTB60N05HDL

**Preferred Device**

# Power MOSFET 60 Amps, 50 Volts, Logic Level

## N–Channel $D^2PAK$

The $D^2PAK$ package has the capability of housing a larger die than any existing surface mount package which allows it to be used in applications that require the use of surface mount components with higher power and lower $R_{DS(on)}$ capabilities. This advanced high–cell density HDTMOS power FET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 50 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 50 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 60<br>42<br>180 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 60 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 540 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{θJC}$<br>$R_{θJA}$ | 1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds | $T_L$ | 260 | °C |

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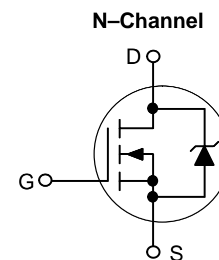
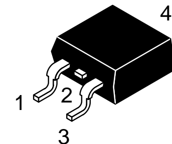
**http://onsemi.com**

**60 AMPERES**
**50 VOLTS**
**$R_{DS(on)}$ = 14 mΩ**

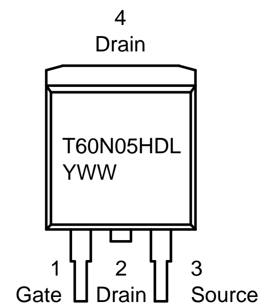
**N–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T60N05HDL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB60N05HD | $D^2PAK$ | 50 Units/Rail |
| MTB60N05HDT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 50 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 55 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = –25°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.5 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 30 Adc) | | $R_{DS(on)}$ | – | 0.010 | 0.014 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5.0 Vdc) ($I_D$ = 60 Adc) | | $V_{DS(on)}$ | – | – | 1.0 | Vdc |
| ($I_D$ = 30 Adc, $T_J$ = 125°C) | | | – | – | 0.75 | |
| Forward Transconductance ($V_{DS}$ = 4.0 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 15 | 48 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2775 | 4000 | pF |
| Output Capacitance | | $C_{oss}$ | – | 750 | 1070 | |
| Transfer Capacitance | | $C_{rss}$ | – | 150 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 21 | 40 | ns |
| Rise Time | | $t_r$ | – | 570 | 1150 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 86 | 170 | |
| Fall Time | | $t_f$ | – | 200 | 400 | |
| Gate Charge | ($V_{DS}$ = 40 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 42 | 62 | nC |
| | | $Q_1$ | – | 8.0 | – | |
| | | $Q_2$ | – | 24 | – | |
| | | $Q_3$ | – | 17 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.95 | 1.1 | Vdc |
| | ($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.85 | – | |
| Reverse Recovery Time | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 50 | – | ns |
| | | $t_a$ | – | 34 | – | |
| | | $t_b$ | – | 15 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.085 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

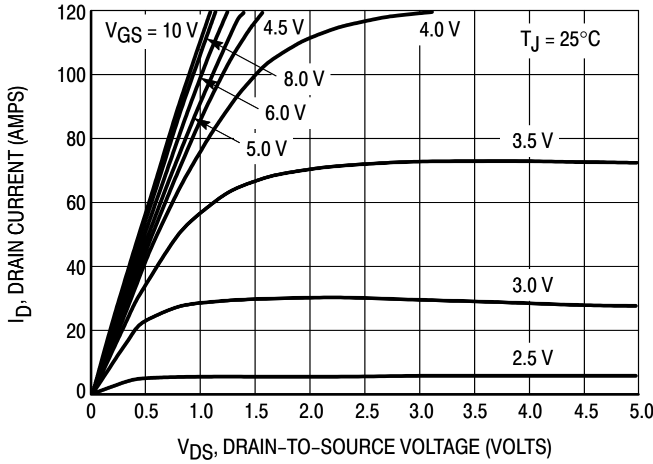



**Figure 1. On−Region Characteristics**

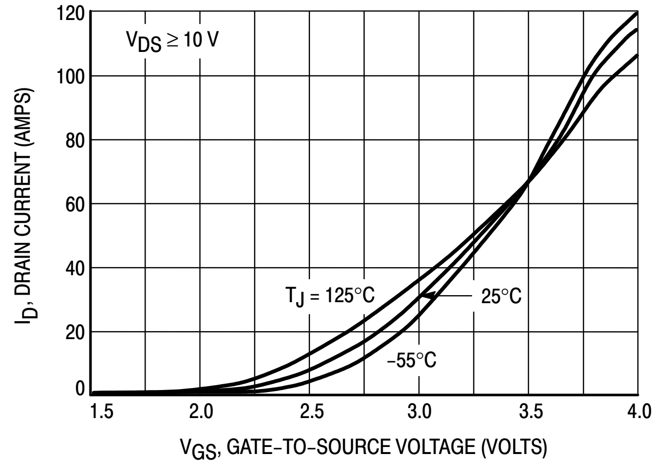



**Figure 2. Transfer Characteristics**

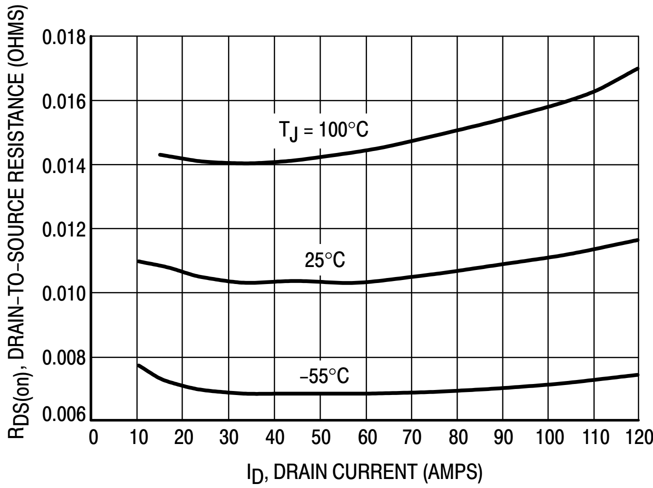



**Figure 3. On−Resistance versus Drain Current and Temperature**

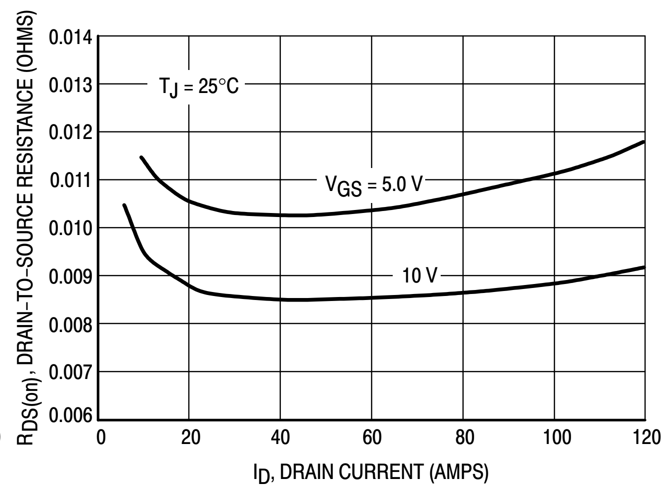



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

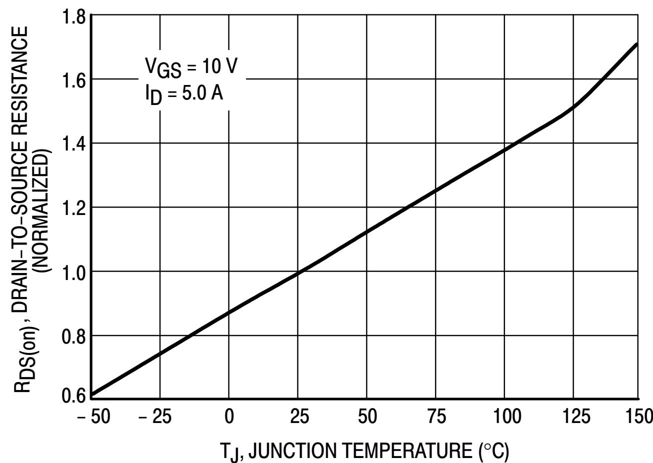



**Figure 5. On−Resistance Variation with Temperature**

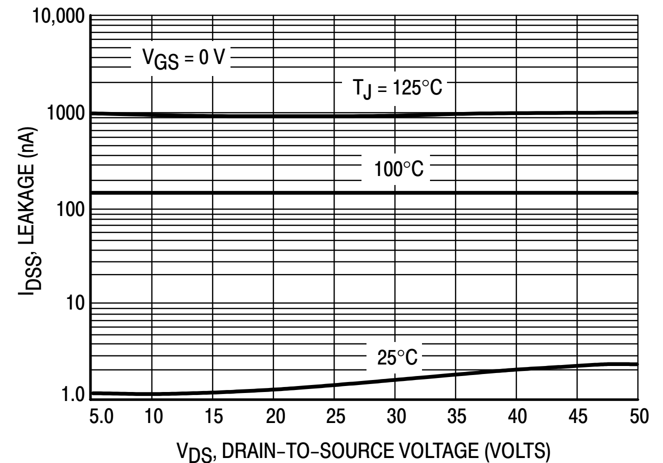



**Figure 6. Drain−to−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \ln [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

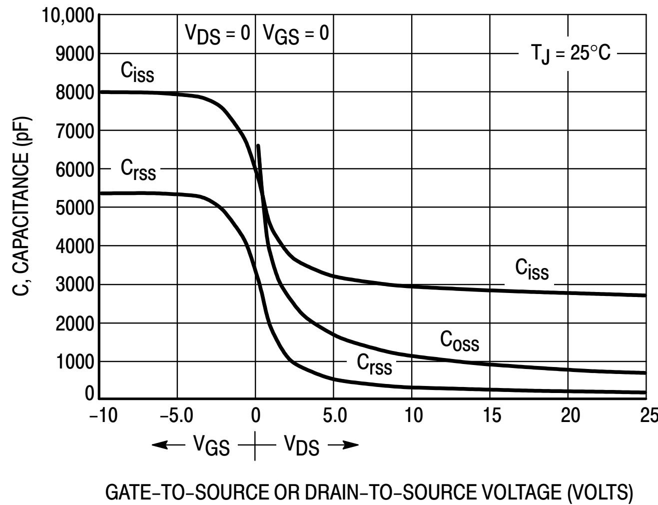



**Figure 7. Capacitance Variation**

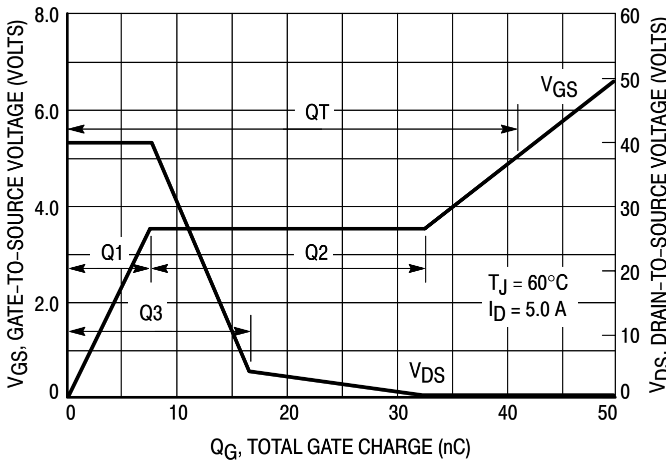



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

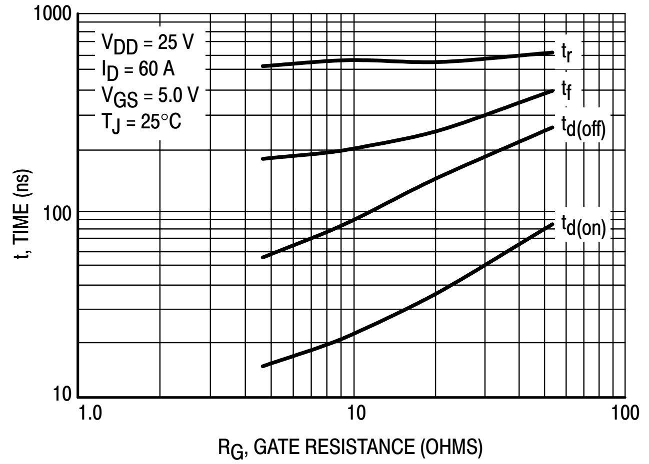



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

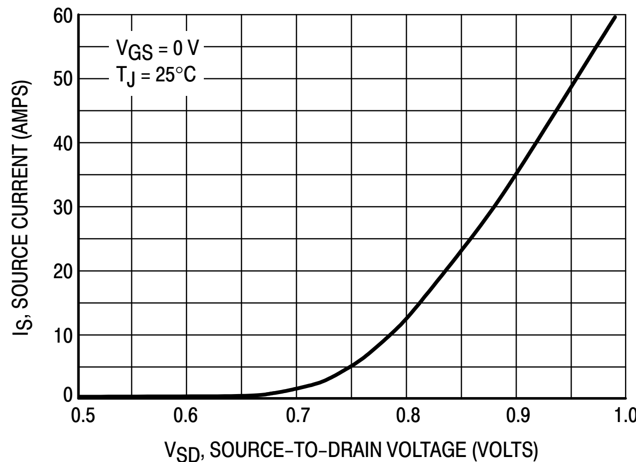



**Figure 10. Diode Forward Voltage versus Current**

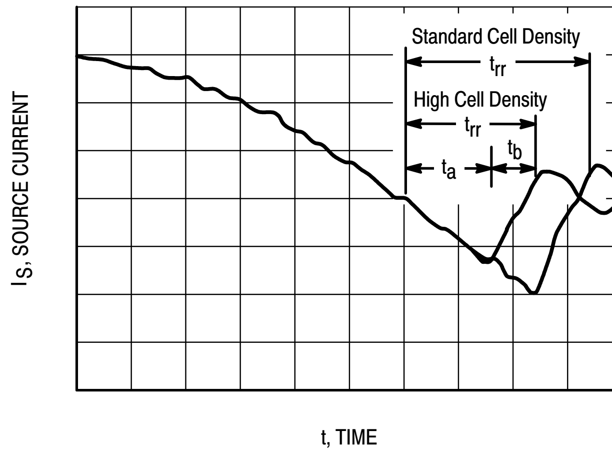



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

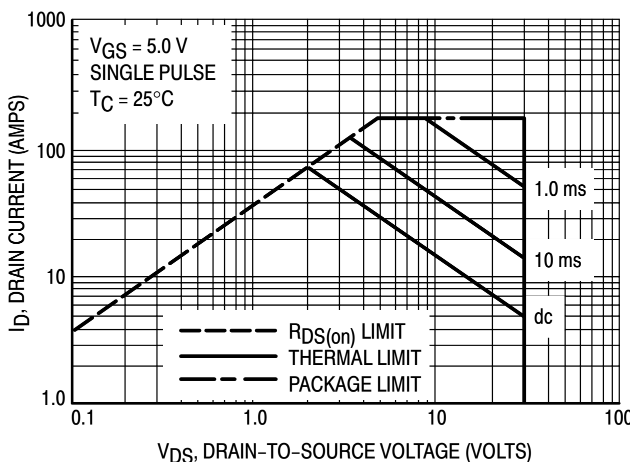



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

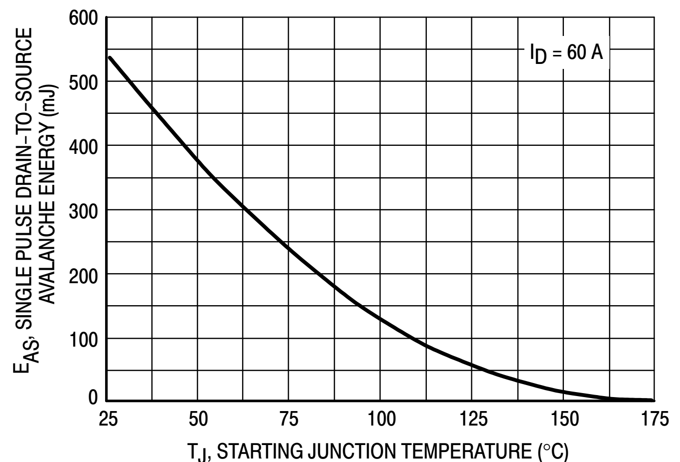



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

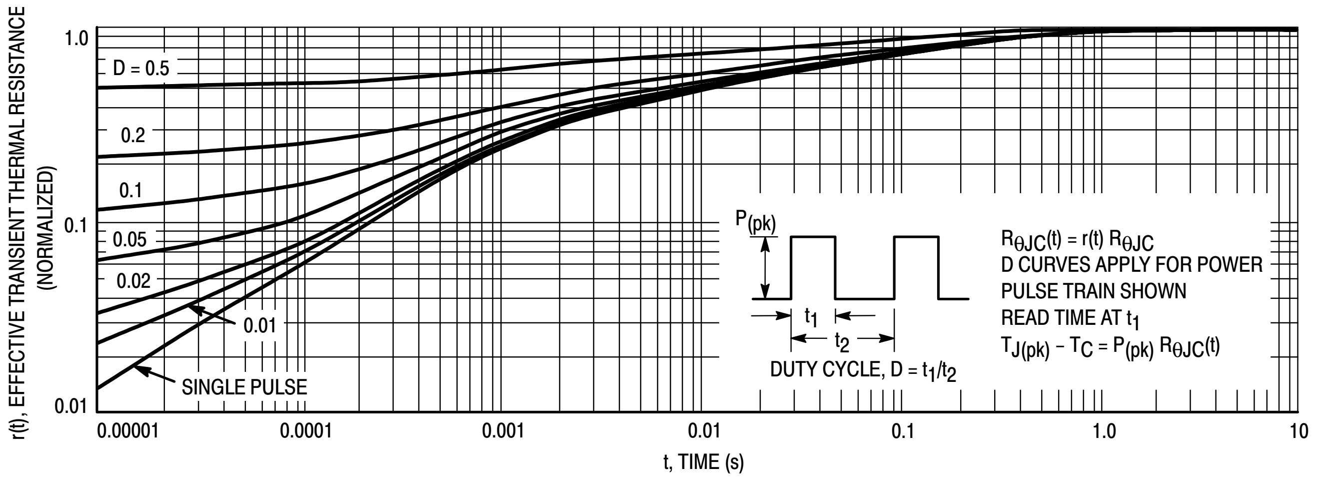



**Figure 14. Thermal Response**

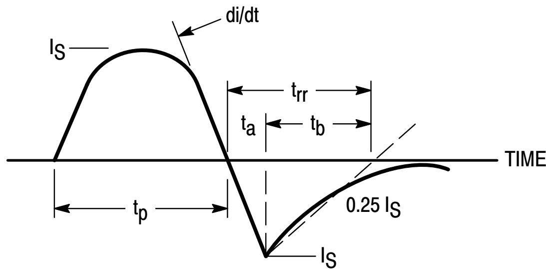



**Figure 15. Diode Reverse Recovery Waveform**

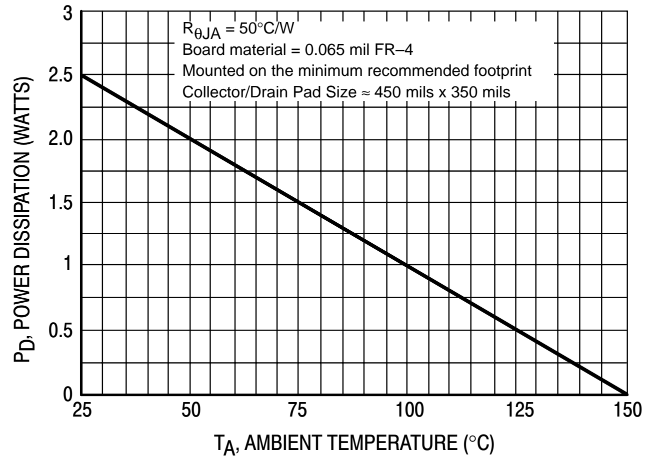
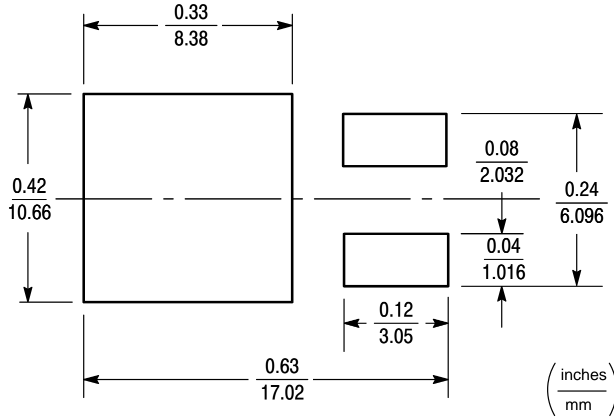



**Figure 16. D2PAK Power Derating Curve**

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

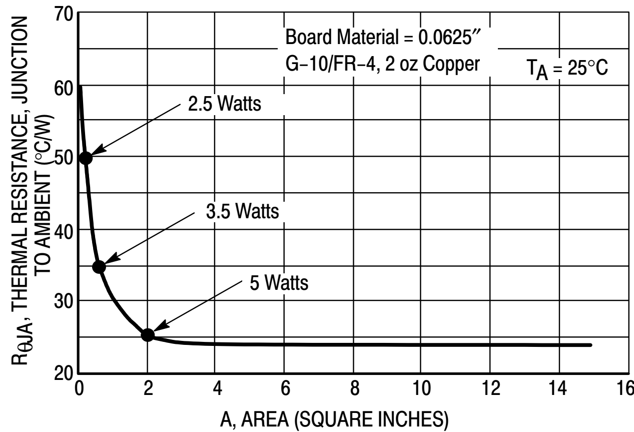



**Figure 17. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 18 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

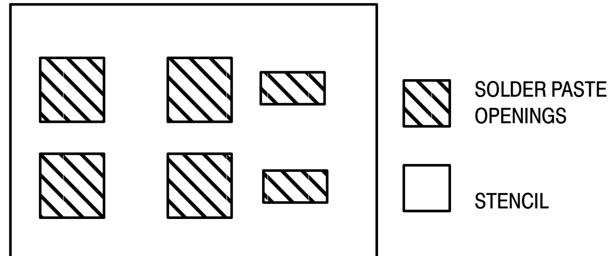



**Figure 18. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 19 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

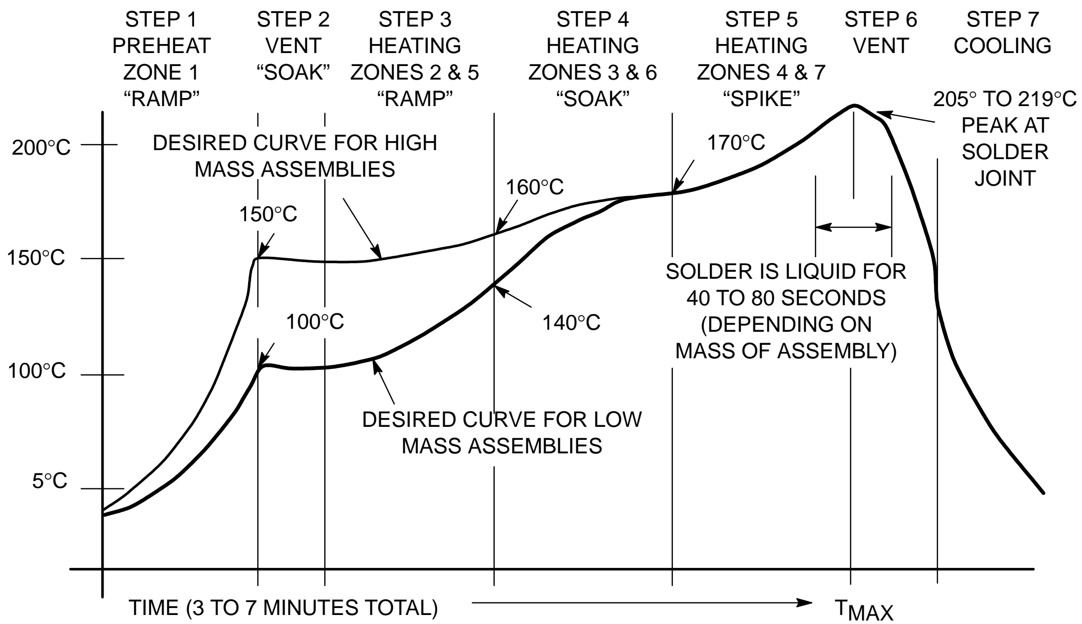



**Figure 19. Typical Solder Heating Profile**

# MTB60N06HD

**Preferred Device**

# Power MOSFET 60 Amps, 60 Volts

## N–Channel $D^2$PAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 60<br>42.3<br>180 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 60 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 540 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

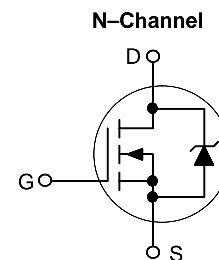
1. When mounted with the minimum recommended pad size.

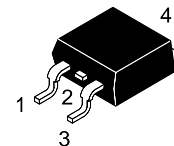
**ON Semiconductor™**

**http://onsemi.com**

**60 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 14 mΩ**

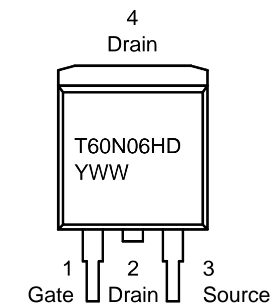
**N–Channel**




**$D^2$PAK**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T60N06HD = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB60N06HD | $D^2$PAK | 50 Units/Rail |
| MTB60N06HDT4 | $D^2$PAK | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>71 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 3.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>7.0 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 3.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 30 Adc) | $R_{DS(on)}$ | <br>– | <br>0.011 | <br>0.014 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 60 Adc)<br>($I_D$ = 30 Adc, $T_J$ =125°C) | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>0.9 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 4.0 Vdc, $I_D$ = 30 Adc) | $g_{FS}$ | <br>15 | <br>20 | <br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance — ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1950 | 2800 | pF |
| Output Capacitance | $C_{oss}$ | – | 660 | 920 | |
| Transfer Capacitance | $C_{rss}$ | – | 147 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | |
| Turn–On Delay Time — ($V_{DD}$= 30 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 26 | ns |
| Rise Time | $t_r$ | – | 197 | 394 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 50 | 102 | |
| Fall Time | $t_f$ | – | 124 | 246 | |
| Gate Charge (See Figure 8) — ($V_{DS}$ = 48 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 51 | 71 | nC |
| | $Q_1$ | – | 12 | – | |
| | $Q_2$ | – | 24 | – | |
| | $Q_3$ | – | 21 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.99<br>0.89 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time (See Figure 15) — ($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 60 | – | ns |
| | $t_a$ | – | 36 | – | |
| | $t_b$ | – | 24 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.143 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

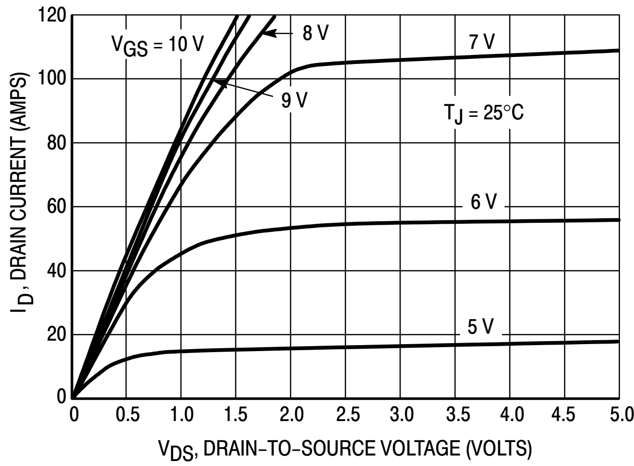



**Figure 1. On–Region Characteristics**

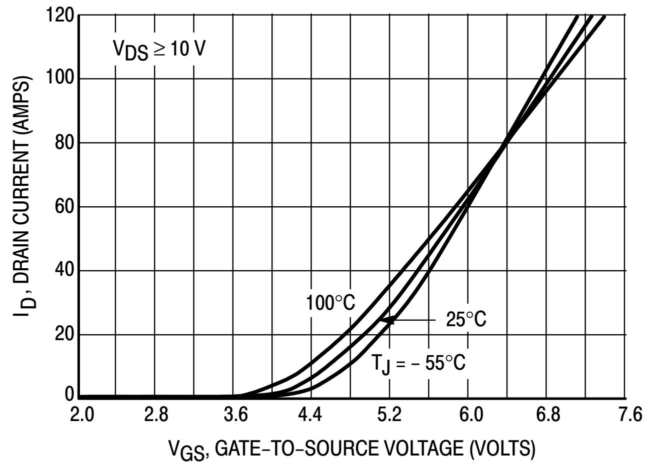



**Figure 2. Transfer Characteristics**

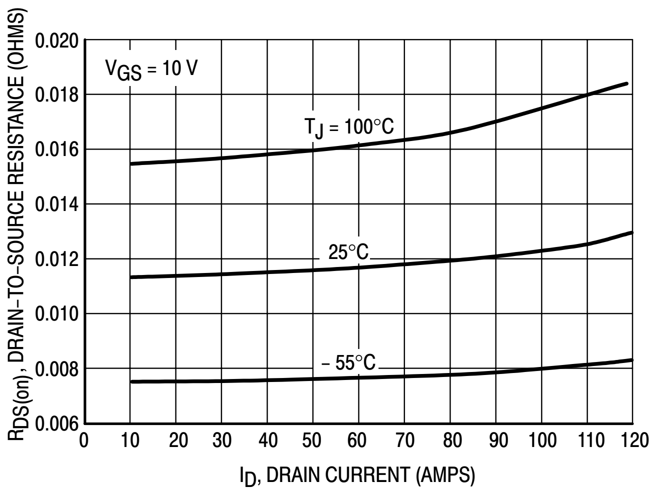



**Figure 3. On–Resistance versus Drain Current and Temperature**

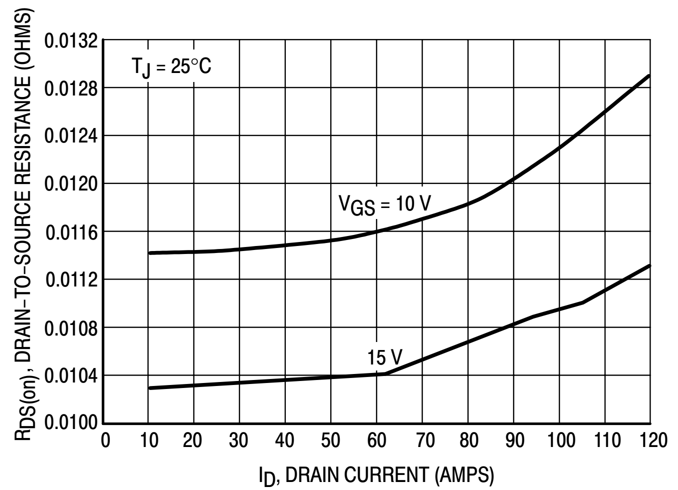



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

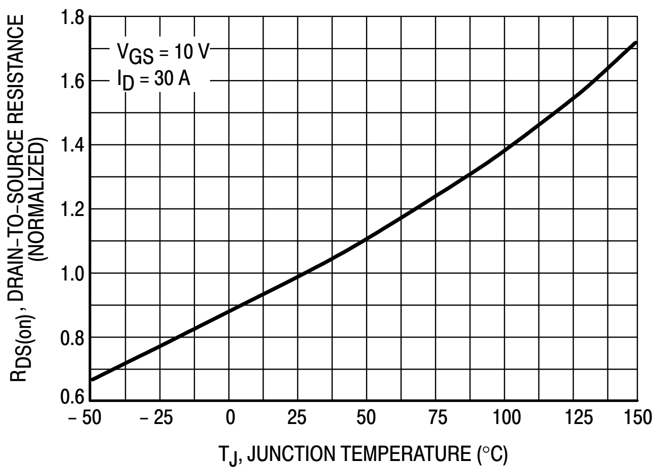



**Figure 5. On–Resistance Variation with Temperature**

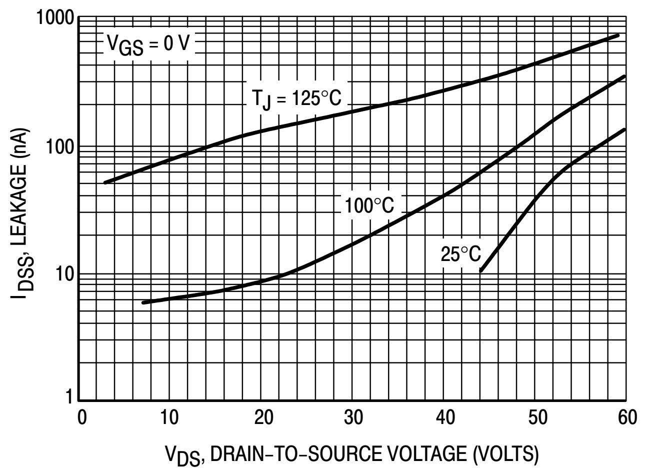



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \ln \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \ln \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

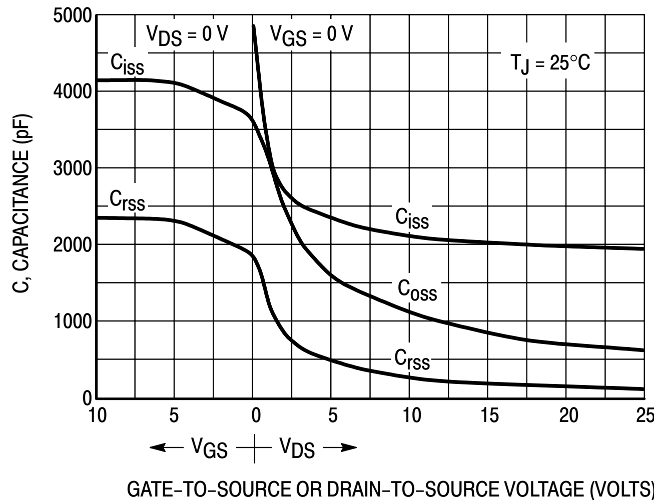



**Figure 7. Capacitance Variation**

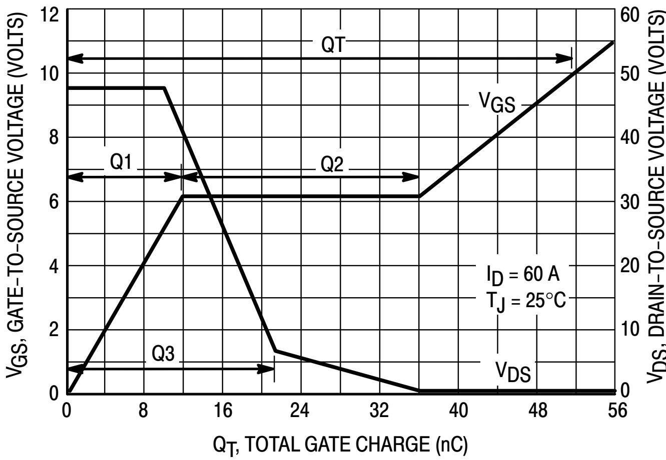



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

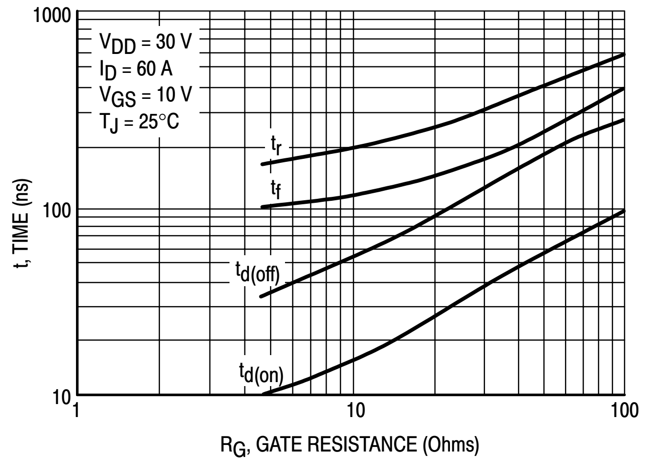



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

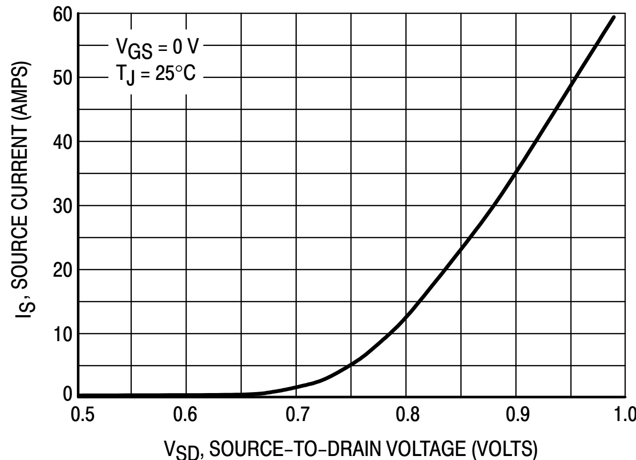



**Figure 10. Diode Forward Voltage versus Current**

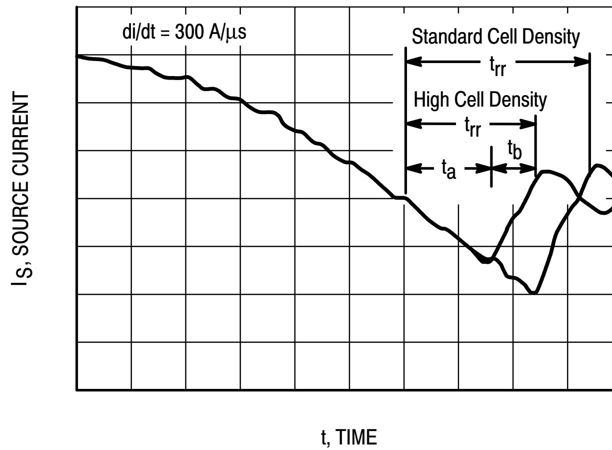



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

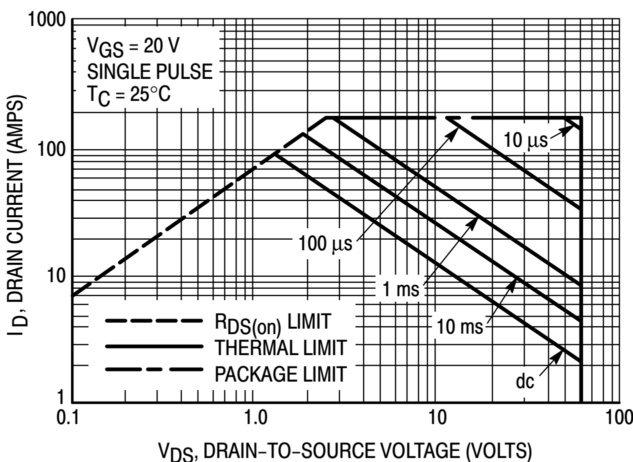



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

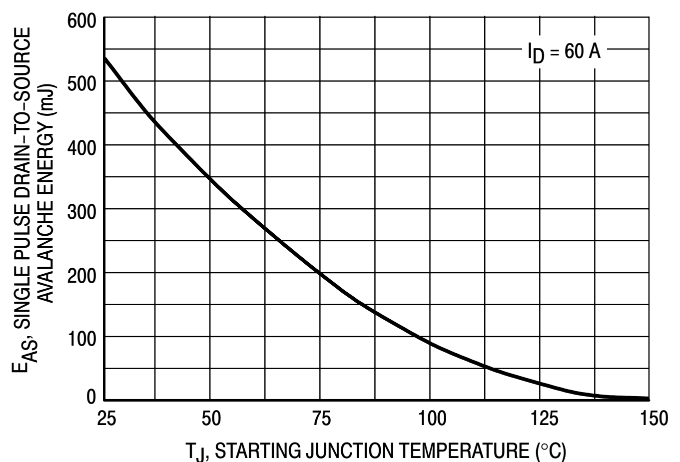



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

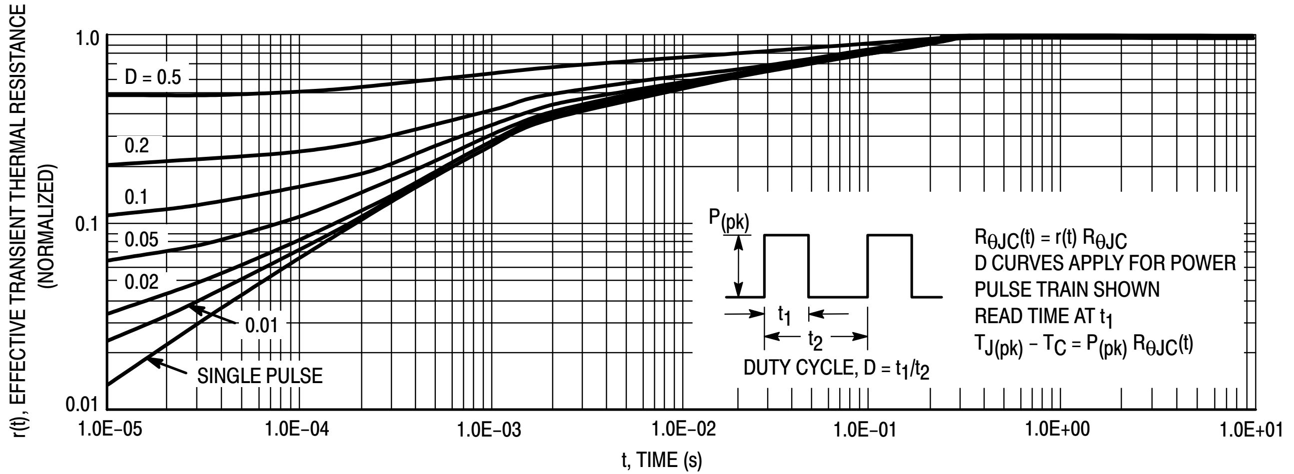



**Figure 14. Thermal Response**

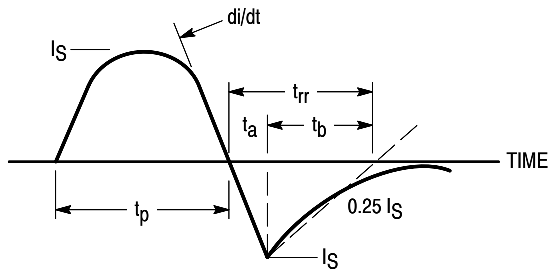



**Figure 15. Diode Reverse Recovery Waveform**

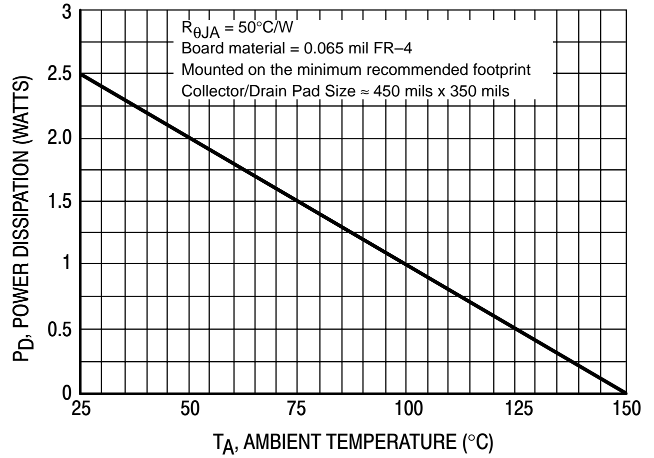
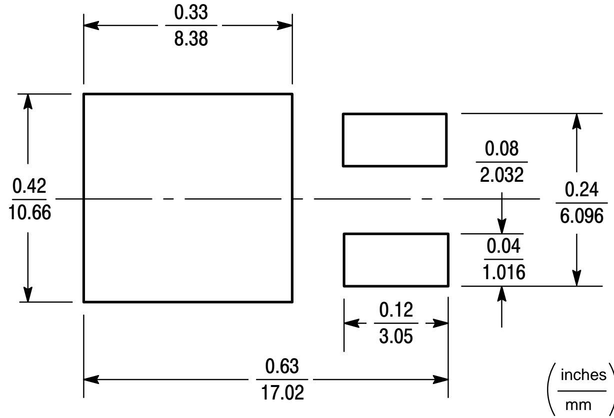



**Figure 16. D²PAK Power Derating Curve**

# INFORMATION FOR USING THE D²PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D²PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D²PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

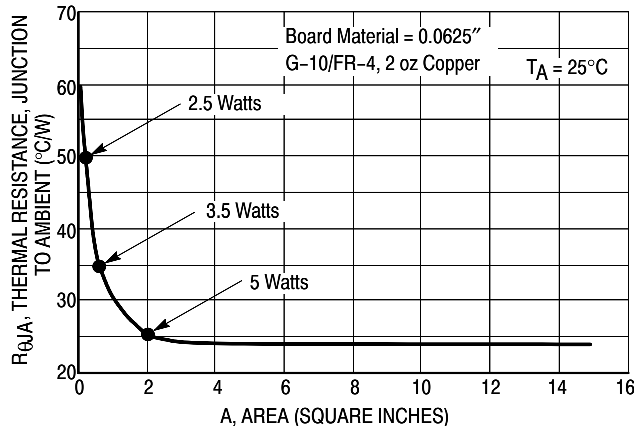



**Figure 17. Thermal Resistance versus Drain Pad Area for the D²PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 18 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

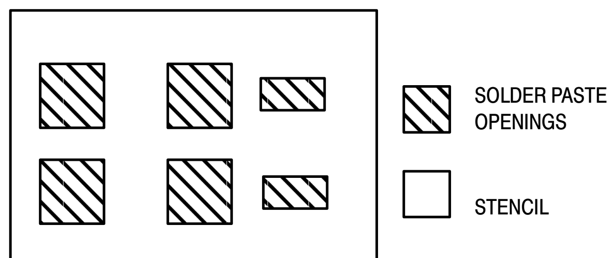



**Figure 18. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 19 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

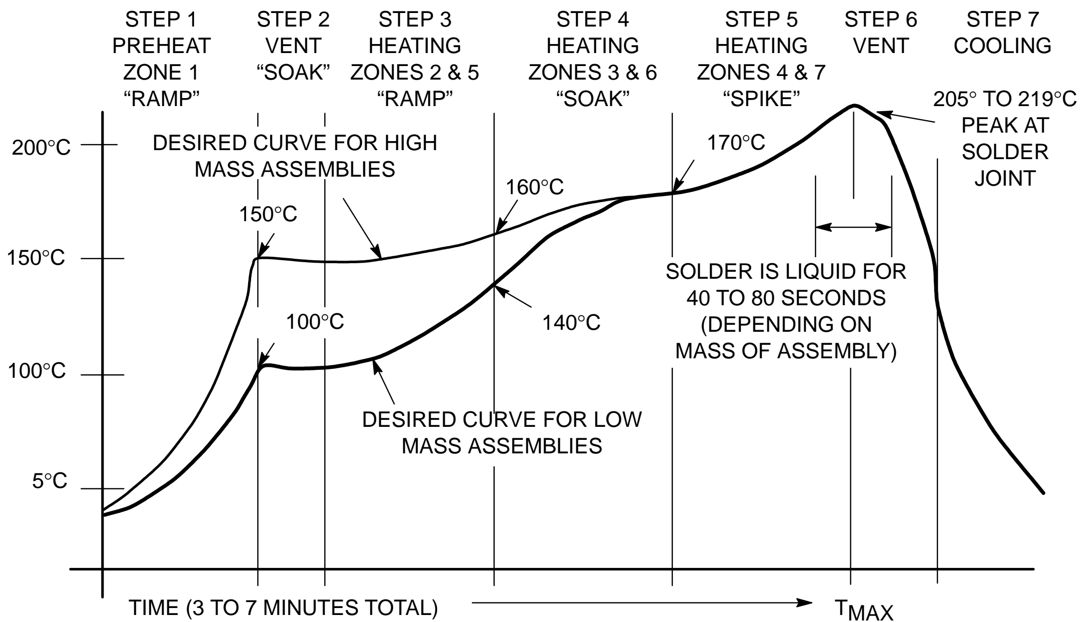



**Figure 19. Typical Solder Heating Profile**

# MTB75N03HDL

**Preferred Device**

# Power MOSFET 75 Amps, 25 Volts, Logic Level

## N–Channel $D^2PAK$

**ON Semiconductor™**

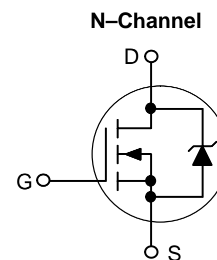
**http://onsemi.com**

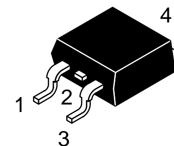
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**75 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 9 mΩ**

**N–Channel**



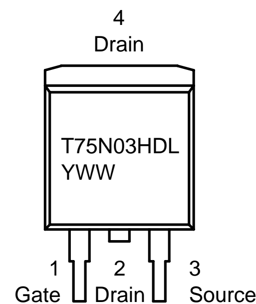

**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 25 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>59<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 75 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 280 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When mounted with the minimum recommended pad size.

**MARKING DIAGRAM & PIN ASSIGNMENT**




T75N03HDL = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB75N03HDL | $D^2PAK$ | 50 Units/Rail |
| MTB75N03HDLT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 25 | – | – | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 100<br>500 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 V) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 3.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 37.5 Adc) | | $R_{DS(on)}$ | – | 6.0 | 9.0 | mΩ |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 75 Adc)<br>($I_D$ = 37.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 0.68<br>0.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 3 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 15 | 55 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 4025 | 5635 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1353 | 1894 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 307 | 430 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$= 15 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | – | 24 | 48 | ns |
| Rise Time | | $t_r$ | – | 493 | 986 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 60 | 120 | |
| Fall Time | | $t_f$ | – | 149 | 300 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 61 | 122 | nC |
| | | $Q_1$ | – | 14 | 28 | |
| | | $Q_2$ | – | 33 | 66 | |
| | | $Q_3$ | – | 27 | 54 | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.97<br>0.87 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 75 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 58 | – | ns |
| | | $t_a$ | – | 27 | – | |
| | | $t_b$ | – | 30 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.088 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

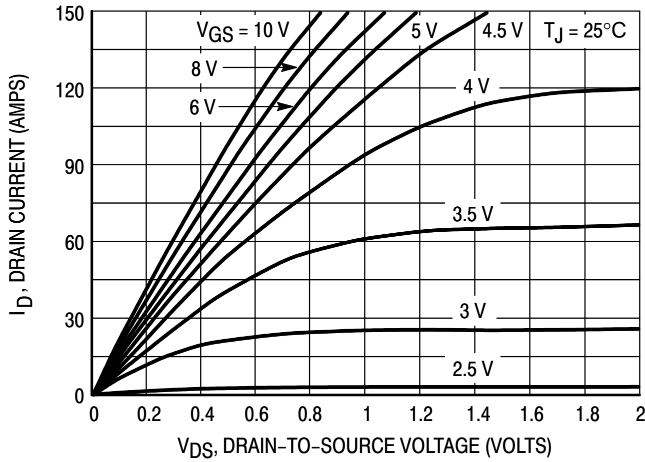



**Figure 1. On–Region Characteristics**

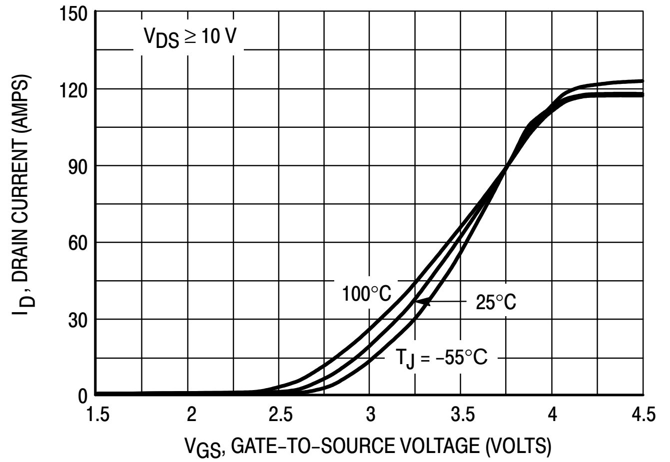



**Figure 2. Transfer Characteristics**

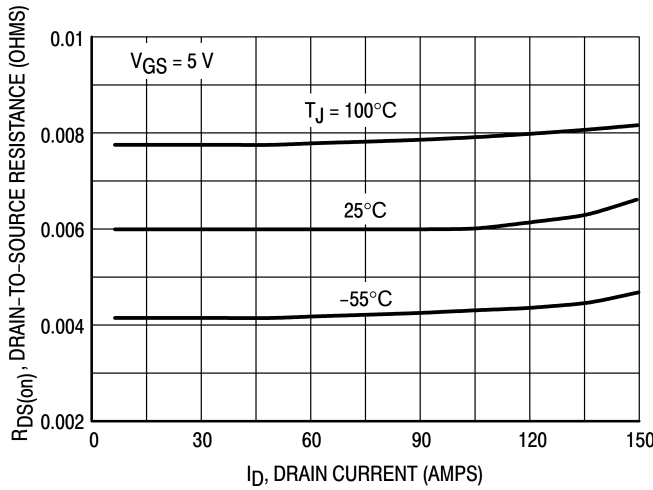



**Figure 3. On–Resistance versus Drain Current and Temperature**

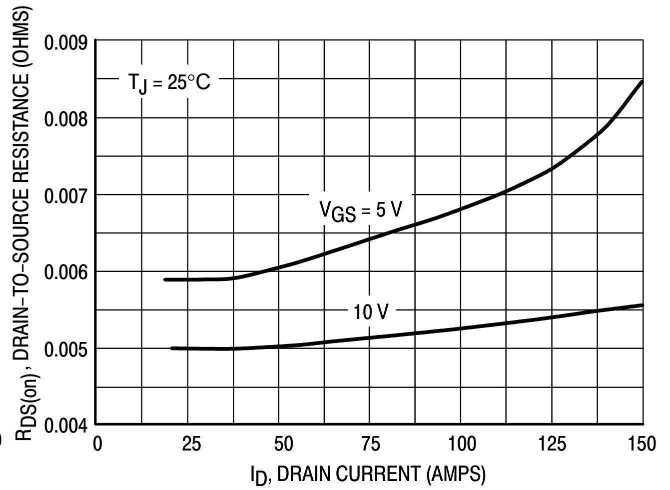



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

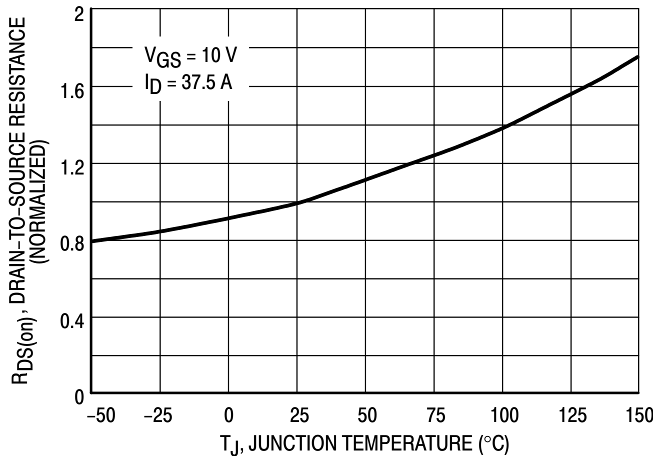



**Figure 5. On–Resistance Variation with Temperature**

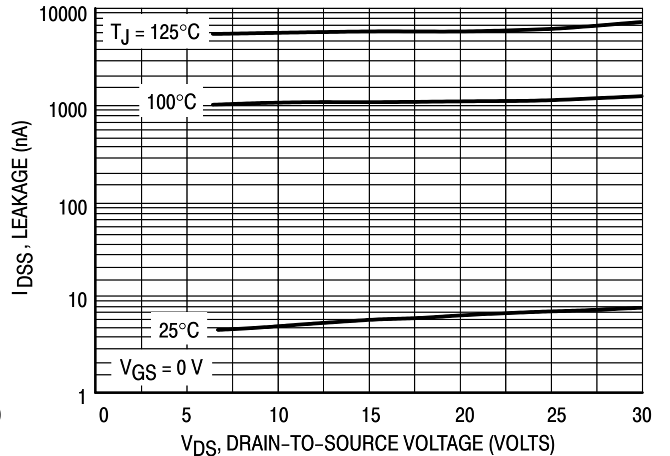



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

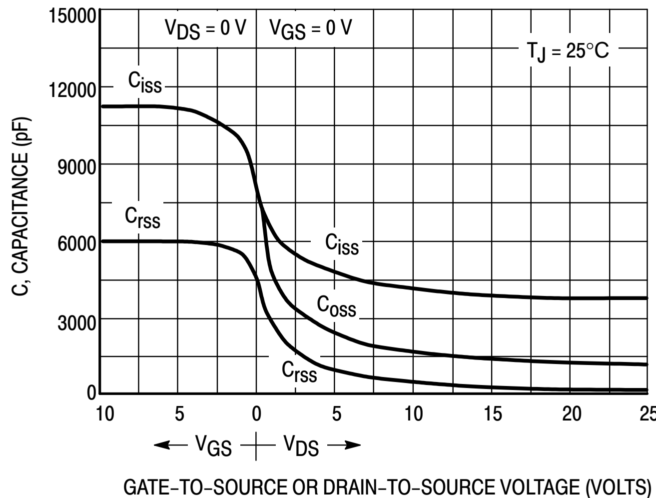



**Figure 7. Capacitance Variation**

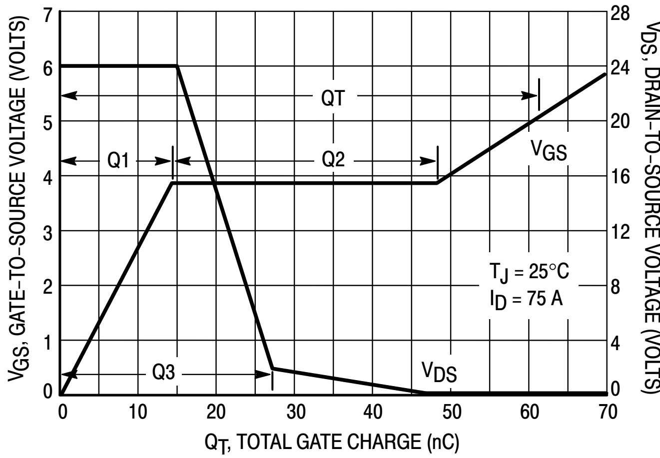



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

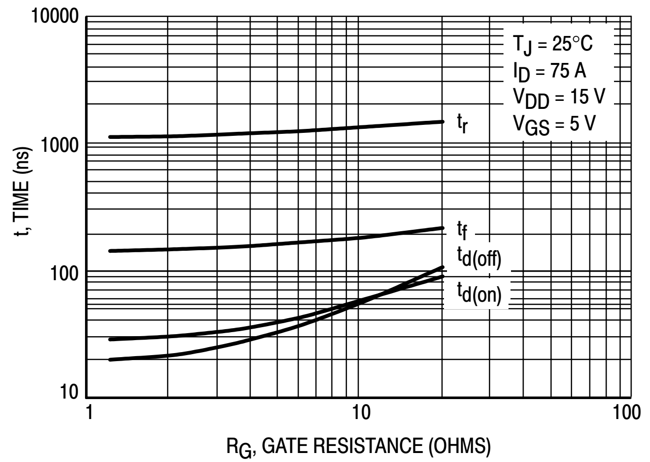



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

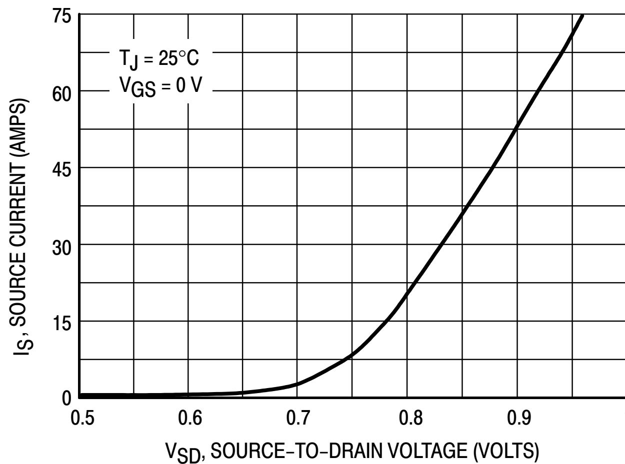



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

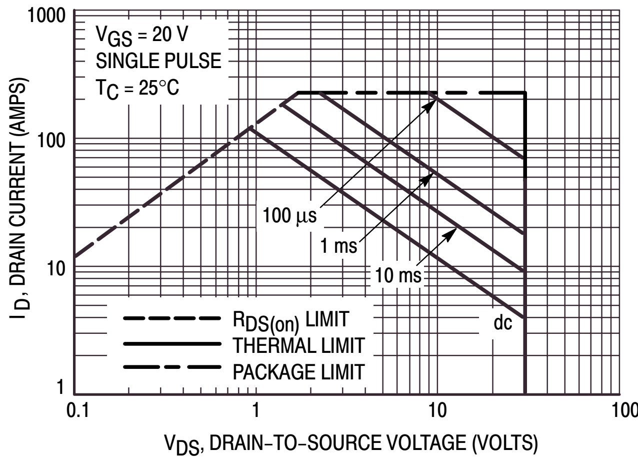



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

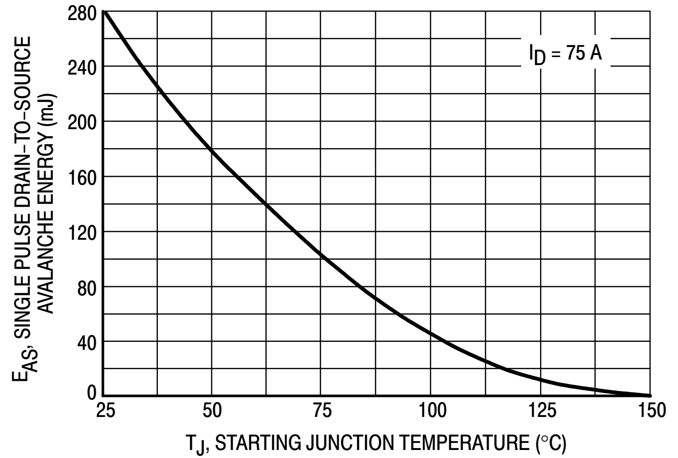



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

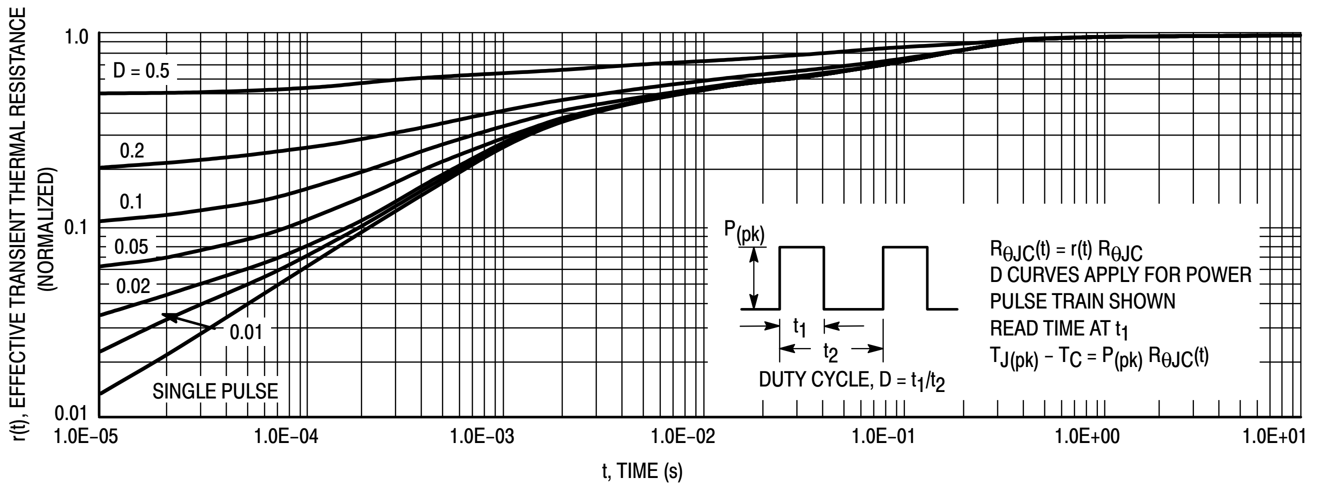



Figure 13. Thermal Response

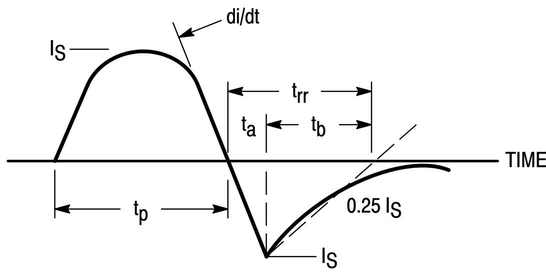



Figure 14. Diode Reverse Recovery Waveform

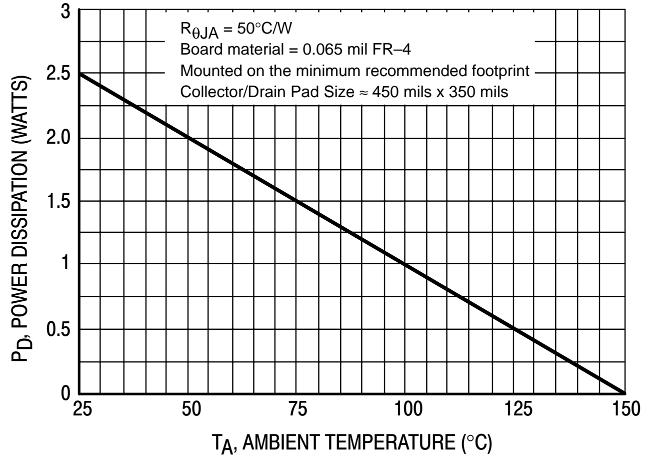
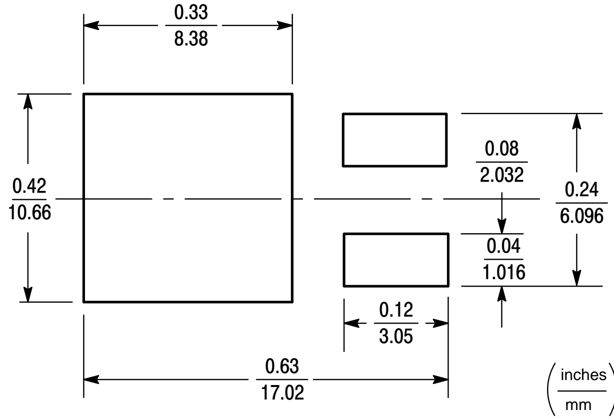



Figure 15. D2PAK Power Derating Curve

# INFORMATION FOR USING THE D2PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a D2PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the D2PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

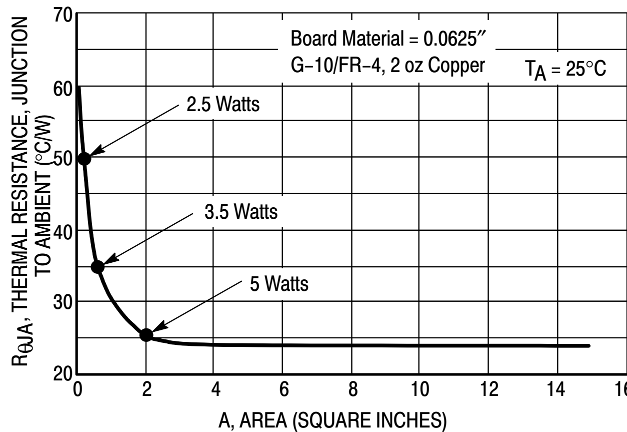



**Figure 16. Thermal Resistance versus Drain Pad Area for the D2PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 18 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

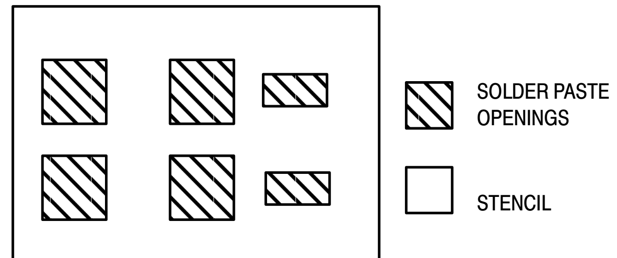



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 19 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

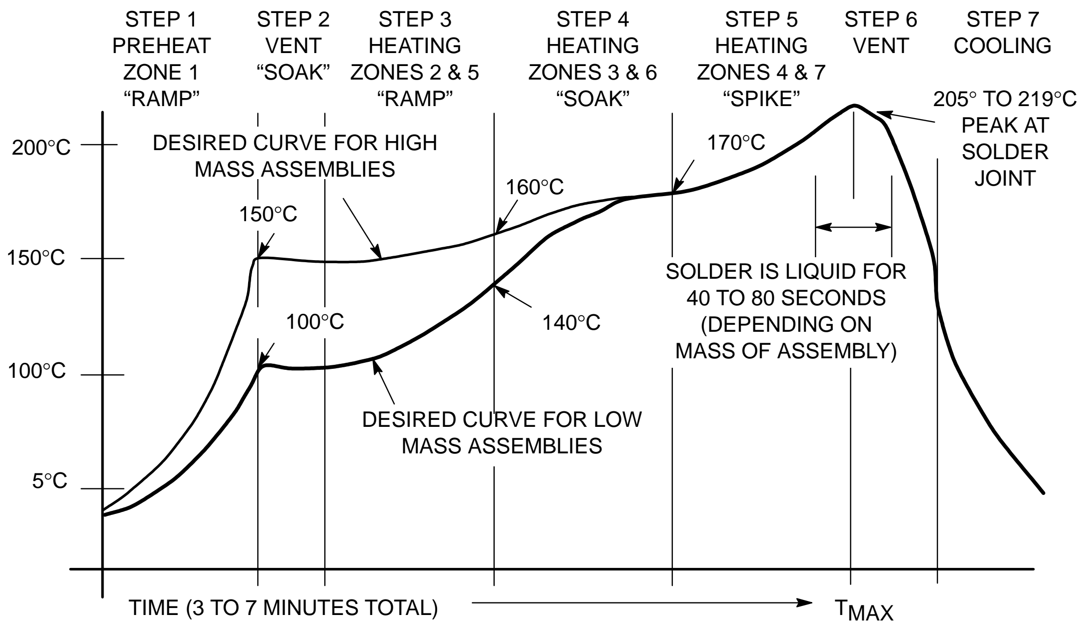



**Figure 18. Typical Solder Heating Profile**

# MTB75N05HD

Preferred Device

# Power MOSFET 75 Amps, 50 Volts

## N–Channel $D^2PAK$

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

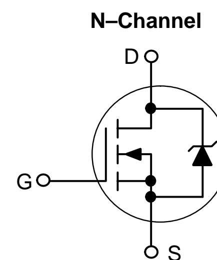
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 50 | Volts |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 50 | |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ±20 | |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq 10\ \mu s$) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>65<br>225 | Amps |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C<br>(minimum footprint, FR–4 board) | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 V, $V_{GS}$ = 10 V, Peak $I_L$ = 75 A, L = 0.177 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (minimum foot-print, FR–4 board) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5<br>50 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

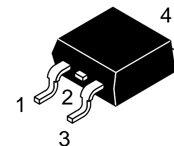
**ON Semiconductor™**

http://onsemi.com

**75 AMPERES**
**50 VOLTS**
**$R_{DS(on)}$ = 9.5 mΩ**

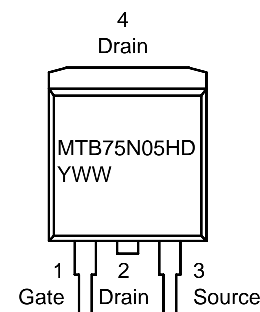
N–Channel




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




MTB75N05HD = Device Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB75N05HD | $D^2PAK$ | 50 Units/Rail |
| MTB75N05HDT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2) (Note 2.)<br>($V_{GS}$ = 0, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>50<br>– | <br>–<br>54.9 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 50 V, $V_{GS}$ = 0)<br>($V_{DS}$ = 50 V, $V_{GS}$ = 0, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 1.5) (Note 2.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>–<br>6.3 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Note 3.) ($C_{pk}$ ≥ 3.0) (Note 2.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc) | | $R_{DS(on)}$ | <br>– | <br>7.0 | <br>9.5 | mΩ |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc) (Note 3.)<br>($I_D$ = 75 A)<br>($I_D$ = 20 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.63<br>– | <br>–<br>0.34 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 15 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** (Note 2.) | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) ($C_{pk}$ ≥ 2.0) | $C_{iss}$ | – | 2600 | 3900 | pF |
| Output Capacitance | ($C_{pk}$ ≥ 2.0) | $C_{oss}$ | – | 1000 | 1300 | |
| Transfer Capacitance | ($C_{pk}$ ≥ 2.0) | $C_{rss}$ | – | 230 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 4.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 75 A, $V_{GS}$ = 10 V, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 170 | 340 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 70 | 140 | |
| Fall Time | | $t_f$ | – | 100 | 200 | |
| Gate Charge | ($V_{DS}$ = 40 V, $I_D$ = 75 A, $V_{GS}$ = 10 V) | $Q_T$ | – | 71 | 100 | nC |
| | | $Q_1$ | – | 13 | – | |
| | | $Q_2$ | – | 33 | – | |
| | | $Q_3$ | – | 26 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 75 A, $V_{GS}$ = 0) ($C_{pk}$ ≥ 10)<br>($I_S$ = 20 A, $V_{GS}$ = 0)<br>(IS = 20 A, $V_{GS}$ = 0, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | 0.97<br>0.80<br>0.68 | –<br>1.00<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 37.5 A, $V_{GS}$ = 0, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 57 | – | ns |
| | | $t_a$ | – | 40 | – | |
| | | $t_b$ | – | 17 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.17 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Reflects Typical Values. $C_{pk}$ = Absolute Value of (SPEC – AVG) / 3 * SIGMA).
3. For accurate measurements, good Kelvin contact required.
4. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS (Note 5.)

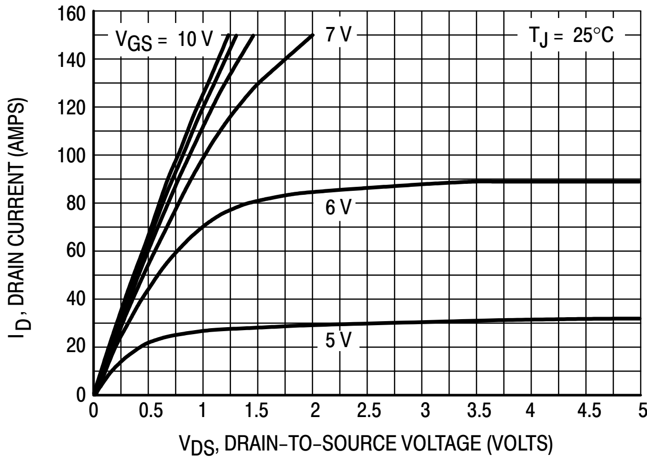



**Figure 1. On–Region Characteristics**

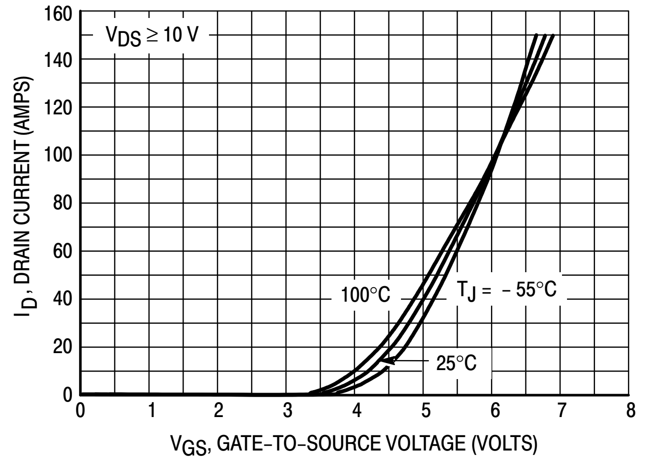



**Figure 2. Transfer Characteristics**

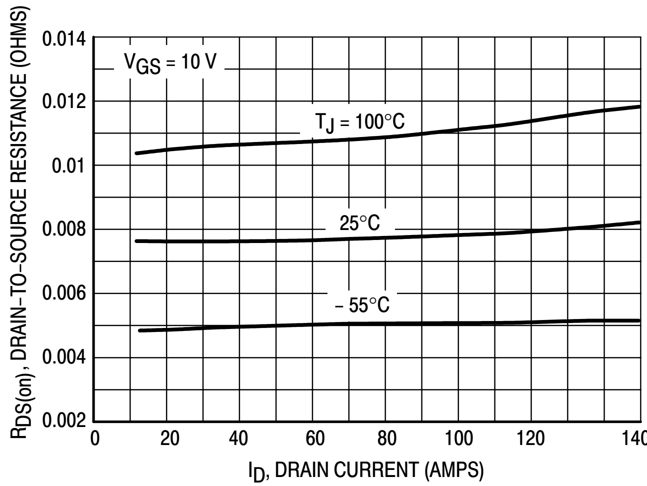



**Figure 3. On–Resistance versus Drain Current and Temperature**

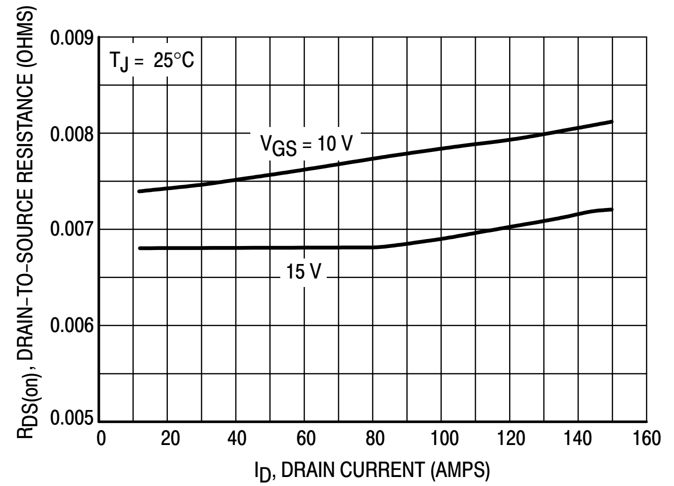



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

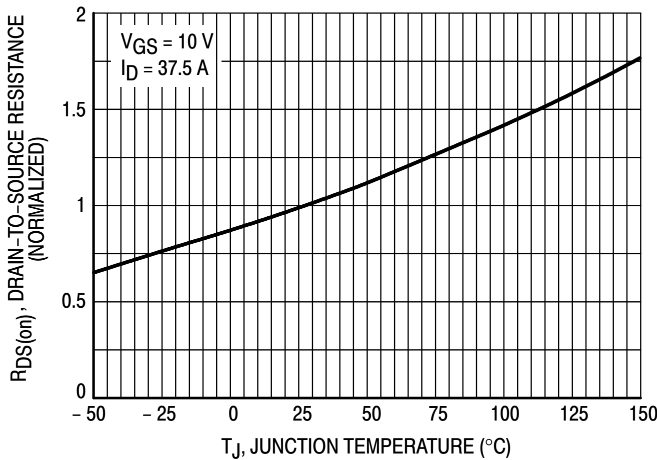



**Figure 5. On–Resistance Variation with Temperature**

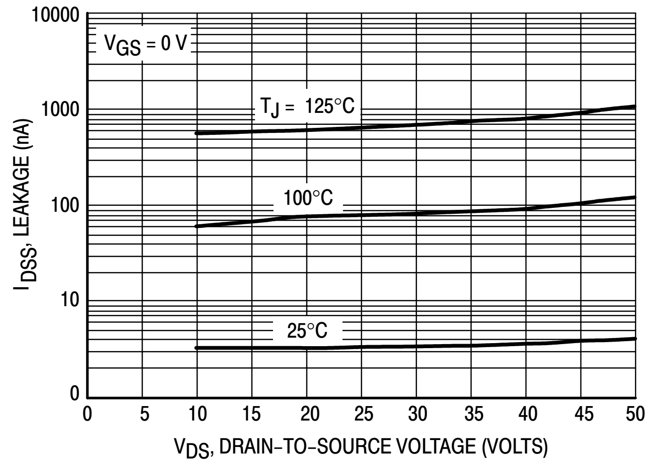



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

5. Pulse Tests: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in a RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board–mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

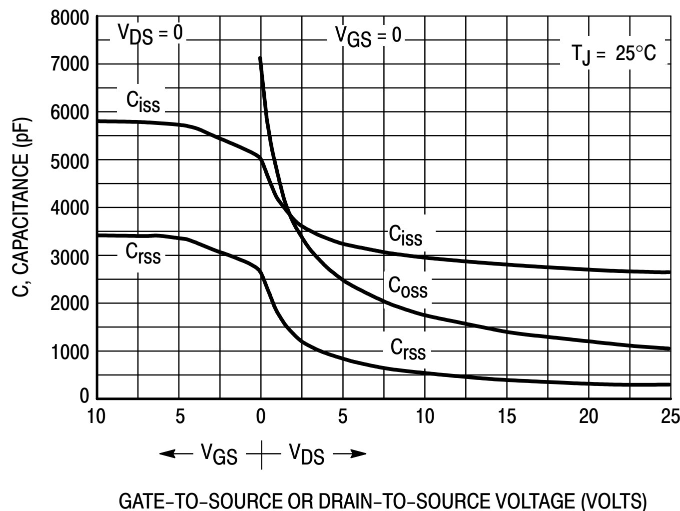



**Figure 7. Capacitance Variation**

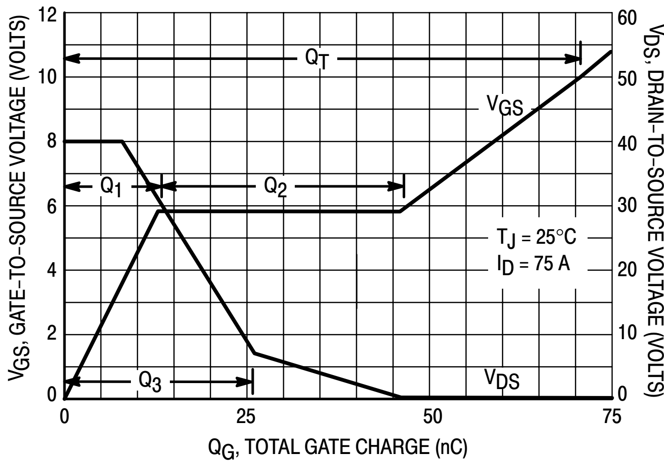



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

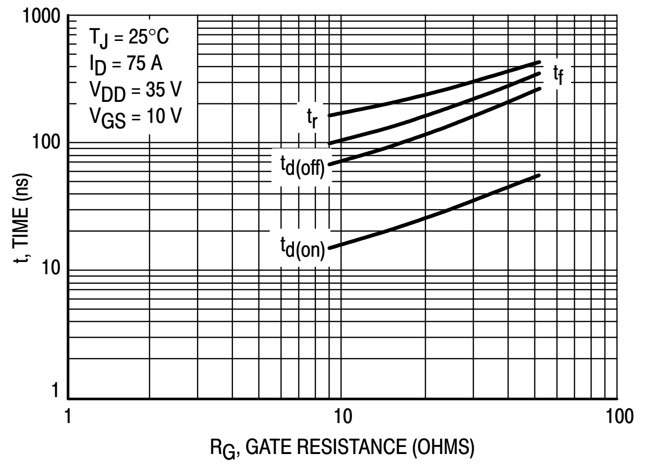



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

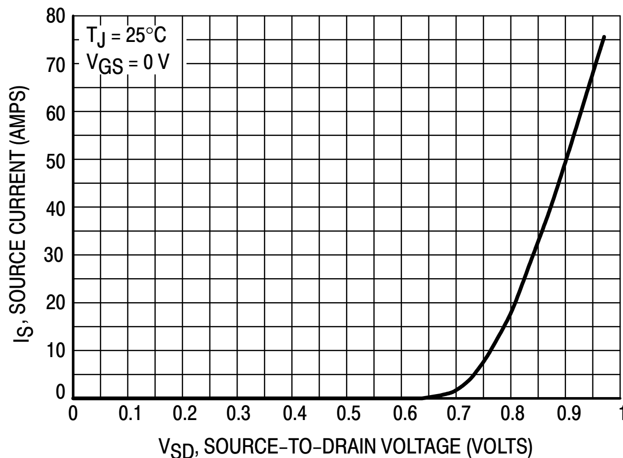



**Figure 10. Diode Forward Voltage versus Current**

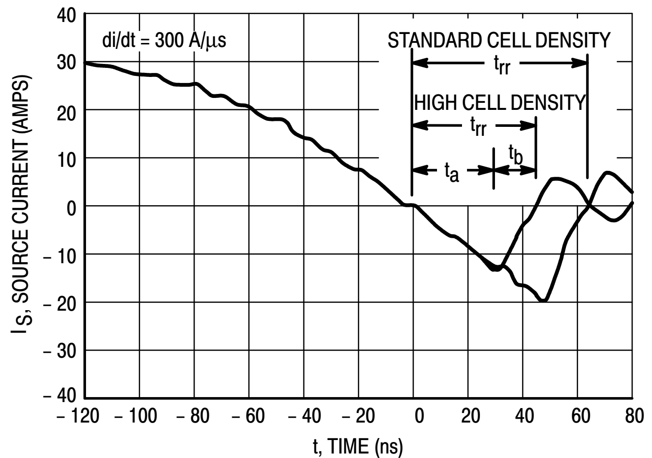



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

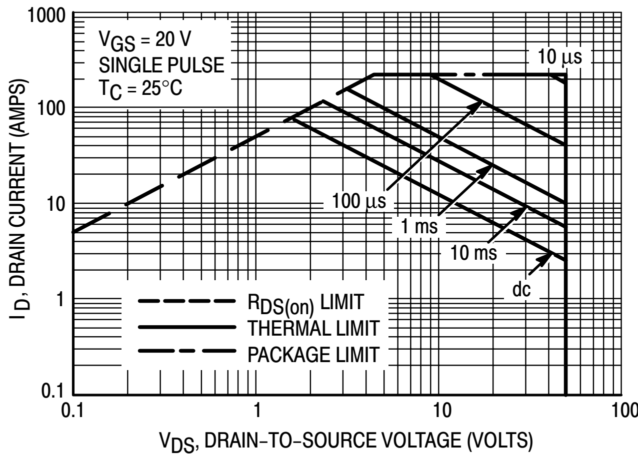



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

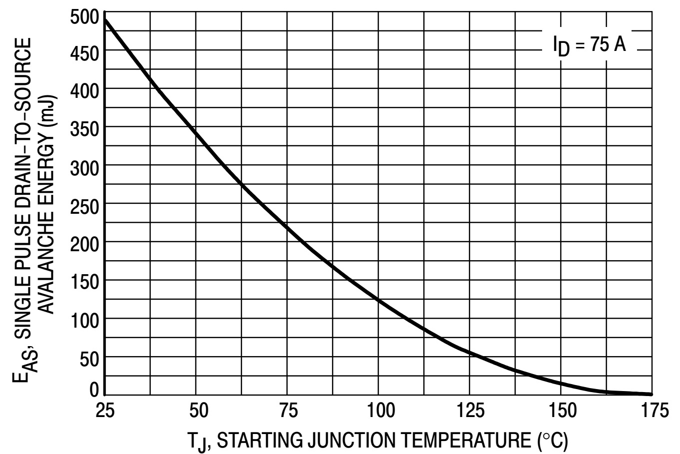



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

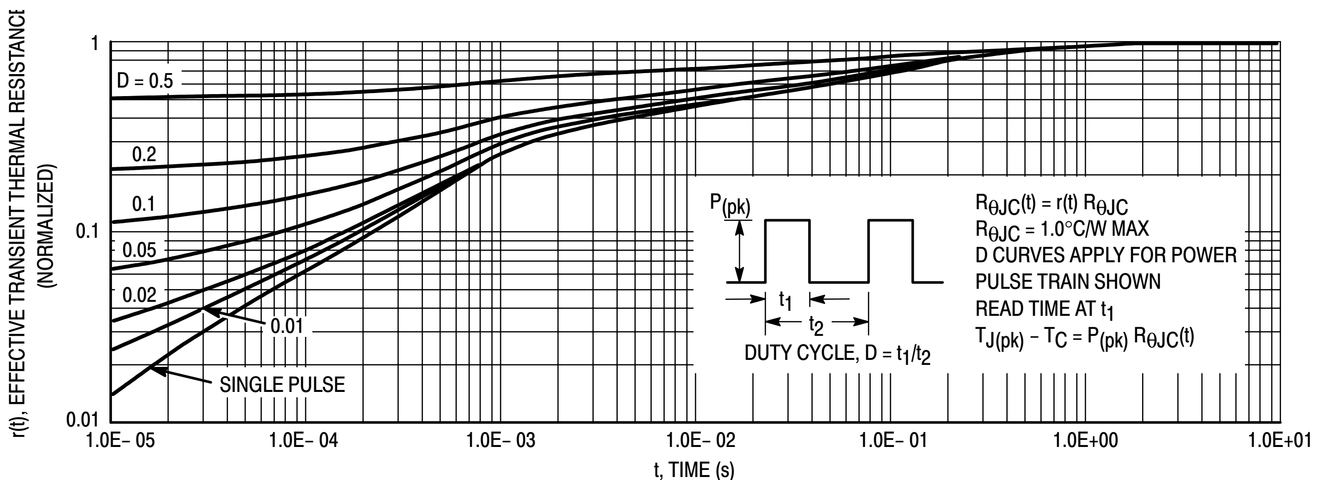



**Figure 14. Thermal Response**

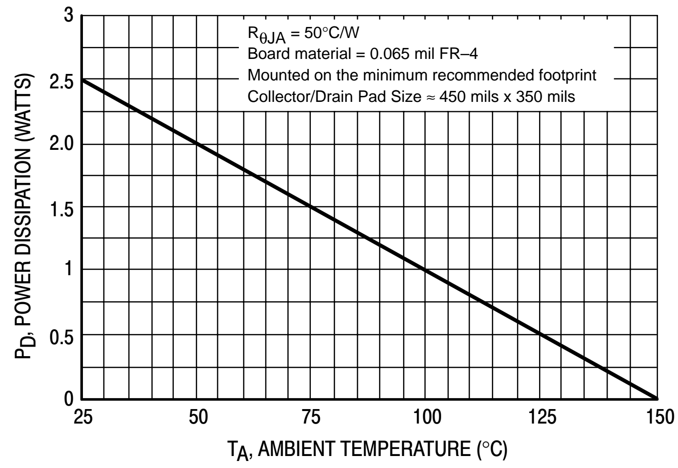



**Figure 15. D2PAK Power Derating Curve**

# MTB75N06HD

**Preferred Device**

# Power MOSFET 75 Amps, 60 Volts

## N–Channel $D^2PAK$

**ON Semiconductor™**

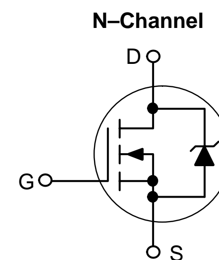
**http://onsemi.com**

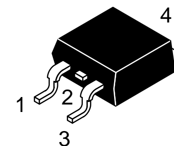
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Short Heatsink Tab Manufactured – Not Sheared
- Specially Designed Leadframe for Maximum Power Dissipation

**75 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 10 mΩ**

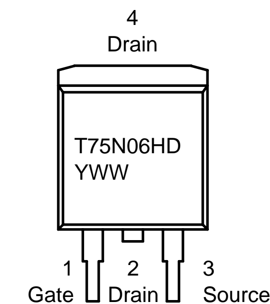
**N–Channel**




**$D^2PAK$**
**CASE 418B**
**STYLE 2**

**MARKING DIAGRAM & PIN ASSIGNMENT**




T75N06HD = Device Code
Y = Year
WW = Work Week

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>50<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note NO TAG) | $P_D$ | 125<br>1.0<br>2.5 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 75 Apk, L = 0.177 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note NO TAG) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 1.0<br>62.5<br>50 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTB75N06HD | $D^2PAK$ | 50 Units/Rail |
| MTB75N06HDT4 | $D^2PAK$ | 800/Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>68<br>60.4 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 V) | | $I_{GSS}$ | – | 5.0 | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 5.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>8.38 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>8.3 | <br>10 | mΩ |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 75 Adc)<br>($I_D$ = 37.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.7<br>0.53 | <br>0.9<br>0.8 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 37.5 Adc) | | $g_{FS}$ | 15 | 32 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2800 | 3920 | pF |
| Output Capacitance | | $C_{oss}$ | – | 928 | 1300 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 180 | 252 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 30 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 18 | 26 | ns |
| Rise Time | | $t_r$ | – | 218 | 306 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 67 | 94 | |
| Fall Time | | $t_f$ | – | 125 | 175 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 71 | 100 | nC |
| | | $Q_1$ | – | 16.3 | – | |
| | | $Q_2$ | – | 31 | – | |
| | | $Q_3$ | – | 29.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.97<br>0.88 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 75 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 44 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.103 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

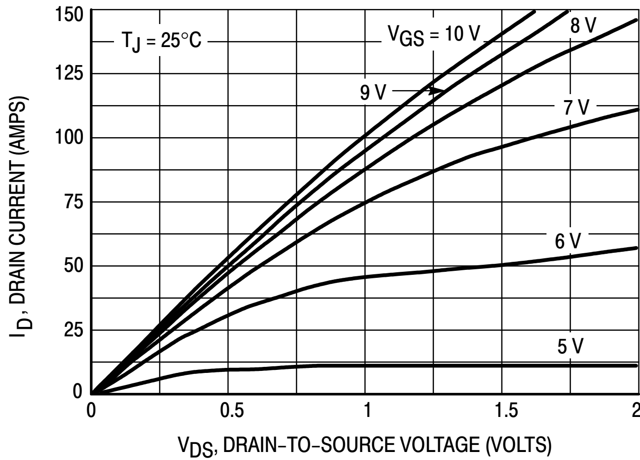



**Figure 1. On–Region Characteristics**

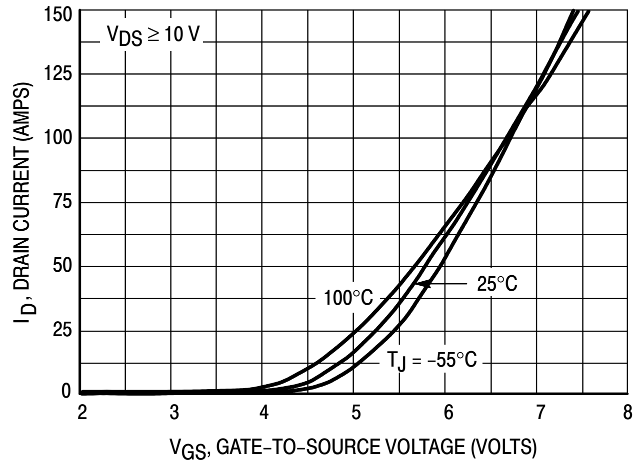



**Figure 2. Transfer Characteristics**

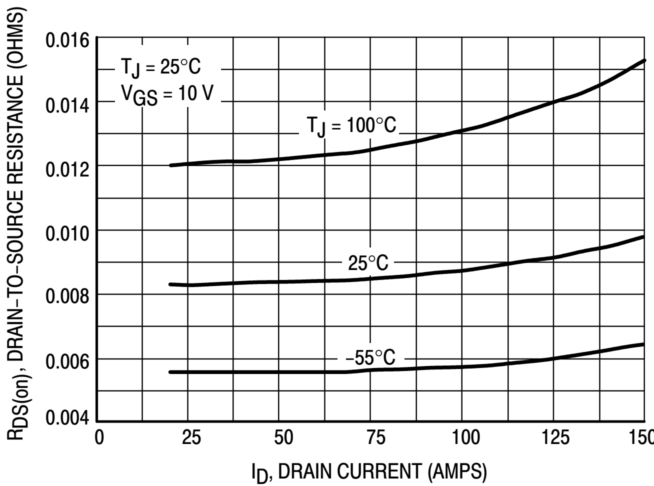



**Figure 3. On–Resistance versus Drain Current and Temperature**

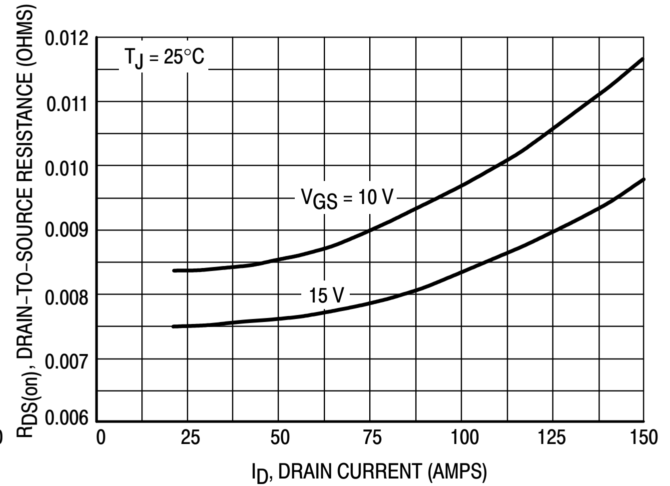



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

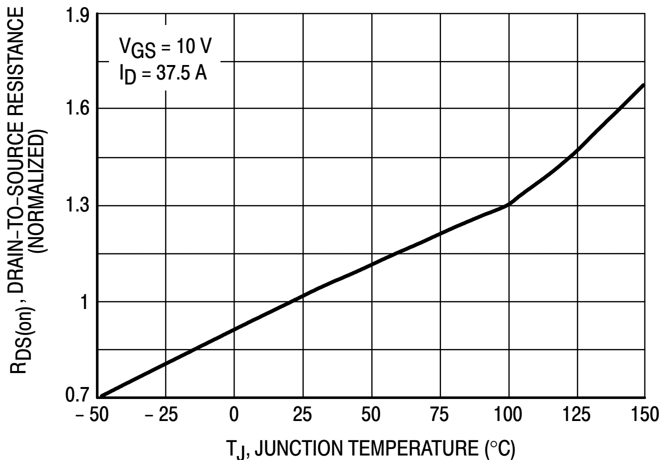



**Figure 5. On–Resistance Variation with Temperature**

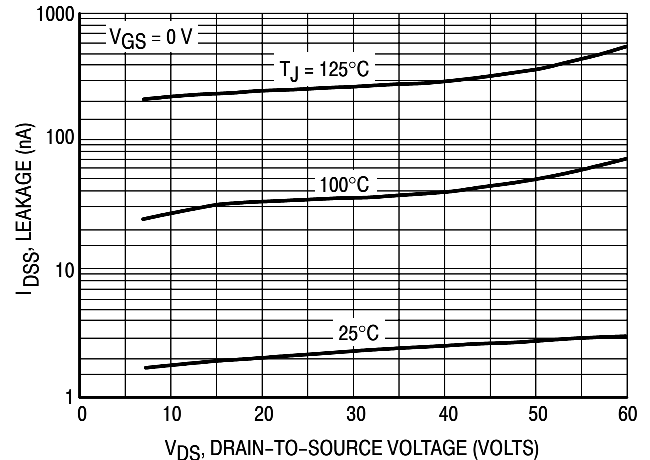



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

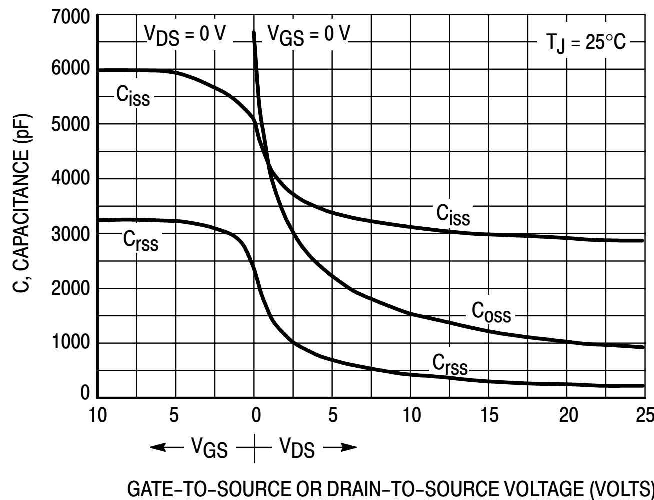



**Figure 7. Capacitance Variation**

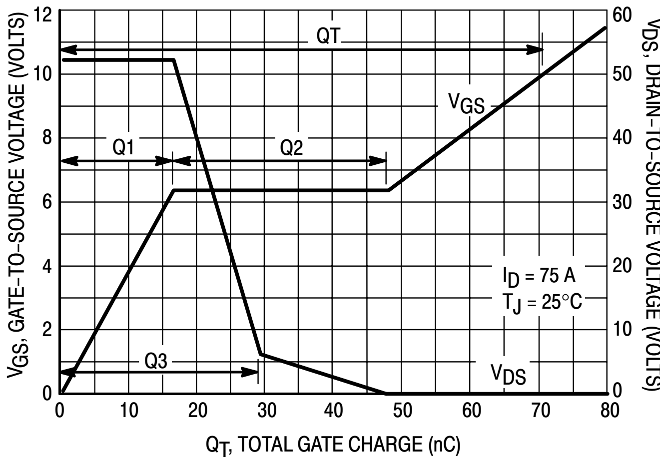



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

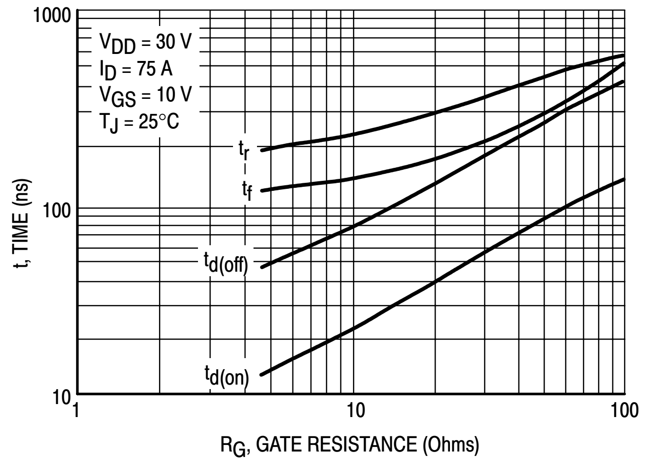



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

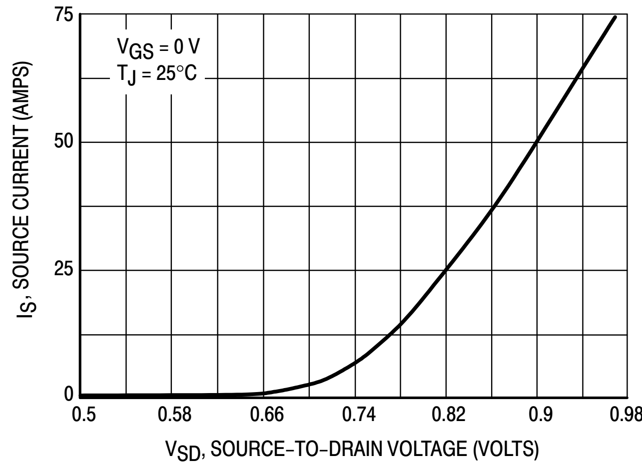



**Figure 10. Diode Forward Voltage versus Current**

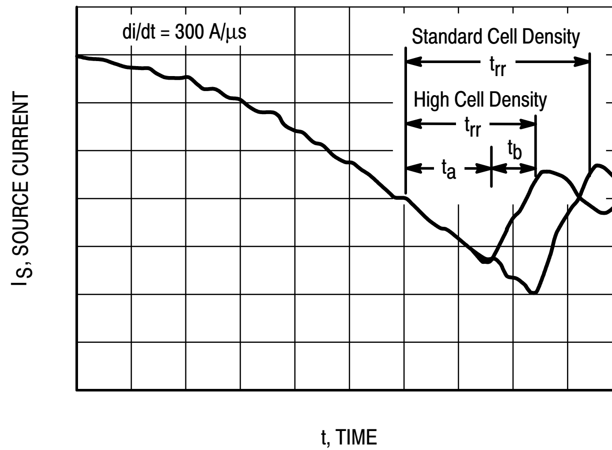



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

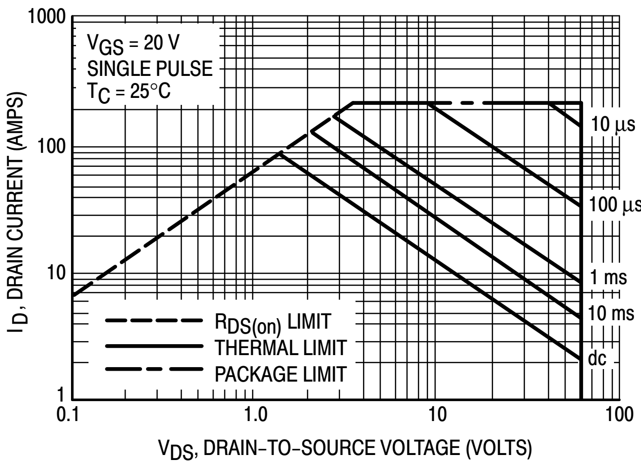



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

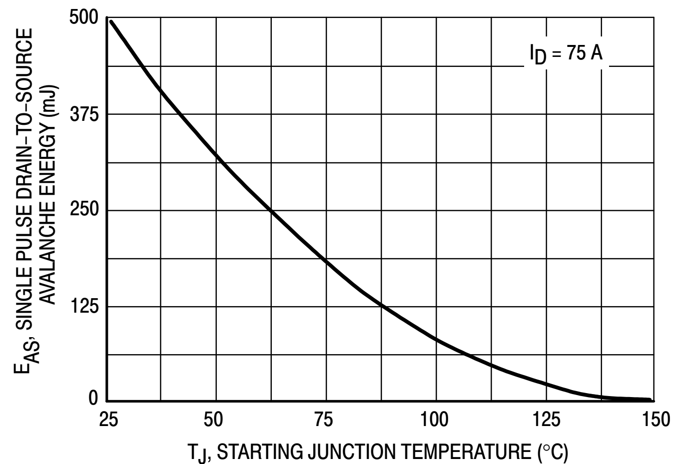



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

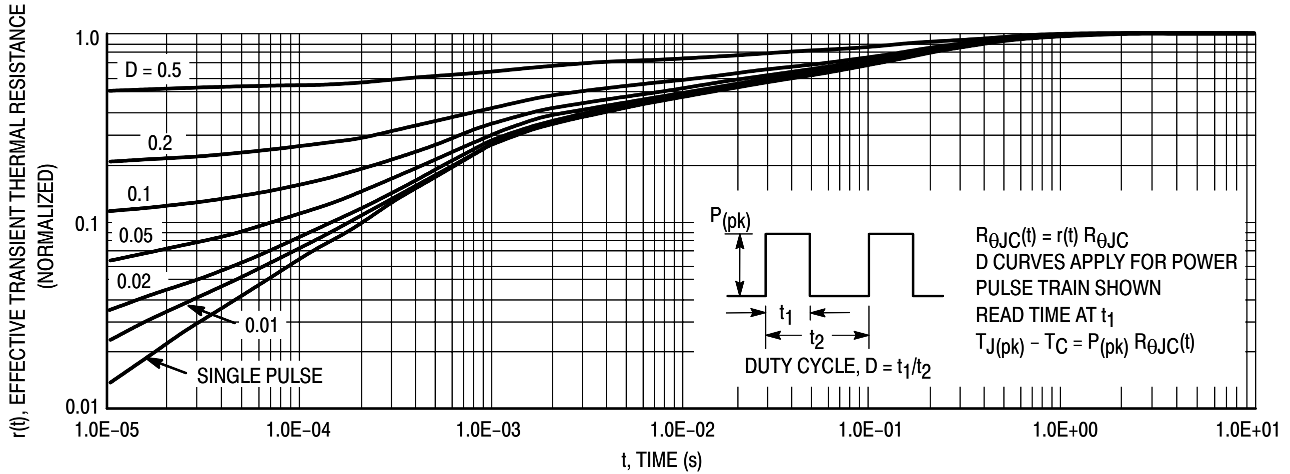



**Figure 14. Thermal Response**

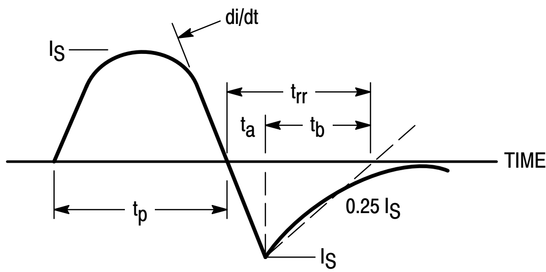



**Figure 15. Diode Reverse Recovery Waveform**

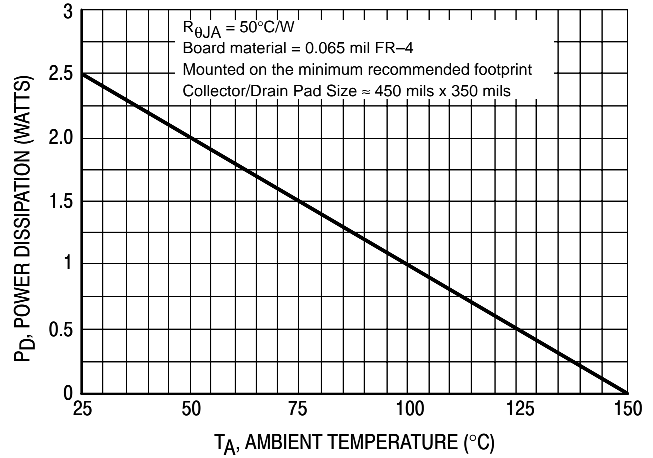
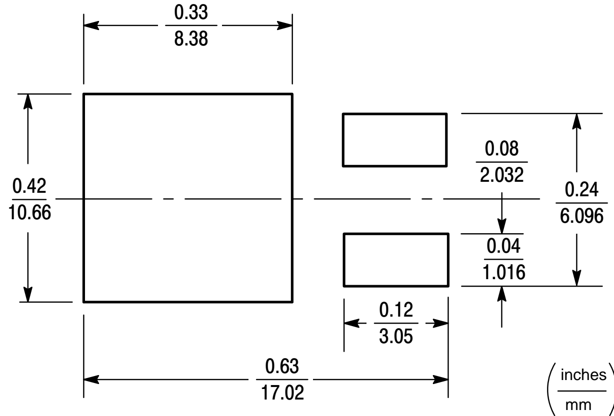



**Figure 16. D2PAK Power Derating Curve**

# INFORMATION FOR USING THE $D^2$PAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a $D^2$PAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{50°C/W} = 2.5 \text{ Watts}$$

The 50°C/W for the $D^2$PAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.5 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 17.

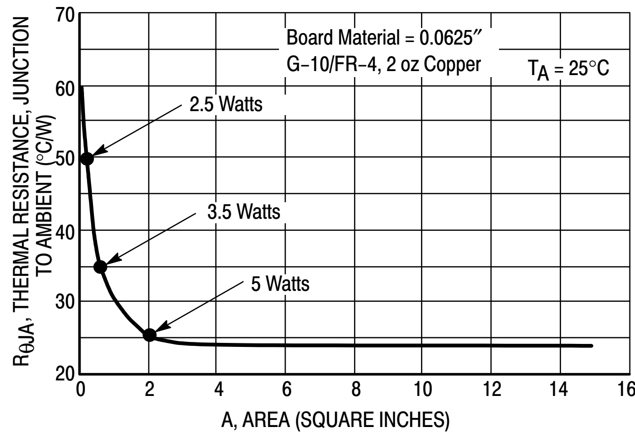



**Figure 17. Thermal Resistance versus Drain Pad Area for the $D^2$PAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 18 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

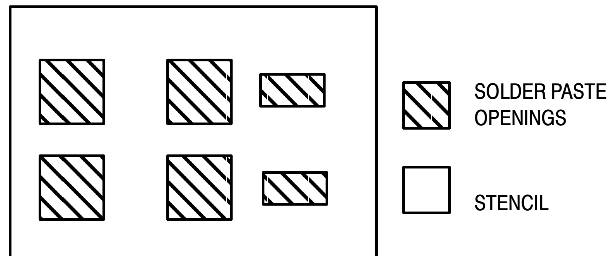



**Figure 18. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 19 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

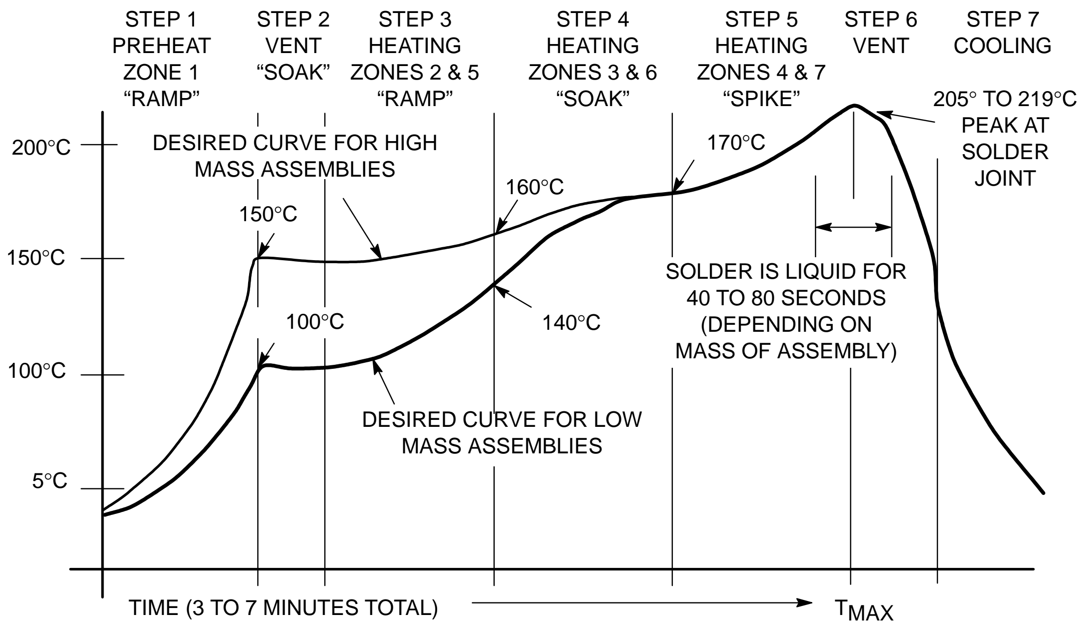



**Figure 19. Typical Solder Heating Profile**

# MTD1302

*Advance Information*

# Power MOSFET 20 Amps, 30 Volts

## N–Channel DPAK

ON Semiconductor™

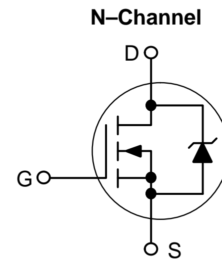
http://onsemi.com

**20 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 22 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters, and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode Is Characterized for Use In Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

N–Channel



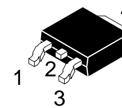

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive (tp ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>16<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C<br>(Note 1.) | $P_D$ | 74<br>0.592<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 20 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 200 | mJ |
| Thermal Resistance<br>Junction to Case<br>Junction–to–Ambient<br>Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5.0 seconds | $T_L$ | 260 | °C |

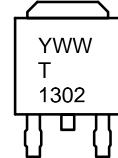
1. When surface mounted to an FR4 board using the minimum recommended pad size.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

**MARKING DIAGRAM**

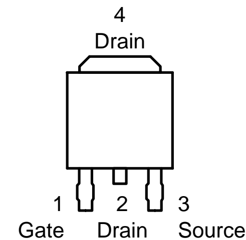



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD1302 | DPAK | 75 Units/Rail |
| MTD1302–1 | DPAK | 75 Units/Rail |
| MTD1302T4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 0.019 | 0.022 | Ohms |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | | – | 0.026 | 0.029 | |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc) | | $V_{DS(on)}$ | – | 0.38 | 0.5 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc, $T_J$ = 150°C) | | | – | – | 0.33 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 10 | 16 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 755 | 1162 | pF |
| Output Capacitance | | $C_{oss}$ | – | 370 | 518 | |
| Transfer Capacitance | | $C_{rss}$ | – | 102 | 204 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.2 | 15 | ns |
| Rise Time | | $t_r$ | – | 52 | 104 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 90 | |
| Fall Time | | $t_f$ | – | 73 | 146 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 14.5 | 21.8 | nC |
| | | $Q_1$ | – | 2.2 | – | |
| | | $Q_2$ | – | 8.8 | – | |
| | | $Q_3$ | – | 6.8 | – | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 27 | 40.5 | nC |
| | | $Q_1$ | – | 2.2 | – | |
| | | $Q_2$ | – | 10 | – | |
| | | $Q_3$ | – | 7.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.83 | 1.1 | Vdc |
| | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.79 | – | |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 19 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 36 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

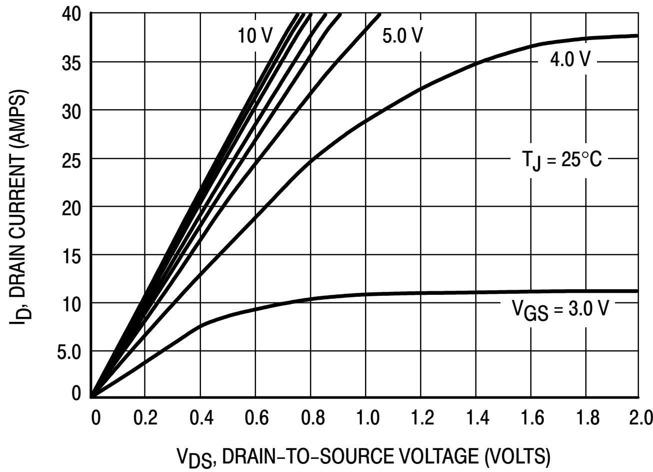



**Figure 1. On–Region Characteristics**

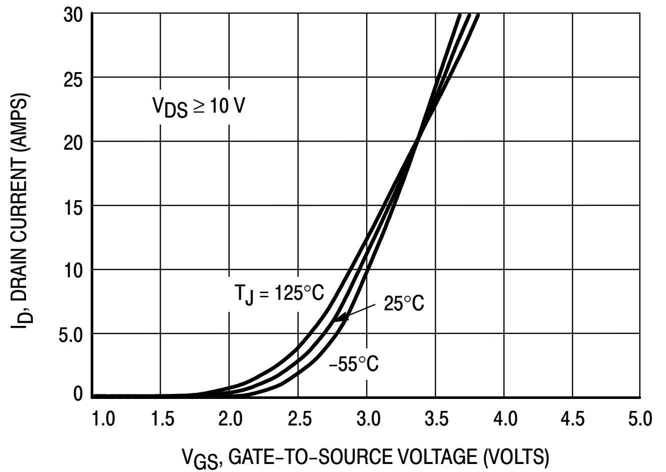



**Figure 2. Transfer Characteristics**

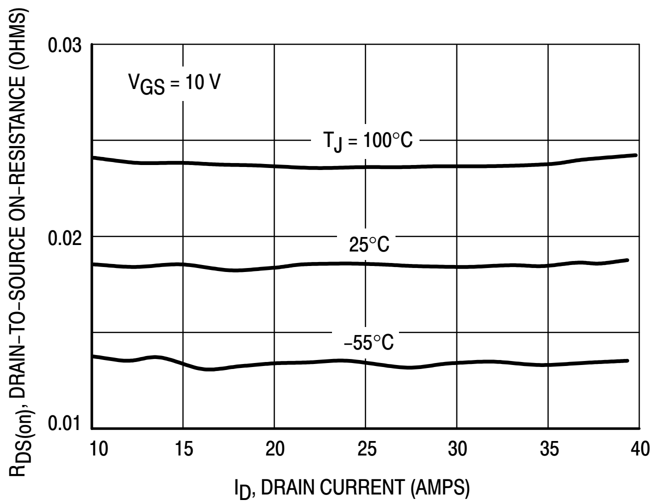



**Figure 3. On–Resistance versus Drain Current and Temperature**

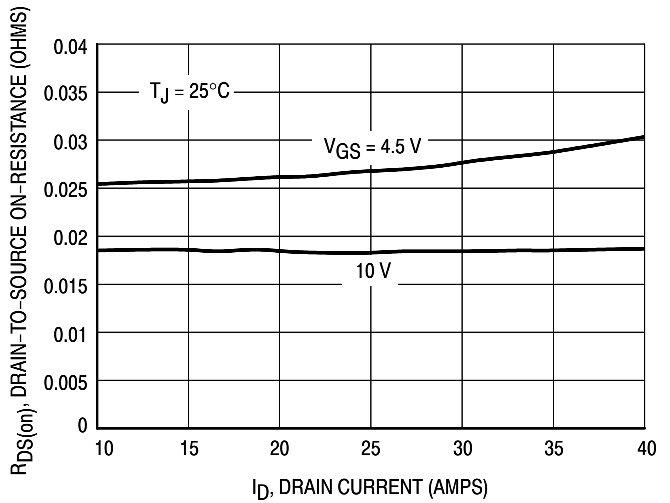



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

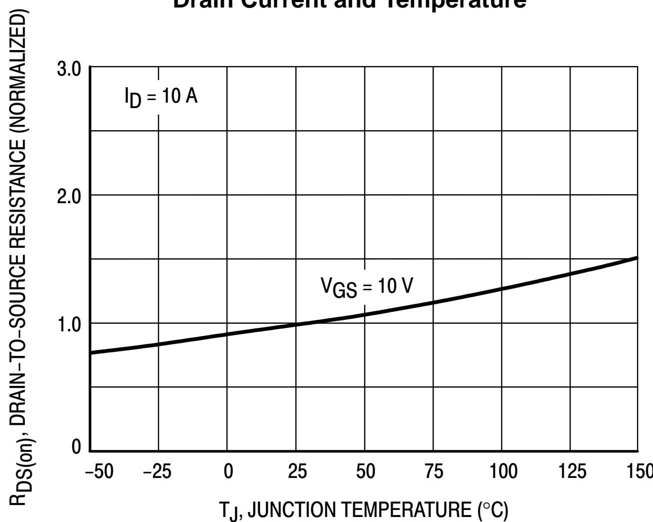



**Figure 5. On–Resistance Variation with Temperature**

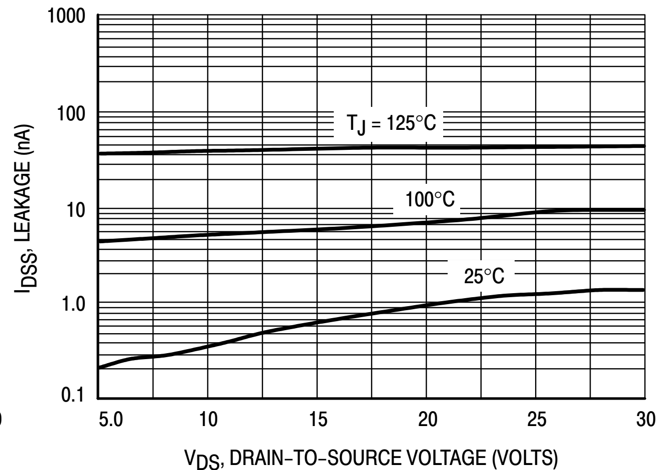



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \mathrm{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \mathrm{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

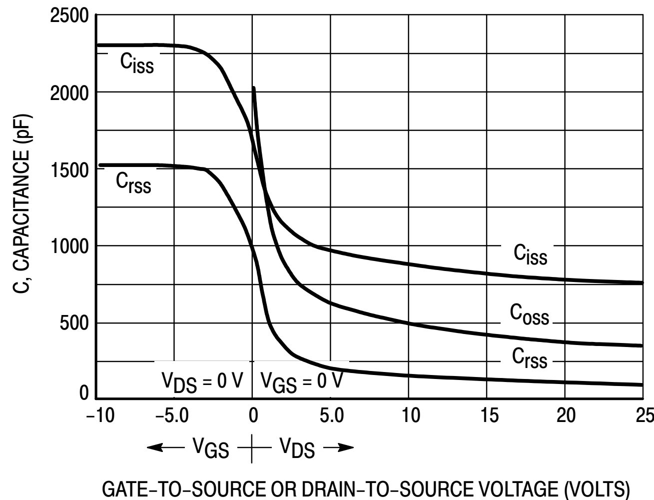



**Figure 7. Capacitance Variation**

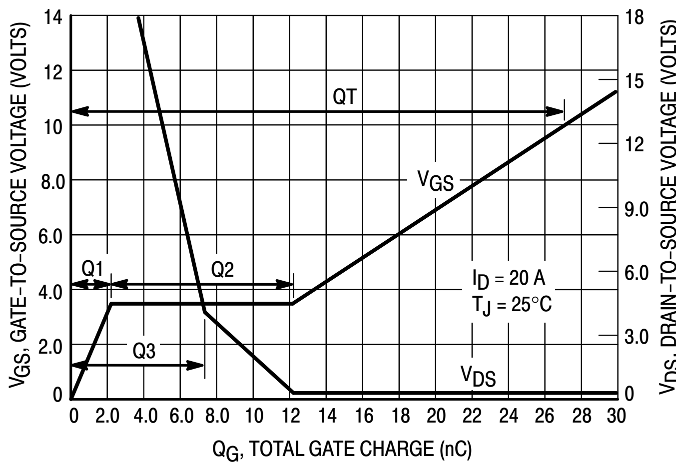



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

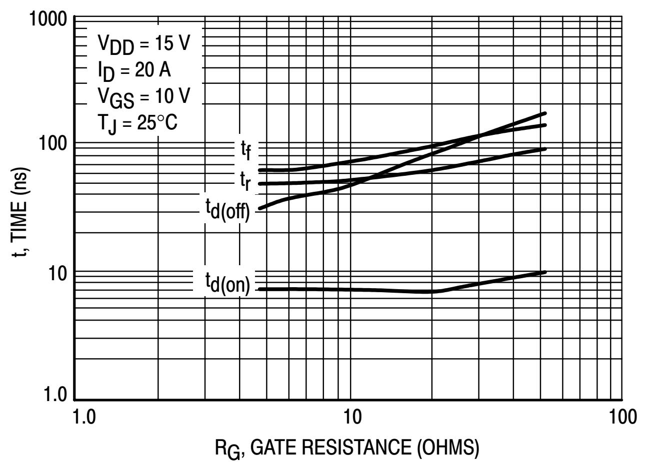



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

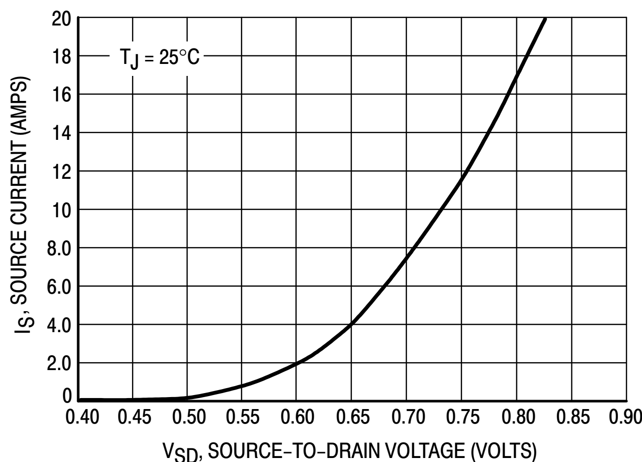



**Figure 10. Diode Forward Voltage versus Current**

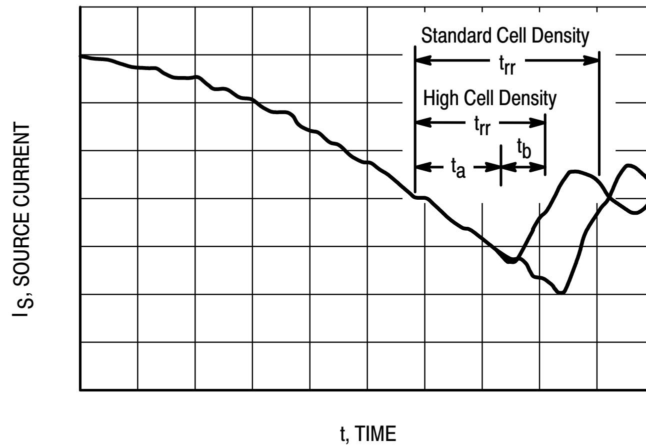



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

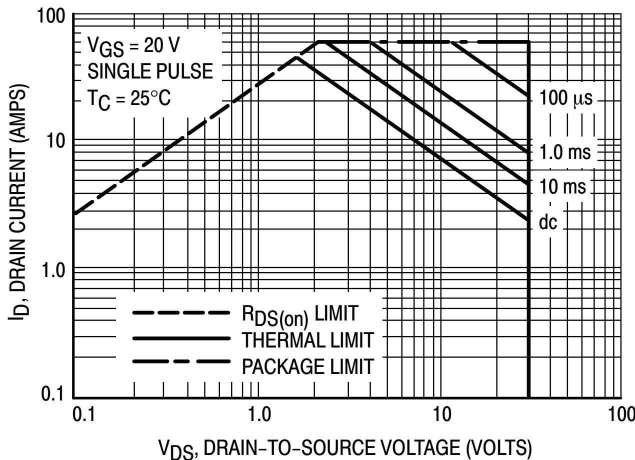



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

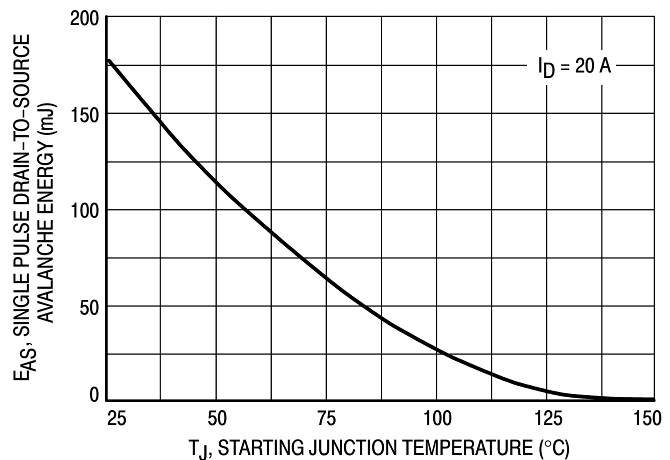



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

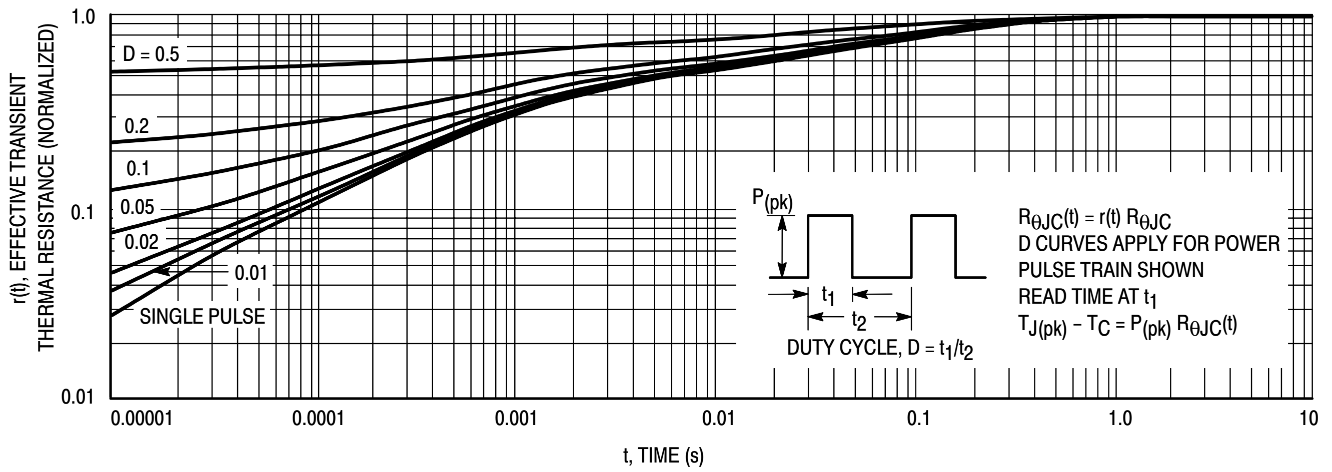



**Figure 14. Thermal Response**

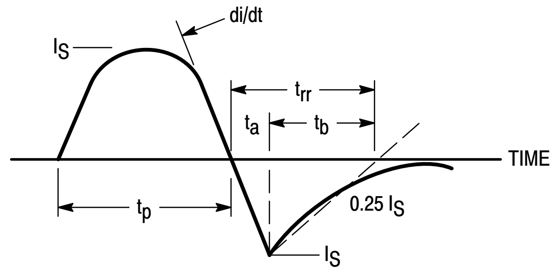
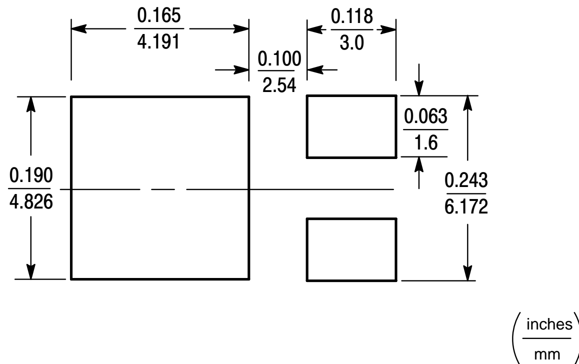



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

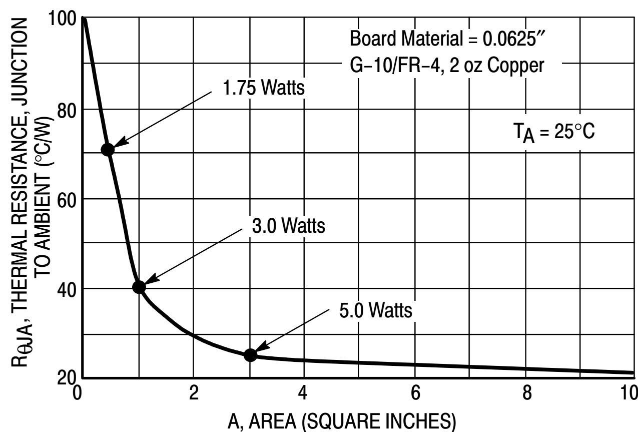



**Figure 16. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

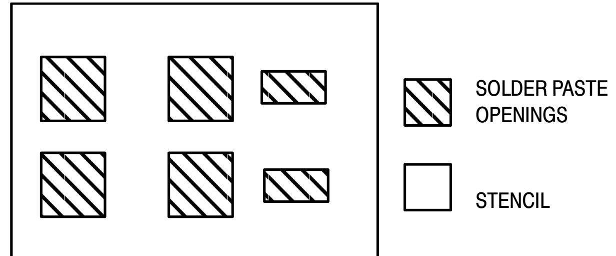



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

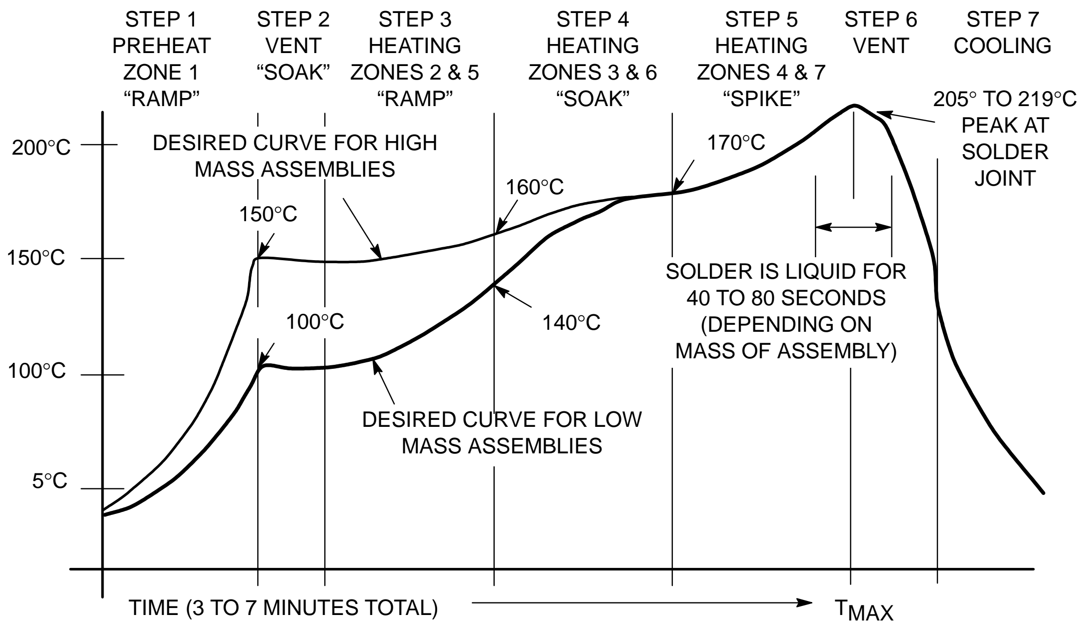



**Figure 18. Typical Solder Heating Profile**

# MTD15N06V

Preferred Device

# Power MOSFET 15 Amps, 60 Volts
## N–Channel DPAK

**ON Semiconductor™**

http://onsemi.com

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

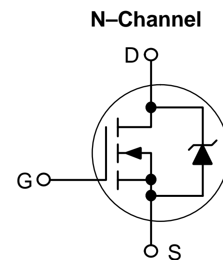
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

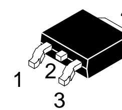
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Single Pulse ($t_p \leq$ 50 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 15<br>8.7<br>45 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 55<br>0.36<br>2.1 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 15 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 113 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.73<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**15 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

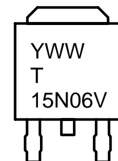
**N–Channel**




**MARKING DIAGRAM**

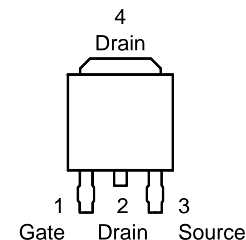



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD15N06V | DPAK | 75 Units/Rail |
| MTD15N06V1 | DPAK | 75 Units/Rail |
| MTD15N06VT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 3
Publication Order Number:
MTD15N06V/D

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>67 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>5.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 7.5 Adc) | | $R_{DS(on)}$ | – | 0.08 | 0.12 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 15 Adc)<br>($I_D$ = 7.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 2.0<br>– | 2.2<br>1.9 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 7.5 Adc) | | $g_{FS}$ | 4.0 | 6.2 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 469 | 660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 148 | 200 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 35 | 60 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.6 | 20 | ns |
| Rise Time | | $t_r$ | – | 51 | 100 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 18 | 40 | |
| Fall Time | | $t_f$ | – | 33 | 70 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 14.4 | 20 | nC |
| | | $Q_1$ | – | 2.8 | – | |
| | | $Q_2$ | – | 6.4 | – | |
| | | $Q_3$ | – | 6.1 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.05<br>1.5 | 1.6<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 59.3 | – | ns |
| | | $t_a$ | – | 46 | – | |
| | | $t_b$ | – | 13.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.165 | – | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

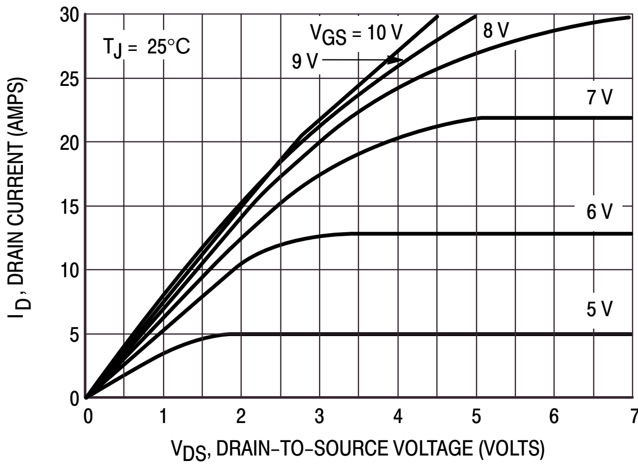



**Figure 1. On−Region Characteristics**

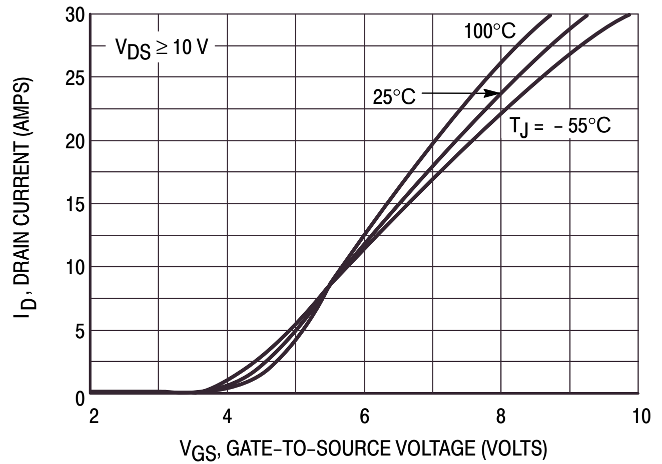



**Figure 2. Transfer Characteristics**

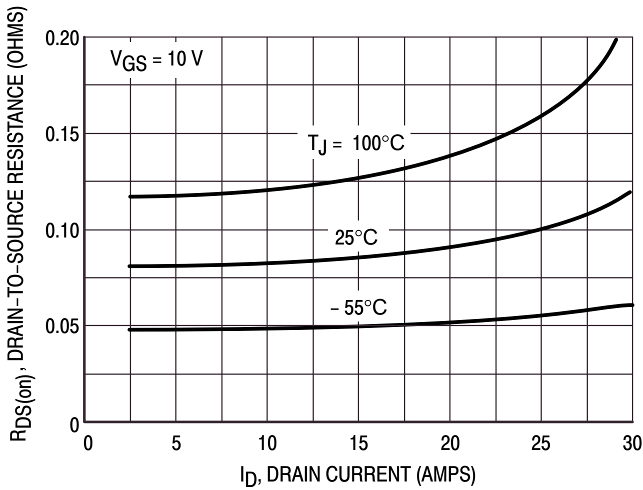



**Figure 3. On−Resistance versus Drain Current and Temperature**

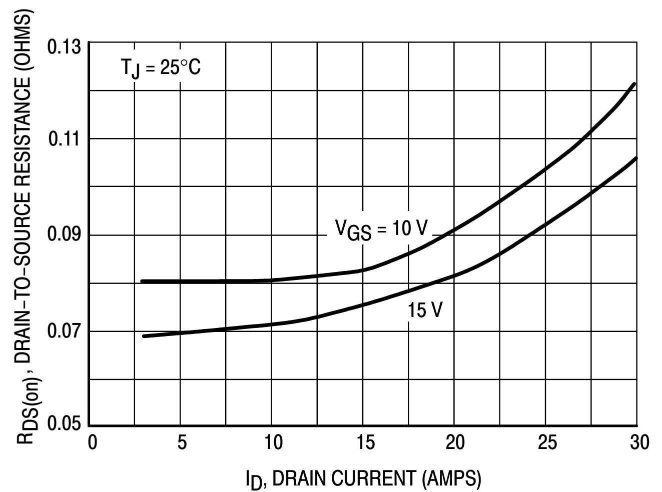



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

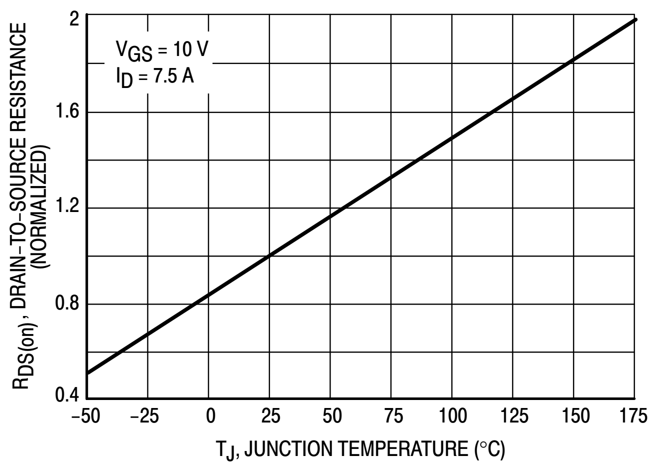



**Figure 5. On−Resistance Variation with Temperature**

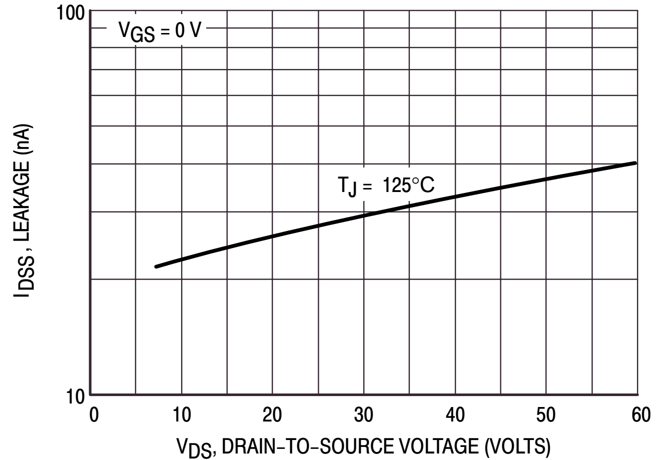



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, In \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, In \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

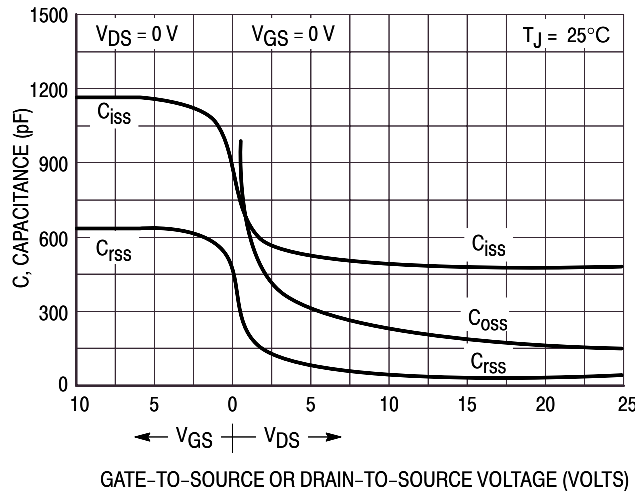



**Figure 7. Capacitance Variation**

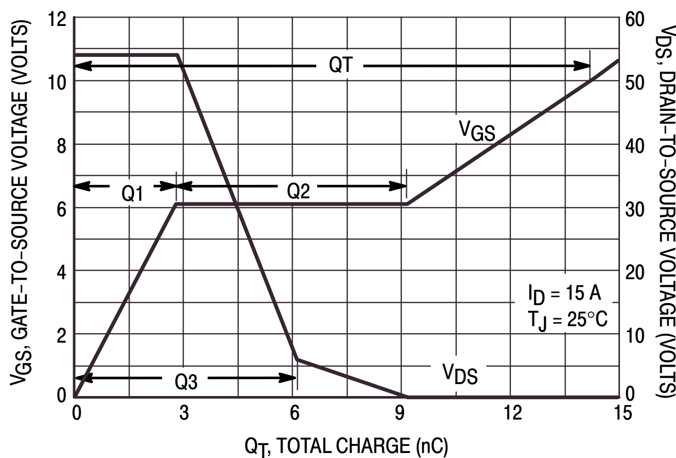



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

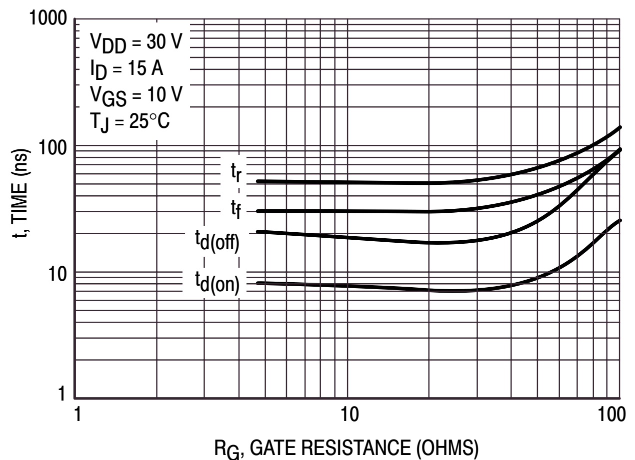



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

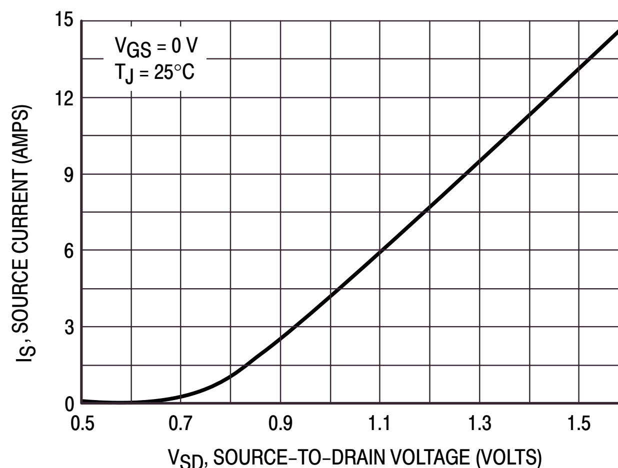



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

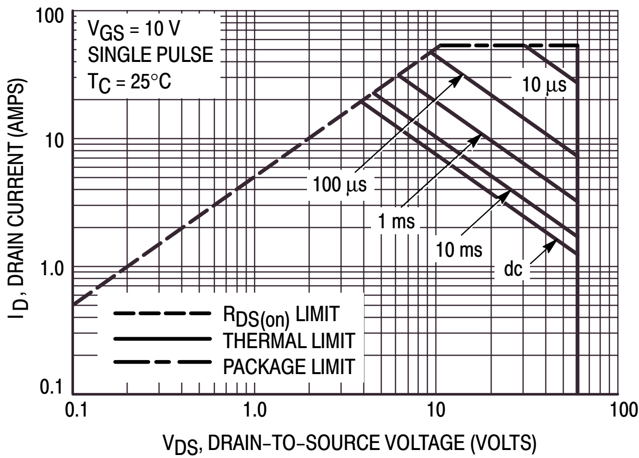



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

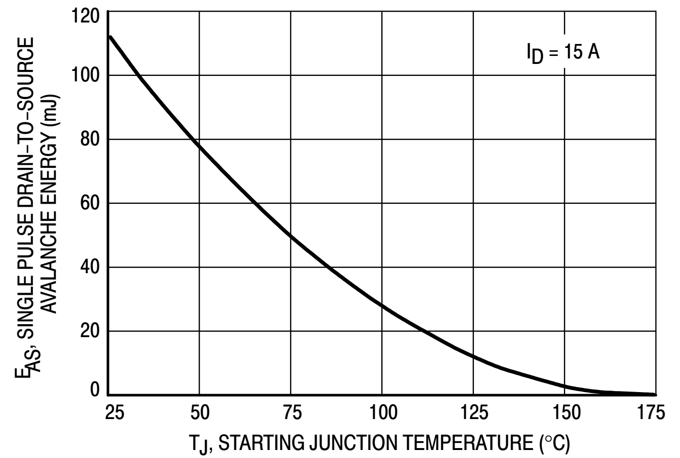



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

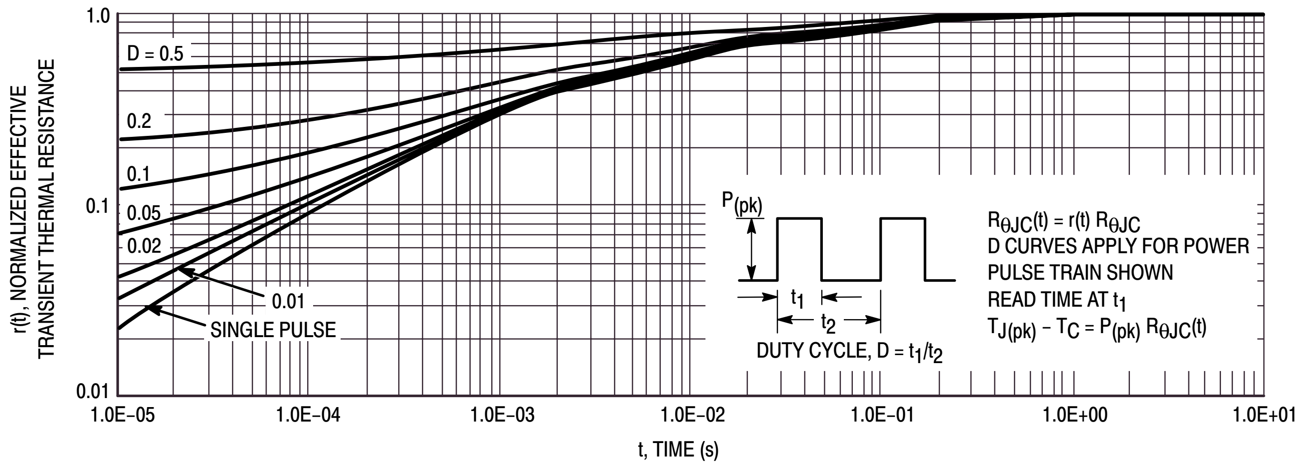



**Figure 13. Thermal Response**

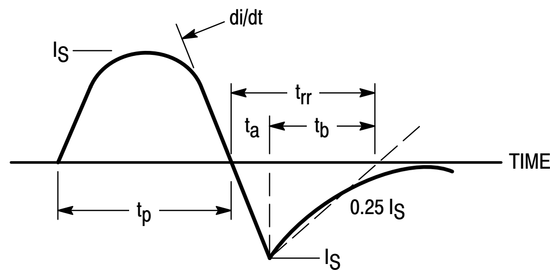
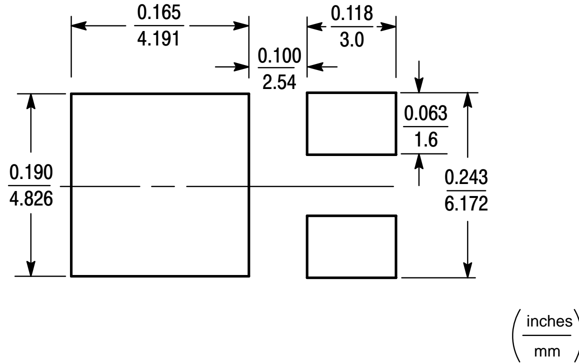



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




(inches / mm)

## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

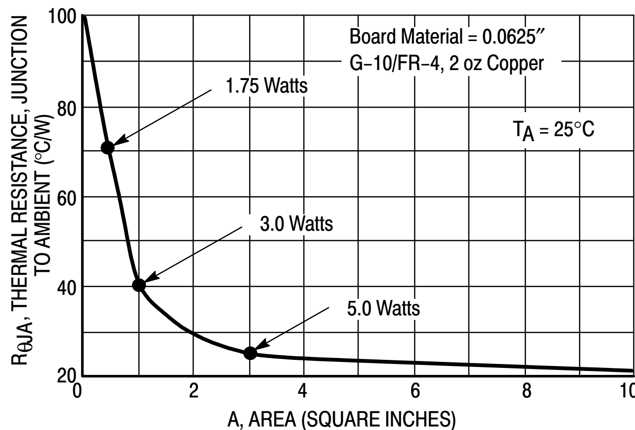



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D2PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and D2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

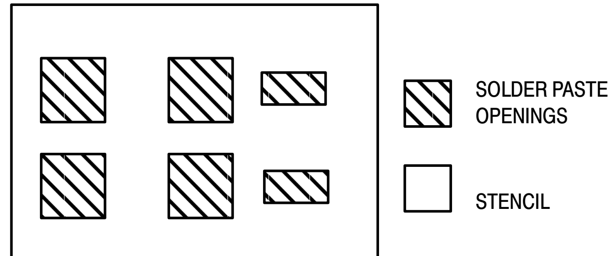



**Figure 16. Typical Stencil for DPAK and D2PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D2PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

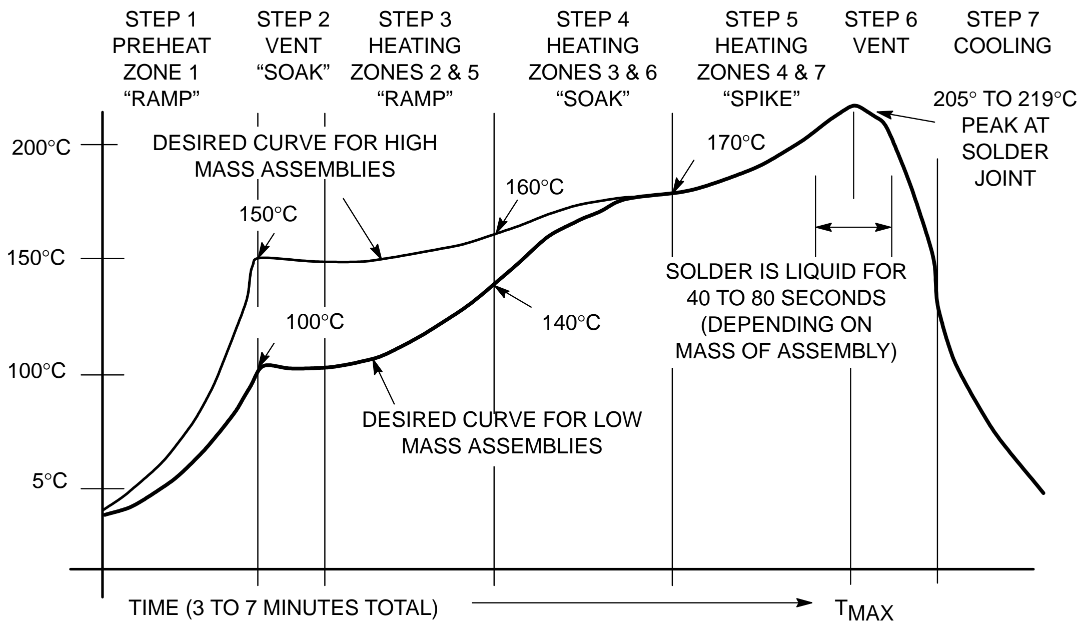



**Figure 17. Typical Solder Heating Profile**

# MTD15N06VL

# Power MOSFET 15 Amps, 60 Volts

## N–Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 15<br>12<br>53 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ 25°C (Note 1.) | $P_D$ | 60<br>0.4<br>2.1 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 113 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.5<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

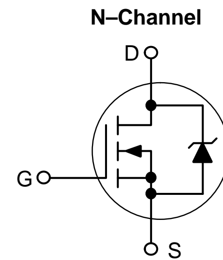
1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ON Semiconductor™**

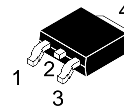
http://onsemi.com

**15 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 85 mΩ**

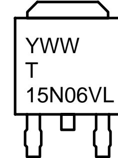
**N–Channel**




**MARKING DIAGRAM**

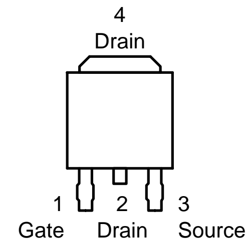



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD15N06VL | DPAK | 75 Units/Rail |
| MTD15N06VL1 | DPAK | 75 Units/Rail |
| MTD15N06VLT4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>68 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 7.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.075 | <br>0.085 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 15 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 7.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.5<br>1.3 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 7.5 Adc) | | $g_{FS}$ | 8.0 | 10 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 570 | 880 | pF |
| Output Capacitance | | $C_{oss}$ | – | 180 | 380 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 45 | 110 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 50 | ns |
| Rise Time | | $t_r$ | – | 150 | 210 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27 | 160 | |
| Fall Time | | $t_f$ | – | 70 | 140 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 12 | 20 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 7.0 | – | |
| | | $Q_3$ | – | 11 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>–<br>– | <br>0.96<br>0.85 | <br>1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 63 | – | ns |
| | | $t_a$ | – | 42 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.140 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

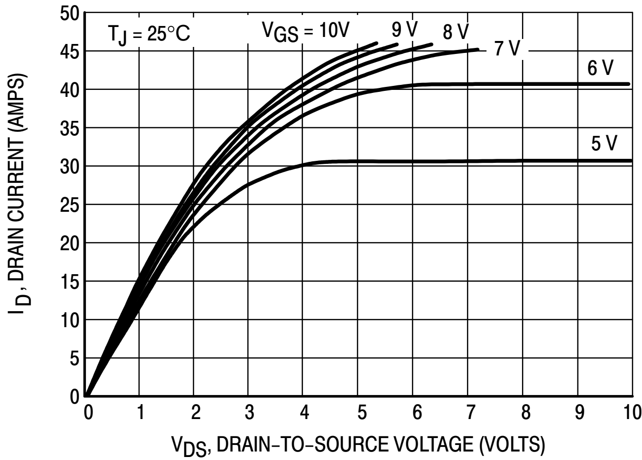



**Figure 1. On−Region Characteristics**

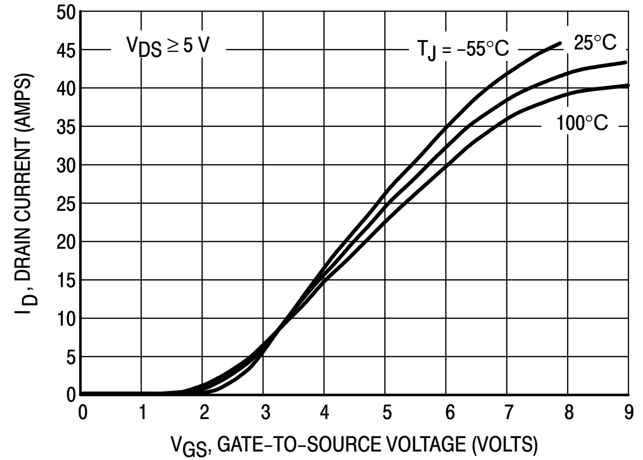



**Figure 2. Transfer Characteristics**

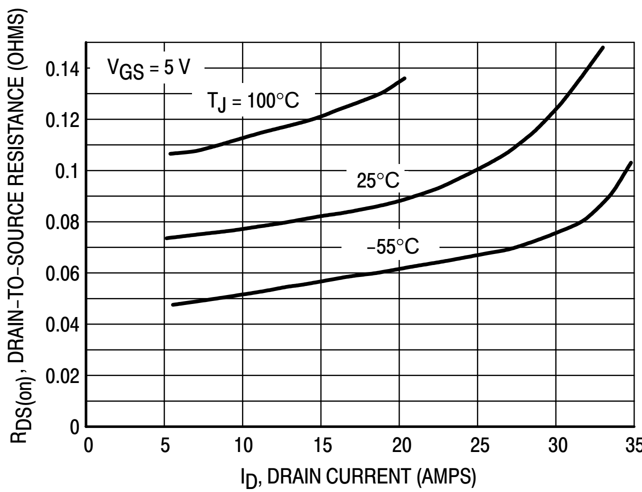



**Figure 3. On−Resistance versus Drain Current and Temperature**

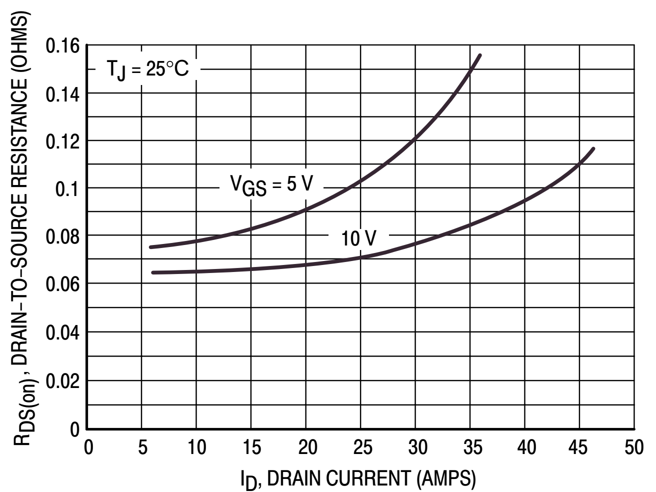



**Figure 4. On−Resistance versus Drain Current and Gate Voltage**

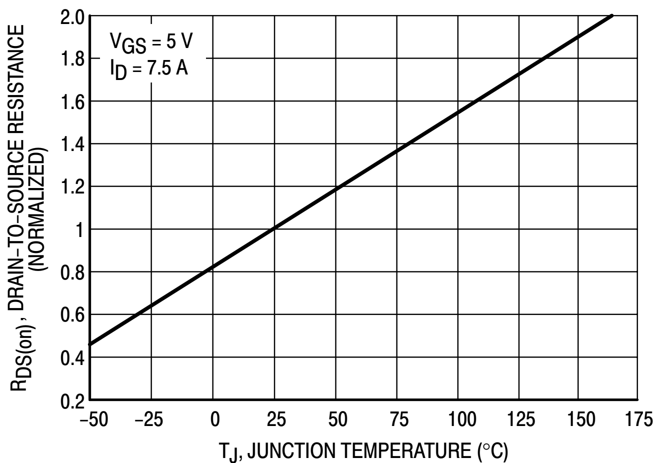



**Figure 5. On−Resistance Variation with Temperature**

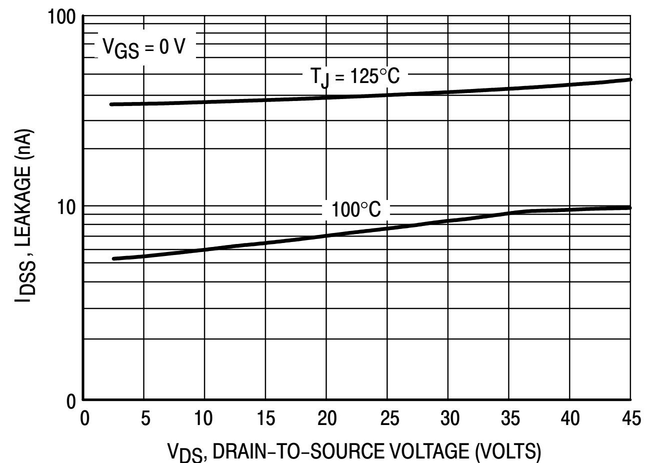



**Figure 6. Drain−To−Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

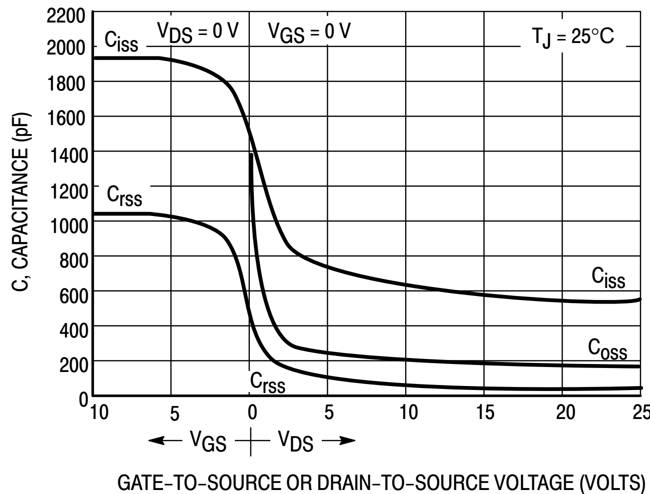



**Figure 7. Capacitance Variation**

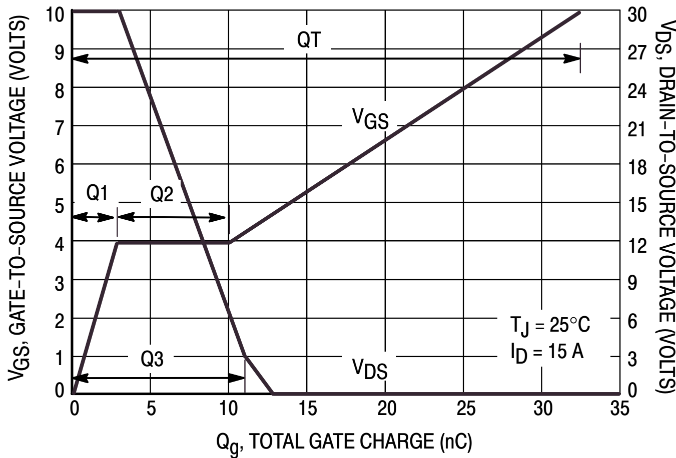



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

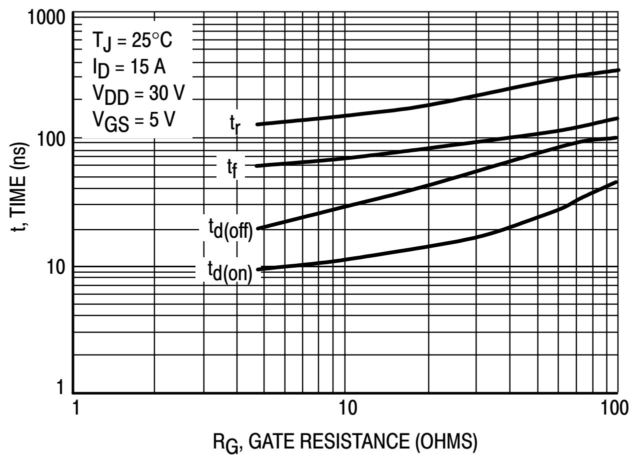



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

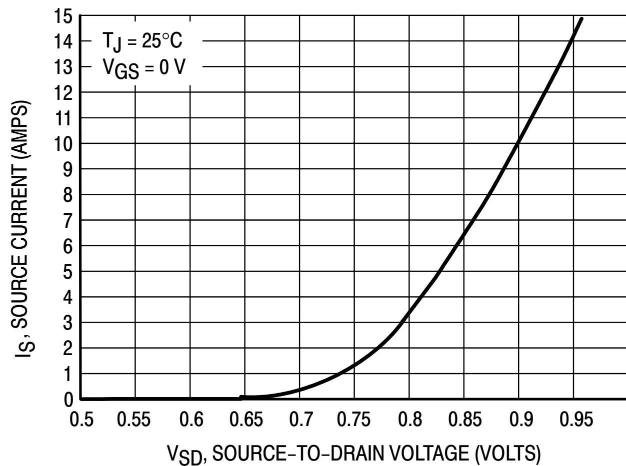



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

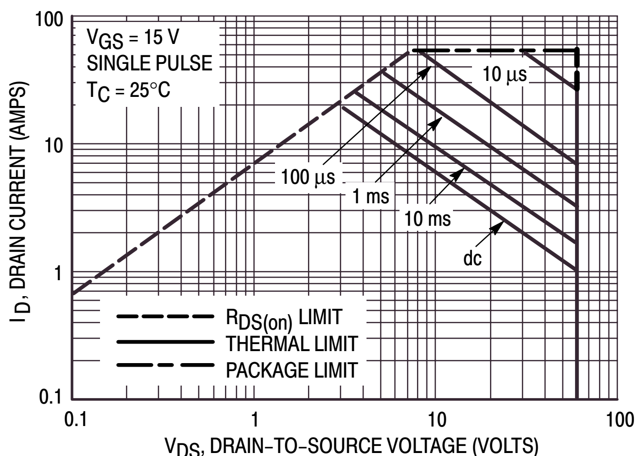



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

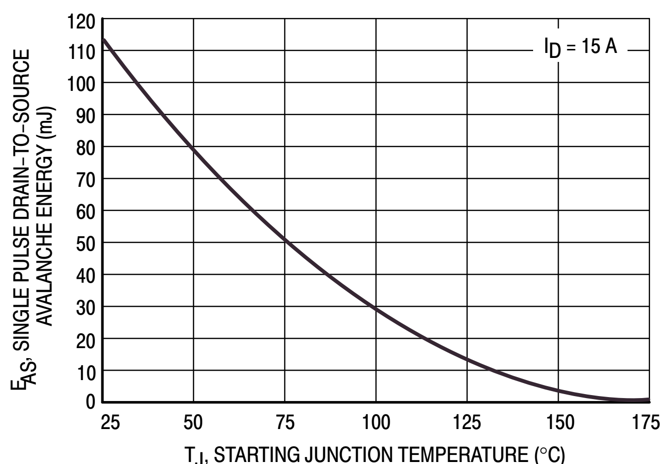



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

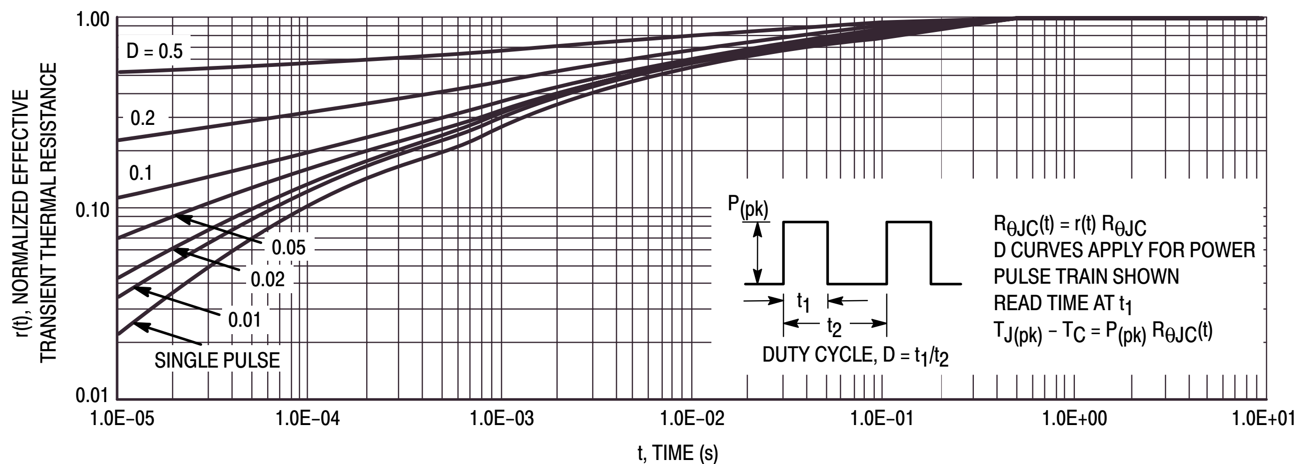



**Figure 13. Thermal Response**

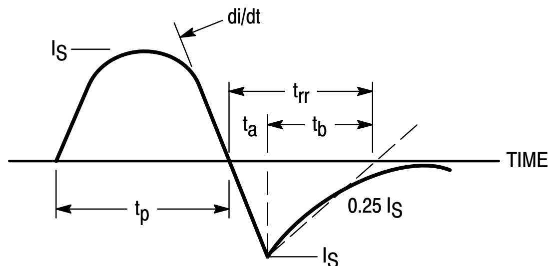
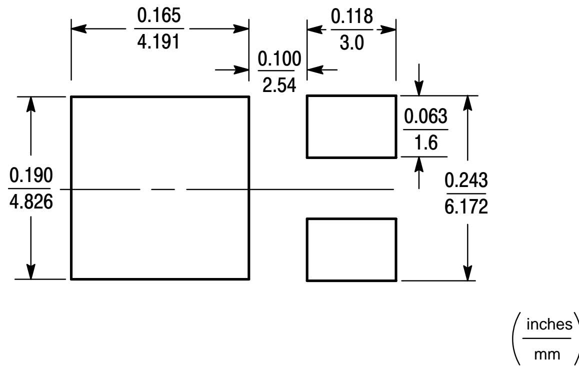



**Figure 14. Diode Reverse Recovery Waveform**

## INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

### RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




### POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

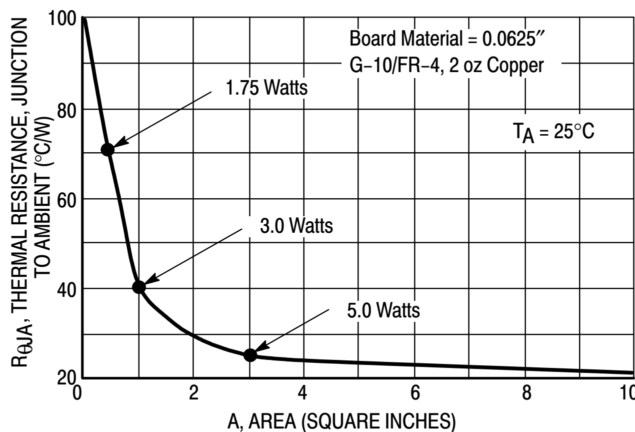



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

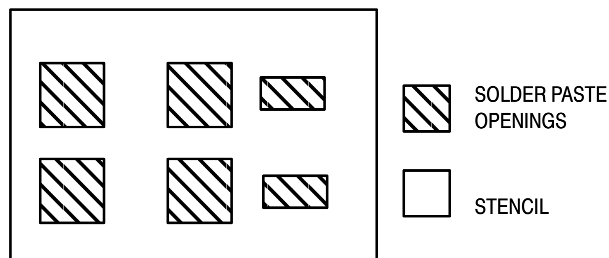



**Figure 16. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

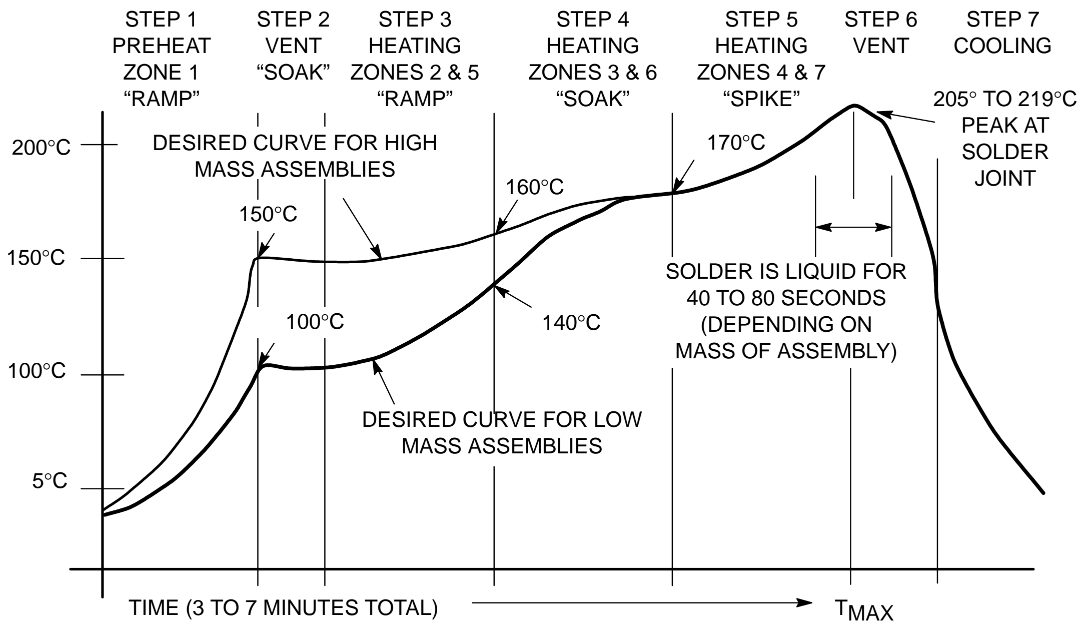



**Figure 17. Typical Solder Heating Profile**

# MTD20N03HDL

**Preferred Device**

# Power MOSFET
# 20 Amps, 30 Volts, Logic Level
## N–Channel DPAK

**ON Semiconductor™**

**http://onsemi.com**

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

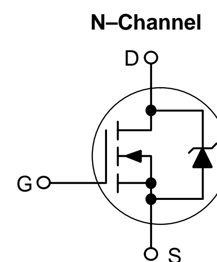
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

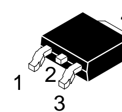
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>16<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C, when mounted with the minimum recommended pad size | $P_D$ | 74<br>0.6<br>1.75 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 20 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 200 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**20 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 35 mΩ**

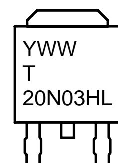
**N–Channel**




**MARKING DIAGRAM**

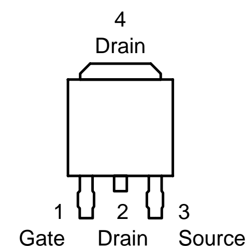



**CASE 369A**
**DPAK**
**STYLE 2**




20N03HL = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD20N03HDL | DPAK | 75 Units/Rail |
| MTD20N03HDL1 | DPAK | 75 Units/Rail |
| MTD20N03HDLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**November, 2000 – Rev. 3**

Publication Order Number:
**MTD20N03HDL/D**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>43 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>5.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 4.0 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.034<br>0.030 | <br>0.040<br>0.035 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 20 Adc)<br>($I_D$ = 10 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.55<br>– | <br>0.8<br>0.7 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | <br>10 | <br>13 | <br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 880 | 1260 | pF |
| Output Capacitance | | $C_{oss}$ | – | 300 | 420 | |
| Transfer Capacitance | | $C_{rss}$ | – | 80 | 150 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 13 | 20 | ns |
| Rise Time | | $t_r$ | – | 212 | 238 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 23 | 40 | |
| Fall Time | | $t_f$ | – | 84 | 140 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 24 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 13.4 | 18.9 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 7.3 | – | |
| | | $Q_3$ | – | 6.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage<br>($C_{pk}$ ≥ 2.0) (Note 3.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.95<br>0.87 | <br>1.1<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 15) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 33 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 10 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 33 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk}$ = Absolute Value of Spec (Spec–AVG/3.516 μA).

## TYPICAL ELECTRICAL CHARACTERISTICS

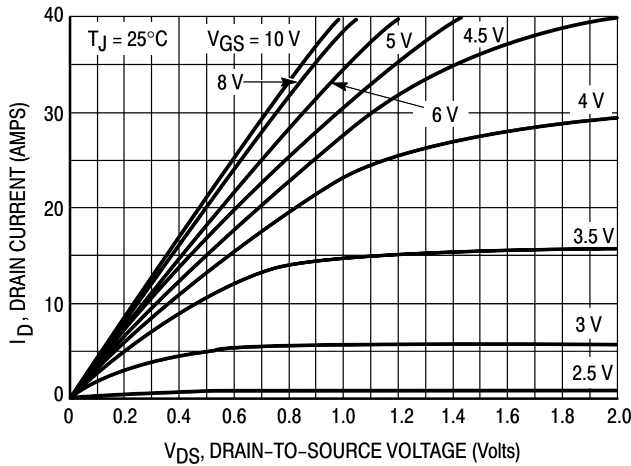



**Figure 1. On–Region Characteristics**

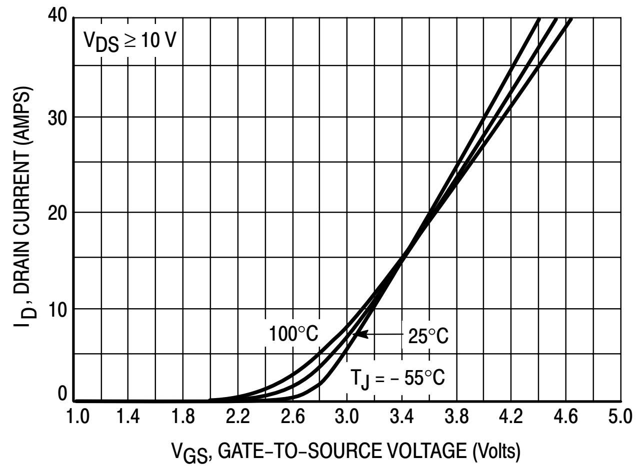



**Figure 2. Transfer Characteristics**

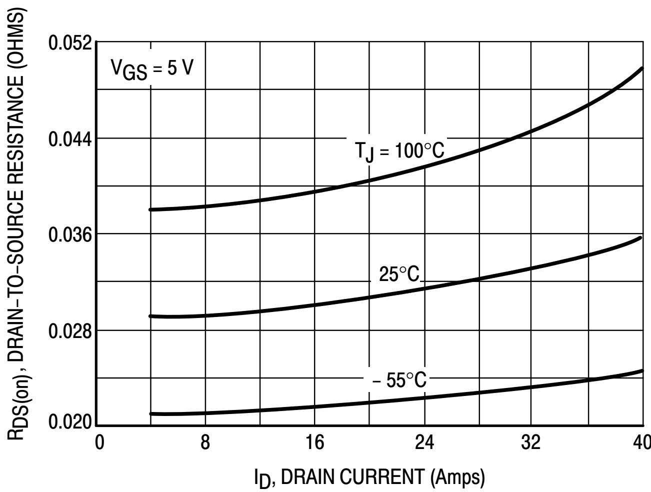



**Figure 3. On–Resistance versus Drain Current and Temperature**

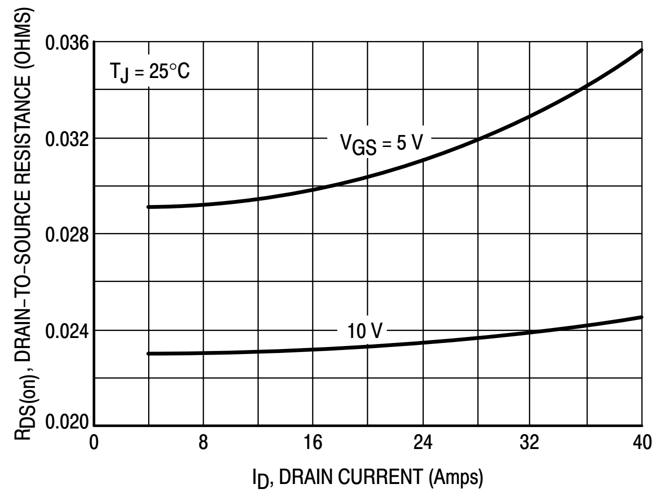



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

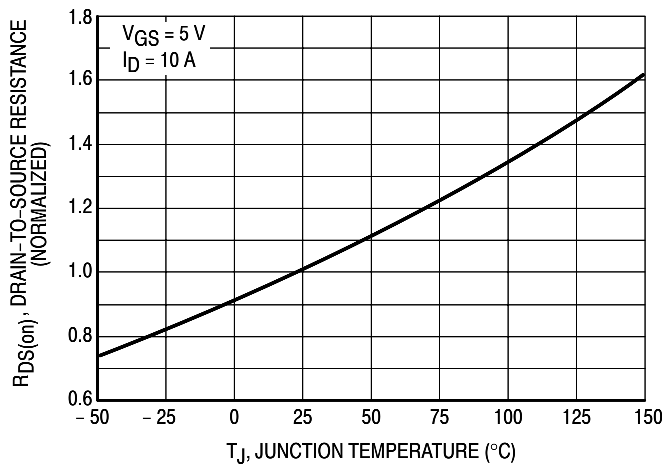



**Figure 5. On–Resistance Variation with Temperature**

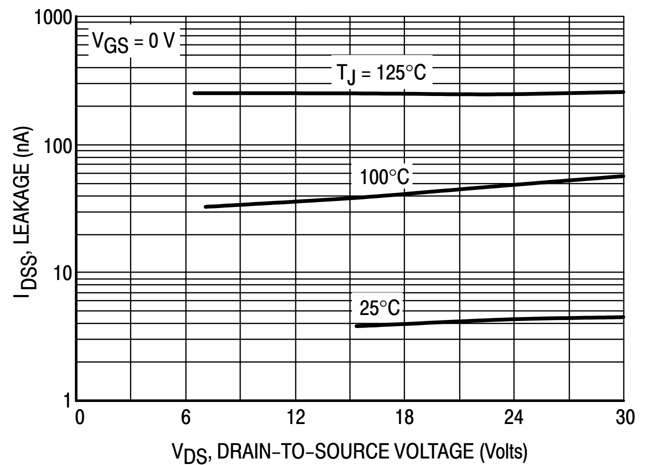



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

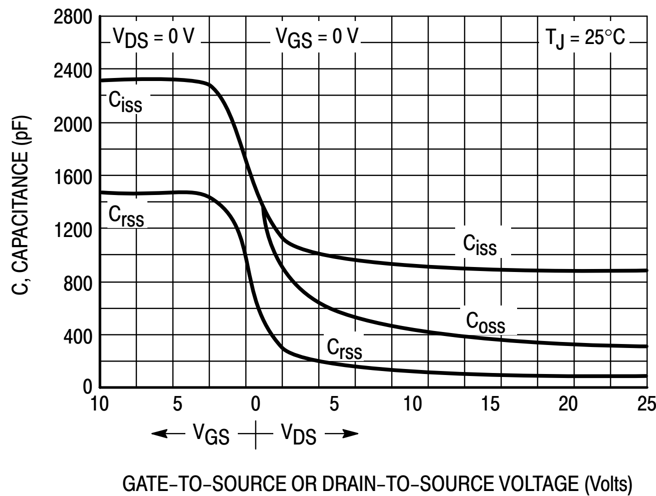



**Figure 7. Capacitance Variation**

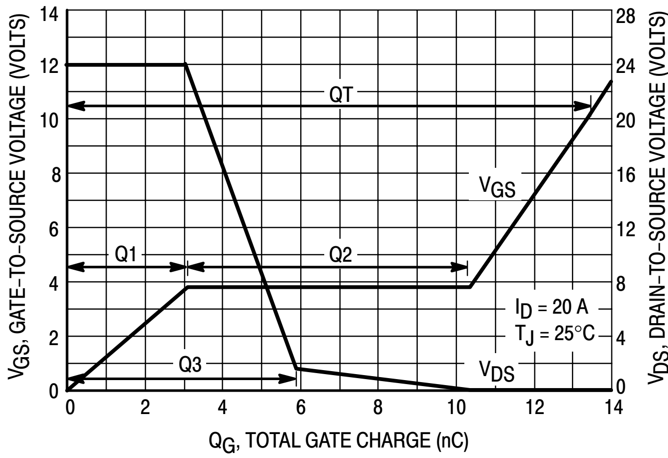



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

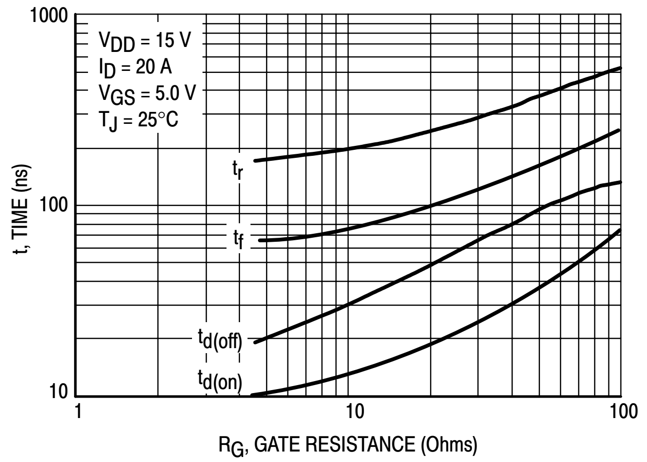



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

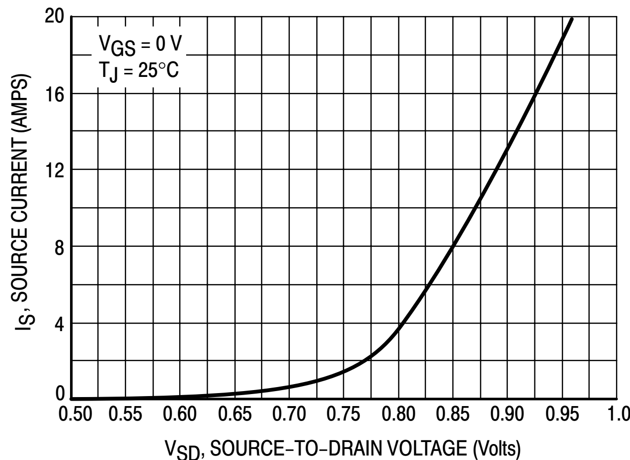



**Figure 10. Diode Forward Voltage versus Current**

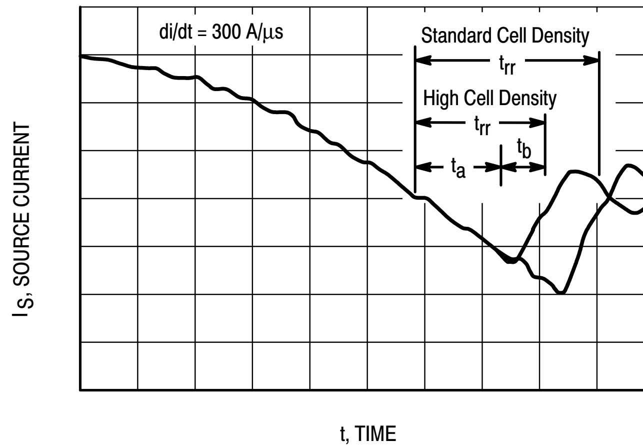



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

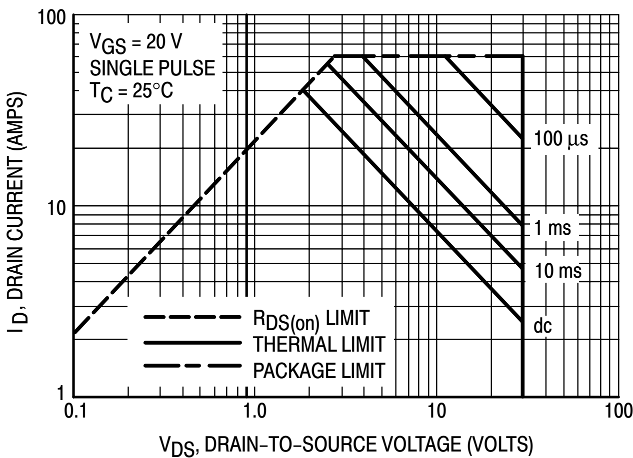



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

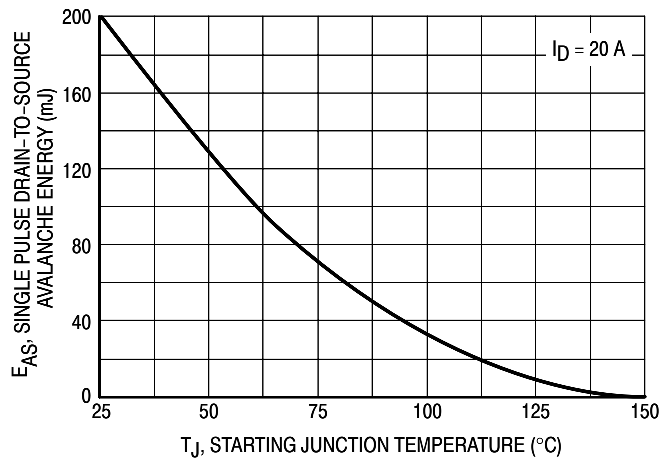



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

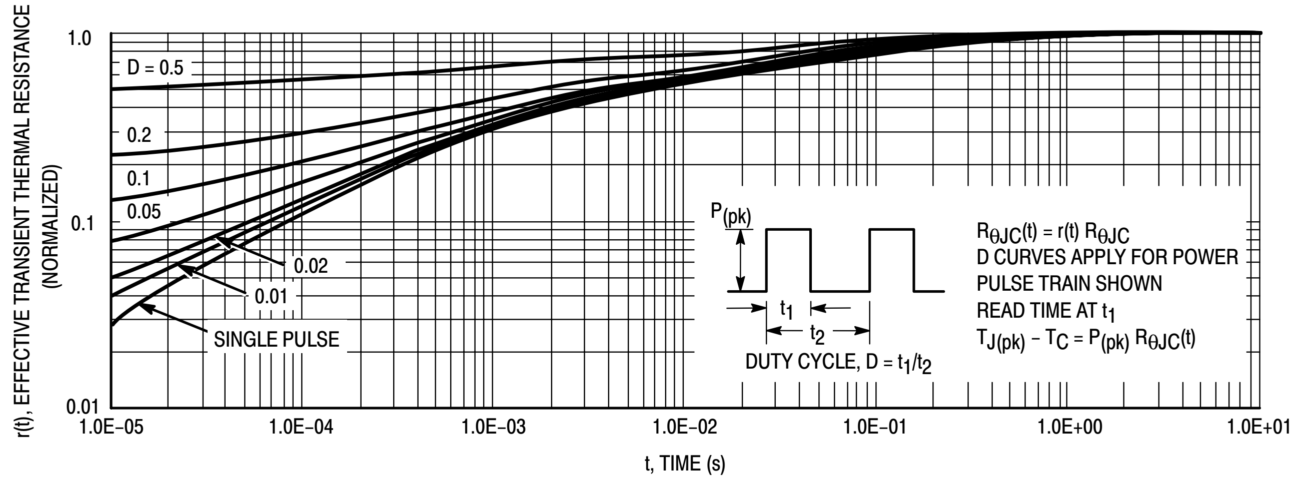



**Figure 14. Thermal Response**

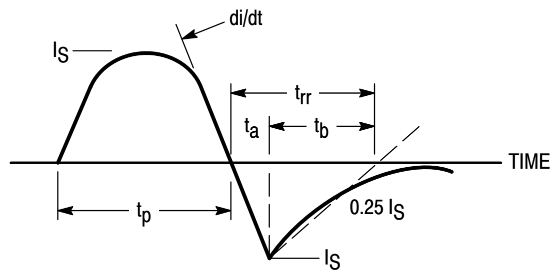
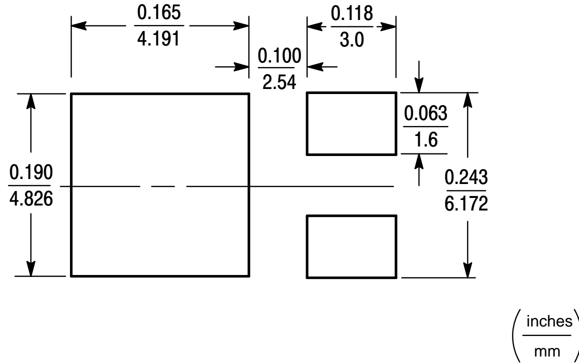



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

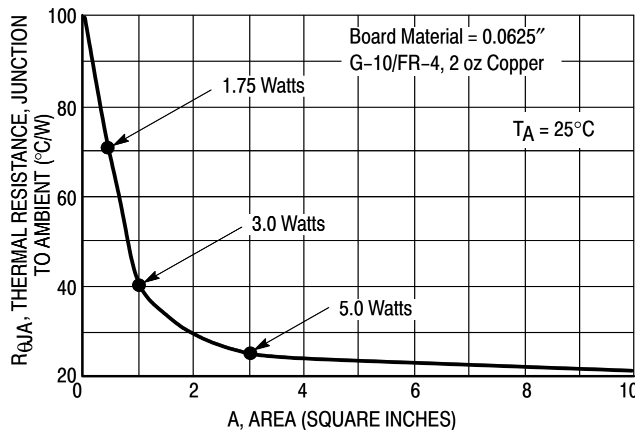



**Figure 16. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

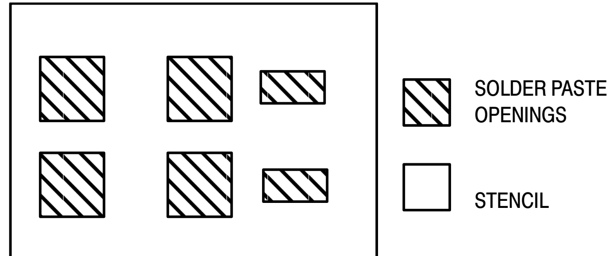



**Figure 17. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

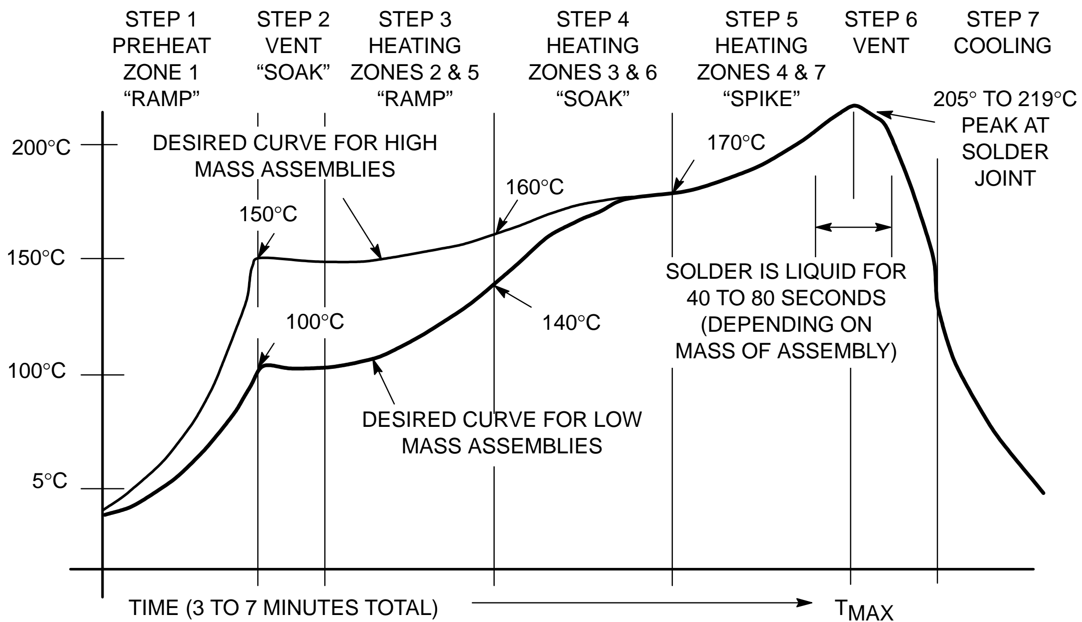



**Figure 18. Typical Solder Heating Profile**

# MTD20N06HD

**Preferred Device**

# Power MOSFET 20 Amps, 60 Volts

## N–Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

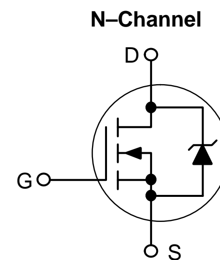
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>16<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 40<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 20 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 60 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

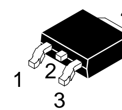
**ON Semiconductor™**

**http://onsemi.com**

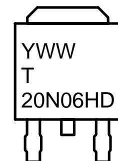
**20 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 45 mΩ**




**MARKING DIAGRAM**

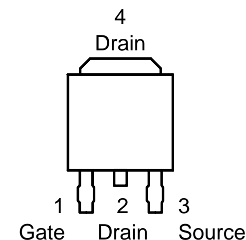



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD20N06HD | DPAK | 75 Units/Rail |
| MTD20N06HD1 | DPAK | 75 Units/Rail |
| MTD20N06HDT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>54 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>–<br>7.0 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.035 | <br>0.045 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 20 Adc)<br>($I_D$ = 10 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.2<br>1.1 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 4.0 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | <br>5.0 | <br>6.0 | <br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 607 | 840 | pF |
| Output Capacitance | | $C_{oss}$ | – | 218 | 290 | |
| Transfer Capacitance | | $C_{rss}$ | – | 55 | 110 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 9.2 | 18 | ns |
| Rise Time | | $t_r$ | – | 61.2 | 122 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 19 | 38 | |
| Fall Time | | $t_f$ | – | 36 | 72 | |
| Gate Charge<br>(See Figure 7) | ($V_{DS}$ = 48 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 17 | 24 | nC |
| | | $Q_1$ | – | 3.4 | – | |
| | | $Q_2$ | – | 7.75 | – | |
| | | $Q_3$ | – | 7.46 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage<br>($C_{pk}$ ≥ 8.0) (Note 3.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.95<br>0.88 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 14) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 35.7 | – | ns |
| | | $t_a$ | – | 24 | – | |
| | | $t_b$ | – | 11.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.055 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>– | <br>4.5 | <br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk}$ = Absolute Value of Spec (Spec–AVG/3.516 μA).

## TYPICAL ELECTRICAL CHARACTERISTICS

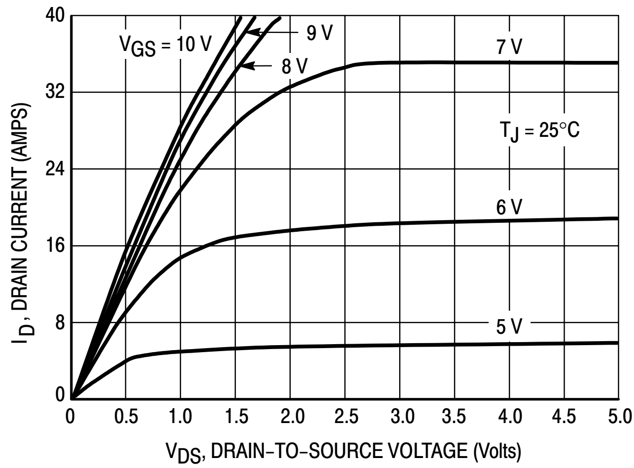



**Figure 1. On–Region Characteristics**

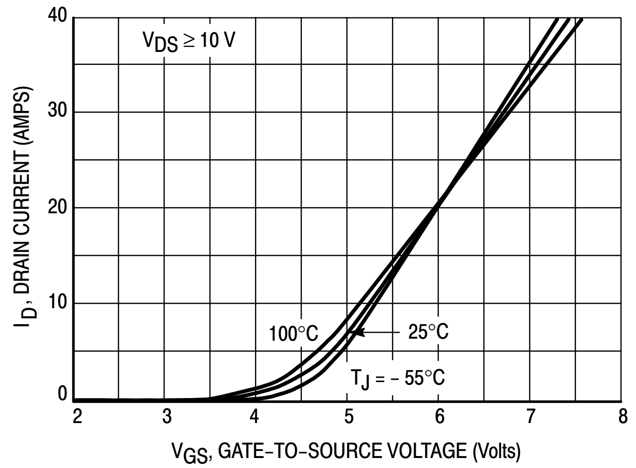



**Figure 2. Transfer Characteristics**

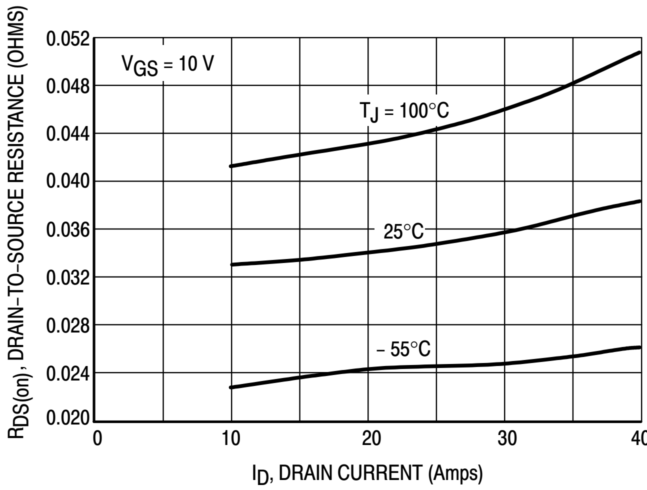



**Figure 3. On–Resistance versus Drain Current and Temperature**

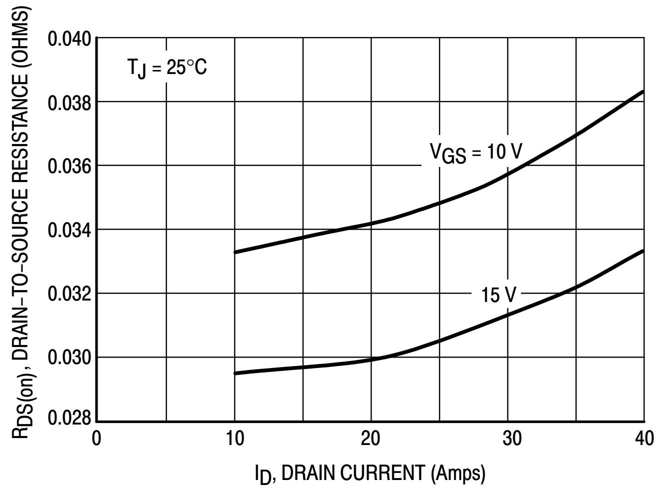



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

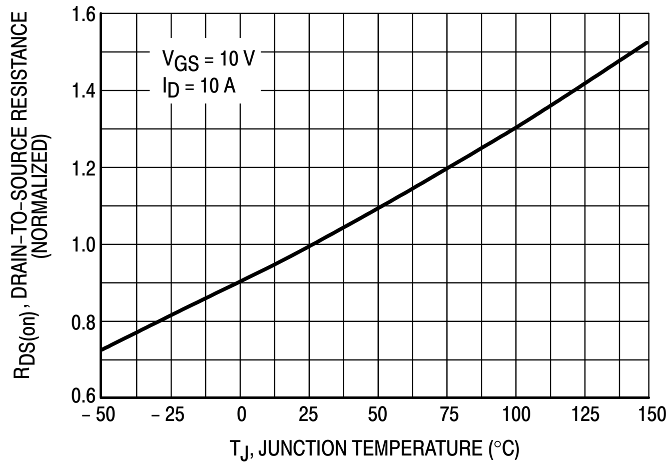



**Figure 5. On–Resistance Variation with Temperature**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

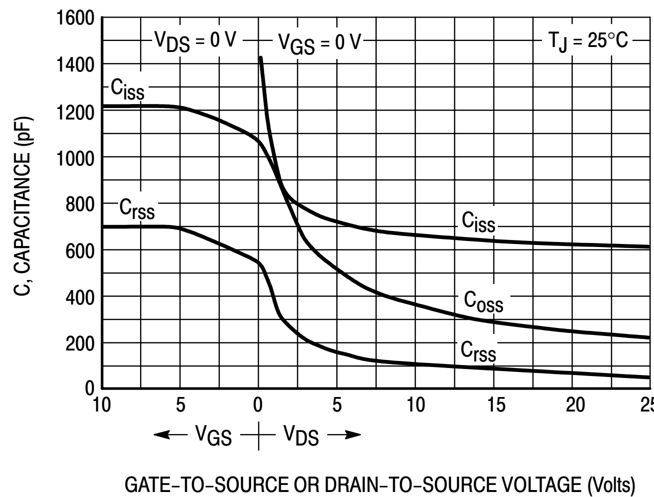



**Figure 6. Capacitance Variation**

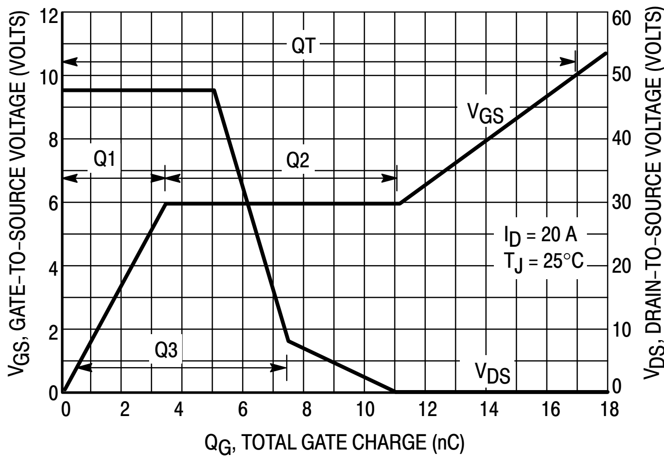



**Figure 7. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

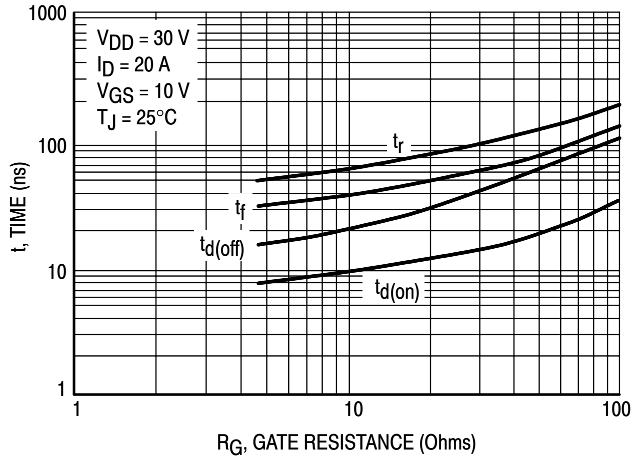



**Figure 8. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

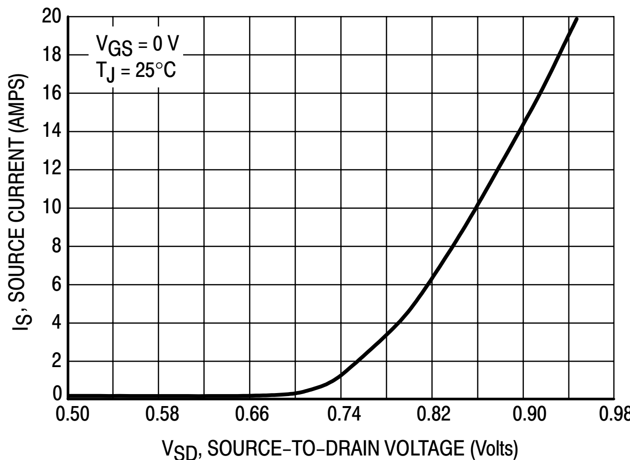



**Figure 9. Diode Forward Voltage versus Current**

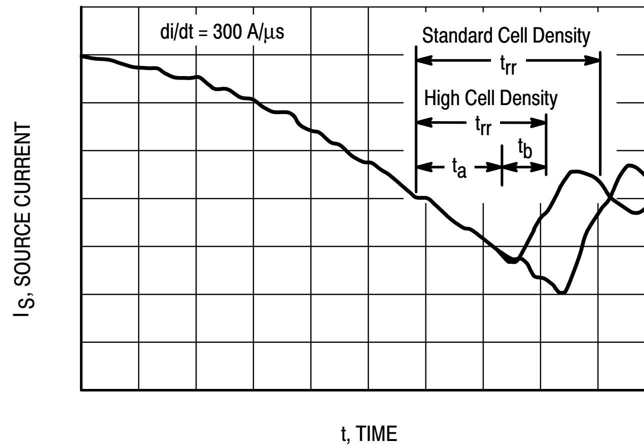



**Figure 10. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

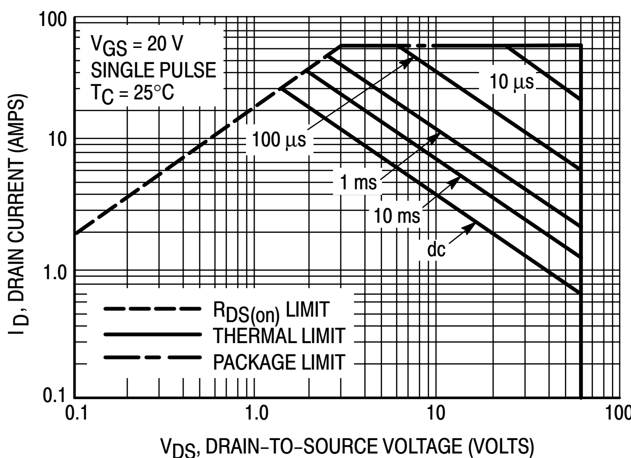



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

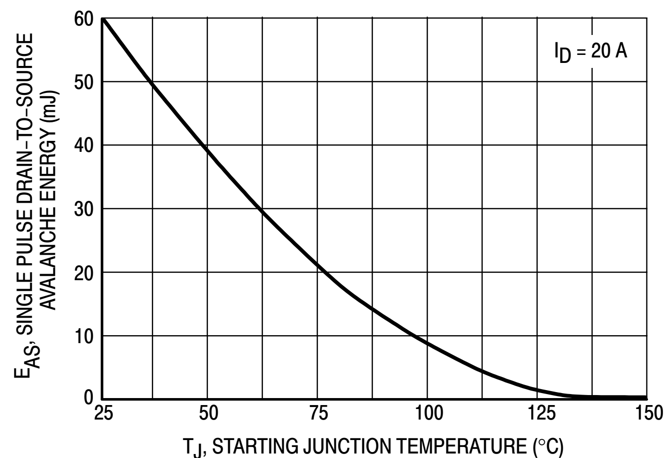



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

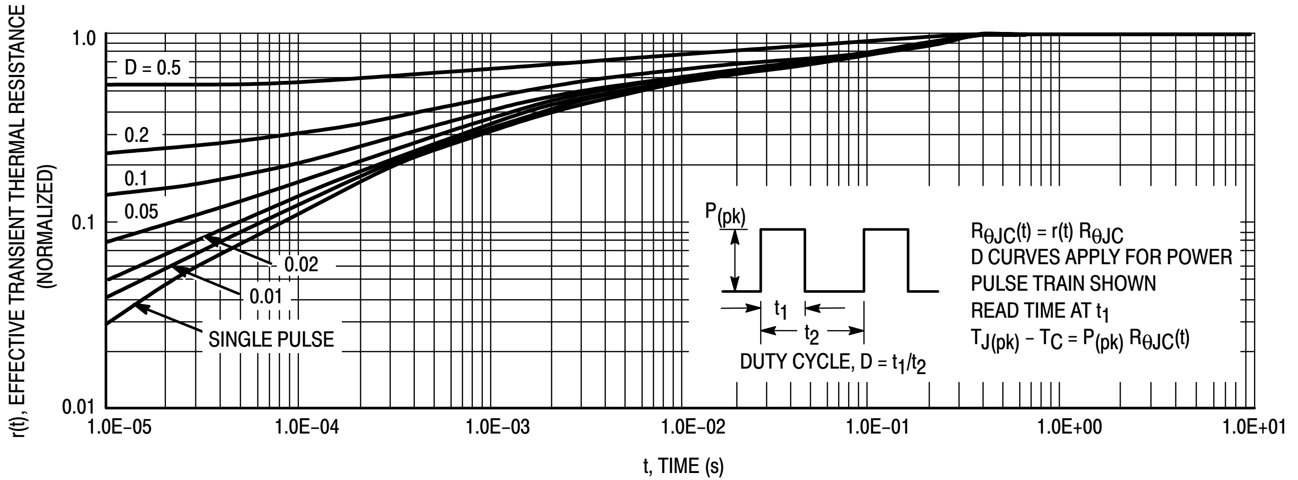



**Figure 13. Thermal Response**

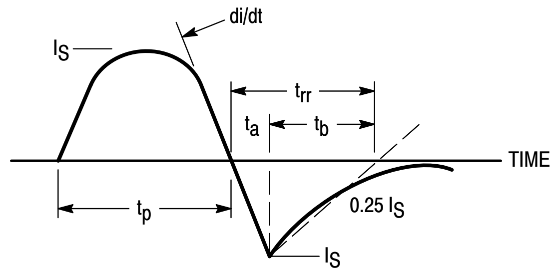
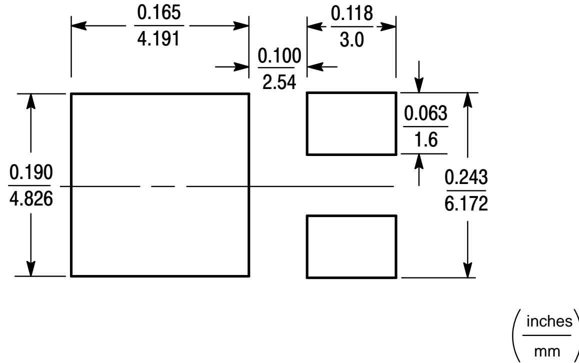



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

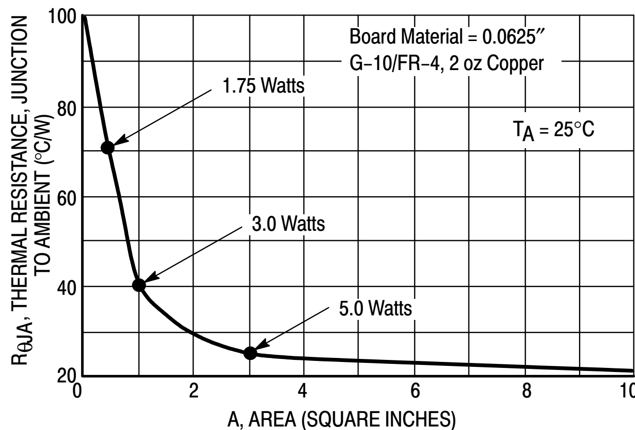



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

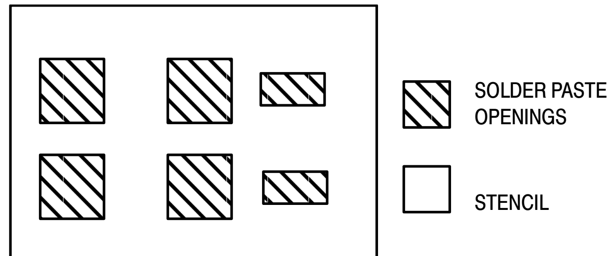



**Figure 16. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

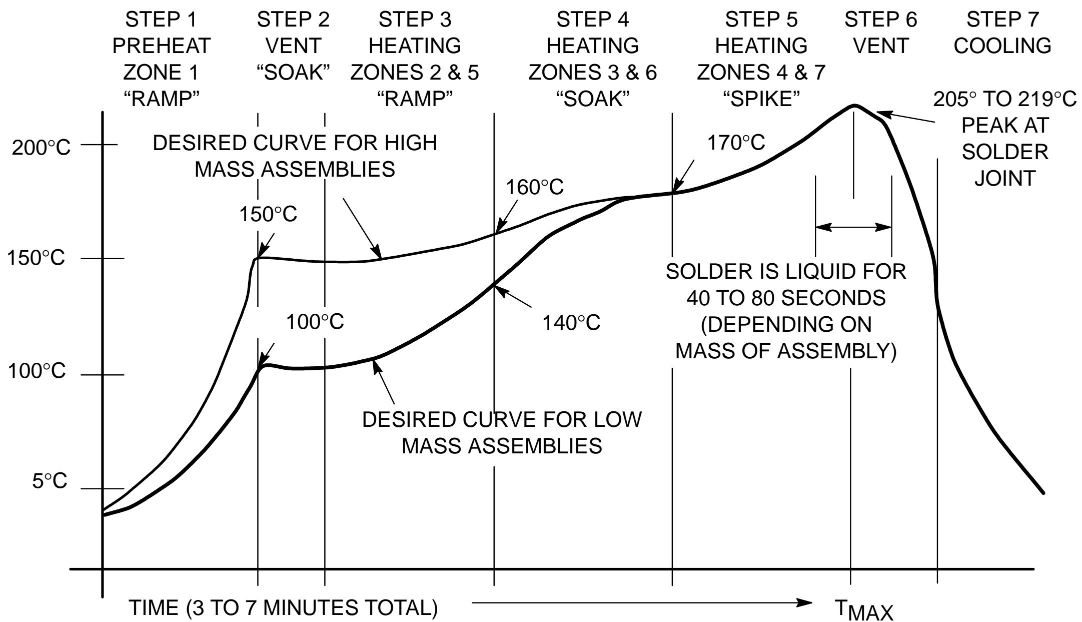



**Figure 17. Typical Solder Heating Profile**

# MTD20N06HDL

**Preferred Device**

# Power MOSFET
# 20 Amps, 60 Volts, Logic Level
## N–Channel DPAK

**ON Semiconductor™**

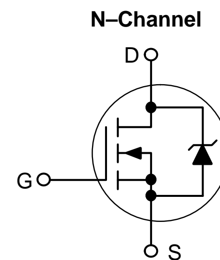
http://onsemi.com

**20 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 45 mΩ**

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

N–Channel

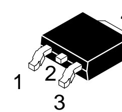



**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

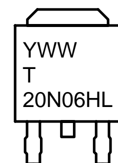
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>12<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note 1.) | $P_D$ | 40<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 20 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 200 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR–4 board using the minimum recommended pad size.

**MARKING DIAGRAM**

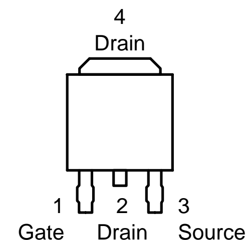



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD20N06HDL | DPAK | 75 Units/Rail |
| MTD20N06HDL1 | DPAK | 75 Units/Rail |
| MTD20N06HDLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>25 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>6.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance<br>($V_{GS}$ = 4.0 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | $R_{DS(on)}$ | <br>–<br>– | <br>0.045<br>0.037 | <br>0.070<br>0.045 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 20 Adc)<br>($I_D$ = 10 Adc, $T_J$ = 125°C) | $V_{DS(on)}$ | <br>–<br>– | <br>0.76<br>– | <br>1.2<br>1.1 | Vdc |
| Forward Transconductance ($V_{DS}$ = 4.0 Vdc, $I_D$ = 10 Adc) | $g_{FS}$ | 6.0 | 12 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance — ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 863 | 1232 | pF |
| Output Capacitance | $C_{oss}$ | – | 216 | 300 | |
| Reverse Transfer Capacitance | $C_{rss}$ | – | 53 | 73 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | |
| Turn–On Delay Time — ($V_{DS}$ = 30 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 15 | ns |
| Rise Time | $t_r$ | – | 151 | 190 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 34 | 35 | |
| Fall Time | $t_f$ | – | 75 | 98 | |
| Gate Charge — ($V_{DS}$ = 48 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 14.6 | 22 | nC |
| | $Q_1$ | – | 3.25 | – | |
| | $Q_2$ | – | 7.75 | – | |
| | $Q_3$ | – | 7.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.95<br>0.88 | <br>1.1<br>– | Vdc |
| Reverse Recovery Time — ($I_S$ = 20 Adc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 22 | – | ns |
| | $t_a$ | – | 12 | – | |
| | $t_b$ | – | 34 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.049 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

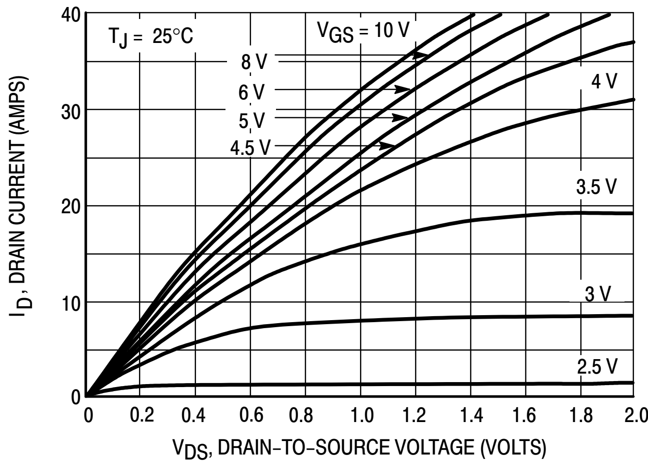



**Figure 1. On–Region Characteristics**

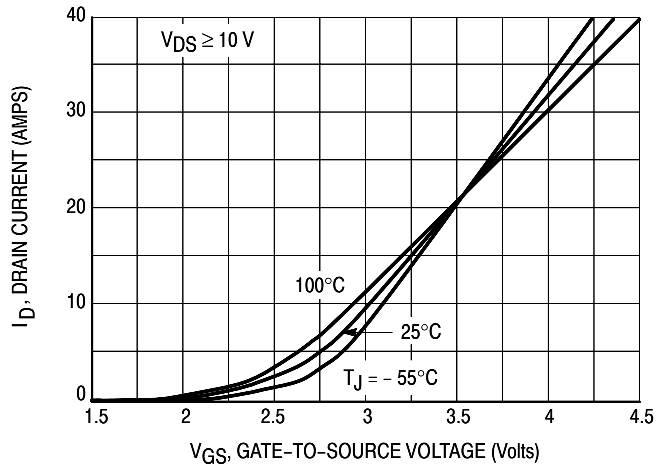



**Figure 2. Transfer Characteristics**

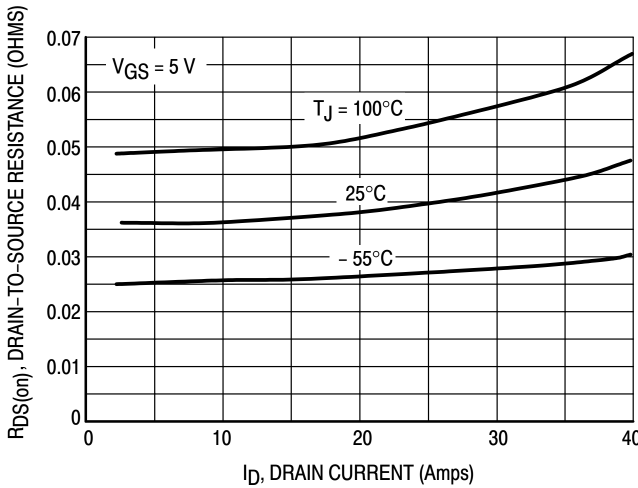



**Figure 3. On–Resistance versus Drain Current and Temperature**

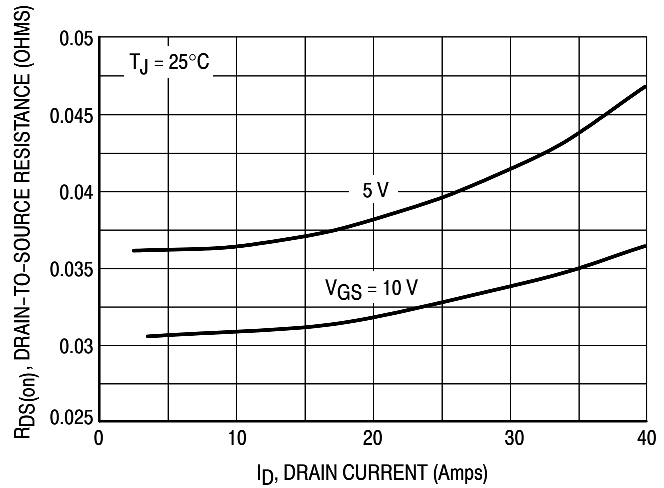



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

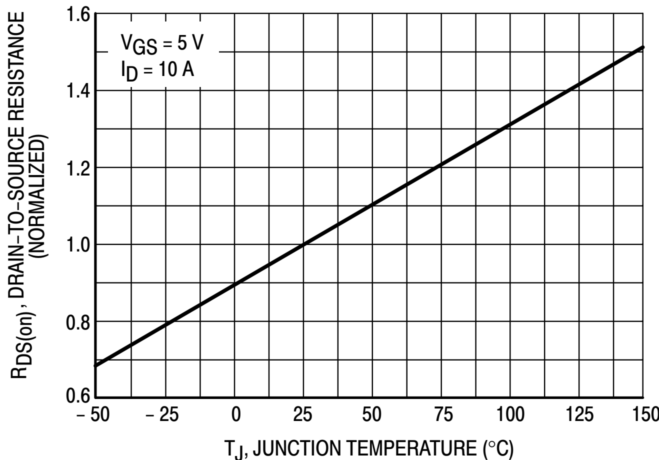



**Figure 5. On–Resistance Variation with Temperature**

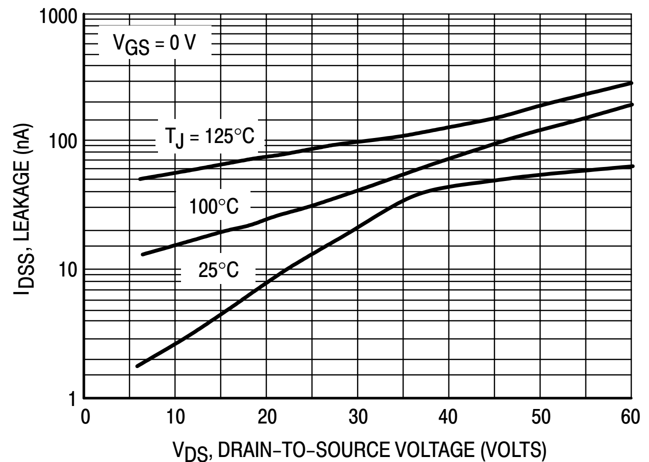



**Figure 6. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 8) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

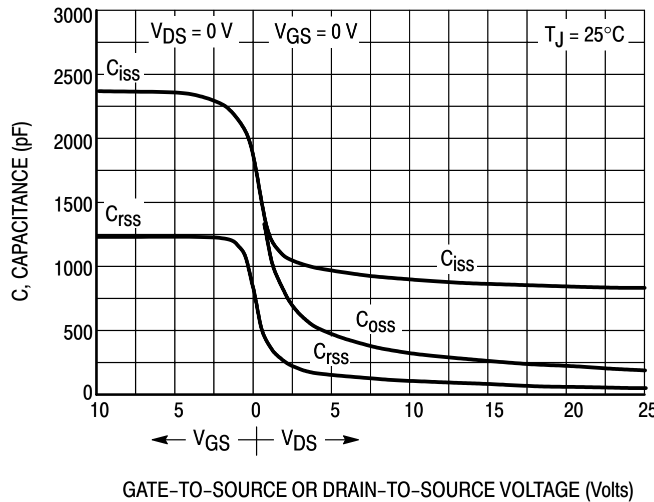



**Figure 7. Capacitance Variation**

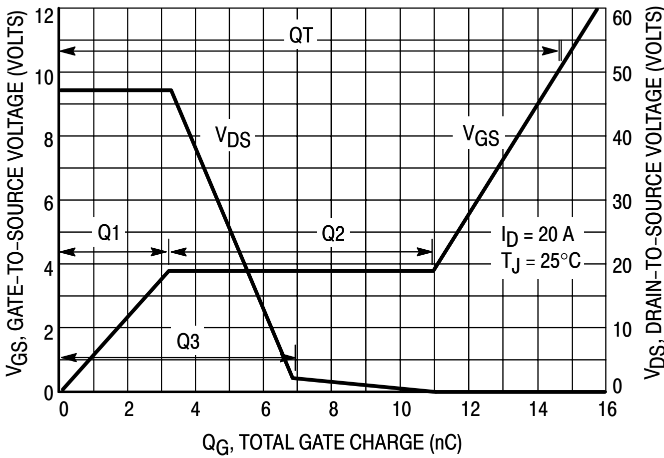



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

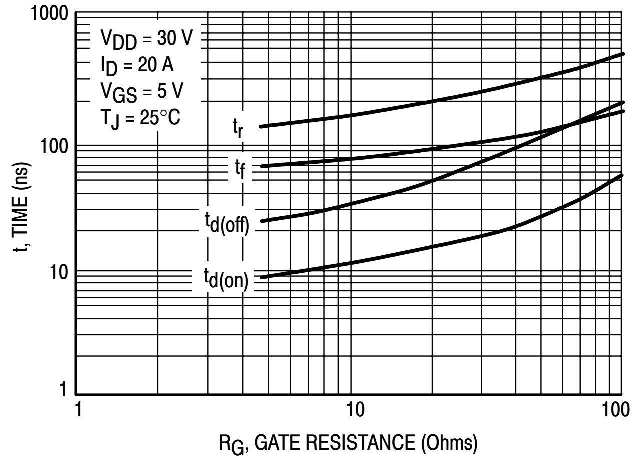



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 10. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

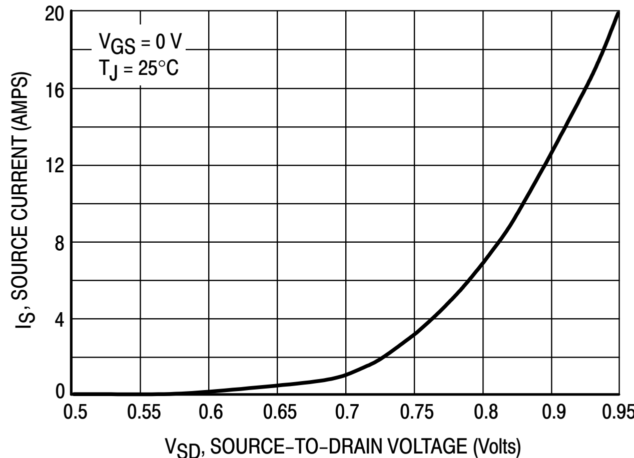



**Figure 10. Diode Forward Voltage versus Current**

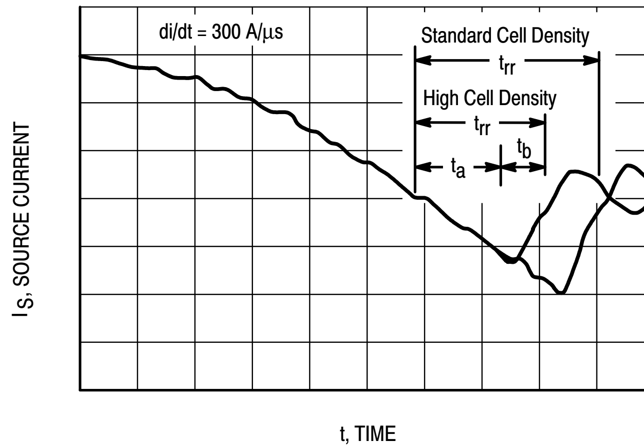



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)}$ – $T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

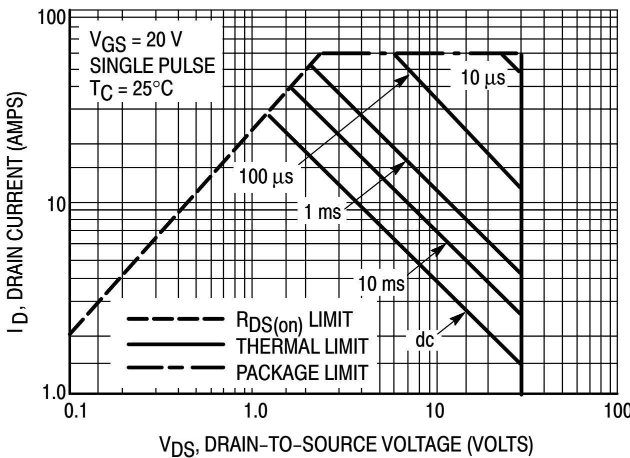



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

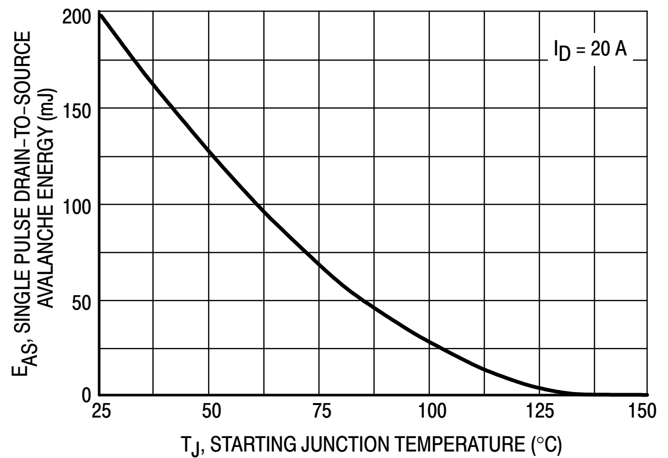



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

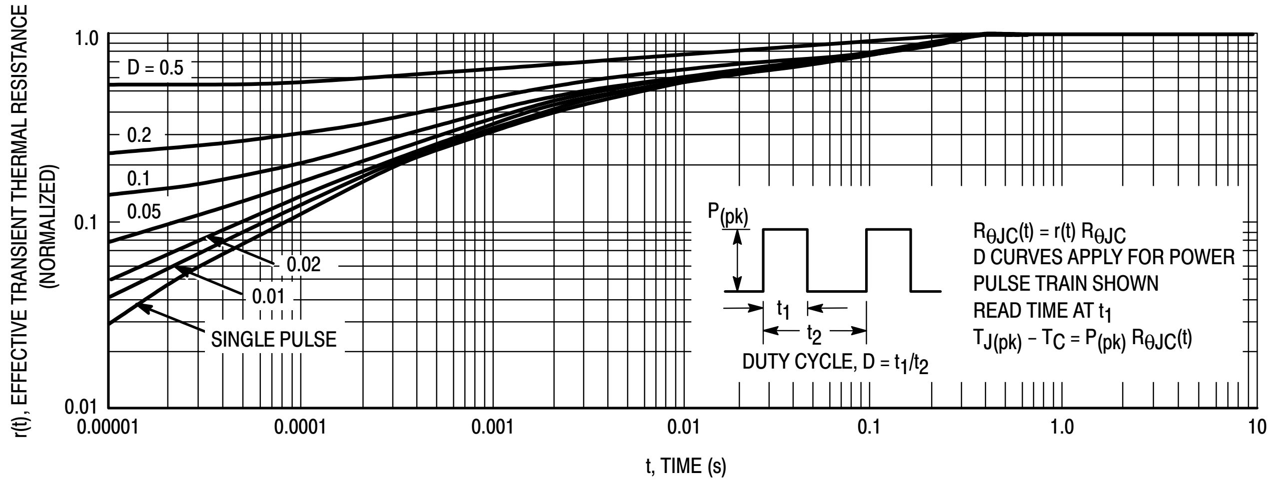



**Figure 14. Thermal Response**

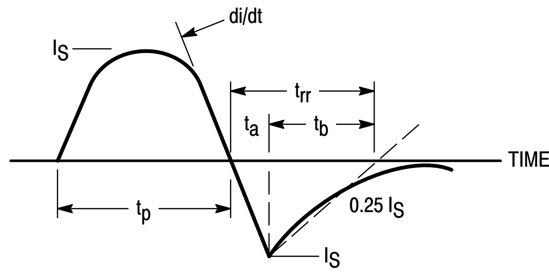
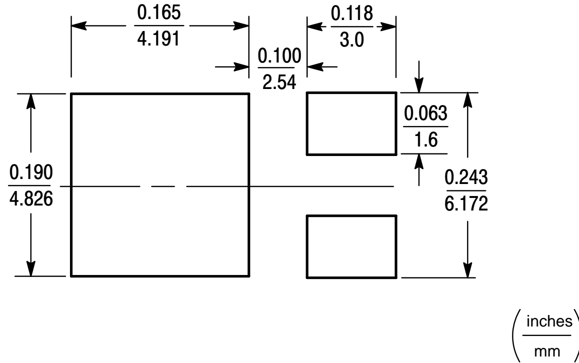



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

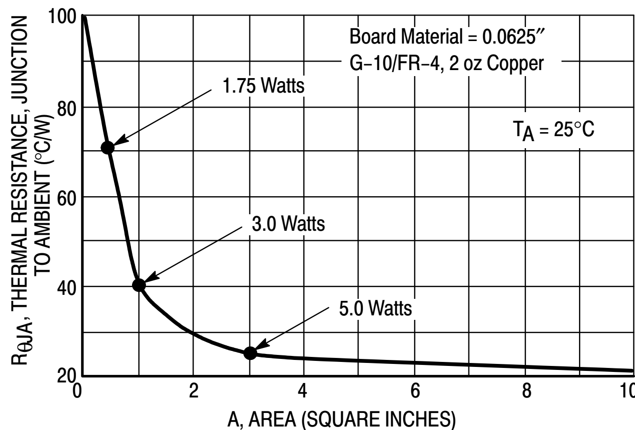



**Figure 16. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

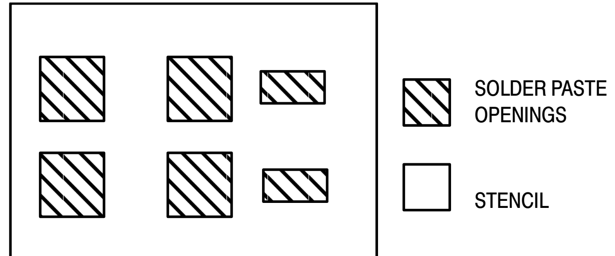



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

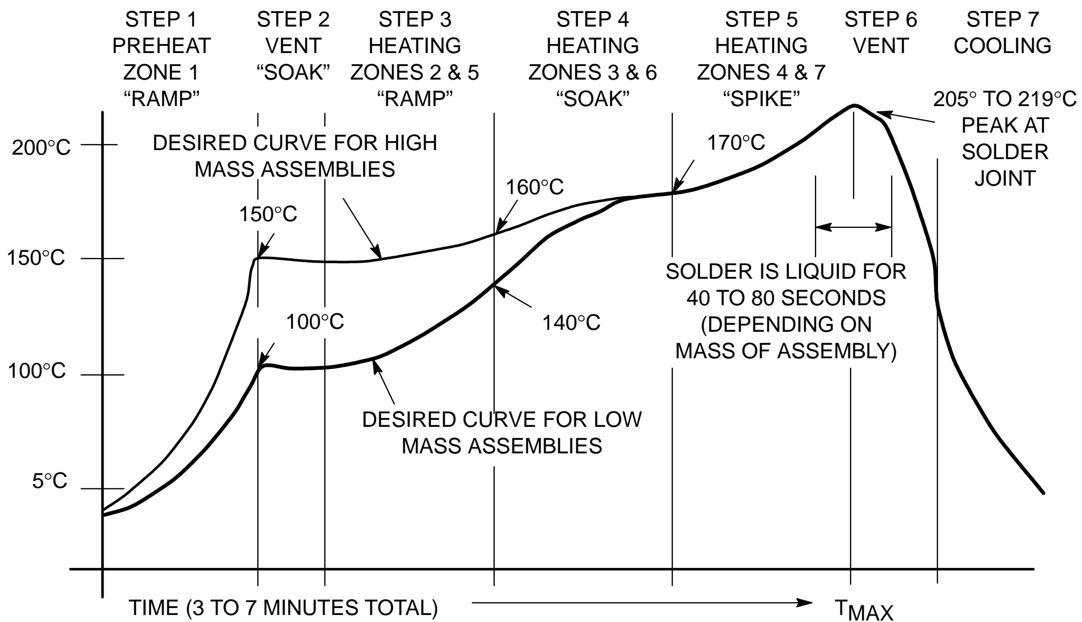



**Figure 18. Typical Solder Heating Profile**

# MTD20P03HDL

**Preferred Device**

# Power MOSFET 20 Amps, 30 Volts, Logic Level

## P–Channel DPAK

**ON Semiconductor™**

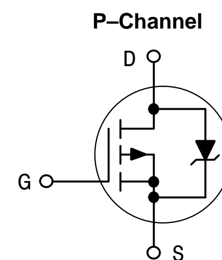
**http://onsemi.com**

**20 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 99 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**P–Channel**

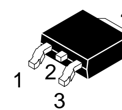



**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

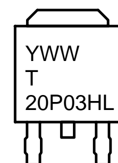
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>19<br>12<br>57 | <br>Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note 1.) | $P_D$ | 75<br>0.6<br>1.75 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 19 Apk, L = 1.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 200 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.67<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

**MARKING DIAGRAM**

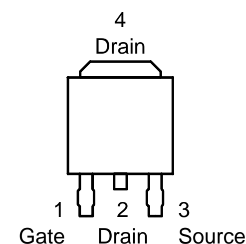



**CASE 369A**
**DPAK**
**STYLE 2**




20P03HL = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD20P03HDL | DPAK | 75 Units/Rail |
| MTD20P03HDL1 | DPAK | 75 Units/Rail |
| MTD20P03HDLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>15 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 4.0 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 9.5 Adc) | | $R_{DS(on)}$ | <br>–<br> | <br>120<br>90 | <br>–<br>99 | mΩ |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 19 Adc)<br>($I_D$ = 9.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>0.94<br>– | <br>2.2<br>1.9 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 9.5 Adc) | | $g_{FS}$ | 5.0 | 6.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 770 | 1064 | pF |
| Output Capacitance | | $C_{oss}$ | – | 360 | 504 | |
| Transfer Capacitance | | $C_{rss}$ | – | 130 | 182 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 19 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 1.3 Ω) | $t_{d(on)}$ | – | 18 | 25.2 | ns |
| Rise Time | | $t_r$ | – | 178 | 246.4 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 21 | 26.6 | |
| Fall Time | | $t_f$ | – | 72 | 98 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 24 Vdc, $I_D$ =19 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 15 | 22.4 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 11 | – | |
| | | $Q_3$ | – | 8.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage ($C_{pk}$ ≥ 2.0) (Note 4.) | ($I_S$ = 19 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 19 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>3.1<br>2.56 | <br>3.4<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 15) | ($I_S$ = 19 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 78 | – | ns |
| | | $t_a$ | – | 50 | – | |
| | | $t_b$ | – | 28 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.209 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk}$ = Absolute Value of Spec (Spec–AVG/3.516 μA).

## TYPICAL ELECTRICAL CHARACTERISTICS

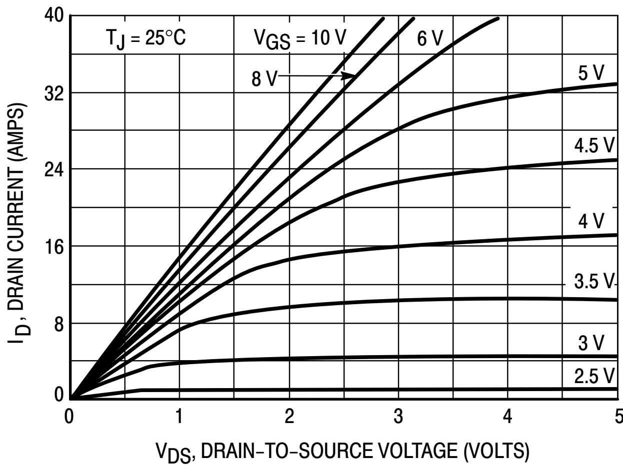



**Figure 1. On–Region Characteristics**

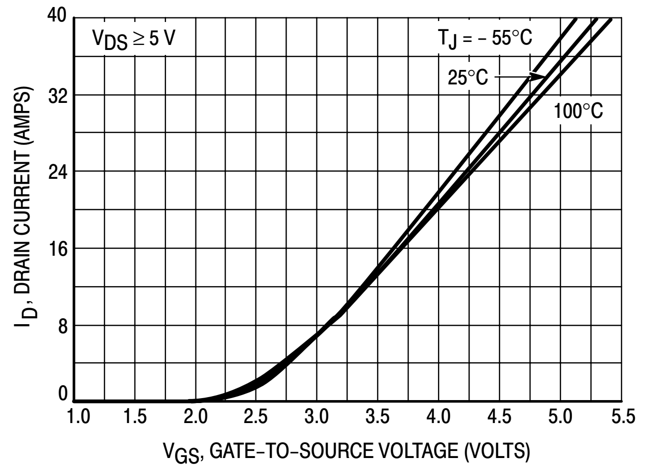



**Figure 2. Transfer Characteristics**

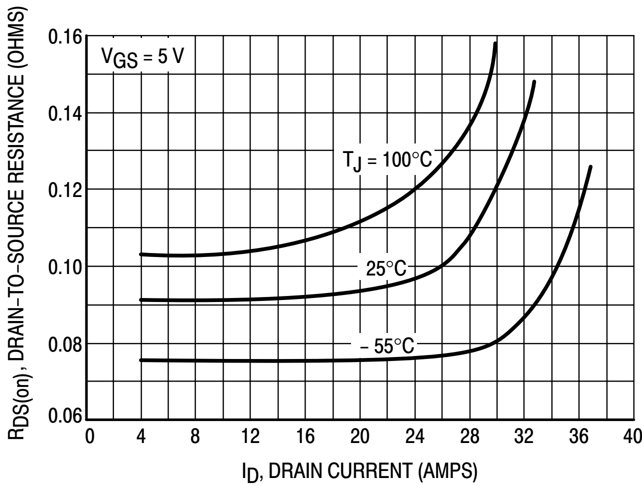



**Figure 3. On–Resistance versus Drain Current and Temperature**

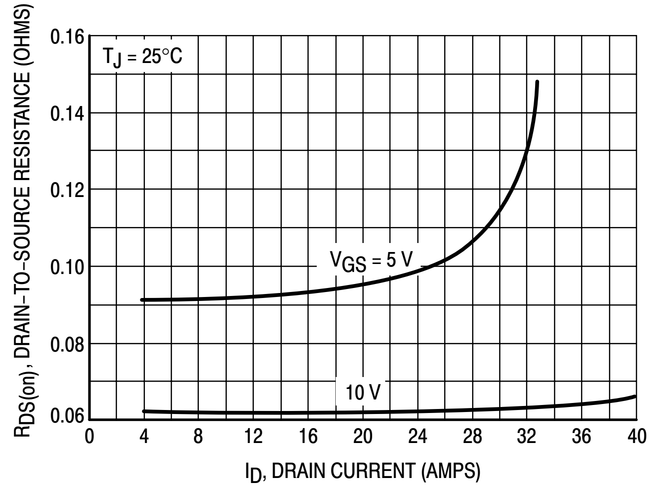



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

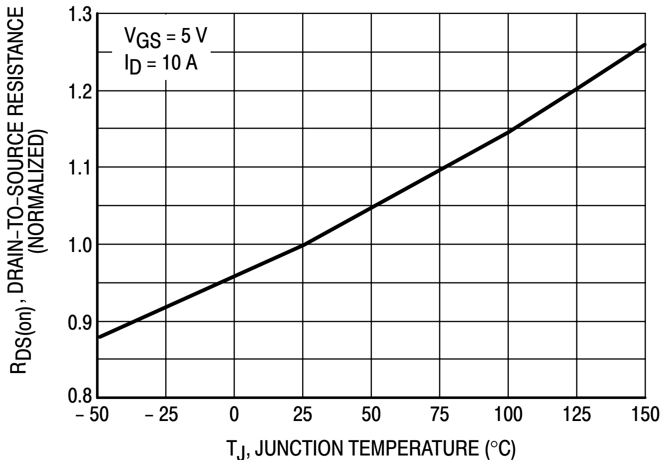



**Figure 5. On–Resistance Variation with Temperature**

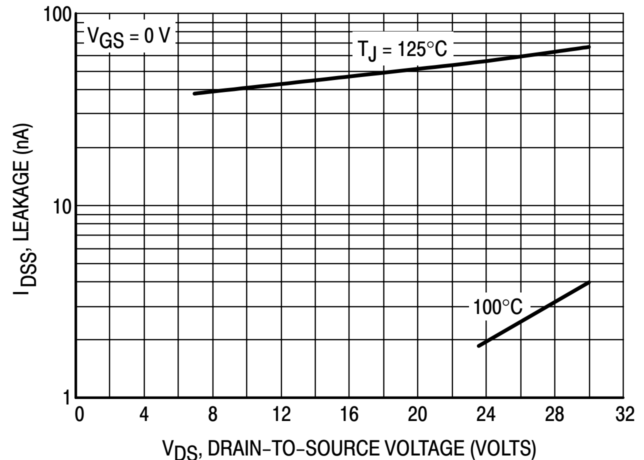



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \mathrm{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \mathrm{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

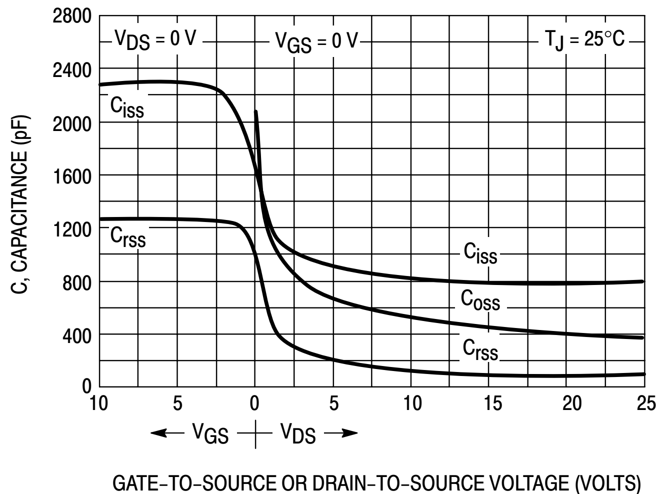



**Figure 7. Capacitance Variation**

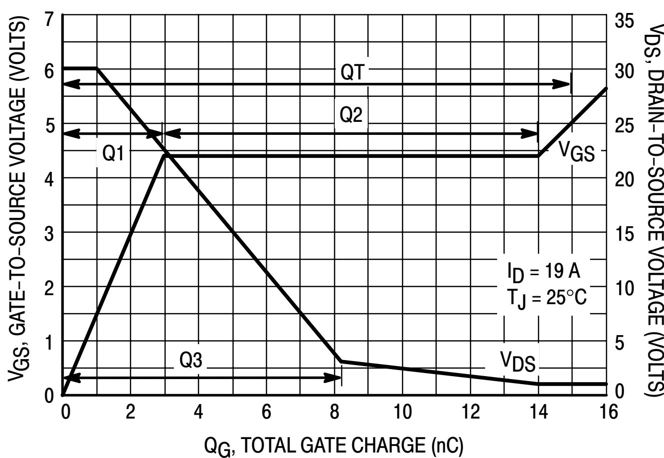



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

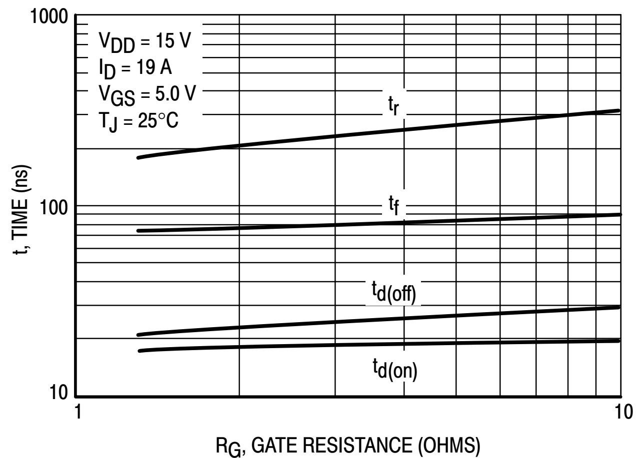



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

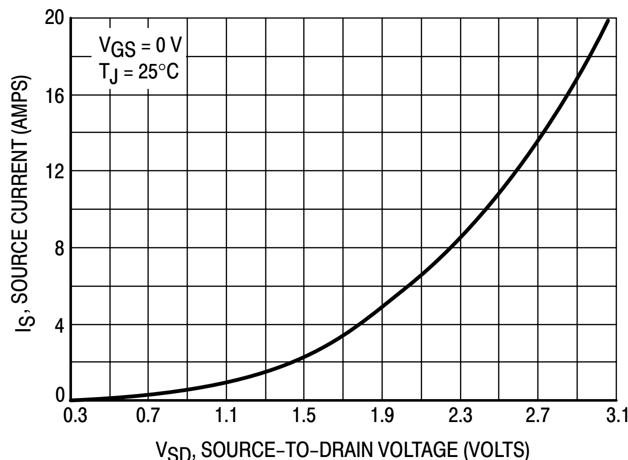



**Figure 10. Diode Forward Voltage versus Current**

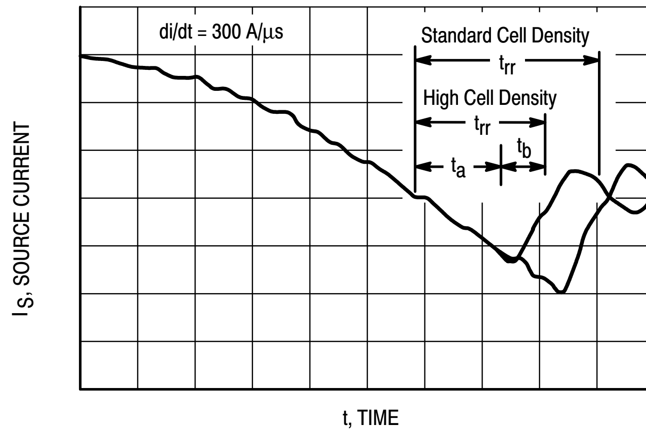



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

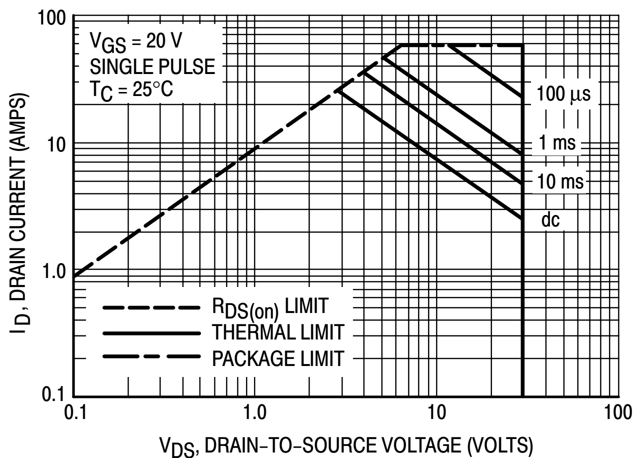



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

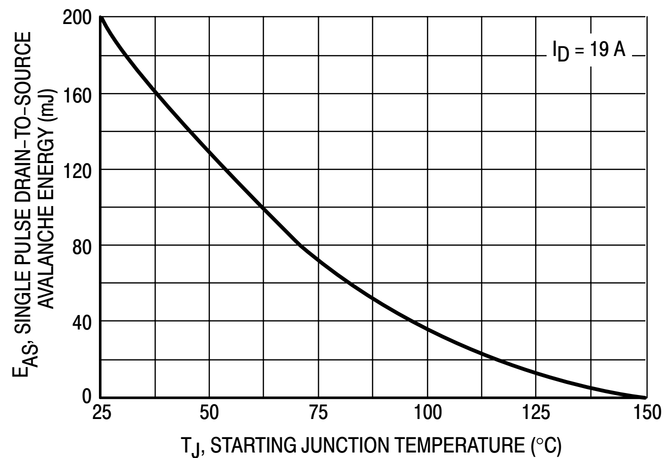



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

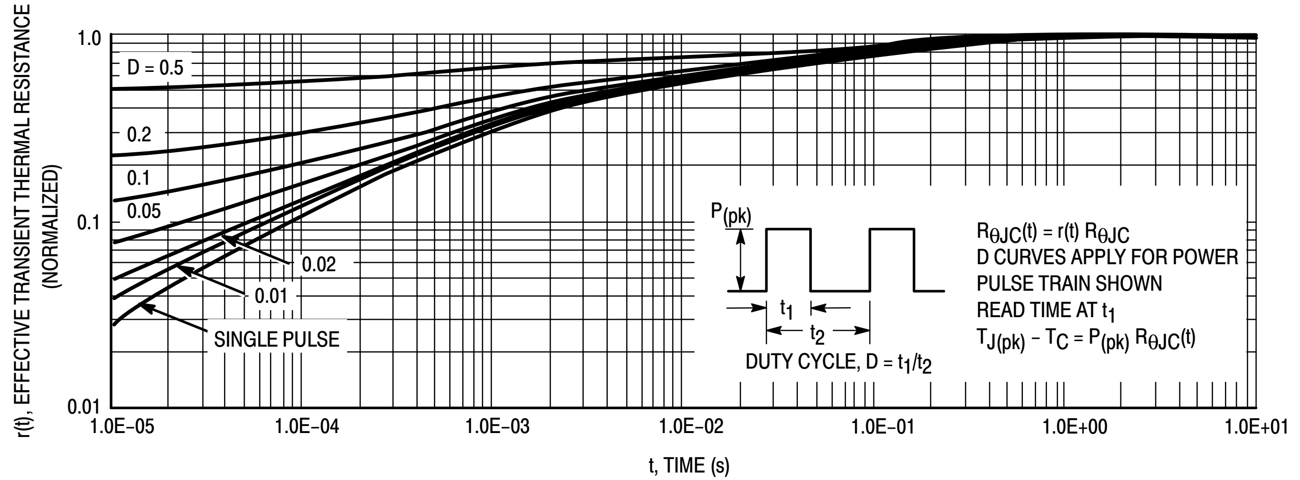



**Figure 14. Thermal Response**

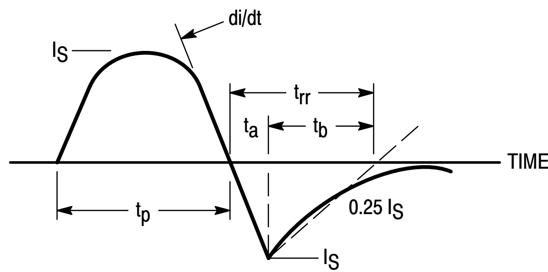
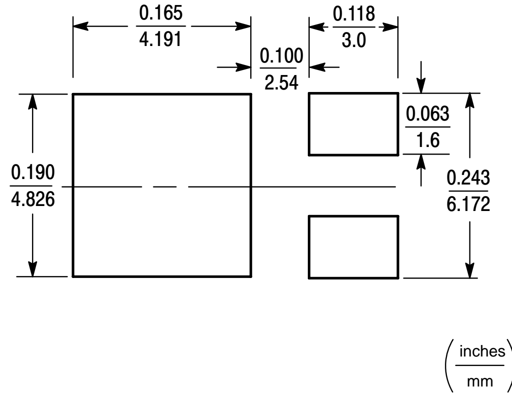



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

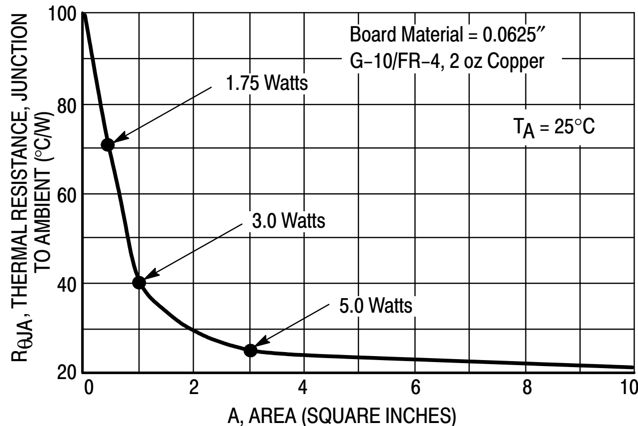



**Figure 16. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

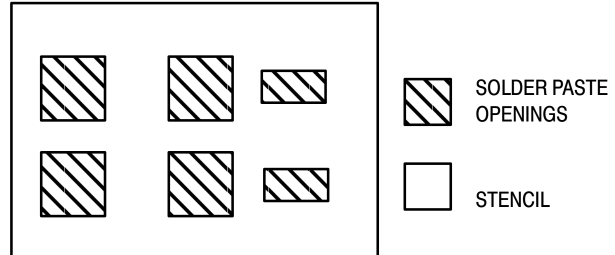



**Figure 17. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

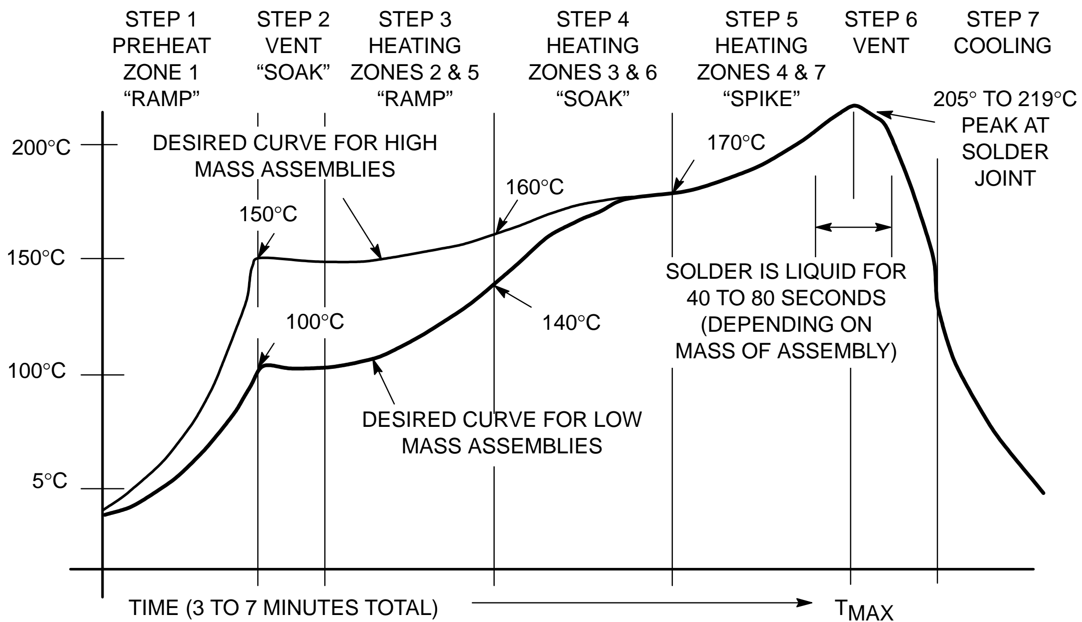



**Figure 18. Typical Solder Heating Profile**

# MTD20P06HDL

**Preferred Device**

# Power MOSFET 20 Amps, 60 Volts, Logic Level

## P–Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Ultra Low $R_{DS(on)}$, High–Cell Density, HDTMOS
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ± 15<br>± 20 | Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 15<br>9.0<br>45 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note 1.) | $P_D$ | 72<br>0.58<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 15 Apk, L = 2.7 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 300 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient<br>– Junction–to–Ambient (Note 1.) | $R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | 1.73<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

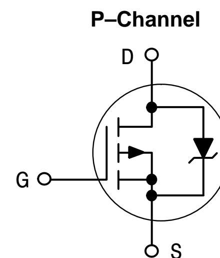
1. When surface mounted to an FR4 board using the minimum recommended pad size.

**ON Semiconductor™**

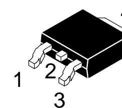
**http://onsemi.com**

**20 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 175 mΩ**

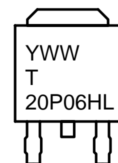
**P–Channel**




**MARKING DIAGRAM**

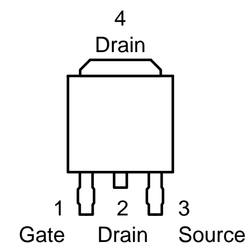



**CASE 369A**
**DPAK**
**STYLE 2**




20P06HL = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD20P06HDL | DPAK | 75 Units/Rail |
| MTD20P06HDLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**November, 2000 – Rev. 3**
Publication Order Number:
**MTD20P06HDL/D**

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 81.3 | – | mV/°C |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 1.0 | |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.7 | 2.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 3.9 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 7.5 Adc) | | $R_{DS(on)}$ | – | 143 | 175 | mΩ |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc) | | $V_{DS(on)}$ | | | | Vdc |
| ($I_D$ = 15 Adc) | | | – | 2.3 | 3.0 | |
| ($I_D$ = 7.5 Adc, $T_J$ = 125°C) | | | – | 1.6 | 2.0 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 7.5 Adc) | | $g_{FS}$ | 9.0 | 11 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 850 | 1190 | pF |
| Output Capacitance | | $C_{oss}$ | – | 210 | 290 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 66 | 130 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 19 | 38 | ns |
| Rise Time | | $t_r$ | – | 175 | 350 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 41 | 82 | |
| Fall Time | | $t_f$ | – | 68 | 136 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 20.6 | 29 | nC |
| | | $Q_1$ | – | 3.7 | – | |
| | | $Q_2$ | – | 7.6 | – | |
| | | $Q_3$ | – | 8.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 2.5 | 3.0 | Vdc |
| | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 1.9 | – | |
| Reverse Recovery Time | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 64 | – | ns |
| | | $t_a$ | – | 50 | – | |
| | | $t_b$ | – | 14 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.177 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

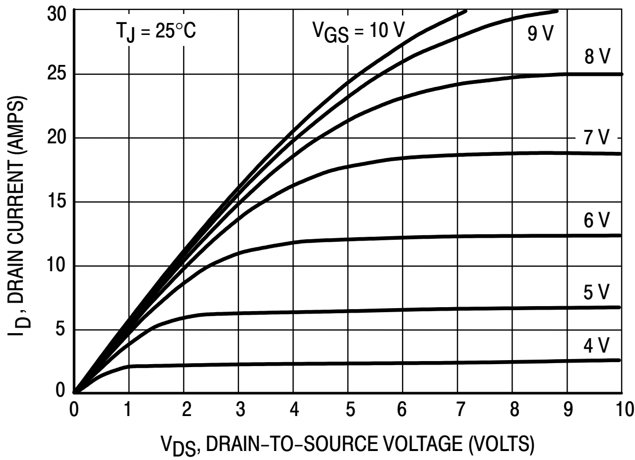



**Figure 1. On–Region Characteristics**

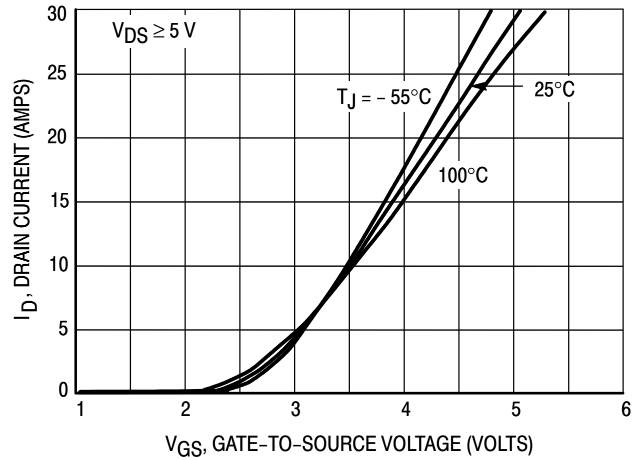



**Figure 2. Transfer Characteristics**

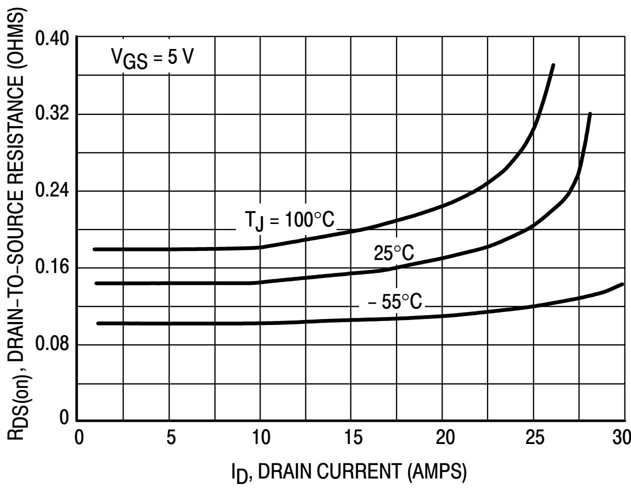



**Figure 3. On–Resistance versus Drain Current and Temperature**

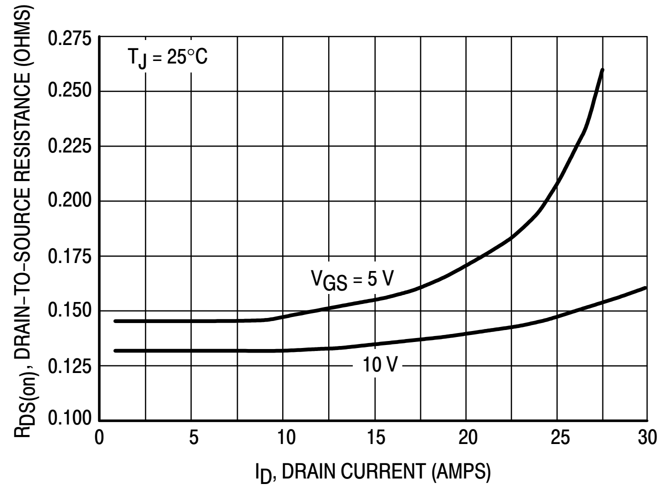



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

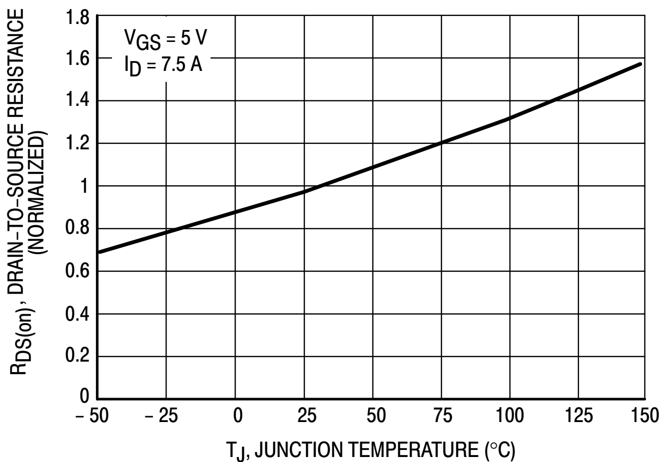



**Figure 5. On–Resistance Variation with Temperature**

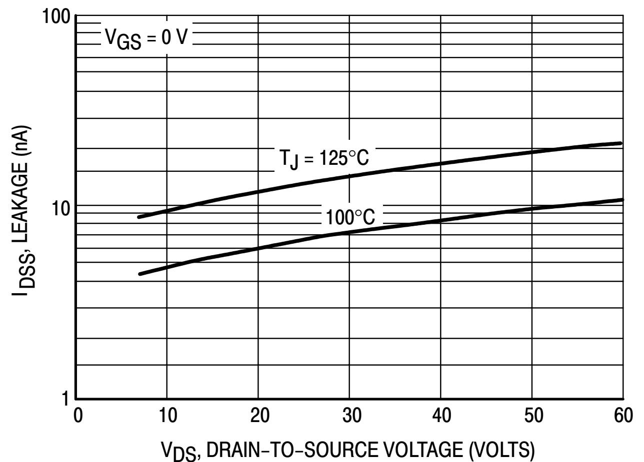



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \; C_{iss} \; \text{In} \; [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \; C_{iss} \; \text{In} \; (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

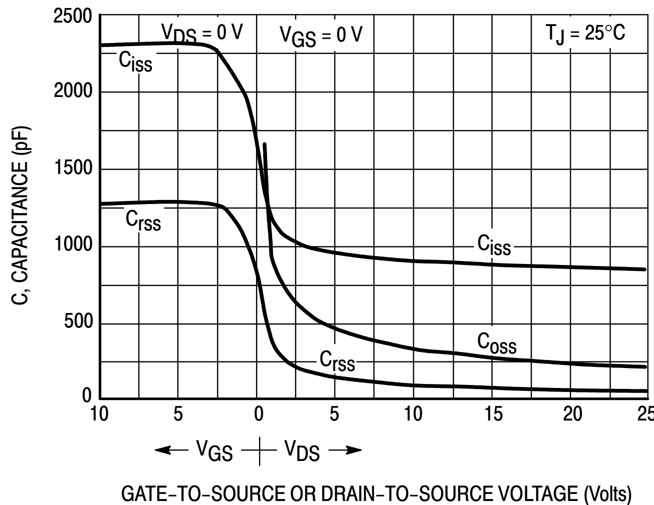



**Figure 7. Capacitance Variation**

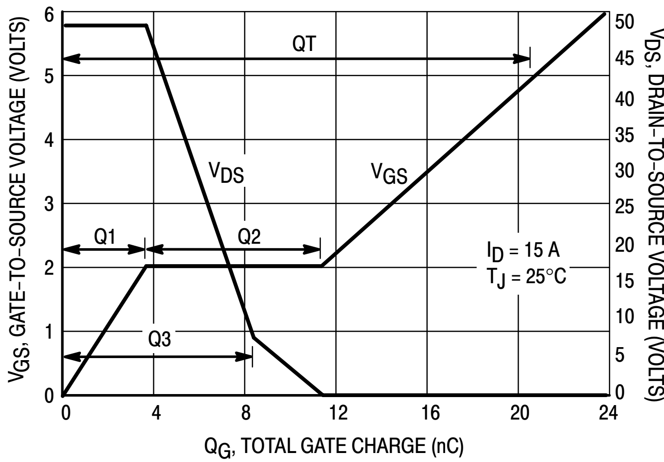



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

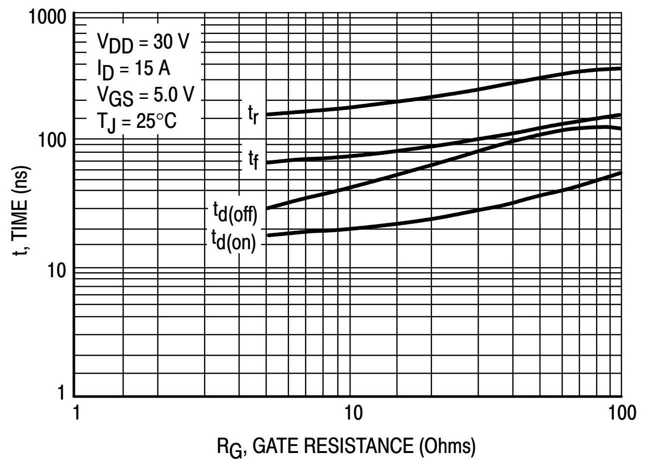



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

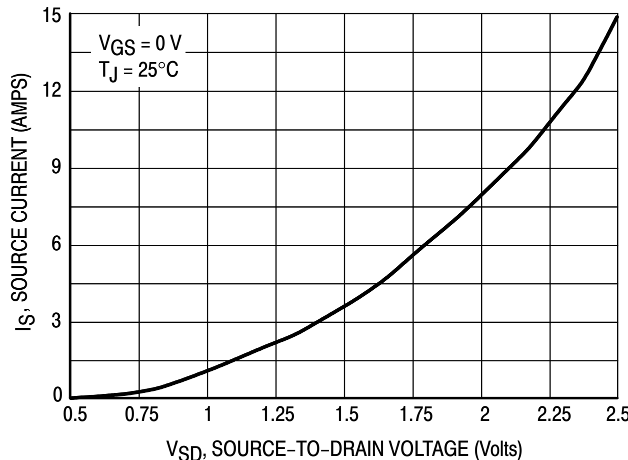



**Figure 10. Diode Forward Voltage versus Current**

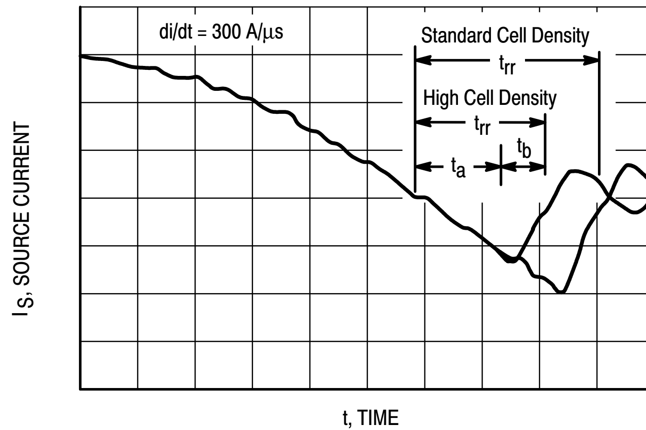



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

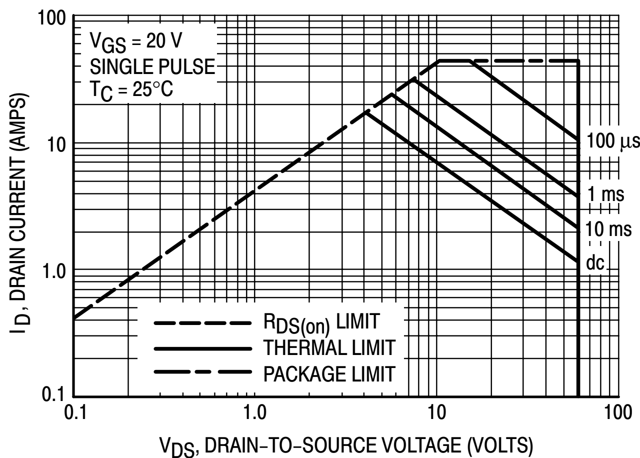



Figure 12. Maximum Rated Forward Biased Safe Operating Area

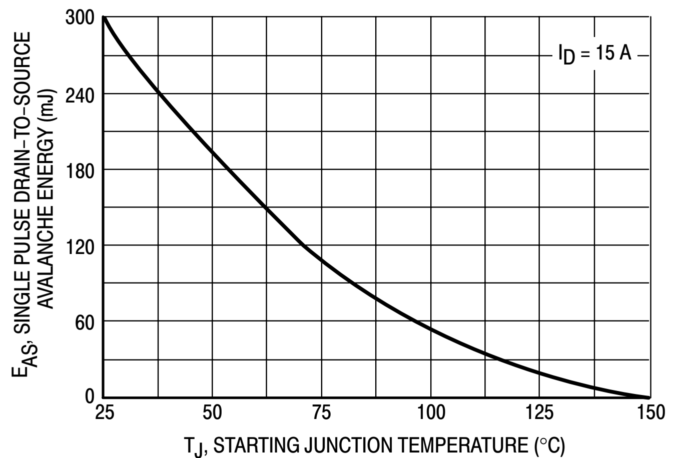



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

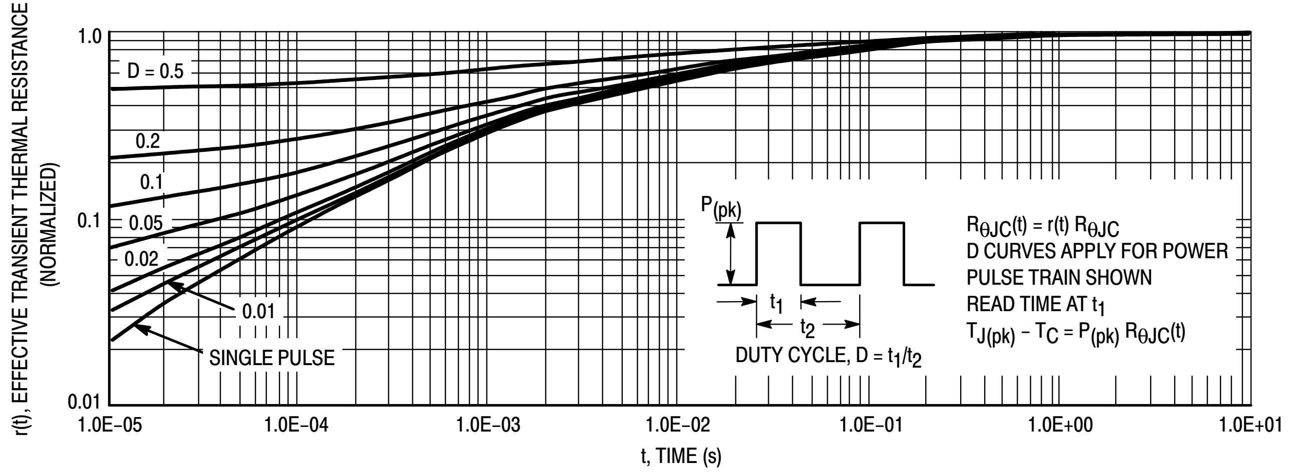



**Figure 14. Thermal Response**

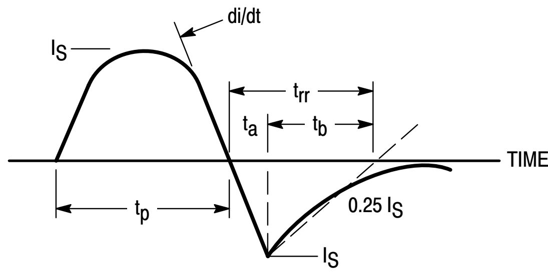
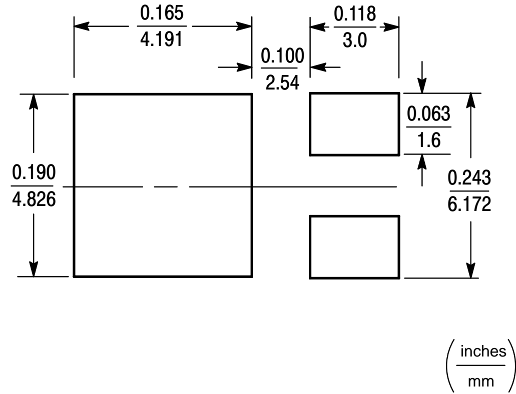



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 16.

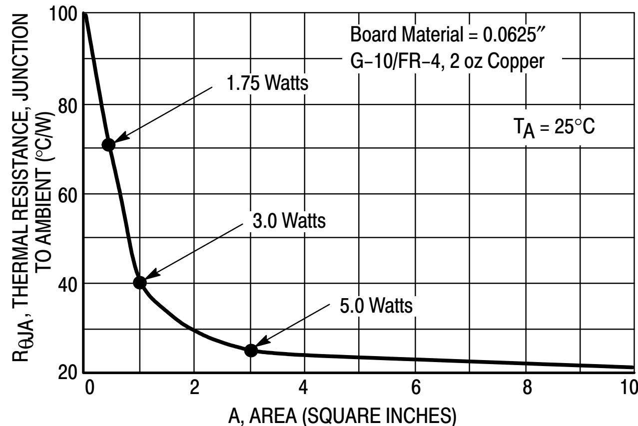



**Figure 16. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 17 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

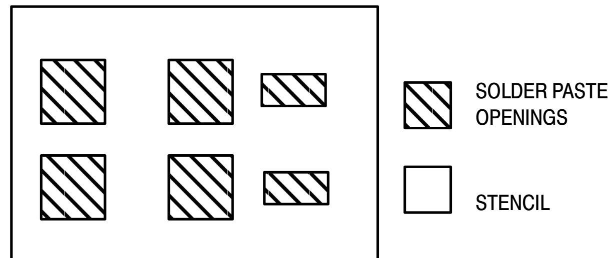



**Figure 17. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

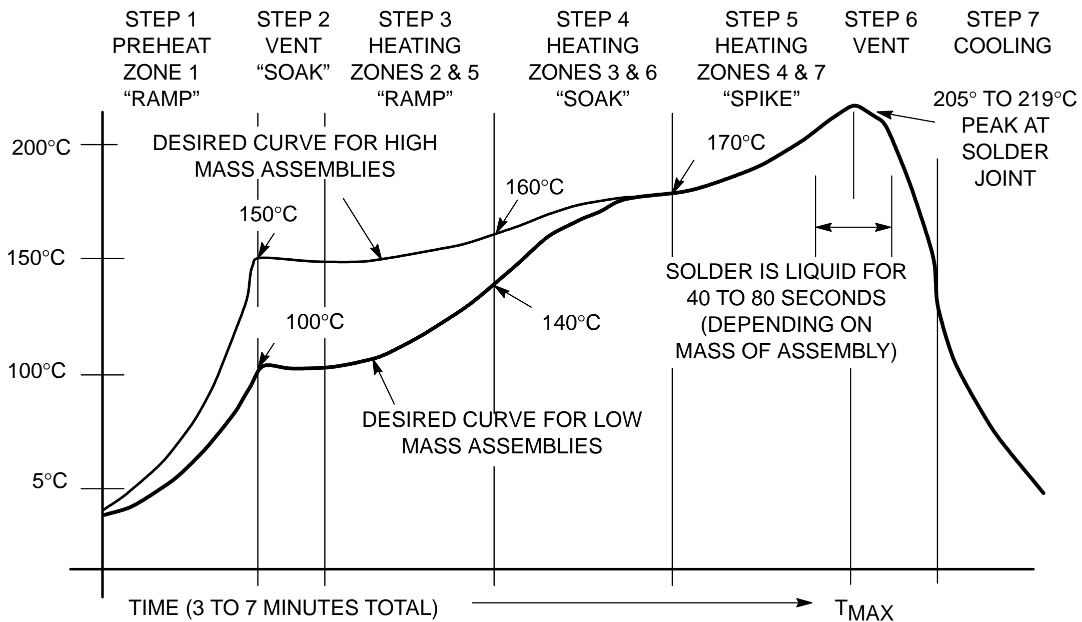



**Figure 18. Typical Solder Heating Profile**

# MTD2955V

# Power MOSFET 12 Amps, 60 Volts
## P–Channel DPAK

**ON Semiconductor™**

http://onsemi.com

**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 230 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

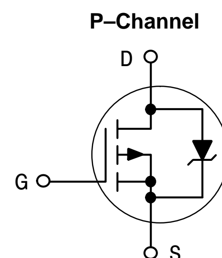
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

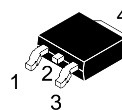
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>8.0<br>42 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ 25°C (Note 1.) | $P_D$ | 60<br>0.4<br>2.1 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 12 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 216 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.5<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

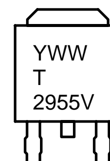
**P–Channel**




**MARKING DIAGRAM**

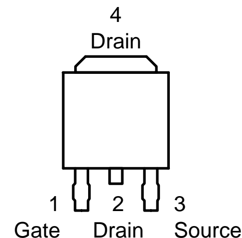



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD2955V | DPAK | 75 Units/Rail |
| MTD2955V1 | DPAK | 75 Units/Rail |
| MTD2955VT4 | DPAK | 2500 Tape & Reel |

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>58 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>5.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 1.5) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.185 | 0.230 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 12 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 2.9<br>2.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 3.0 | 5.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | 770 | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | 280 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 50 | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 50 | 100 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 24 | 50 | |
| Fall Time | | $t_f$ | – | 39 | 80 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 19 | 30 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 9.0 | – | |
| | | $Q_3$ | – | 7.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.8<br>1.5 | 3.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 115 | – | ns |
| | | $t_a$ | – | 90 | – | |
| | | $t_b$ | – | 25 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.53 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

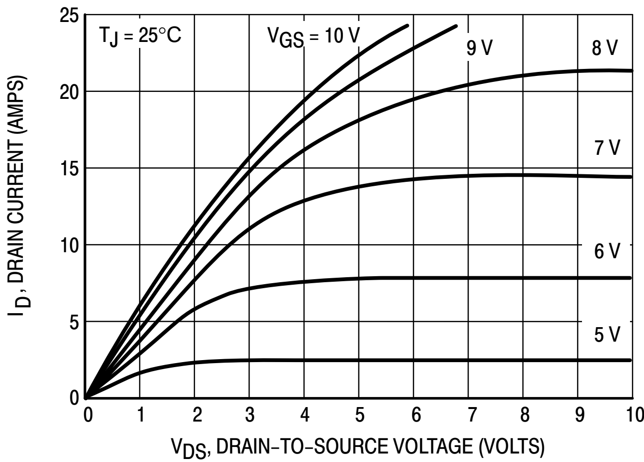



**Figure 1. On–Region Characteristics**

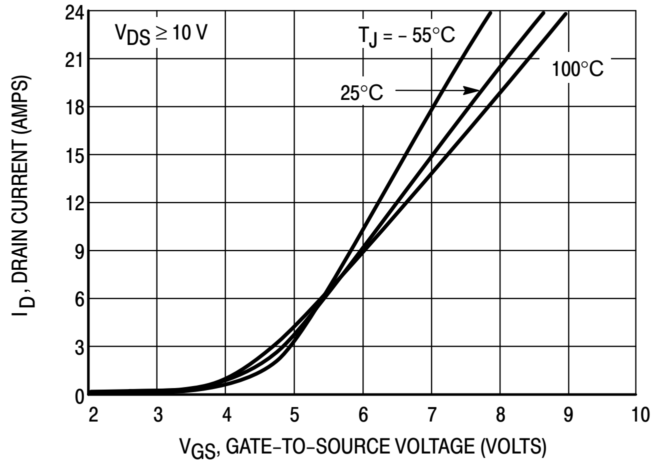



**Figure 2. Transfer Characteristics**

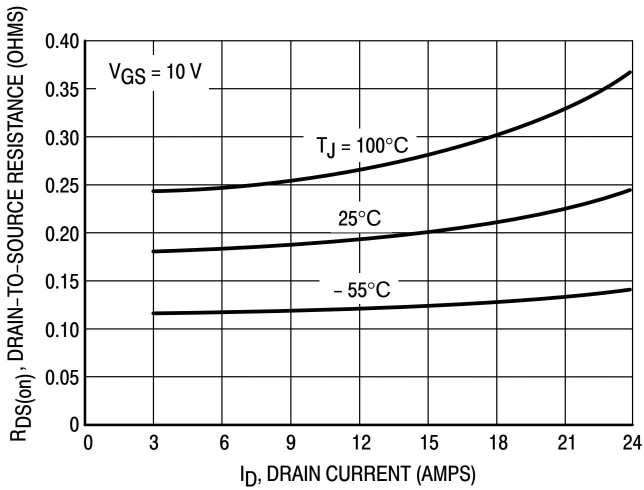



**Figure 3. On–Resistance versus Drain Current and Temperature**

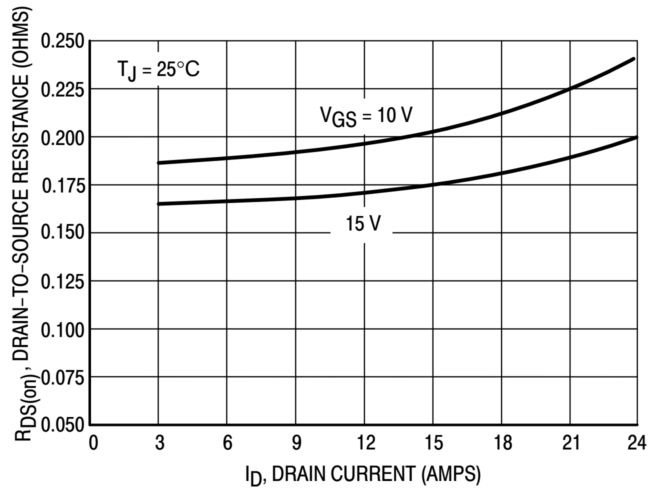



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

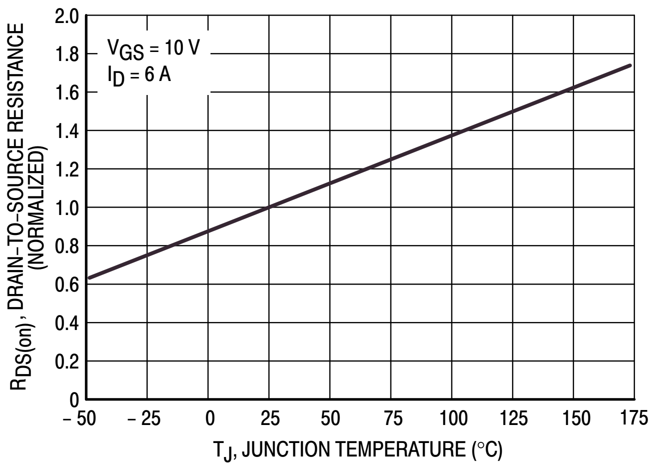



**Figure 5. On–Resistance Variation with Temperature**

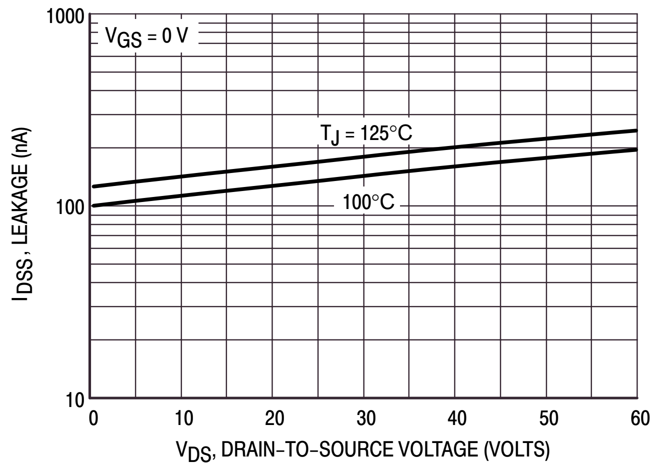



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

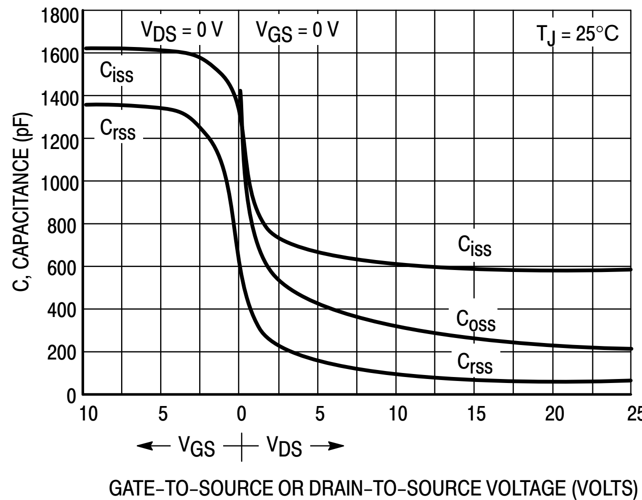



**Figure 7. Capacitance Variation**

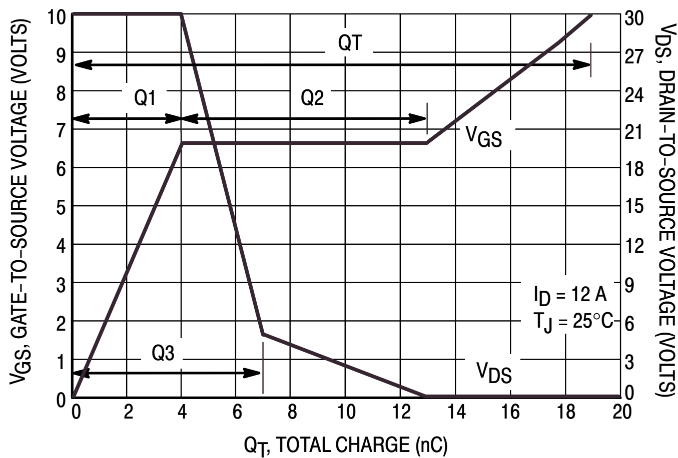



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

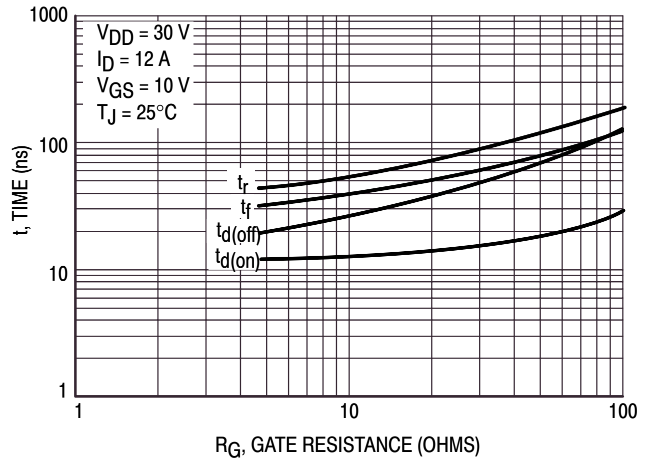



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

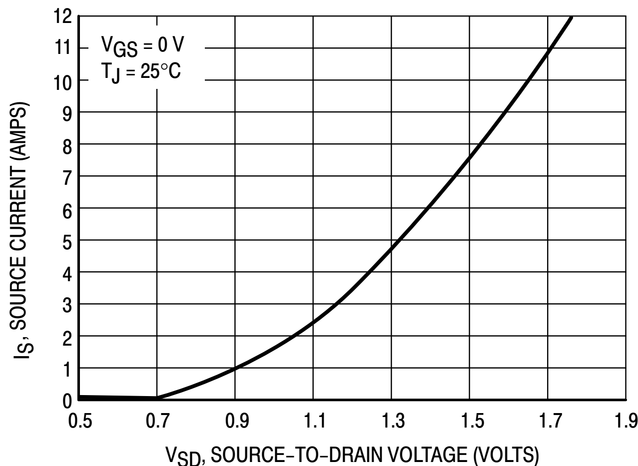



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

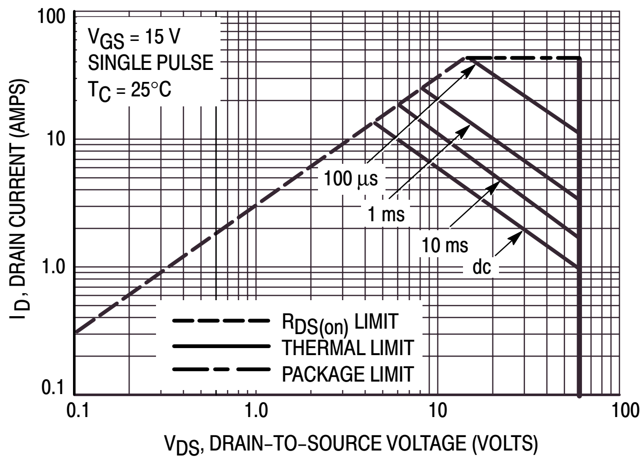



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

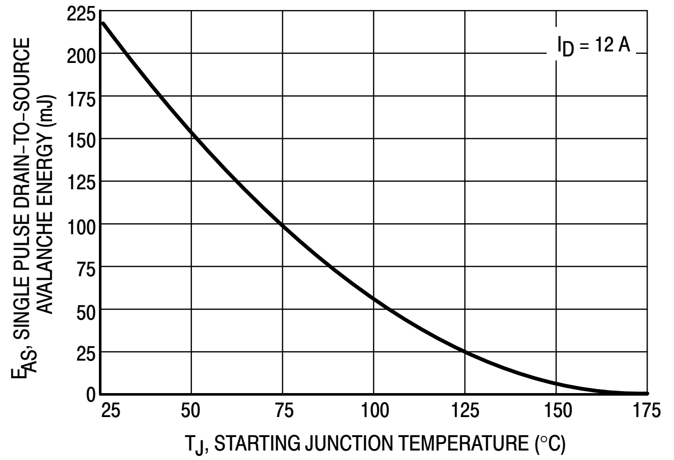



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

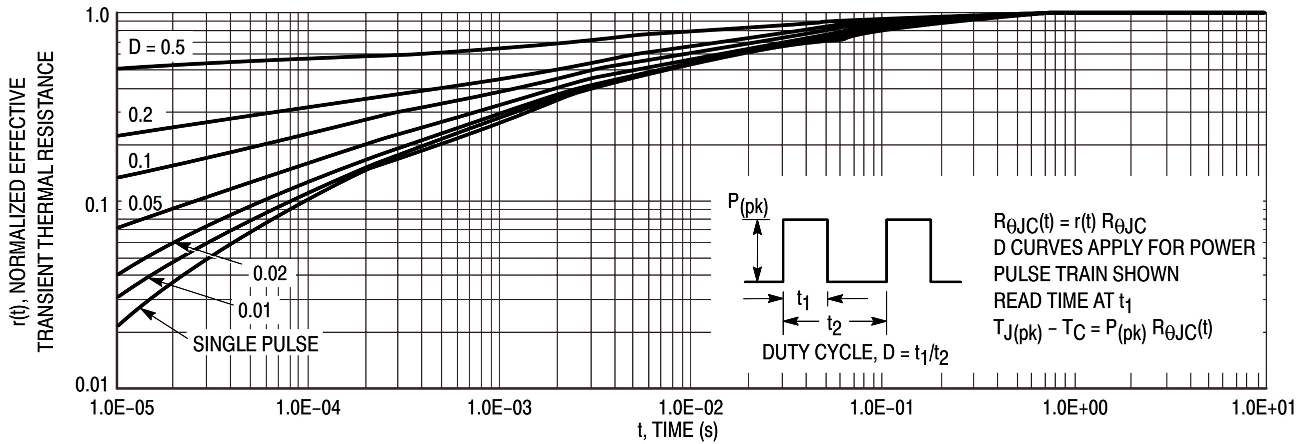



**Figure 13. Thermal Response**

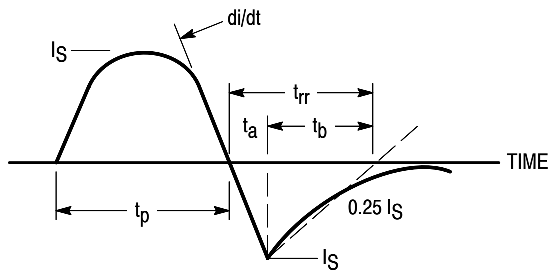
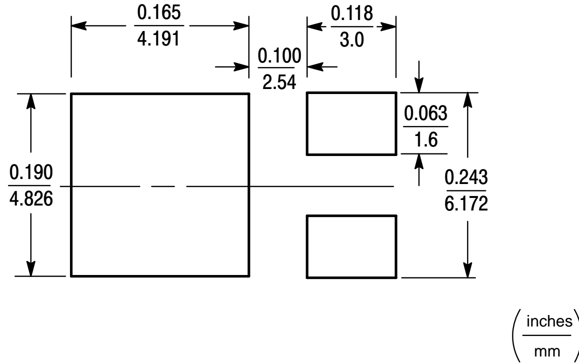



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

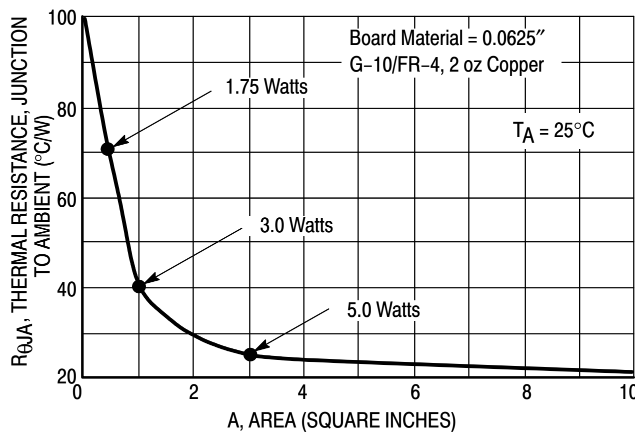



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

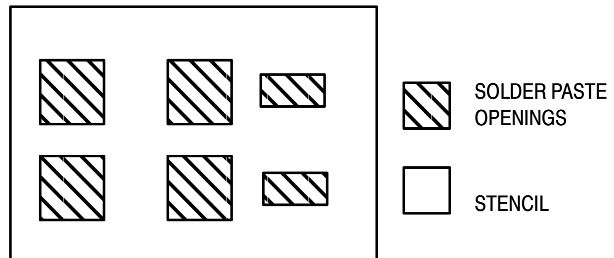



**Figure 16. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

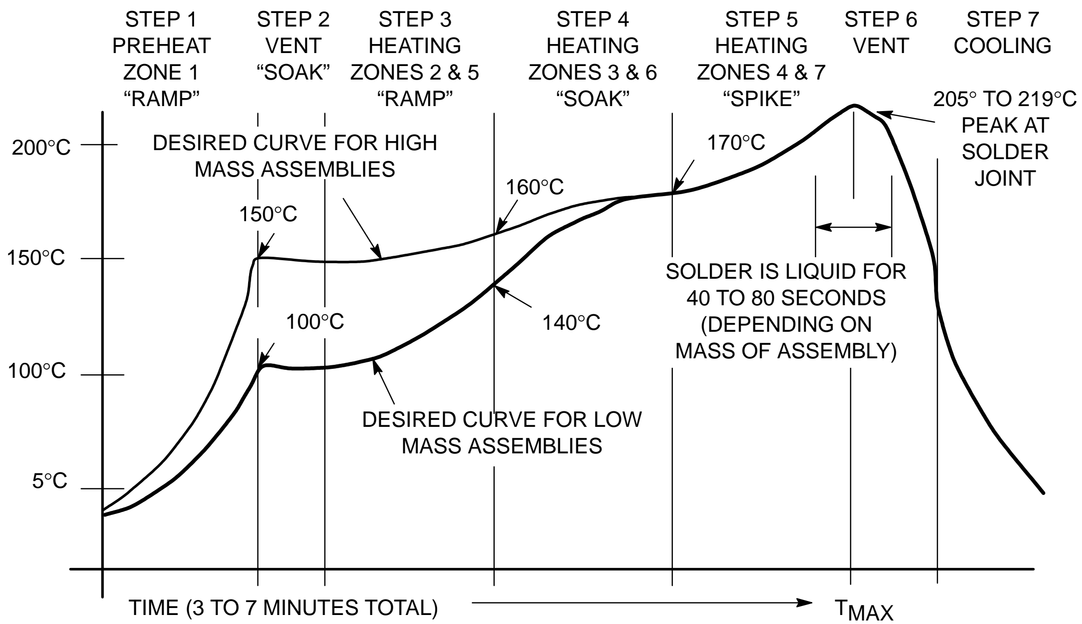



**Figure 15. Typical Solder Heating Profile**

# MTD3055V

**Preferred Device**

# Power MOSFET 12 Amps, 60 Volts

## N–Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

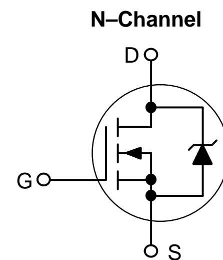
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>7.3<br>37 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 48<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 12 Apk, L = 1.0 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 72 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

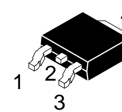
**http://onsemi.com**

**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 150 mΩ**

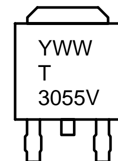
**N–Channel**




**MARKING DIAGRAM**

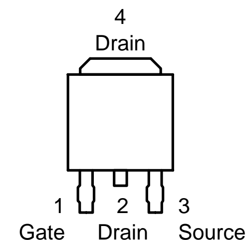



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD3055V | DPAK | 75 Units/Rail |
| MTD3055V1 | DPAK | 75 Units/Rail |
| MTD3055VT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>65 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>5.4 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.10 | 0.15 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 12 Adc)<br>($I_D$ = 6.0 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.3<br>– | 2.2<br>1.9 | Vdc |
| Forward Transconductance ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 4.0 | 5.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 410 | 500 | pF |
| Output Capacitance | | $C_{oss}$ | – | 130 | 180 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 25 | 50 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.0 | 10 | ns |
| Rise Time | | $t_r$ | – | 34 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 30 | |
| Fall Time | | $t_f$ | – | 18 | 50 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 12.2 | 17 | nC |
| | | $Q_1$ | – | 3.2 | – | |
| | | $Q_2$ | – | 5.2 | – | |
| | | $Q_3$ | – | 5.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.0<br>0.91 | 1.6<br>– | Vdc |
| Reverse Recovery Time (See Figure 15) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 40 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.128 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

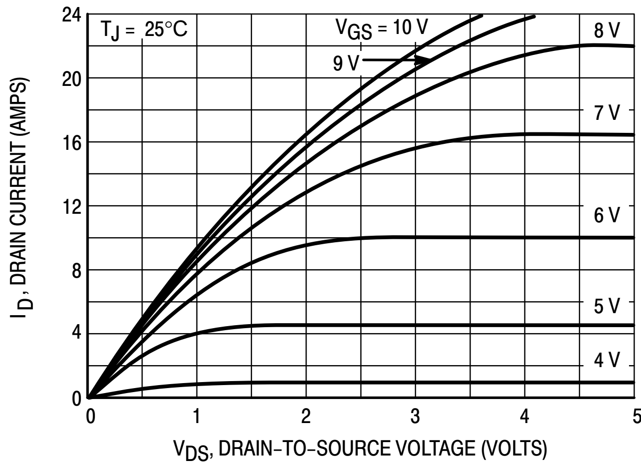



**Figure 1. On–Region Characteristics**

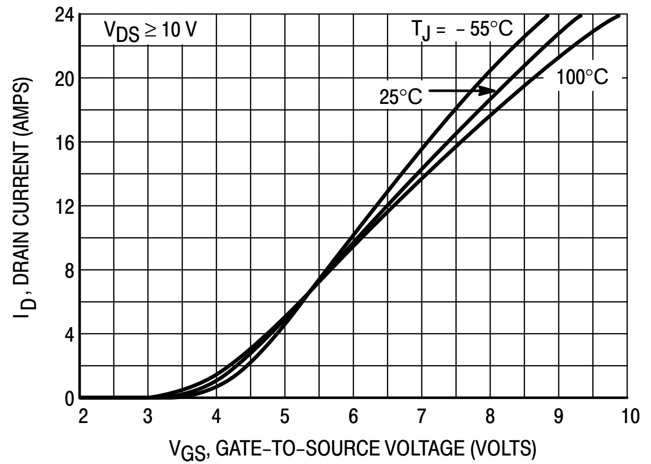



**Figure 2. Transfer Characteristics**

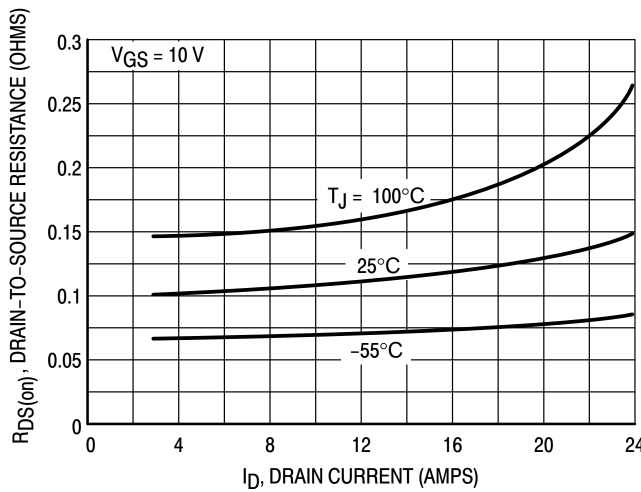



**Figure 3. On–Resistance versus Drain Current and Temperature**

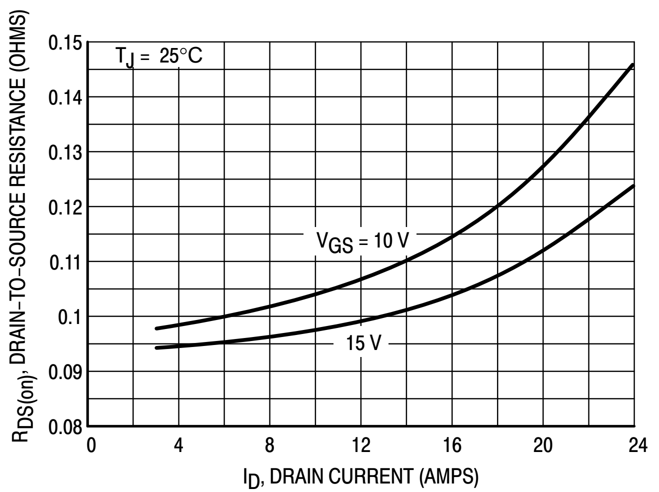



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

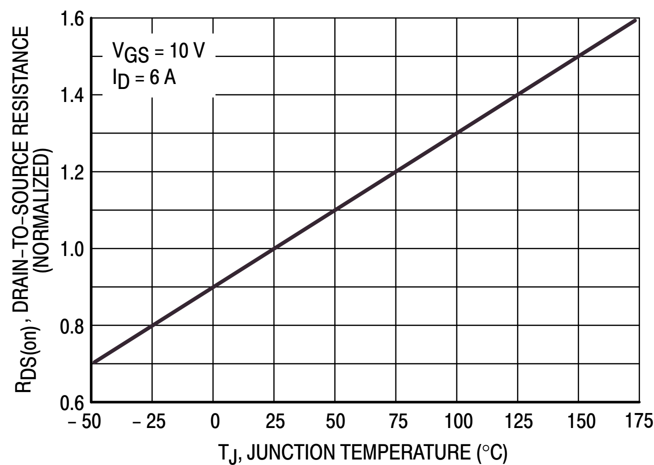



**Figure 5. On–Resistance Variation with Temperature**

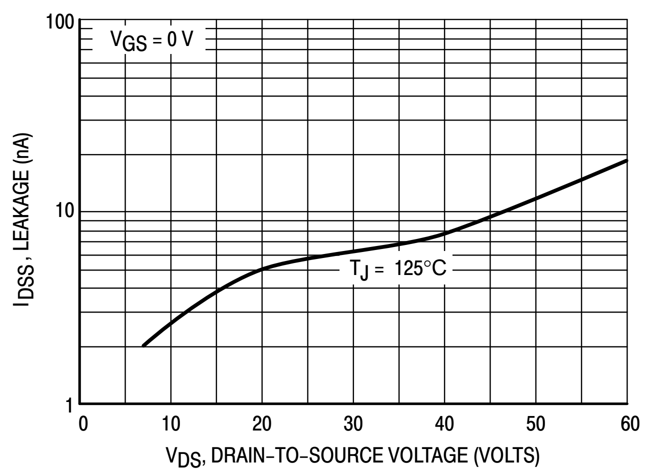



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

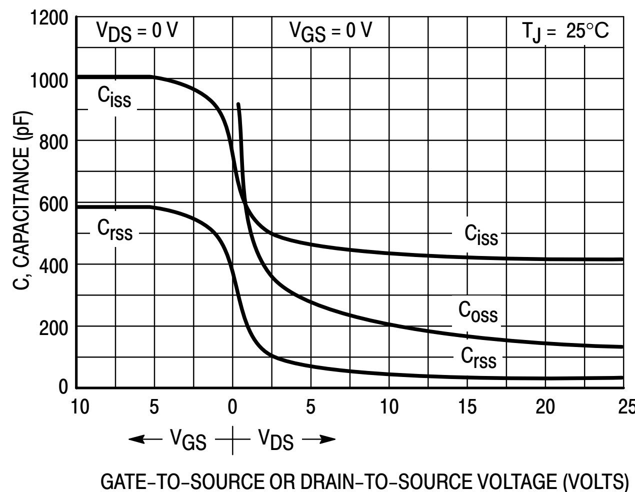



**Figure 7. Capacitance Variation**

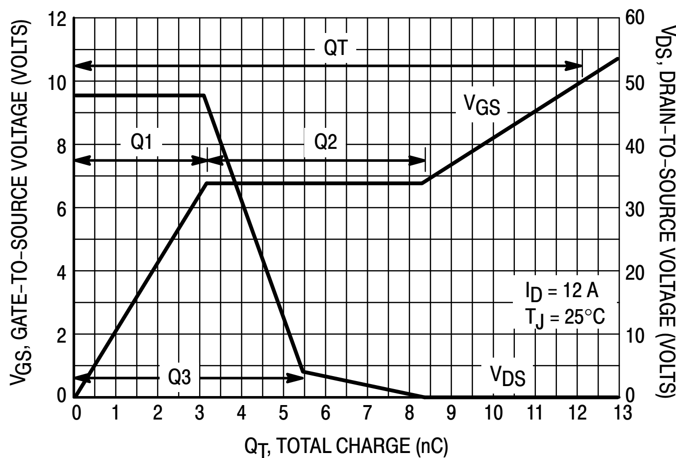



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

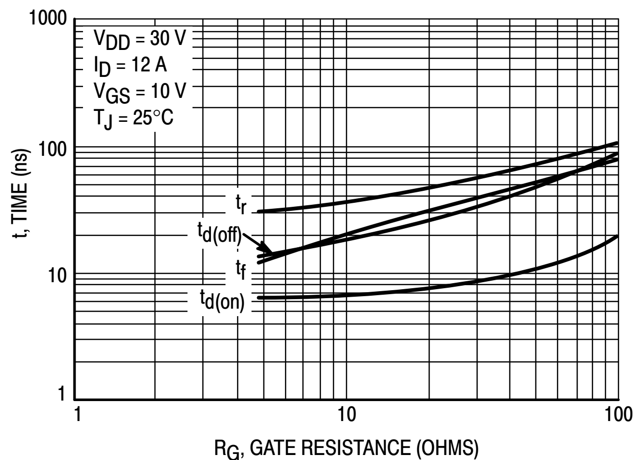



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

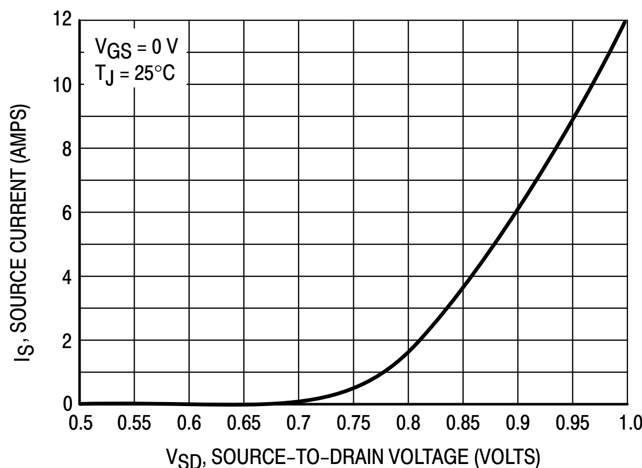



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

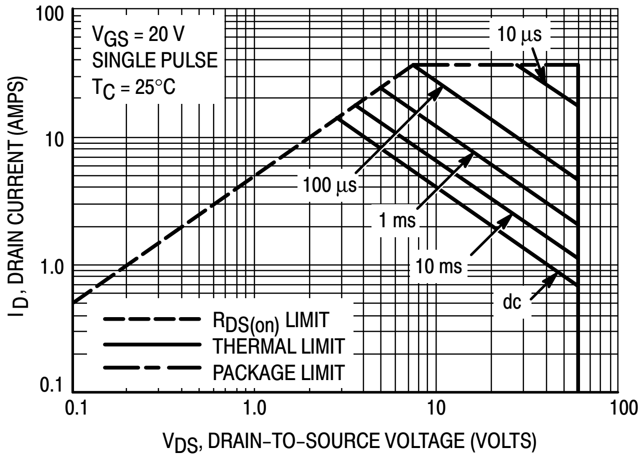



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

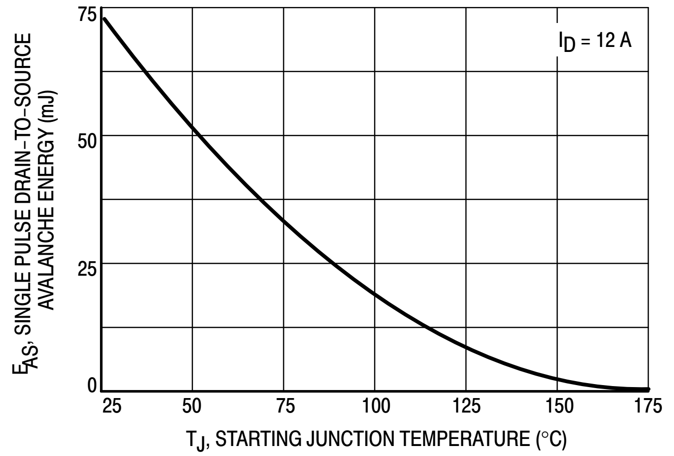



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

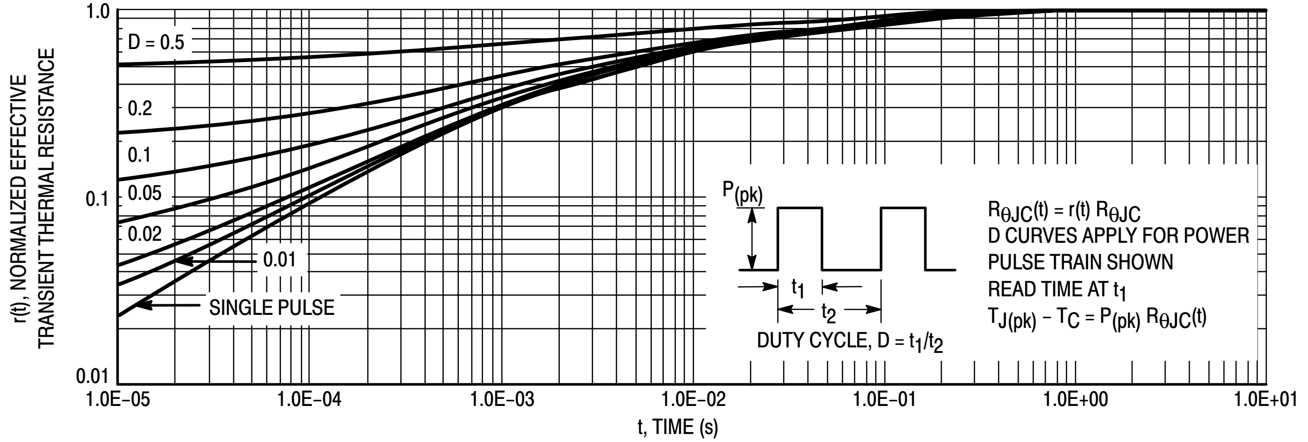



**Figure 13. Thermal Response**

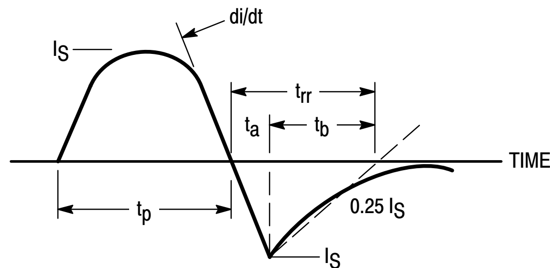
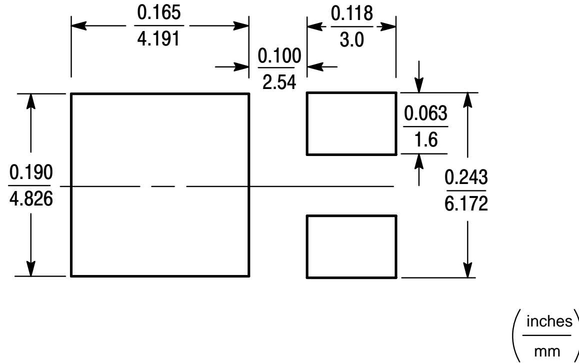



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

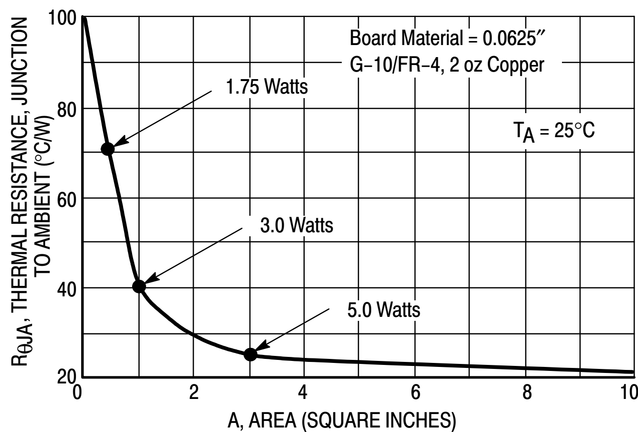



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D2PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and D2PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

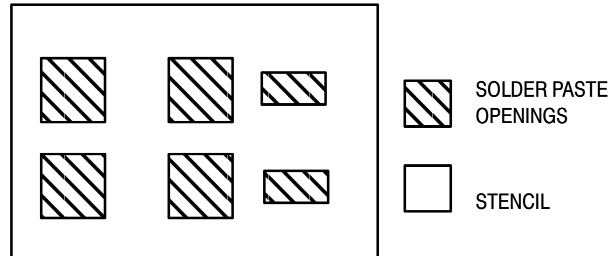



**Figure 16. Typical Stencil for DPAK and D2PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D2PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

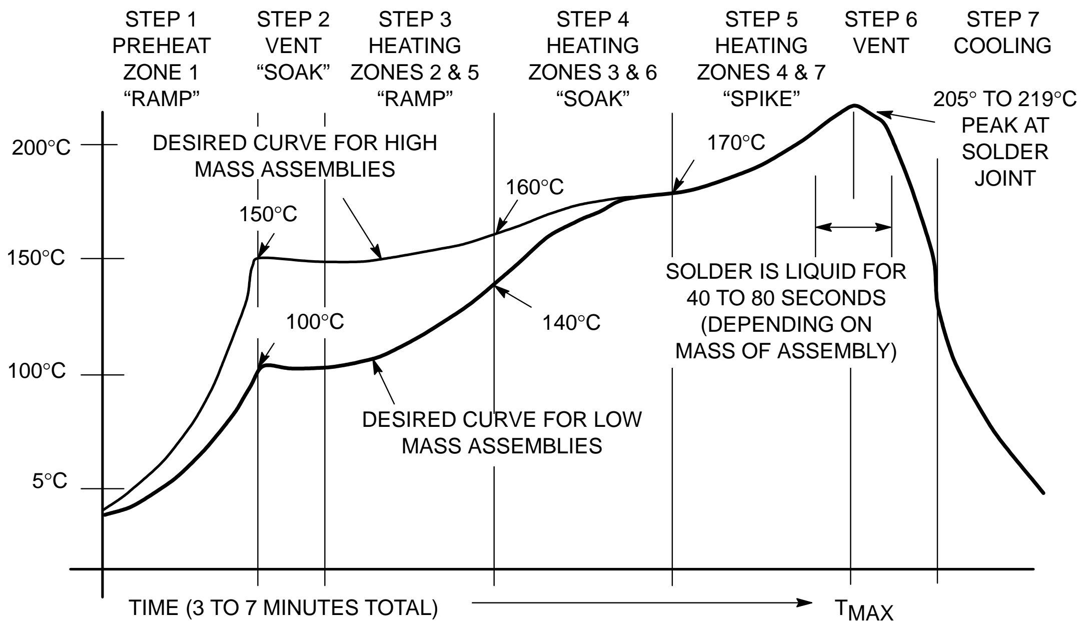



**Figure 15. Typical Solder Heating Profile**

# MTD3055VL

**Preferred Device**

# Power MOSFET 12 Amps, 60 Volts
## N–Channel DPAK

**ON Semiconductor™**

http://onsemi.com

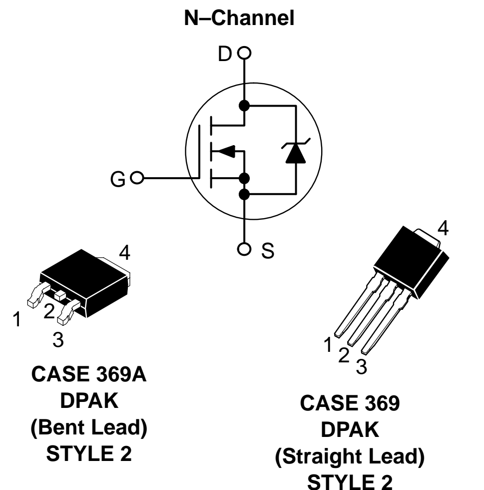
**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 180 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

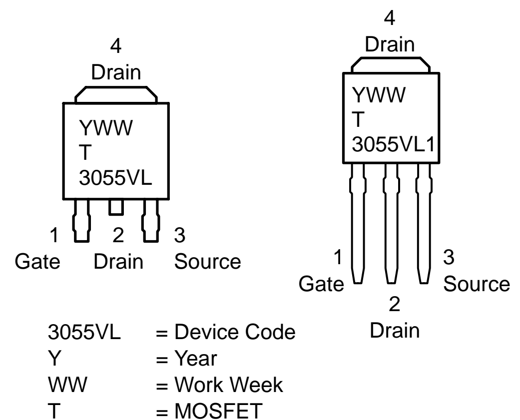
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Single Pulse ($t_p$ ≤ 50 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>8.0<br>42 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 48<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, $I_L$ = 12 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 72 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |




**MARKING DIAGRAMS & PIN ASSIGNMENTS**




3055VL = Device Code
Y = Year
WW = Work Week
T = MOSFET

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD3055VL | DPAK | 75 Units/Rail |
| MTD3055VL1 | DPAK (Straight Lead) | 75 Units/Rail |
| MTD3055VLT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>62 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.6<br>3.0 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.12 | 0.18 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc)<br>($I_D$ = 12 Adc)<br>($I_D$ = 6.0 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.6<br>– | 2.6<br>2.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 5.0 | 8.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 410 | 570 | pF |
| Output Capacitance | | $C_{oss}$ | – | 114 | 160 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 21 | 40 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 9.0 | 20 | ns |
| Rise Time | | $t_r$ | – | 85 | 190 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 14 | 30 | |
| Fall Time | | $t_f$ | – | 43 | 90 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 8.1 | 10 | nC |
| | | $Q_1$ | – | 1.8 | – | |
| | | $Q_2$ | – | 4.2 | – | |
| | | $Q_3$ | – | 3.8 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 0.97<br>0.86 | 1.3<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 55.7 | – | ns |
| | | $t_a$ | – | 37 | – | |
| | | $t_b$ | – | 18.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.116 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

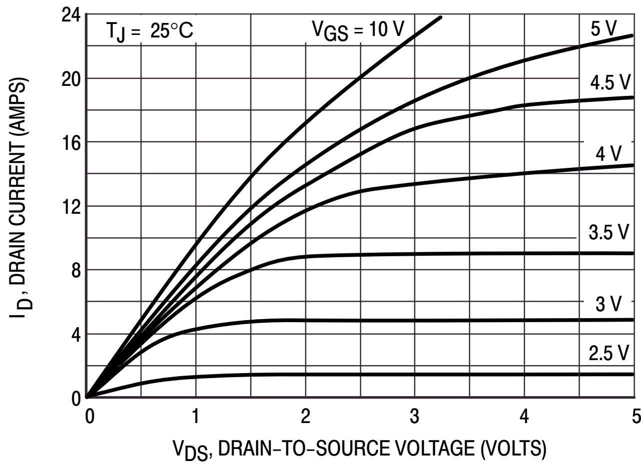



**Figure 1. On–Region Characteristics**

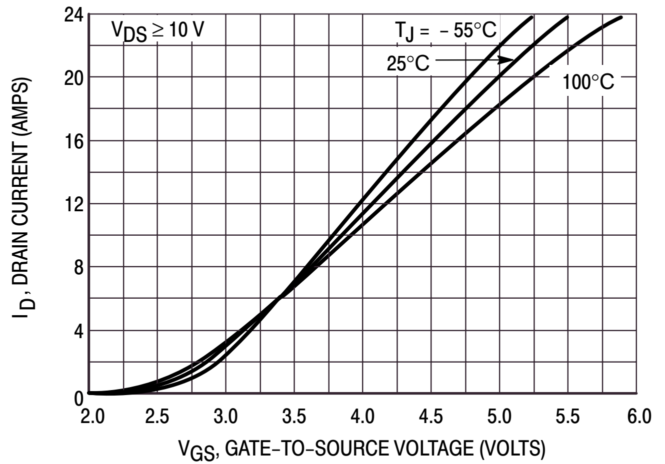



**Figure 2. Transfer Characteristics**

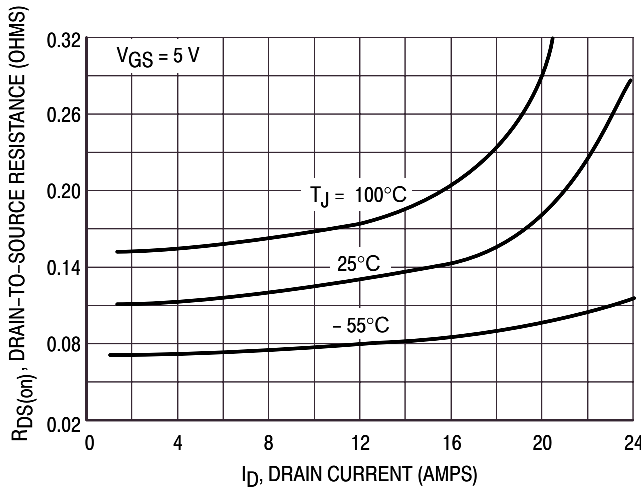



**Figure 3. On–Resistance versus Drain Current and Temperature**

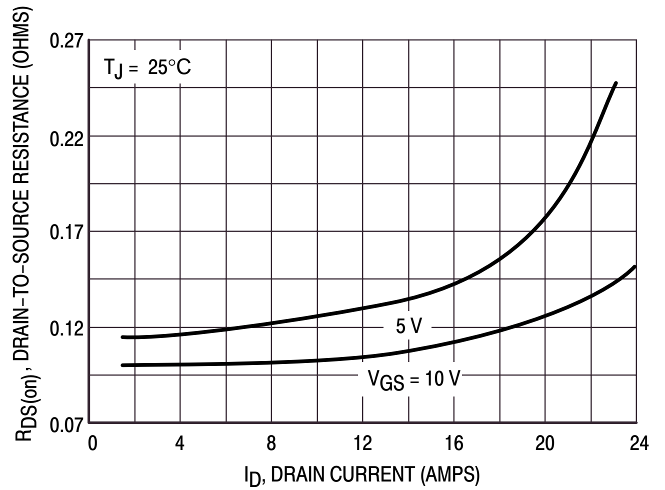



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

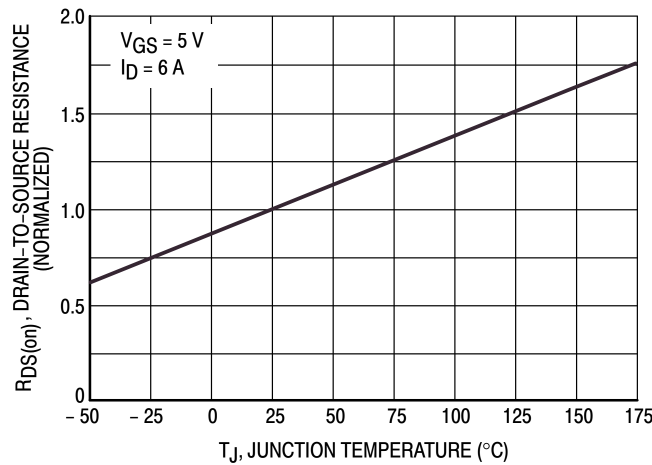



**Figure 5. On–Resistance Variation with Temperature**

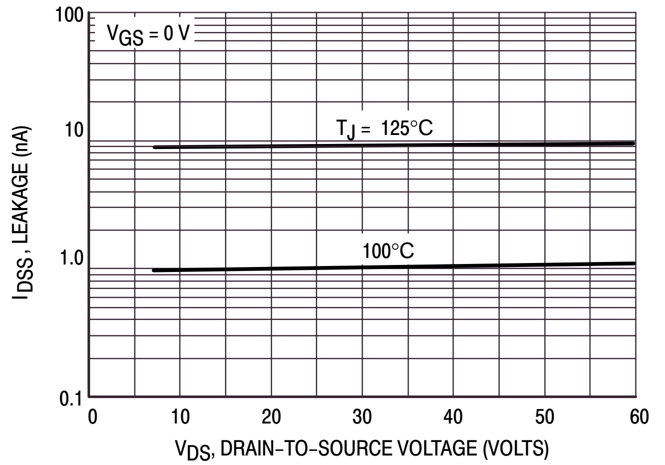



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

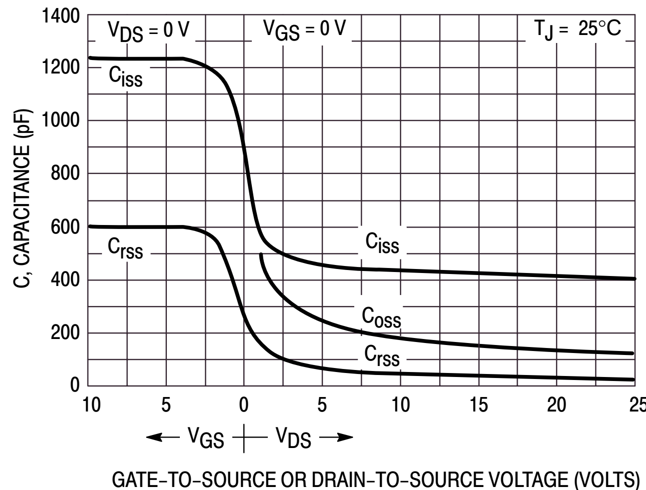



**Figure 7. Capacitance Variation**

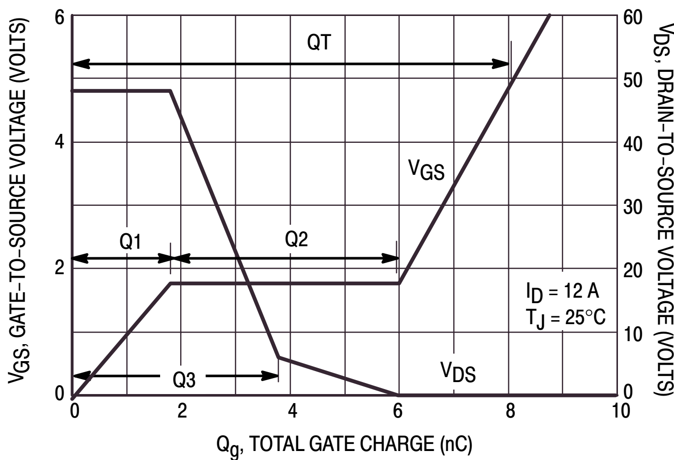



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

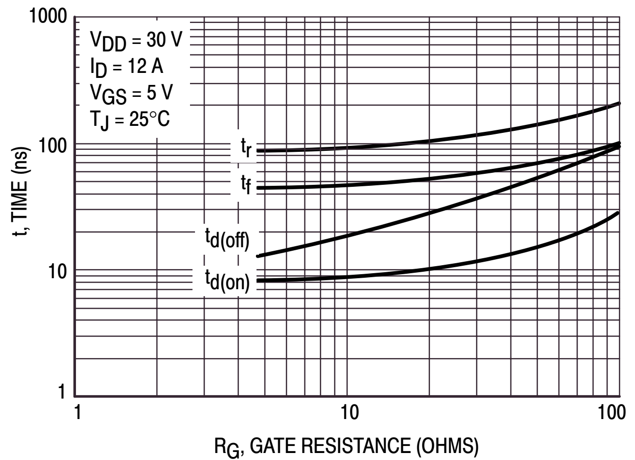



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

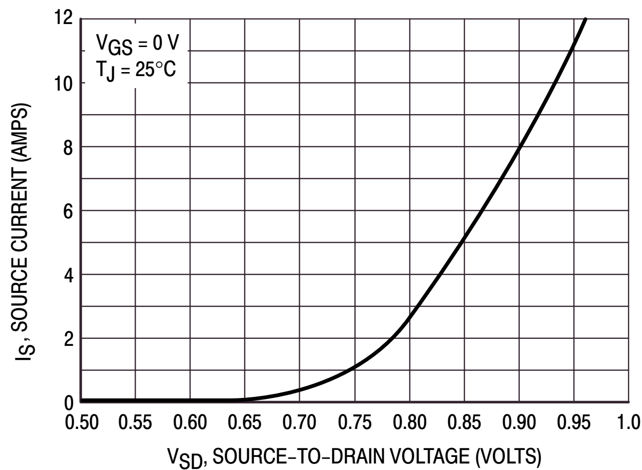



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

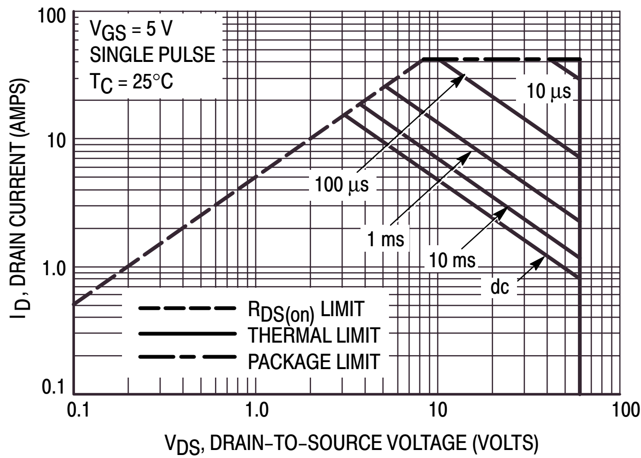



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

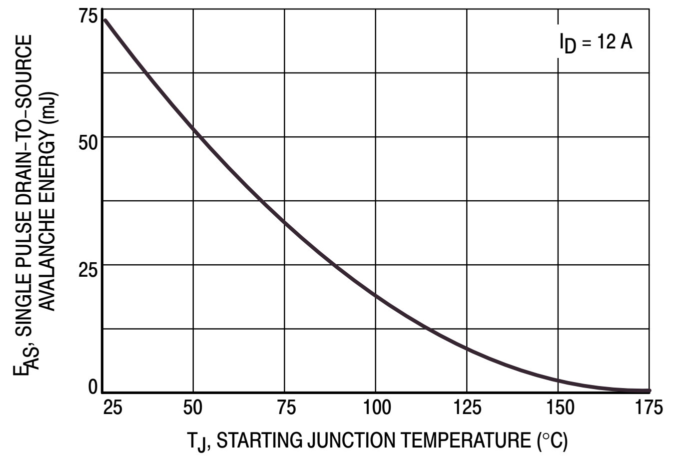



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

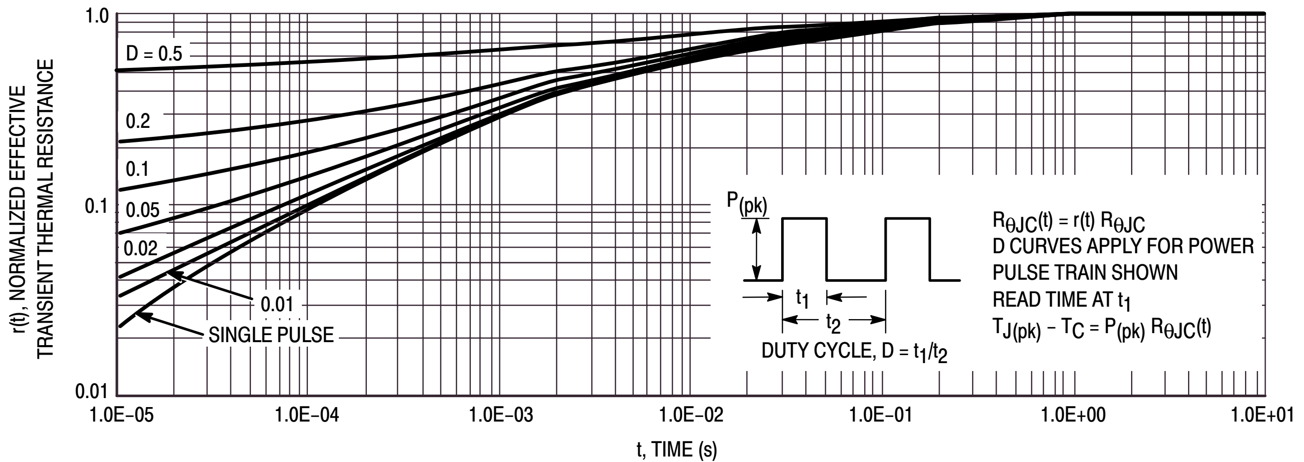



**Figure 13. Thermal Response**

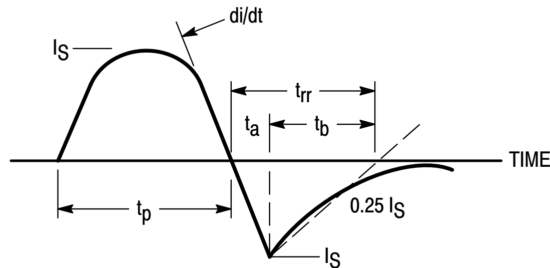
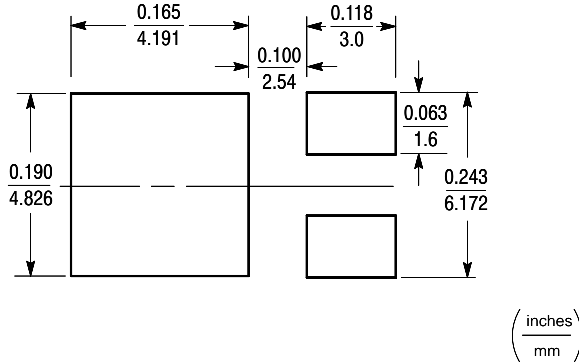



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

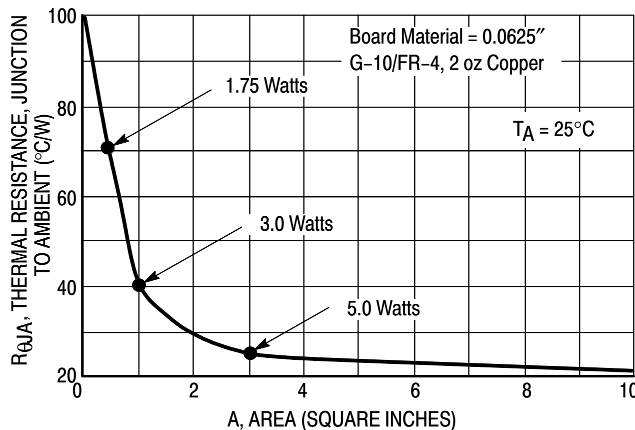



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

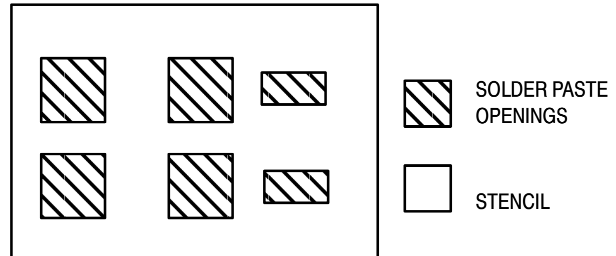



**Figure 16. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

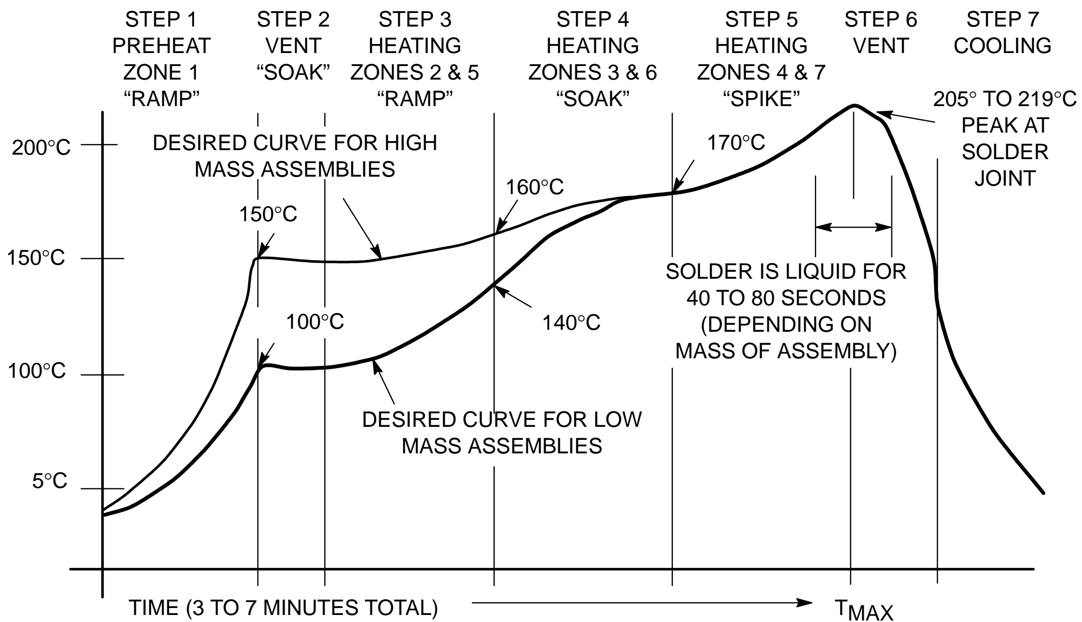



**Figure 17. Typical Solder Heating Profile**

# MTD3302

*Advance Information*

## Power MOSFET 18 Amps, 30 Volts

### N–Channel DPAK

**ON Semiconductor™**

**http://onsemi.com**

**18 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 10 mΩ**

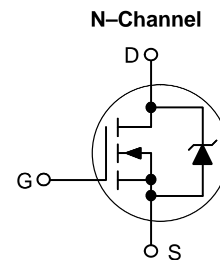
This Power MOSFET is capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. These devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Characterized Over a Wide Range of Power Ratings
- Ultralow $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life in Portable Applications
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified

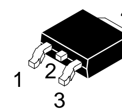
**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage | $V_{GS}$ | ±20 | Vdc |
| Gate–to–Source Operating Voltage | $V_{GS}$ | ±16 | Vdc |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, L = 20 mH, $I_{L(pk)}$ = 10 A, $V_{DS}$ = 30 Vdc) | $E_{AS}$ | 1000 | mJ |

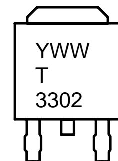
**N–Channel**




**MARKING DIAGRAM**

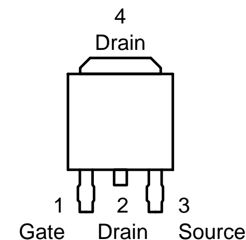



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD3302 | DPAK | 75 Units/Rail |
| MTD3302T4 | DPAK | 2500 Tape & Reel |

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**POWER RATINGS** ($T_J$ = 25°C unless otherwise specified)

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C | | $I_D$ | 30 | Adc |
| – Continuous @ $T_A$ = 100°C | Mounted on heat sink | $I_D$ | 30 | Adc |
| – Single Pulse (tp ≤ 10 µs) | $T_{case}$ = 25°C | $I_{DM}$ | 90 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C | | $P_D$ | 96 | Watts |
| Linear Derating Factor | $V_{GS}$ = 10 Vdc | | 769 | mW/°C |
| Thermal Resistance – Junction–to–Case | Steady State | $R_{\theta JC}$ | 1.3 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 30 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C | | $I_D$ | 18.3 | Adc |
| – Continuous @ $T_A$ = 100°C | Mounted on 1 inch square | $I_D$ | 11.2 | Adc |
| – Single Pulse (tp ≤ 10 µs) | FR–4 or G10 board | $I_{DM}$ | 60 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C | | $P_D$ | 5.0 | Watts |
| Linear Derating Factor | $V_{GS}$ = 10 Vdc | | 40 | mW/°C |
| Thermal Resistance – Junction–to–Ambient | t ≤ 10 seconds | $R_{\theta JA}$ | 25 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 6.4 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C | | $I_D$ | 11.2 | Adc |
| – Continuous @ $T_A$ = 100°C | Mounted on 1 inch square | $I_D$ | 8.6 | Adc |
| – Single Pulse (tp ≤ 10 µs) | FR–4 or G10 board | $I_{DM}$ | 40 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C | | $P_D$ | 1.9 | Watts |
| Linear Derating Factor | $V_{GS}$ = 10 Vdc | | 15 | mW/°C |
| Thermal Resistance – Junction–to–Ambient | Steady State | $R_{\theta JA}$ | 67 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 2.5 | Adc |

| Parameter | | Symbol | Value | Unit |
|---|---|---|---|---|
| Drain Current – Continuous @ $T_A$ = 25°C | | $I_D$ | 8.3 | Adc |
| – Continuous @ $T_A$ = 100°C | Mounted on minimum recommended | $I_D$ | 5.2 | Adc |
| – Single Pulse (tp ≤ 10 µs) | FR–4 or G10 board | $I_{DM}$ | 30 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C | | $P_D$ | 1.0 | Watts |
| Linear Derating Factor | $V_{GS}$ = 10 Vdc | | 8.3 | mW/°C |
| Thermal Resistance – Junction–to–Ambient | Steady State | $R_{\theta JA}$ | 120 | °C/W |
| Continuous Source Current (Diode Conduction) | | $I_S$ | 1.4 | Adc |

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise specified)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 30 | 33 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 23 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | 0.005 | 1.0 | μAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | 0.5 | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | 2 | ±100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.9 | – | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.6 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 8.9 | 10 | mΩ |
| ($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc) | | | – | 13 | 16 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 12 | 19 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1760 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 610 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 185 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 10 | 20 | ns |
| Rise Time | | $t_r$ | – | 30 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 65 | 130 | |
| Fall Time | | $t_f$ | – | 58 | 110 | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) | $t_{d(on)}$ | – | 20 | 40 | ns |
| Rise Time | | $t_r$ | – | 86 | 170 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 44 | 80 | |
| Fall Time | | $t_f$ | – | 48 | 90 | |
| Gate Charge | ($V_{DS}$ = 15 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 47 | 60 | nC |
| | | $Q_1$ | – | 4.8 | – | |
| | | $Q_2$ | – | 16.7 | – | |
| | | $Q_3$ | – | 11.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.87 | 1.1 | Vdc |
| | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.72 | – | |
| Reverse Recovery Time | ($I_S$ = 2.3 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 41 | – | ns |
| | | $t_a$ | – | 21 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.047 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperatures.

## TYPICAL ELECTRICAL CHARACTERISTICS

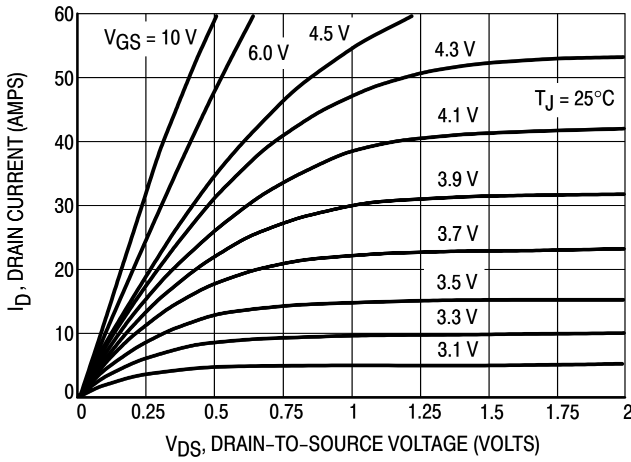



**Figure 1. On–Region Characteristics**

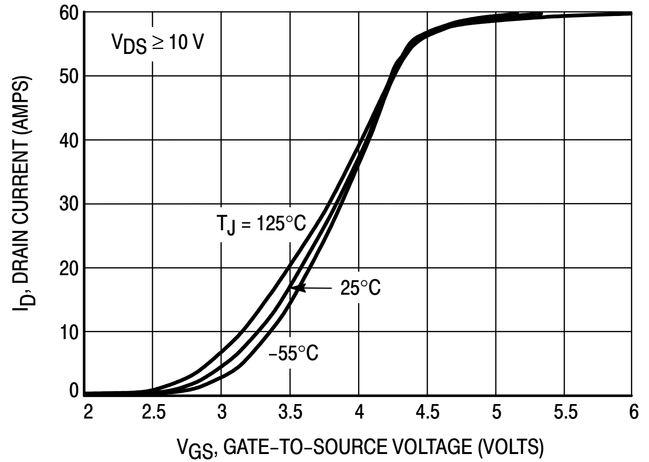



**Figure 2. Transfer Characteristics**

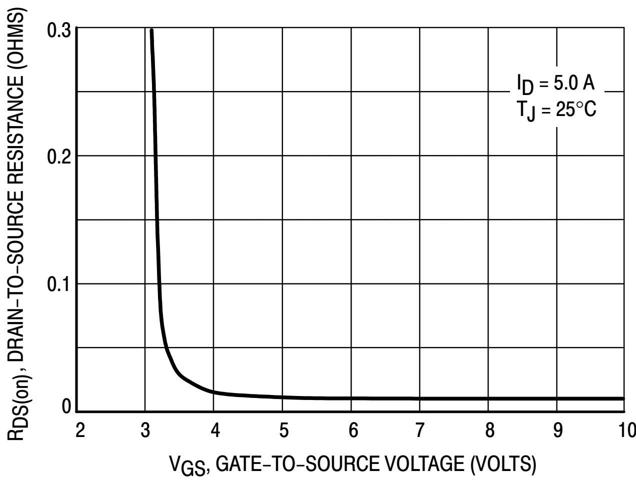



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

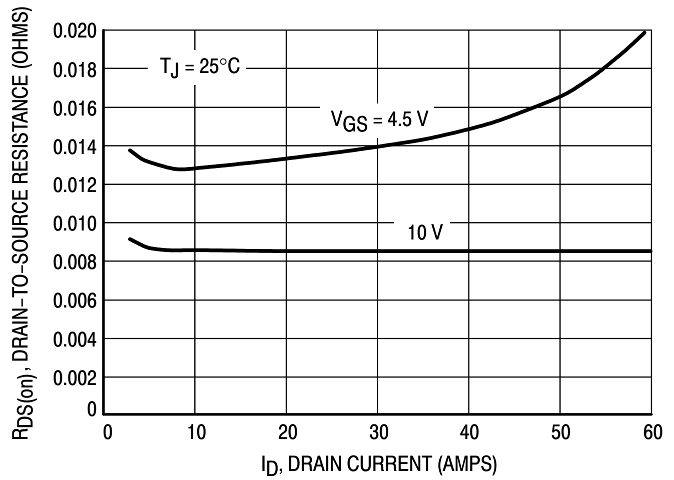



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

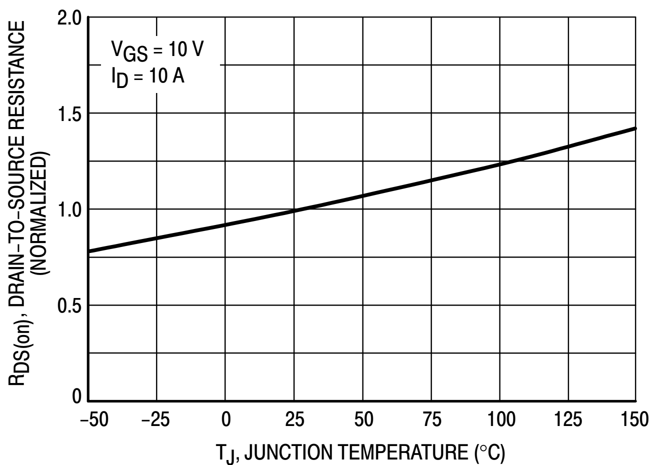



**Figure 5. On–Resistance Variation with Temperature**

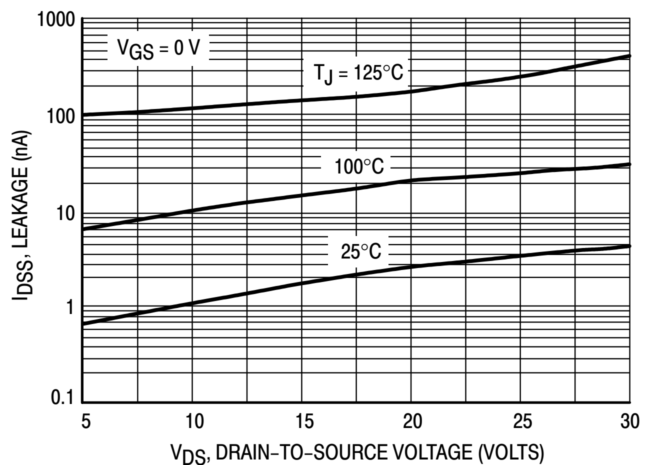



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

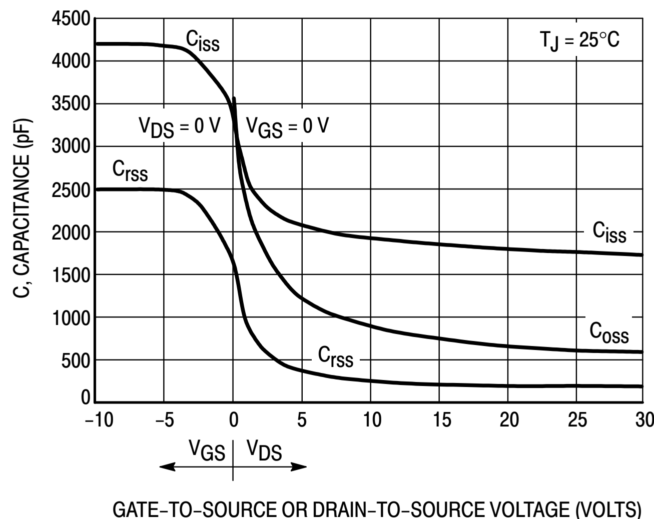



**Figure 7. Capacitance Variation**

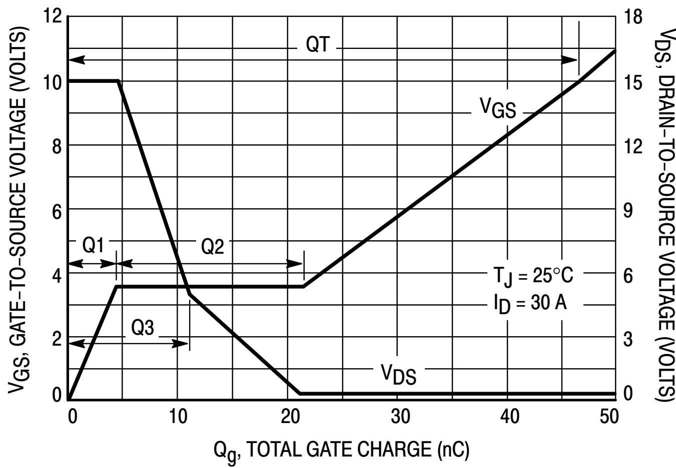



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

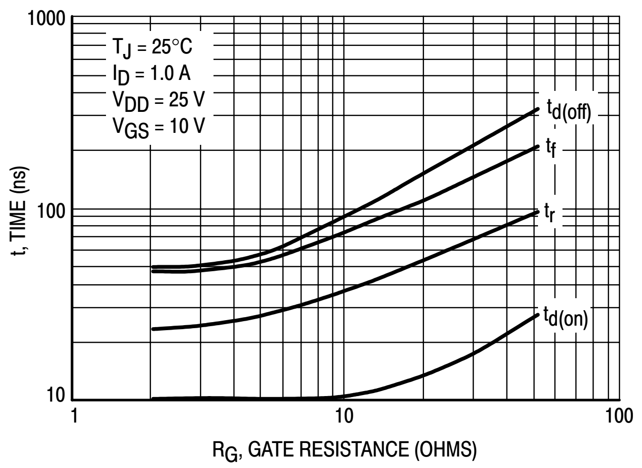



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

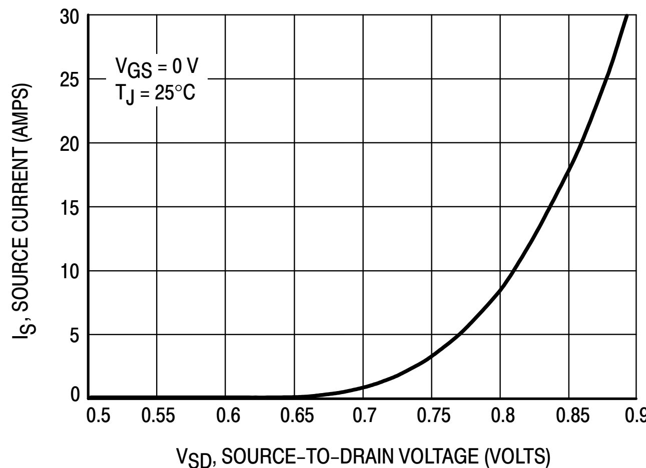



**Figure 10. Diode Forward Voltage versus Current**

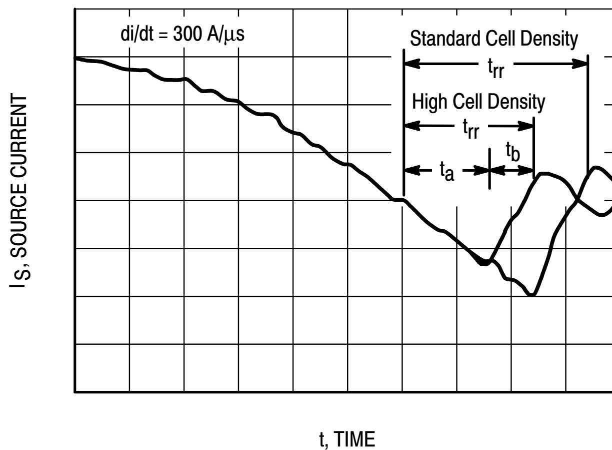



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

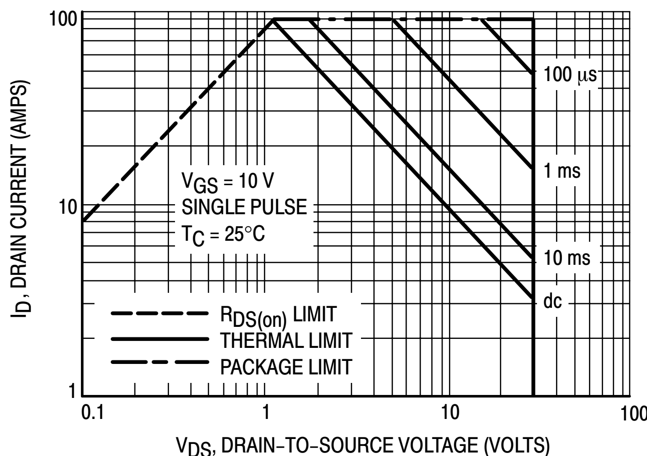



Figure 12. Maximum Rated Forward Biased Safe Operating Area

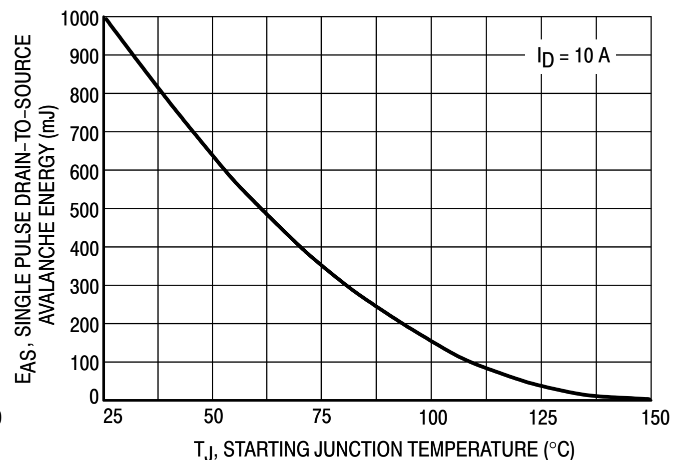



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

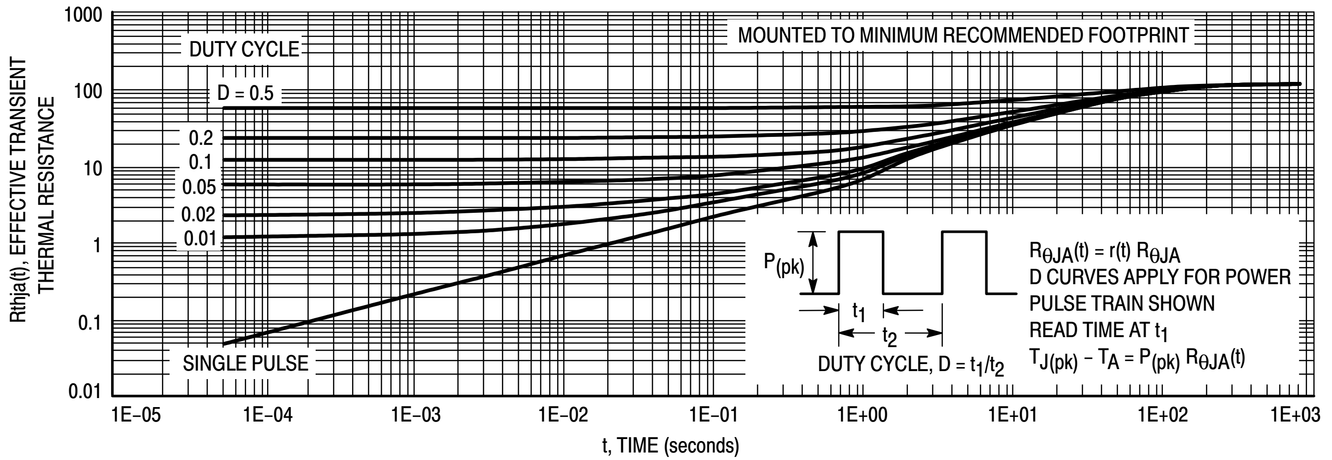
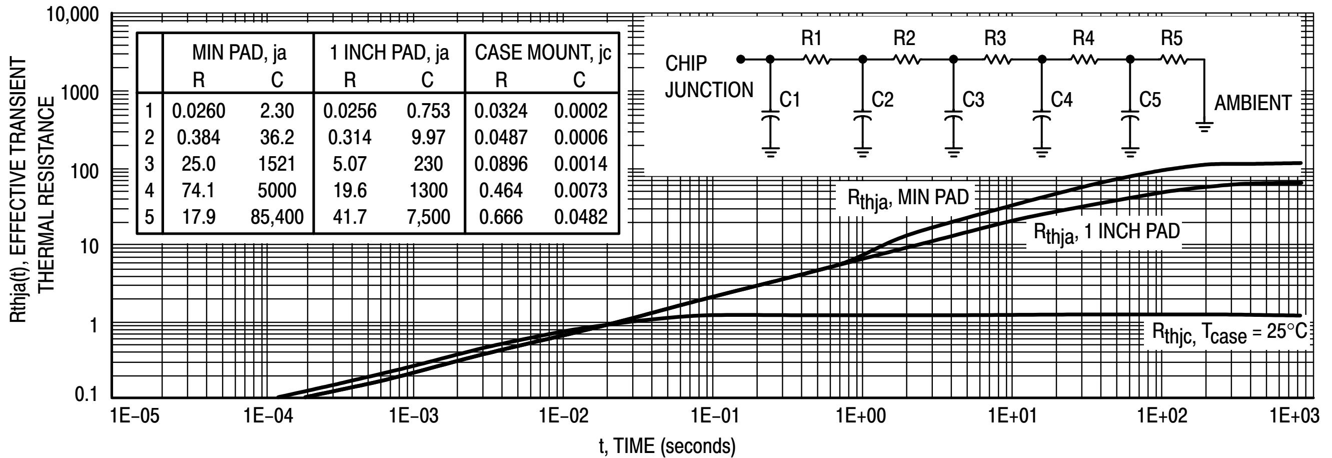



**Figure 14. Thermal Response – Various Duty Cycles**




| | MIN PAD, ja | | 1 INCH PAD, ja | | CASE MOUNT, jc | |
|---|---|---|---|---|---|---|
| | R | C | R | C | R | C |
| 1 | 0.0260 | 2.30 | 0.0256 | 0.753 | 0.0324 | 0.0002 |
| 2 | 0.384 | 36.2 | 0.314 | 9.97 | 0.0487 | 0.0006 |
| 3 | 25.0 | 1521 | 5.07 | 230 | 0.0896 | 0.0014 |
| 4 | 74.1 | 5000 | 19.6 | 1300 | 0.464 | 0.0073 |
| 5 | 17.9 | 85,400 | 41.7 | 7,500 | 0.666 | 0.0482 |

**Figure 15. Thermal Response – Various Mounting/Measurement Conditions**

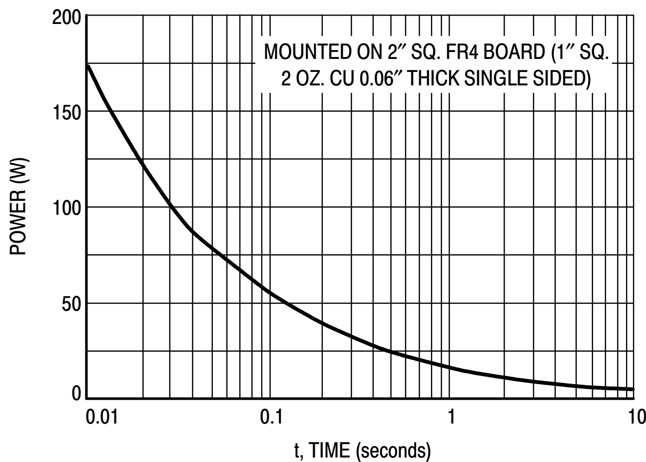



**Figure 16. Single Pulse Power**

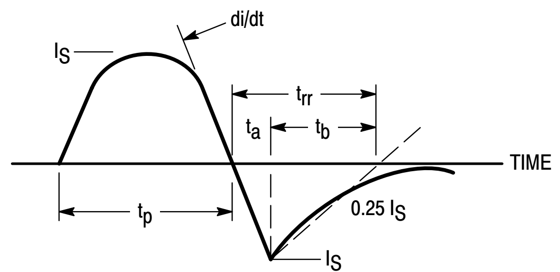
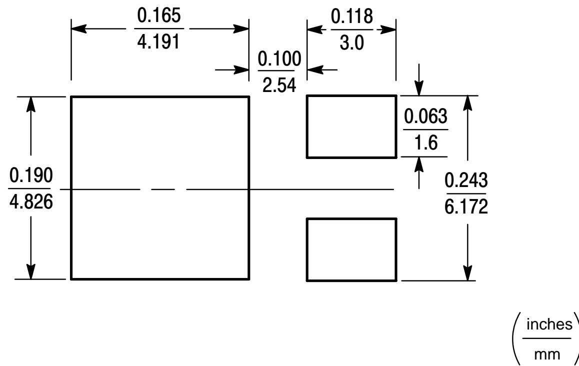



**Figure 17. Diode Reverse Recovery Waveform**

## INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

### RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




### POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. Note that these values may vary depending on the device type. Consult the maximum ratings table on the data sheet to find the actual $P_D$ and $R_{\theta JA}$ values for a particular device. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 18.

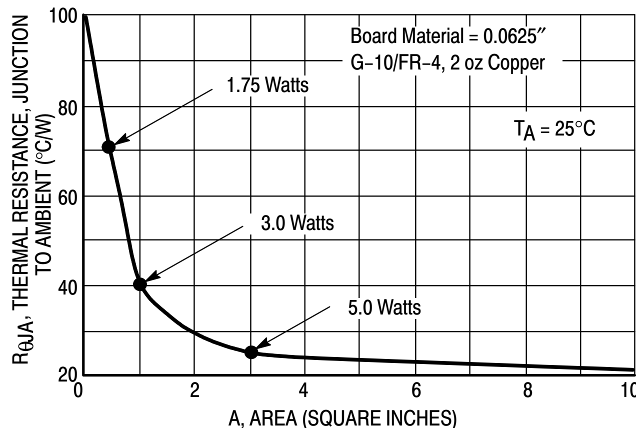



**Figure 18. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and D$^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and D$^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

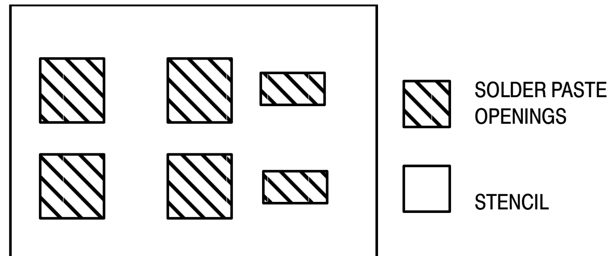



**Figure 19. Typical Stencil for DPAK and D$^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the D$^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 20 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

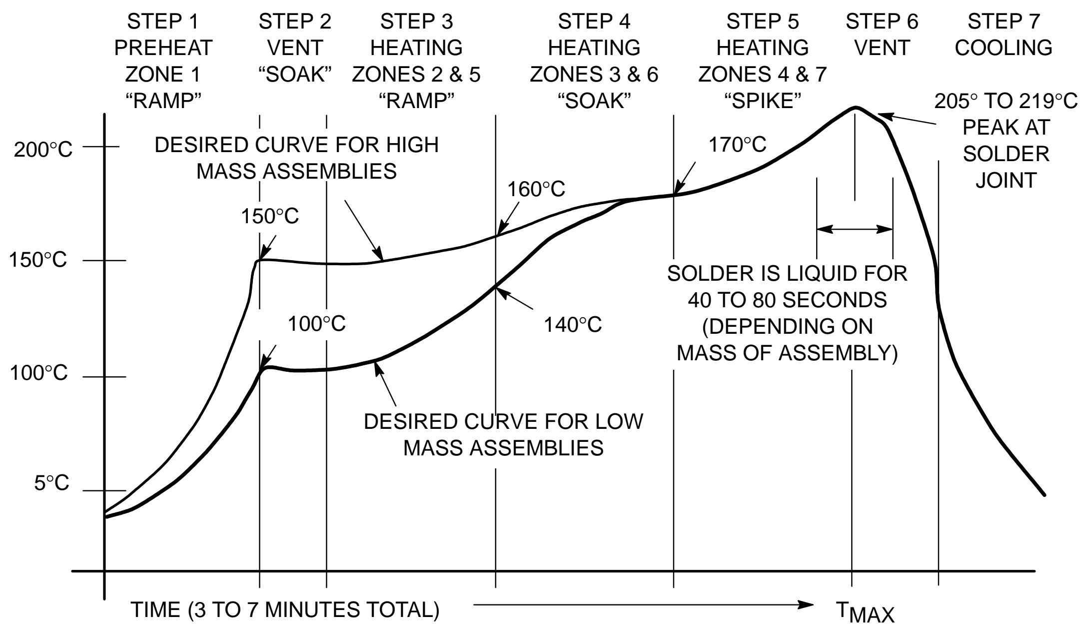



**Figure 20. Typical Solder Heating Profile**

# MTD4N20E

**Preferred Device**

# Power MOSFET 4 Amps, 200 Volts

## N–Channel DPAK

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition this advanced high voltage MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

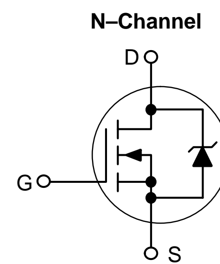
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 4.0<br>2.6<br>12 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 40<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 80 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 4.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 80 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

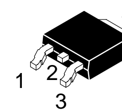
**http://onsemi.com**

**4 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 1.2 Ω**

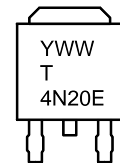
**N–Channel**




**MARKING DIAGRAM**

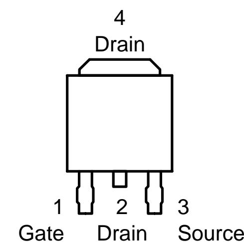



**CASE 369A**
**DPAK**
**STYLE 2**




4N20E = Device Code
Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD4N20E | DPAK | 75 Units/Rail |
| MTD4N20E1 | DPAK | 75 Units/Rail |
| MTD4N20ET4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 2
Publication Order Number:
MTD4N20E/D

## ELECTRICAL CHARACTERISTICS ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 200<br>– | –<br>263 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 3.0<br>7.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.0 Adc) | | $R_{DS(on)}$ | – | 0.98 | 1.2 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 4.0 Adc)<br>($I_D$ = 2.0 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 3.5<br>– | 5.8<br>5.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 2.0 Adc) | | $g_{FS}$ | 1.5 | 2.1 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 311 | 430 | pF |
| Output Capacitance | | $C_{oss}$ | – | 66 | 80 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 11 | 20 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 10 | 17 | ns |
| Rise Time | | $t_r$ | – | 4.0 | 26 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 15 | 29 | |
| Fall Time | | $t_f$ | – | 6.0 | 18 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 4.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 9.2 | 14 | nC |
| | | $Q_1$ | – | 2.4 | – | |
| | | $Q_2$ | – | 4.1 | – | |
| | | $Q_3$ | – | 5.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.92<br>0.82 | <br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 4.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 123 | – | ns |
| | | $t_a$ | – | 82 | – | |
| | | $t_b$ | – | 41 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.58 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

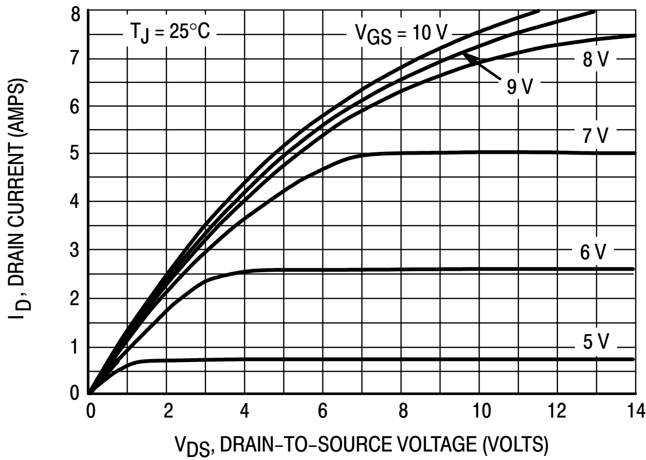



**Figure 1. On–Region Characteristics**

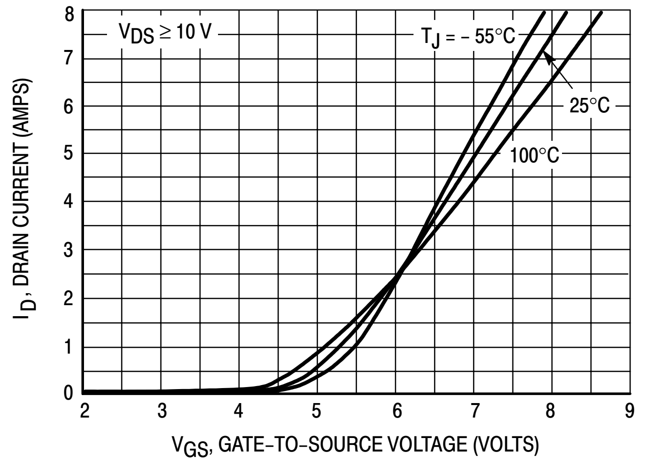



**Figure 2. Transfer Characteristics**

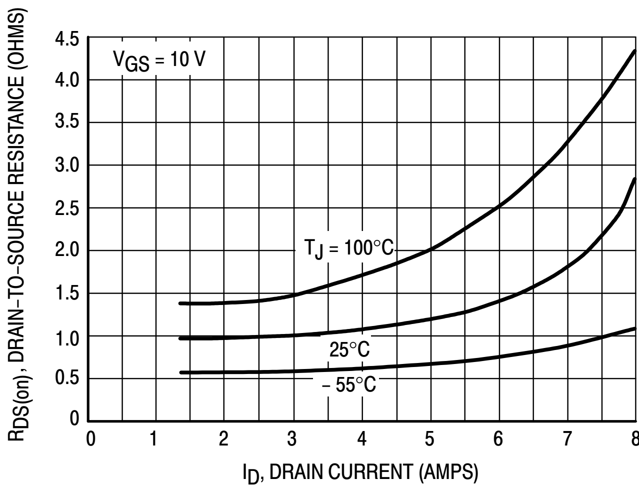



**Figure 3. On–Resistance versus Drain Current and Temperature**

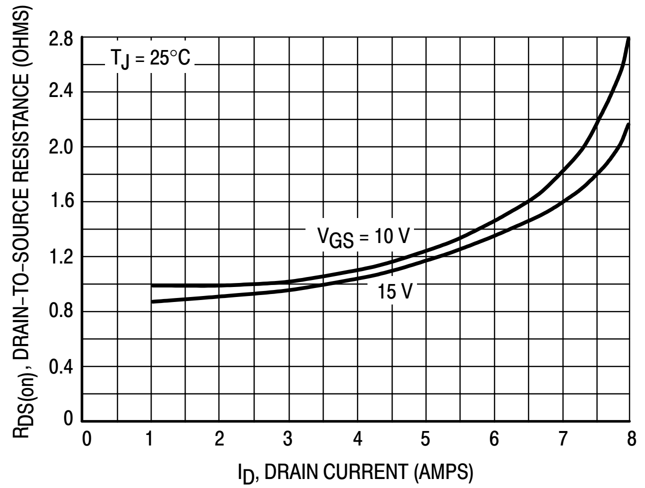



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

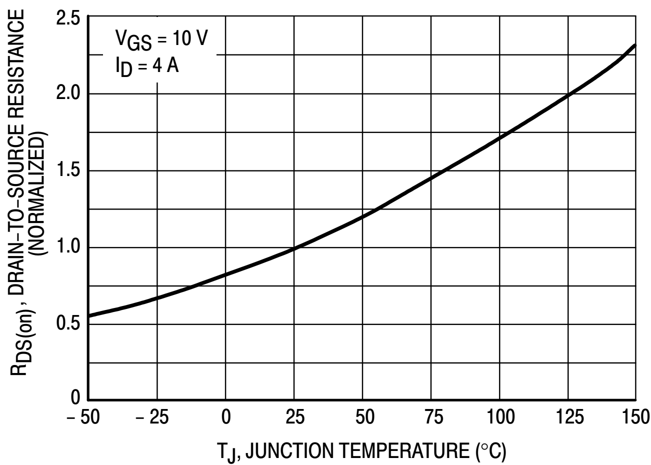



**Figure 5. On–Resistance Variation with Temperature**

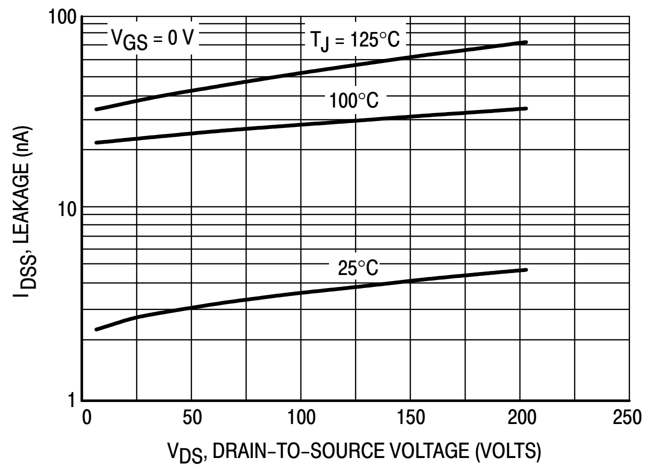



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

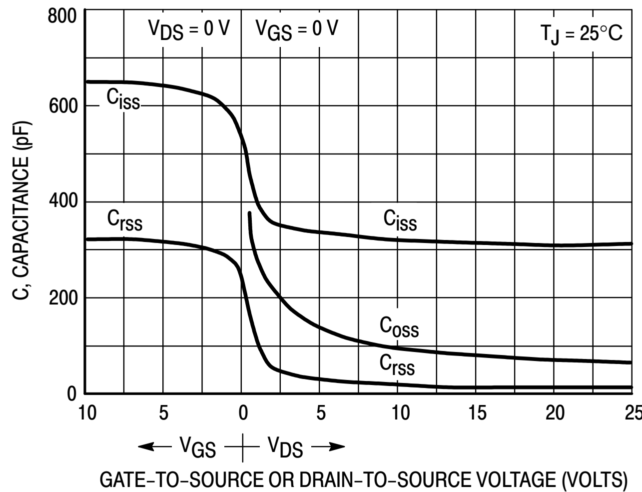



**Figure 7. Capacitance Variation**

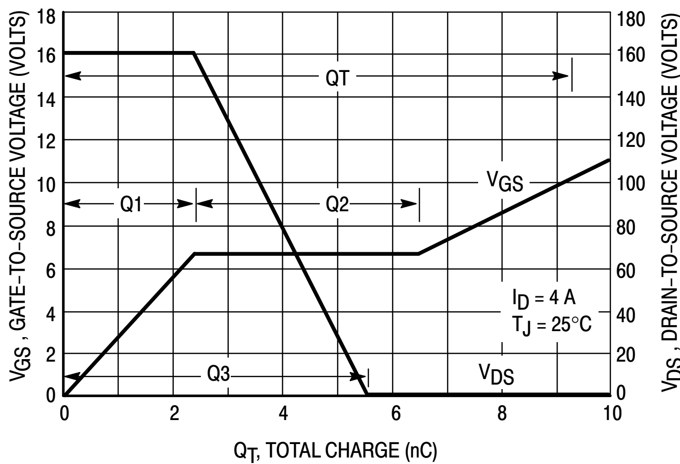



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

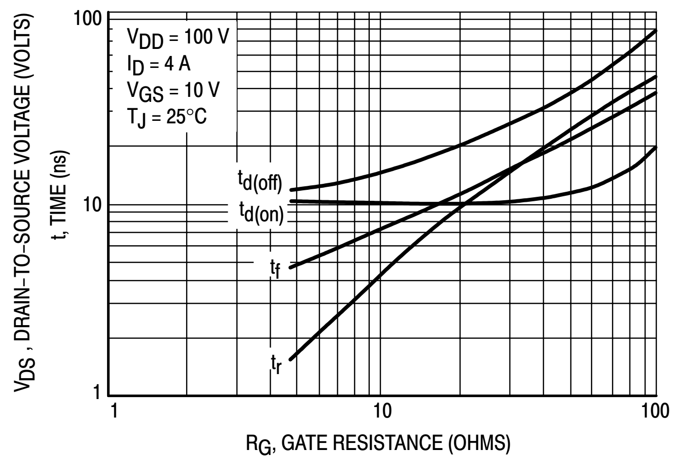



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

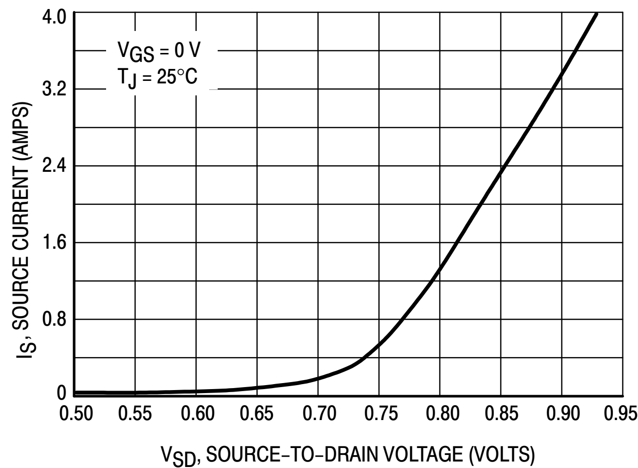



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

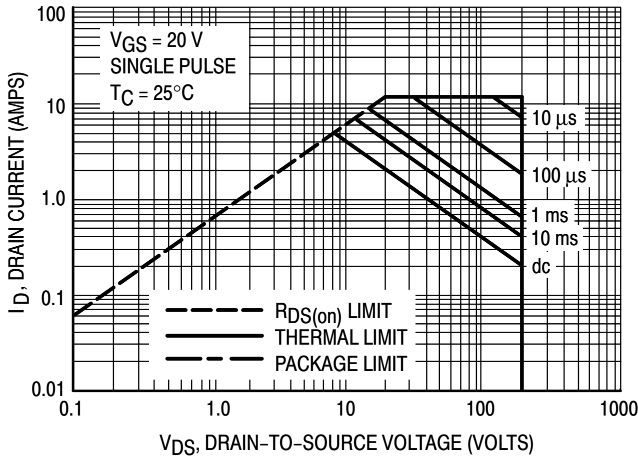



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

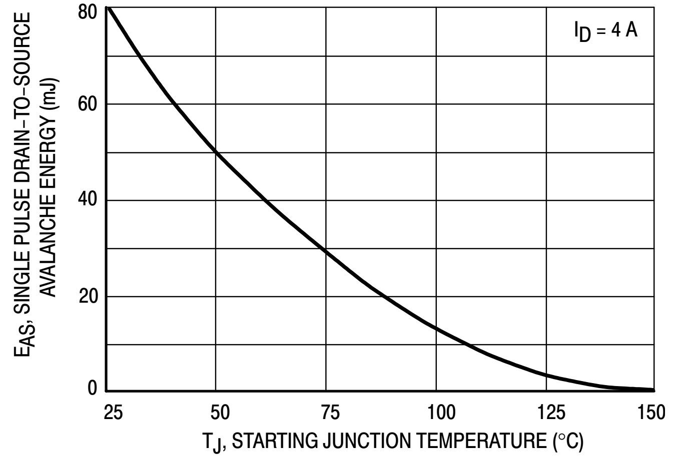



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

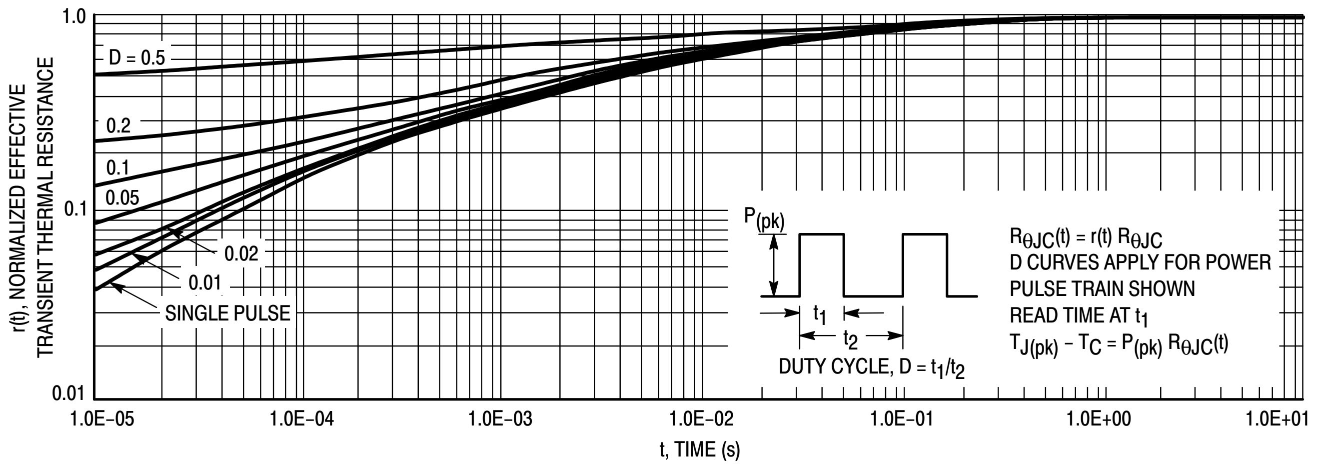



**Figure 13. Thermal Response**

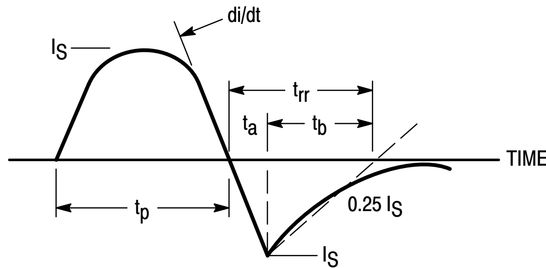
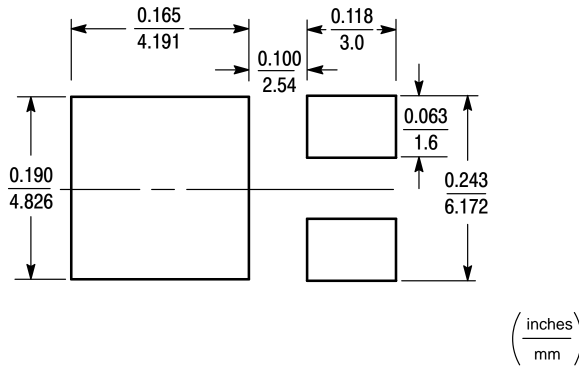



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

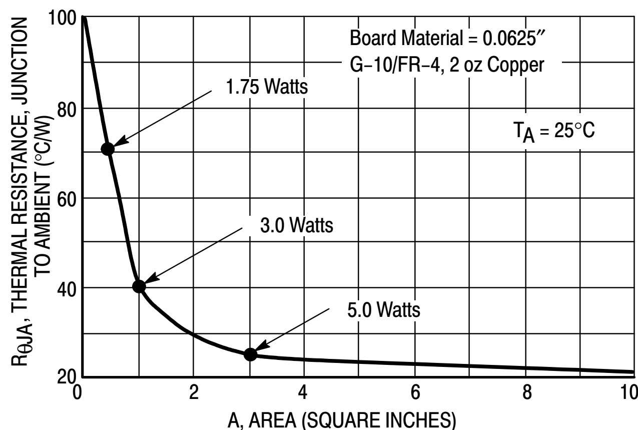



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

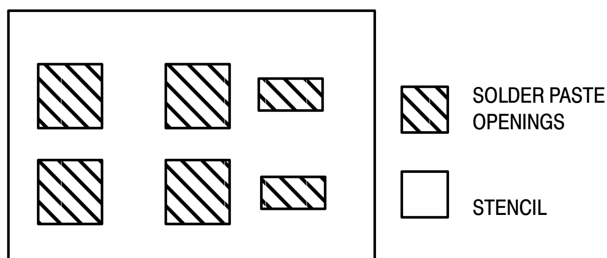



**Figure 16. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

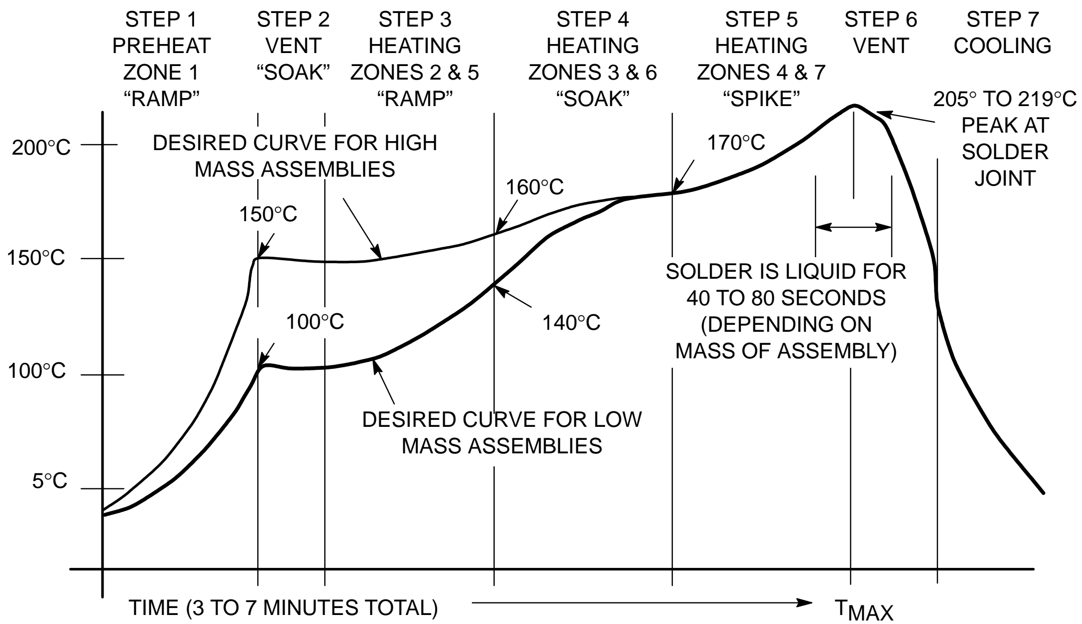



**Figure 17. Typical Solder Heating Profile**

# MTD5P06V

**Preferred Device**

# Power MOSFET 5 Amps, 60 Volts

## P–Channel DPAK

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

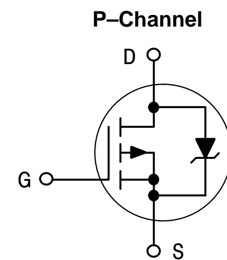
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5<br>4<br>18 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 40<br>0.27<br>2.1 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 5 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 125 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.75<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

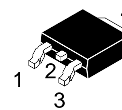
1. When surface mounted to an FR4 board using the minimum recommended pad size.

**5 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 450 mΩ**

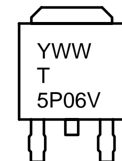
**P–Channel**




**MARKING DIAGRAM**

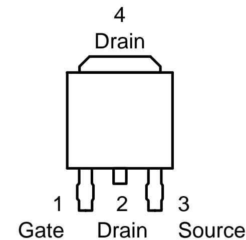



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD5P06V | DPAK | 75 Units/Rail |
| MTD5P06V1 | DPAK | 75 Units/Rail |
| MTD5P06VT4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 61.2 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 2.8 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.7 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | – | 0.34 | 0.45 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 5 Adc) | | $V_{DS(on)}$ | – | – | 2.7 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 2.5 Adc, $T_J$ = 150°C) | | | – | – | 2.6 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 1.5 | 3.6 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 367 | 510 | pF |
| Output Capacitance | | $C_{oss}$ | – | 140 | 200 | |
| Transfer Capacitance | | $C_{rss}$ | – | 29 | 60 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 5 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 26 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 30 | |
| Fall Time | | $t_f$ | – | 19 | 40 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 5 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 12 | 20 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 5.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.72 | 3.5 | Vdc |
| | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 1.34 | – | |
| Reverse Recovery Time | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 97 | – | ns |
| | | $t_a$ | – | 73 | – | |
| | | $t_b$ | – | 24 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.42 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

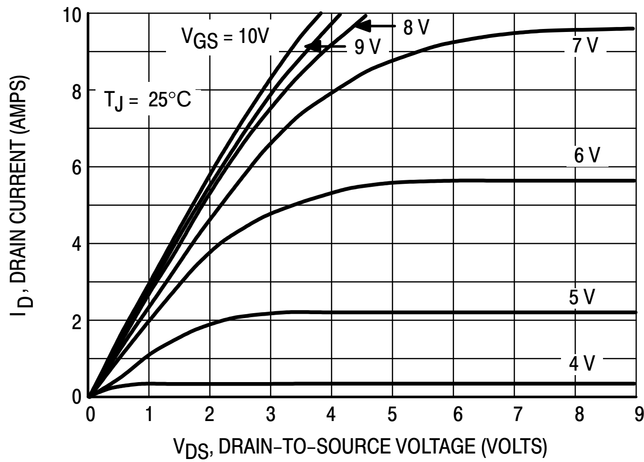



**Figure 1. On–Region Characteristics**

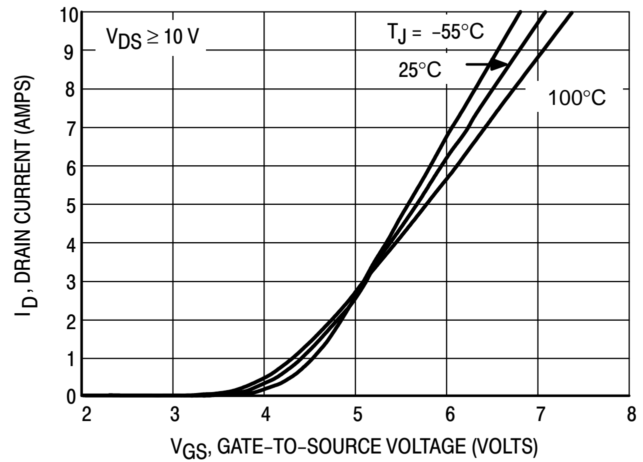



**Figure 2. Transfer Characteristics**

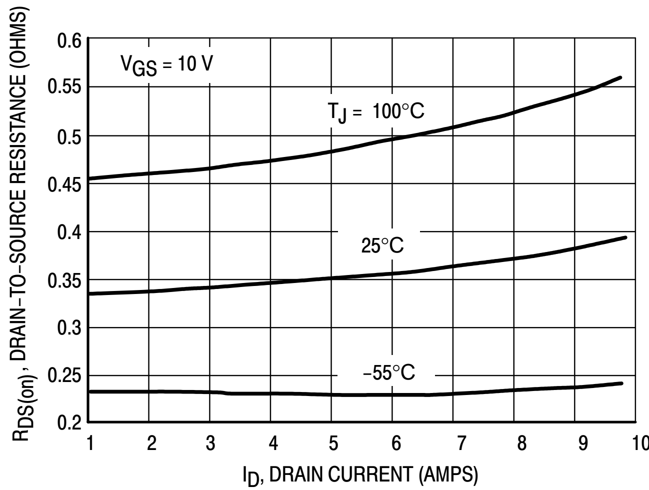



**Figure 3. On–Resistance versus Drain Current and Temperature**

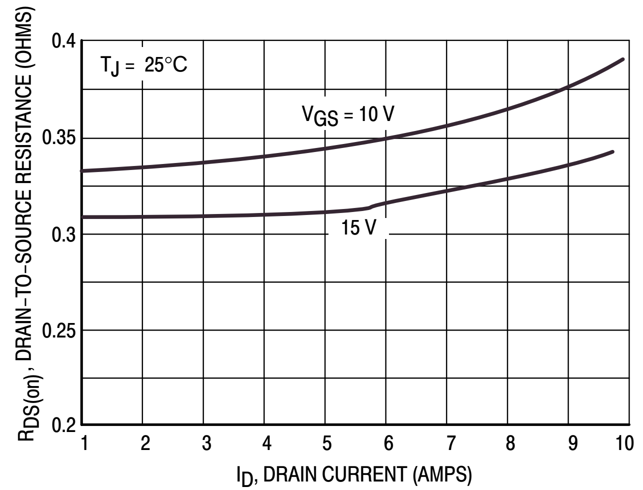



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

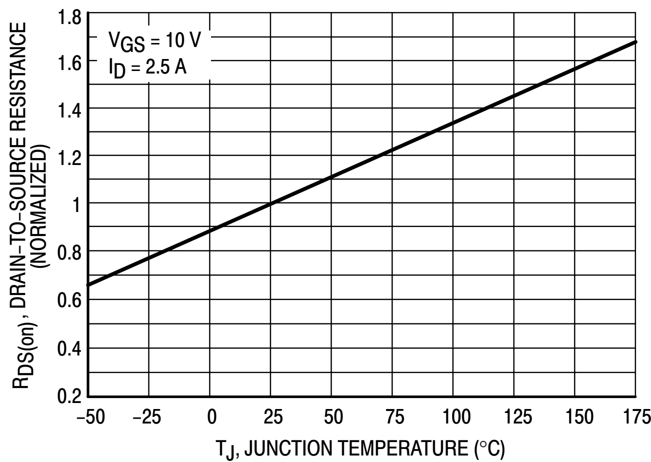



**Figure 5. On–Resistance Variation with Temperature**

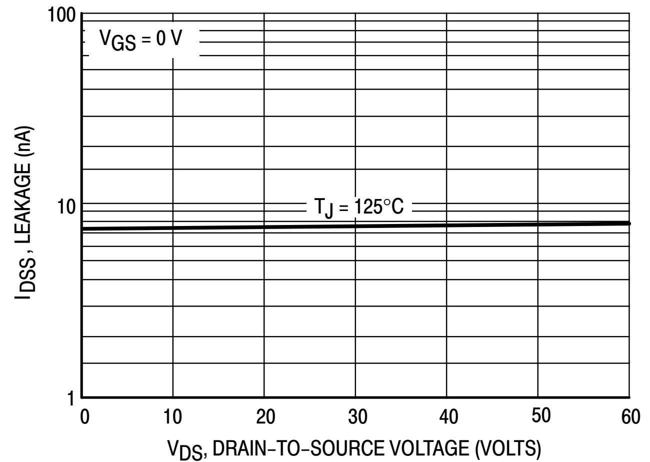



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

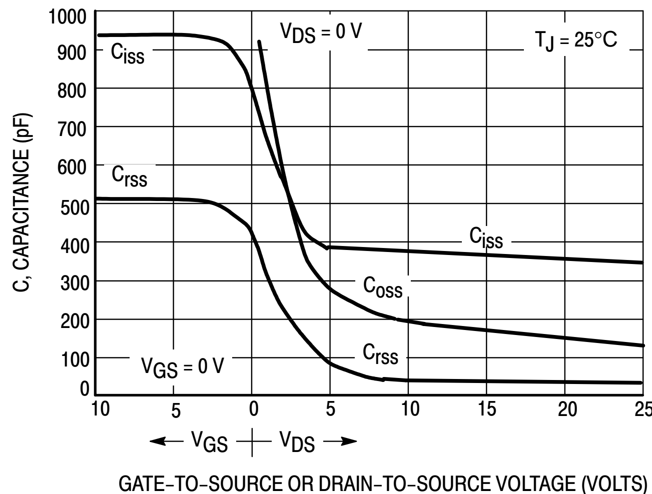



**Figure 7. Capacitance Variation**

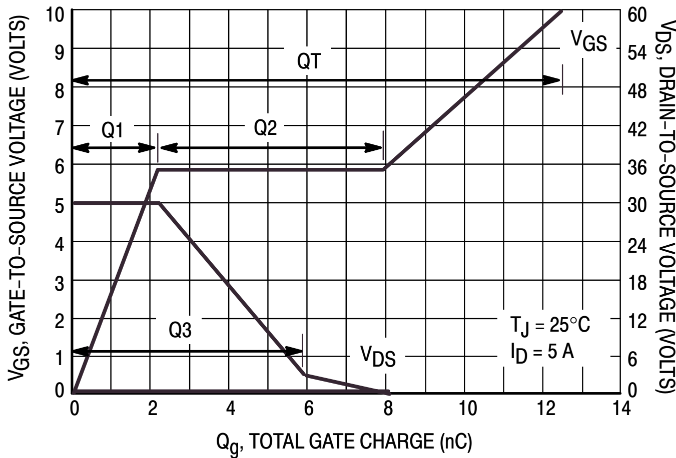



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

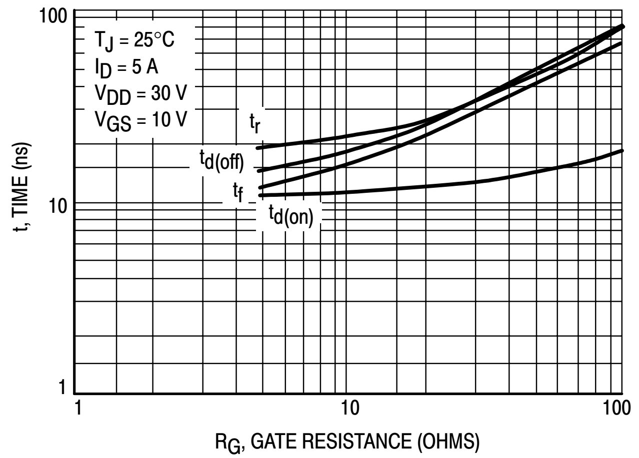



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

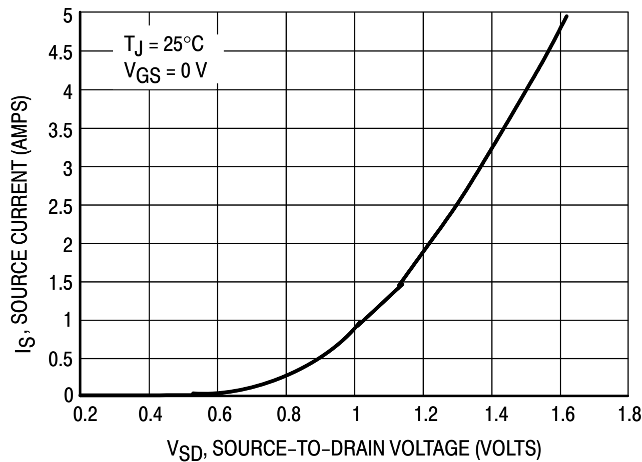



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

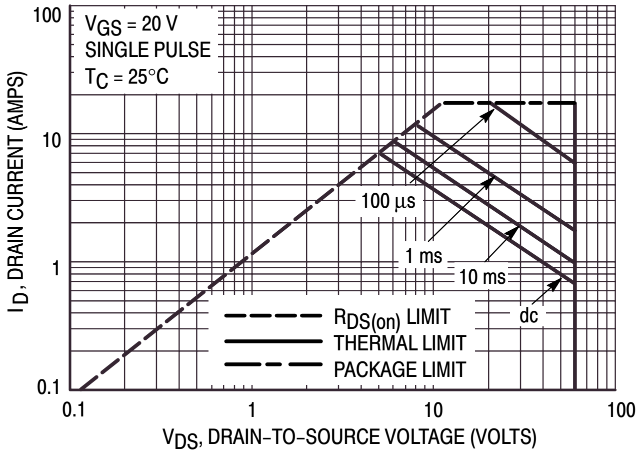



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

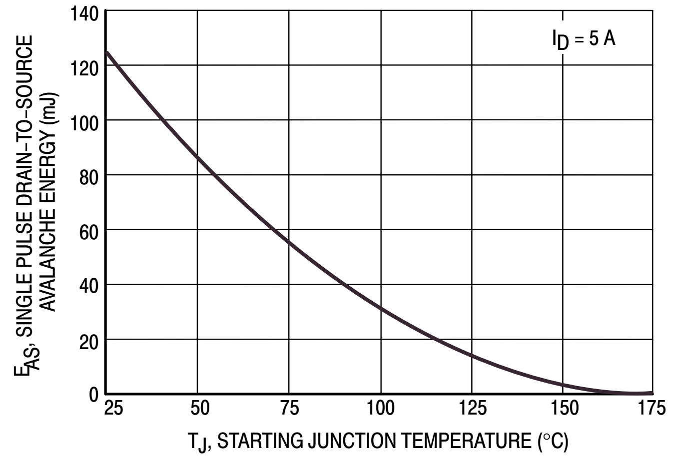



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

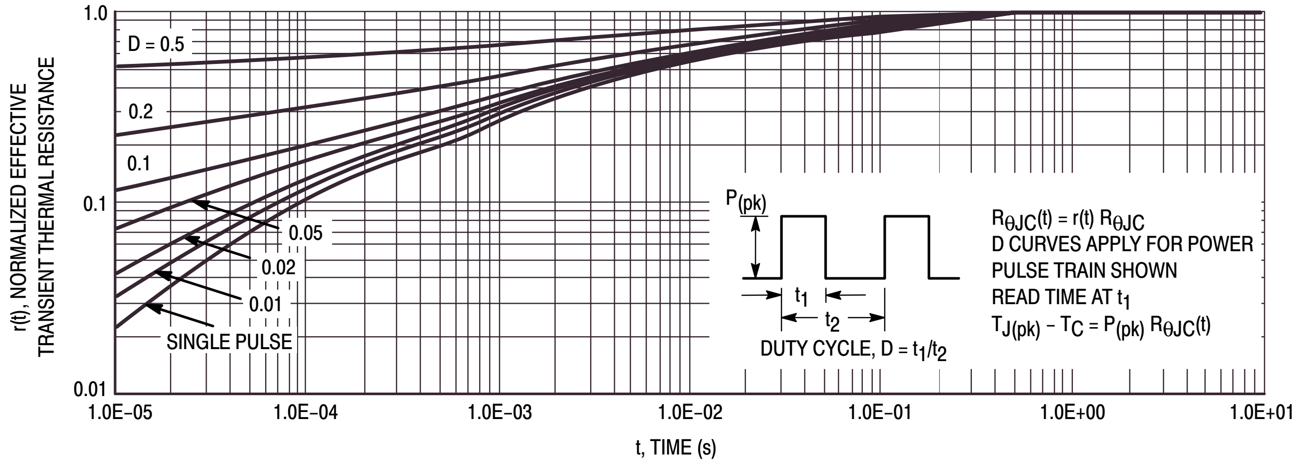



**Figure 13. Thermal Response**

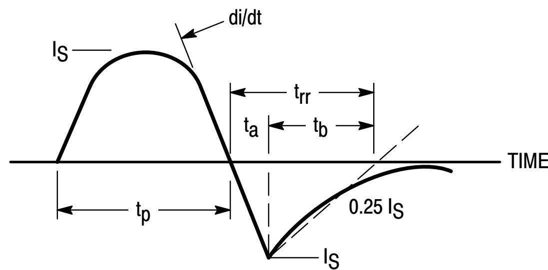
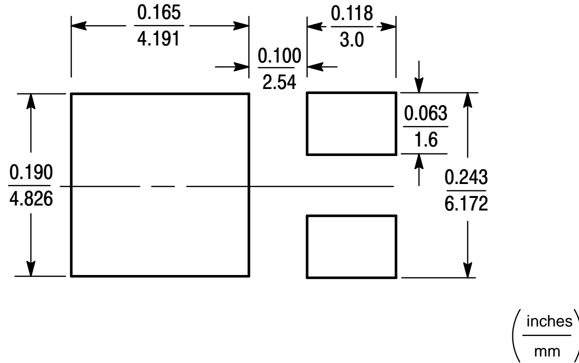



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{175°C - 25°C}{71.4°C/W} = 2.1 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 2.1 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

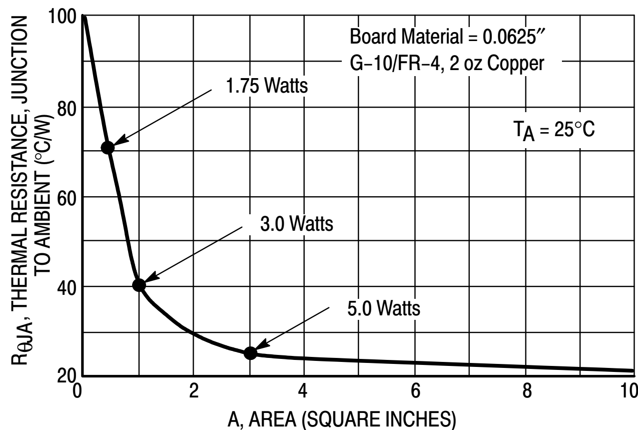



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or “tombstoning” may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

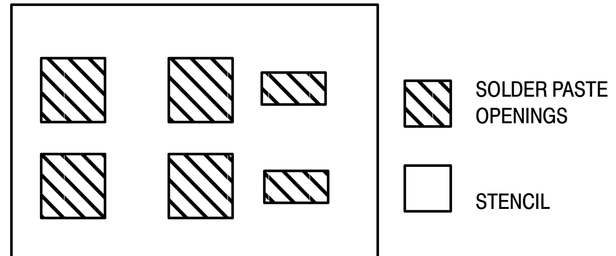



**Figure 16. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

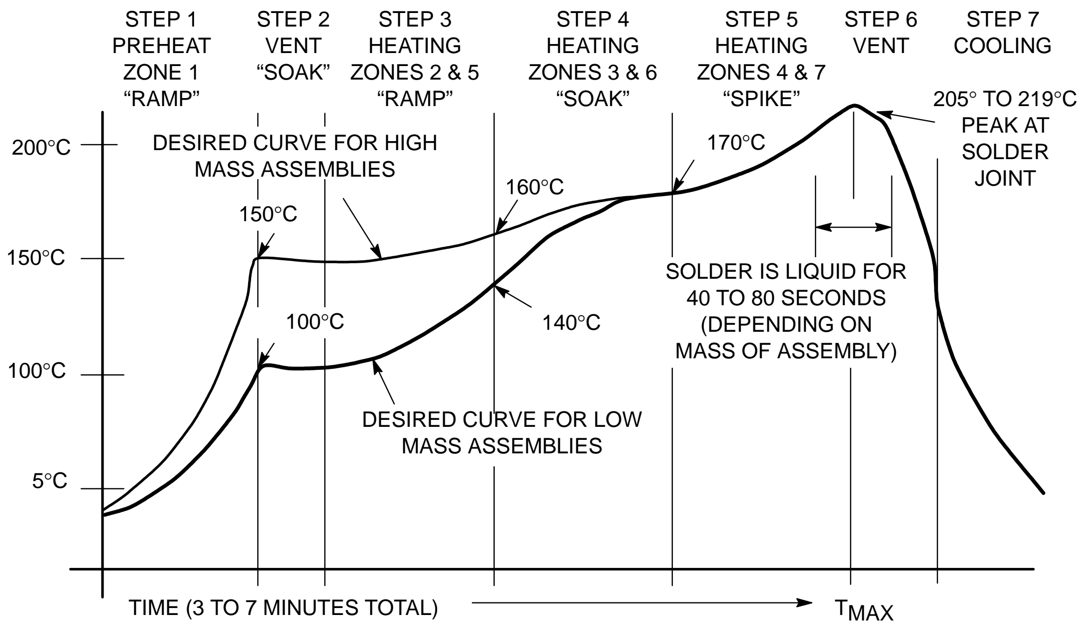



**Figure 17. Typical Solder Heating Profile**

# MTD6N20E

**Preferred Device**

# Power MOSFET 6 Amps, 200 Volts
## N–Channel DPAK

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

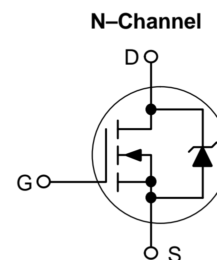
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>6.0<br>3.8<br>18 | <br>Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 50<br>0.4<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 80 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 6.0 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 54 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.50<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

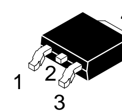
http://onsemi.com

**6 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 700 mΩ**

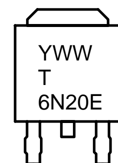
**N–Channel**




**MARKING DIAGRAM**

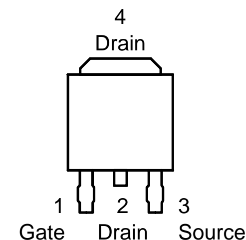



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD6N20E | DPAK | 75 Units/Rail |
| MTD6N20E1 | DPAK | 75 Units/Rail |
| MTD6N20ET4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 200<br>– | –<br>689 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 3.0<br>7.1 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc) | | $R_{DS(on)}$ | – | 0.46 | 0.700 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 6.0 Adc)<br>($I_D$ = 3.0 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 2.9<br>– | 5.0<br>4.4 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 3.0 Adc) | | $g_{FS}$ | 1.5 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 342 | 480 | pF |
| Output Capacitance | | $C_{oss}$ | – | 92 | 130 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 27 | 55 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 8.8 | 17.6 | ns |
| Rise Time | | $t_r$ | – | 29 | 58 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 22 | 44 | |
| Fall Time | | $t_f$ | – | 20 | 40.8 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 13.7 | 21 | nC |
| | | $Q_1$ | – | 2.7 | – | |
| | | $Q_2$ | – | 7.1 | – | |
| | | $Q_3$ | – | 5.9 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.99<br>0.9 | 1.2<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 14) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 138 | – | ns |
| | | $t_a$ | – | 93 | – | |
| | | $t_b$ | – | 45 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.74 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

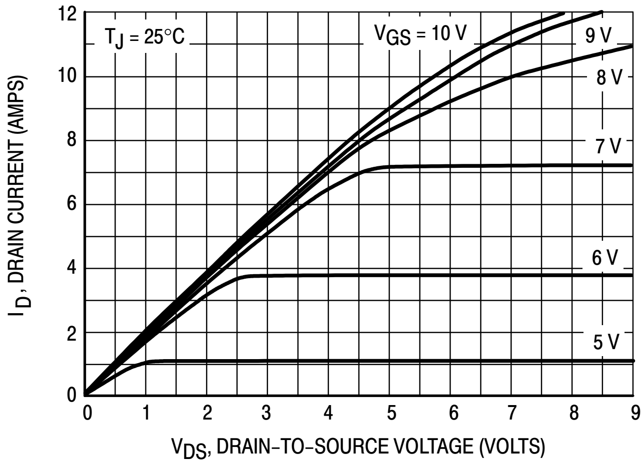



**Figure 1. On–Region Characteristics**

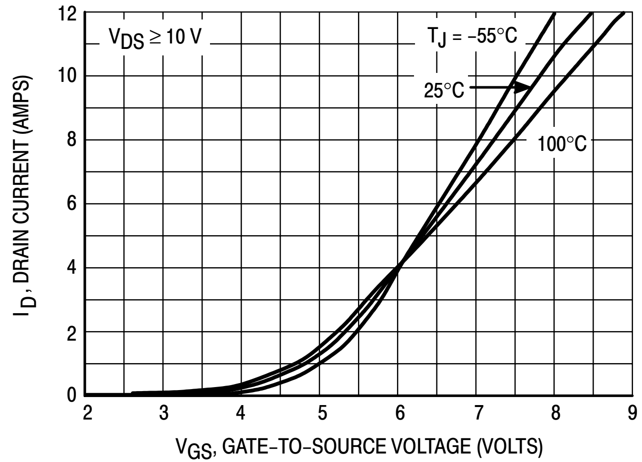



**Figure 2. Transfer Characteristics**

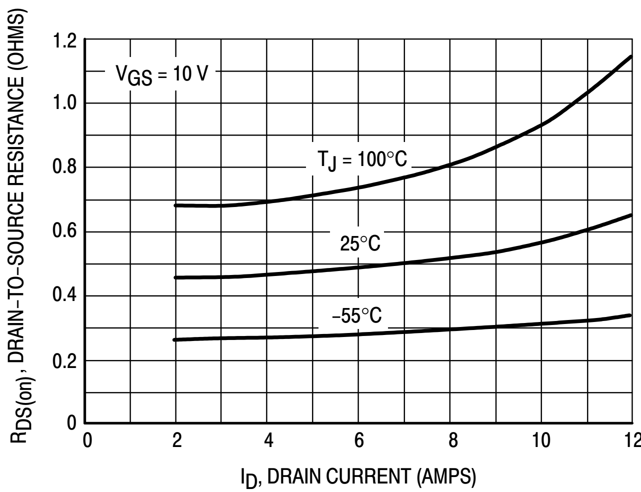



**Figure 3. On–Resistance versus Drain Current and Temperature**

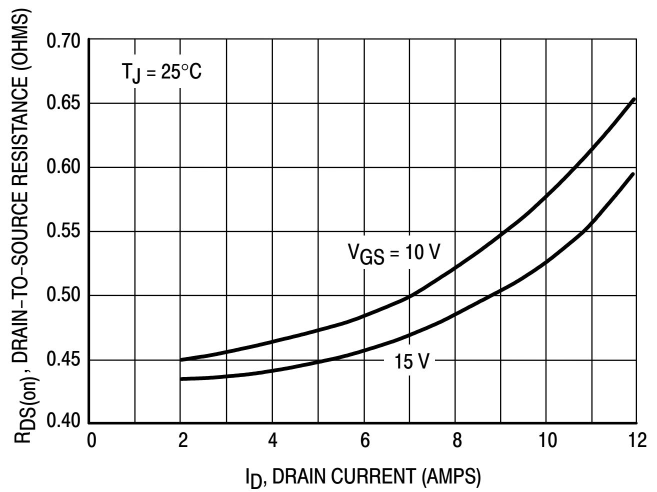



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

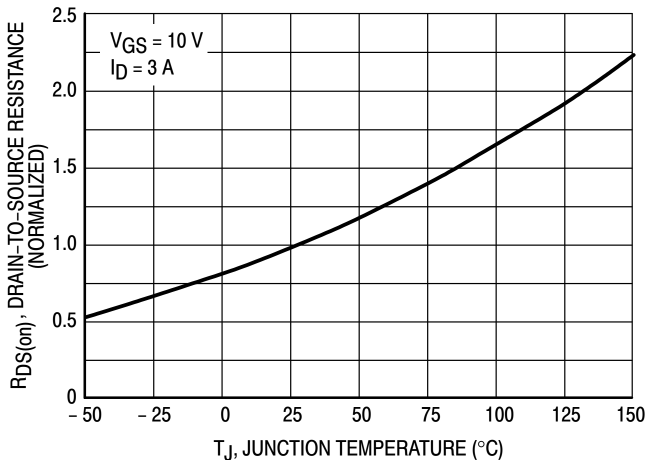



**Figure 5. On–Resistance Variation with Temperature**

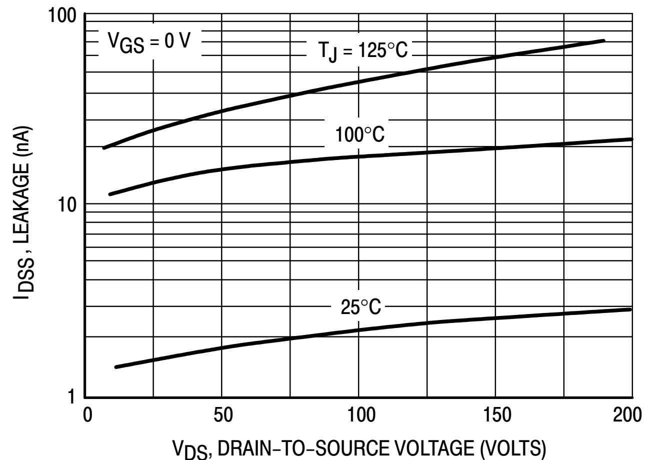



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \text{In} \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \text{In} \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

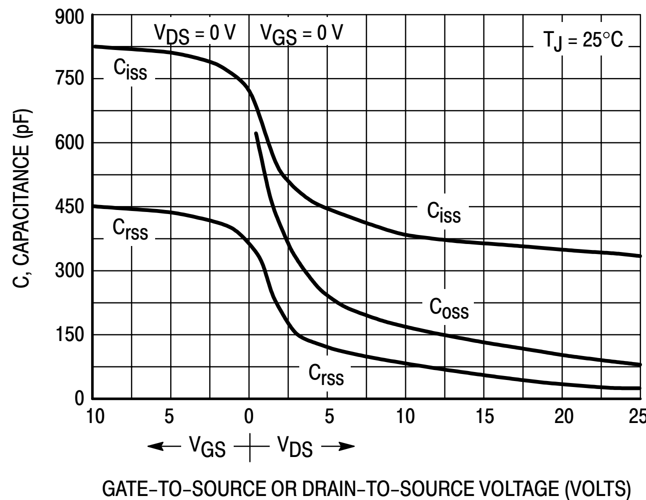



**Figure 7. Capacitance Variation**

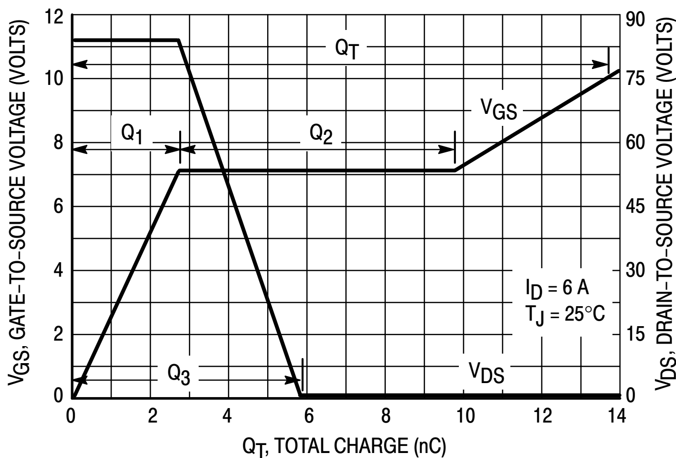



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

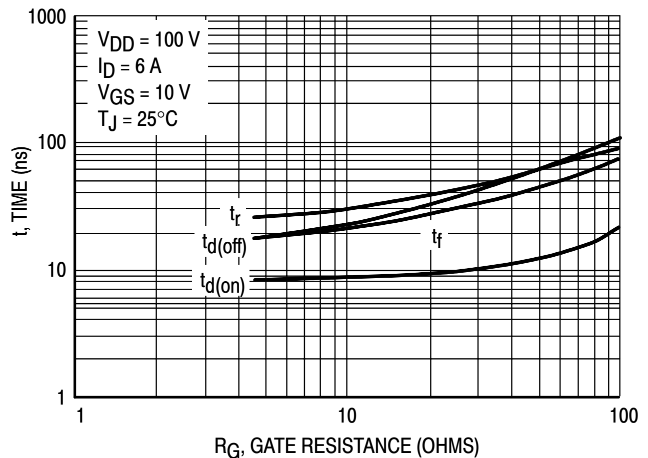



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

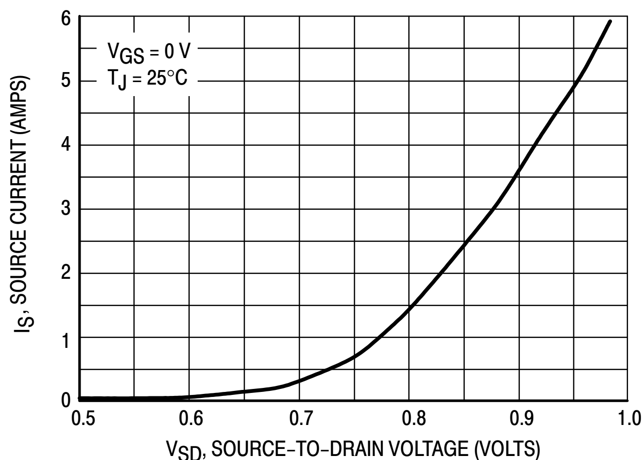



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

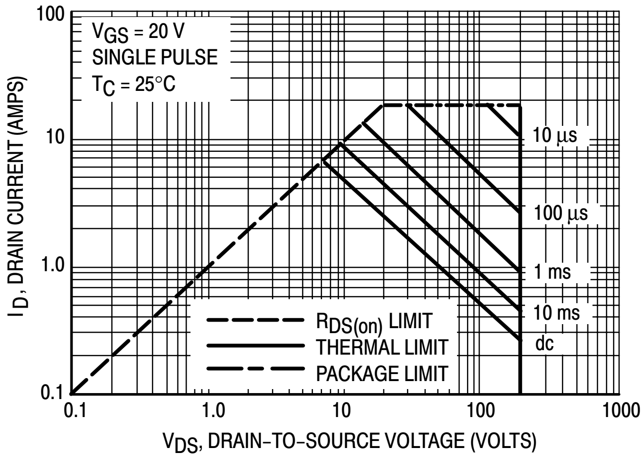



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

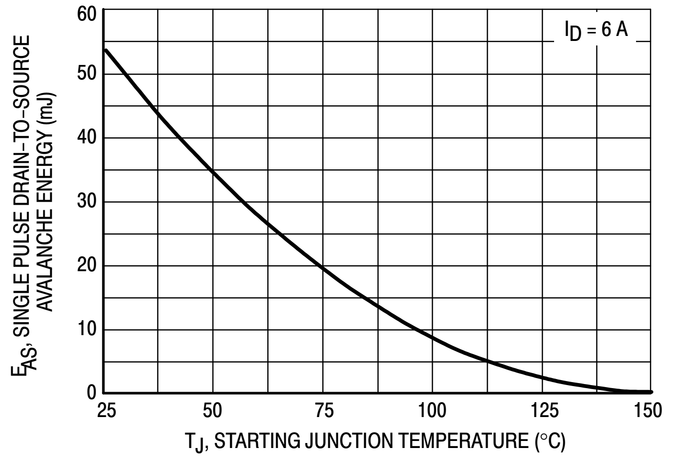



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

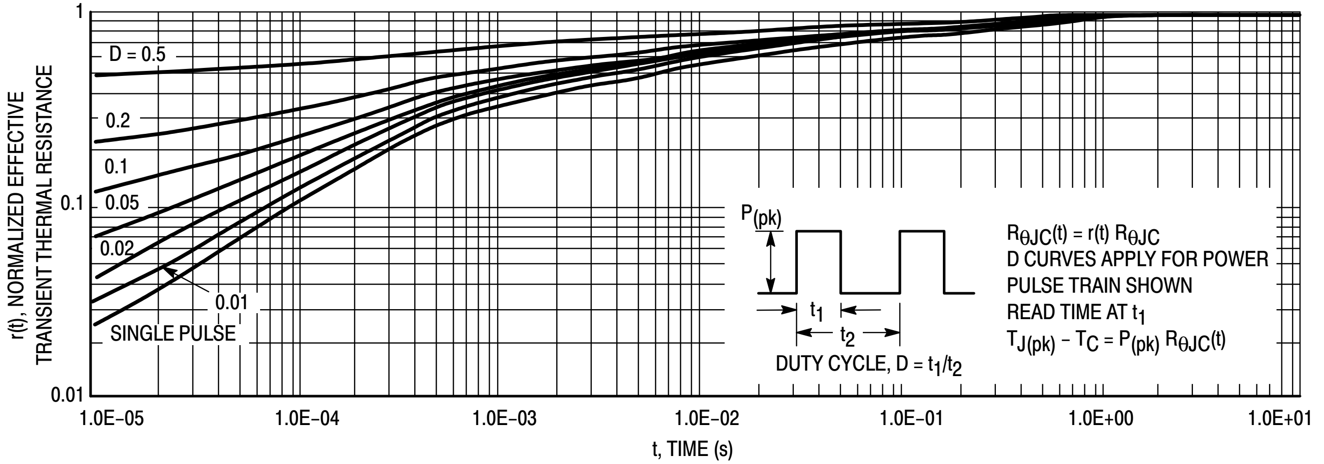



**Figure 13. Thermal Response**

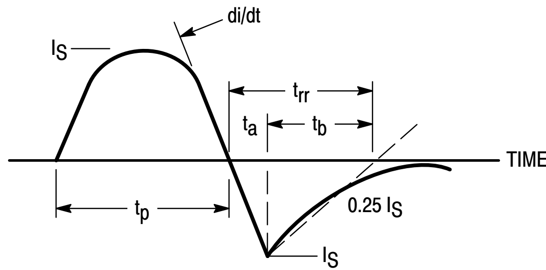
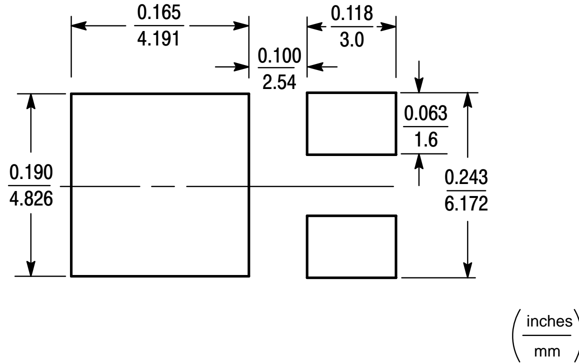



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

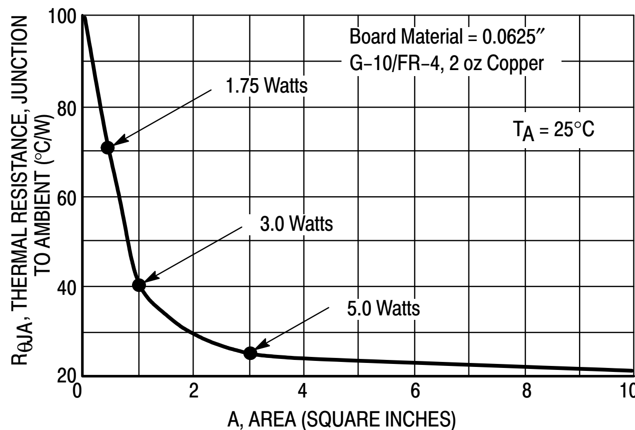



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2$PAK packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2$PAK packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

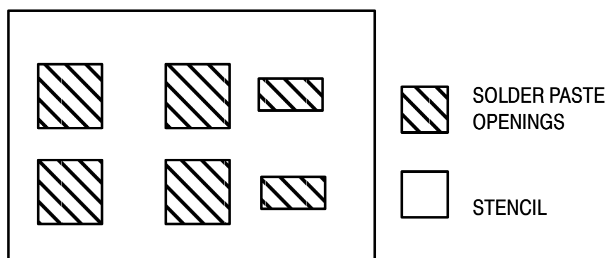



**Figure 16. Typical Stencil for DPAK and $D^2$PAK Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2$PAK is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

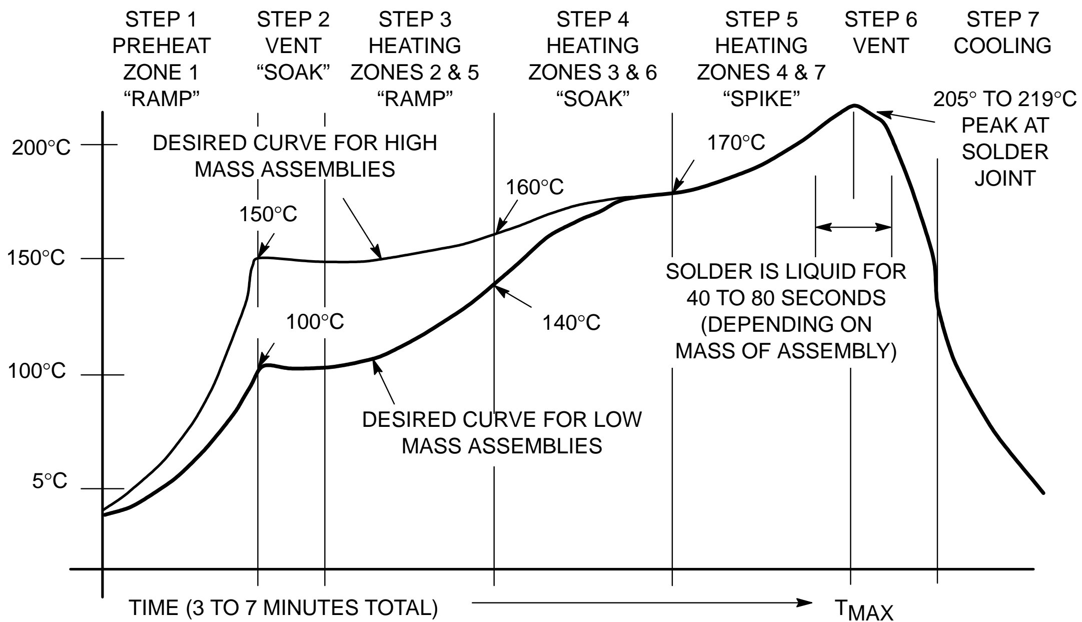



**Figure 17. Typical Solder Heating Profile**

# MTD6P10E

**Preferred Device**

# Power MOSFET 6 Amps, 100 Volts

## P–Channel DPAK

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

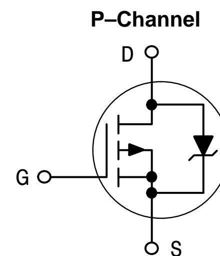
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le 10$ ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le 10$ µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>6.0<br>3.9<br>18 | <br>Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 50<br>0.4<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 6.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 180 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>2.50<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

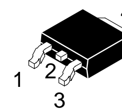
**http://onsemi.com**

**6 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 660 mΩ**

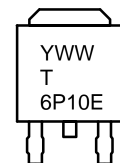
**P–Channel**




**MARKING DIAGRAM**

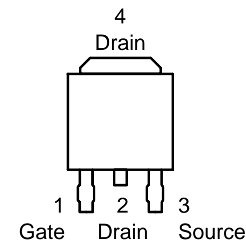



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD6P10E | DPAK | 75 Units/Rail |
| MTD6P10ET4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 100<br>– | –<br>124 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.9<br>4.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc) | | $R_{DS(on)}$ | – | 0.56 | 0.66 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 6.0 Adc)<br>($I_D$ = 3.0 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 3.6<br>– | 4.8<br>4.2 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 3.0 Adc) | | $g_{FS}$ | 1.5 | 3.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | 840 | pF |
| Output Capacitance | | $C_{oss}$ | – | 154 | 240 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 27 | 56 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 50 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 25 | ns |
| Rise Time | | $t_r$ | – | 29 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 18 | 40 | |
| Fall Time | | $t_f$ | – | 9 | 20 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 15.3 | 22 | nC |
| | | $Q_1$ | – | 4.1 | – | |
| | | $Q_2$ | – | 7.1 | – | |
| | | $Q_3$ | – | 6.8 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.8<br>1.5 | 5.0<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 112 | – | ns |
| | | $t_a$ | – | 92 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.603 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

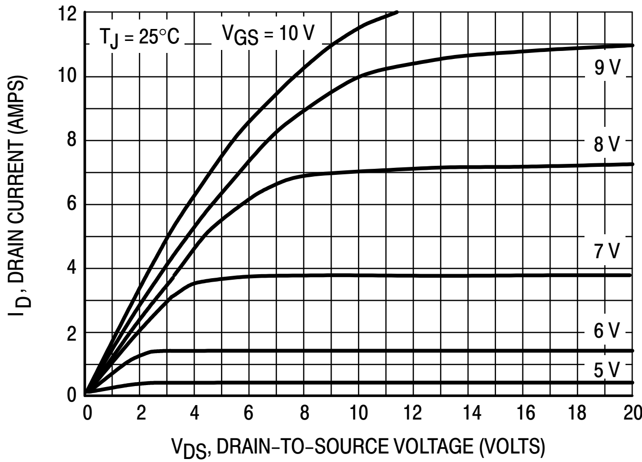



**Figure 1. On–Region Characteristics**

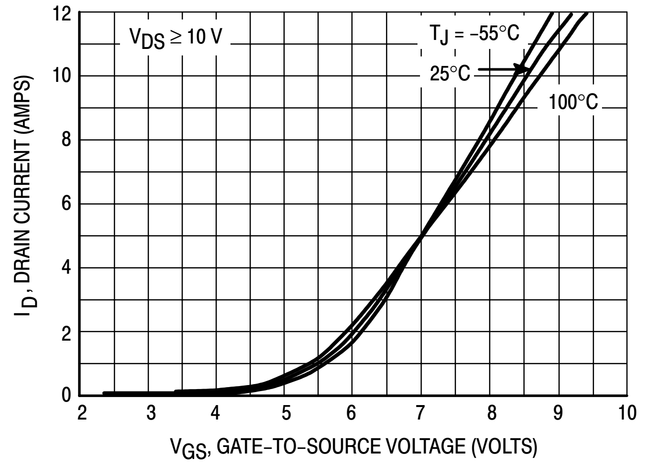



**Figure 2. Transfer Characteristics**

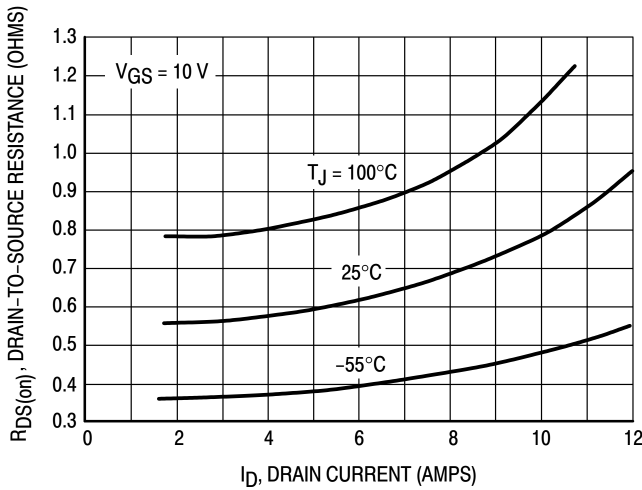



**Figure 3. On–Resistance versus Drain Current and Temperature**

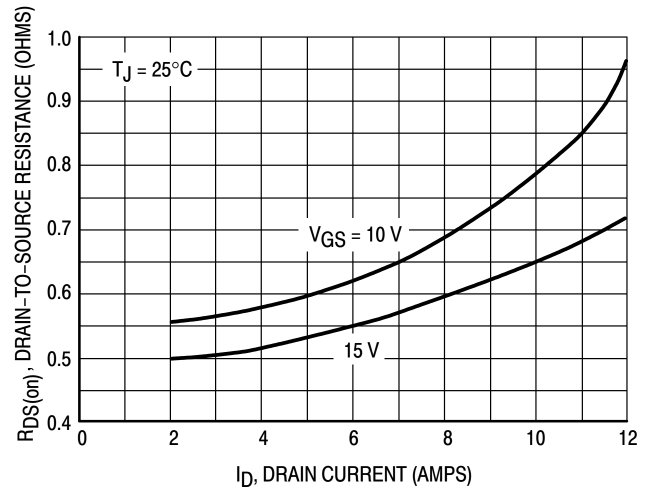



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

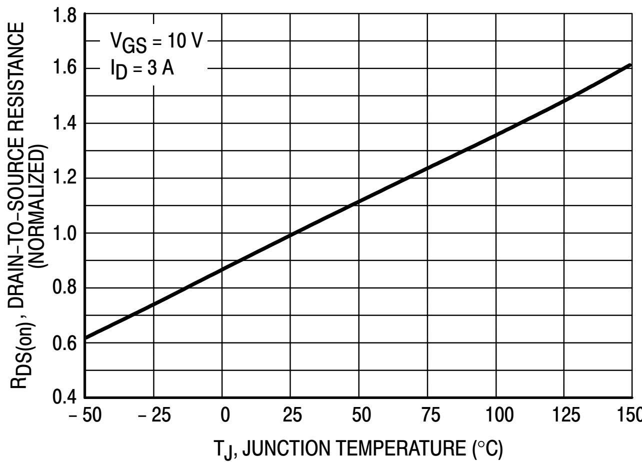



**Figure 5. On–Resistance Variation with Temperature**

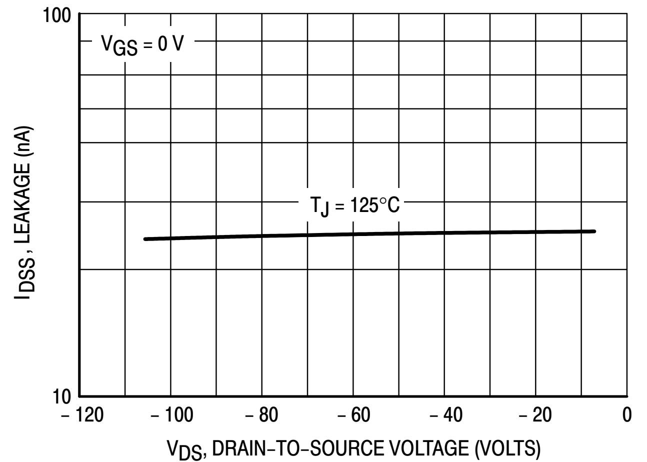



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \mathrm{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \mathrm{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

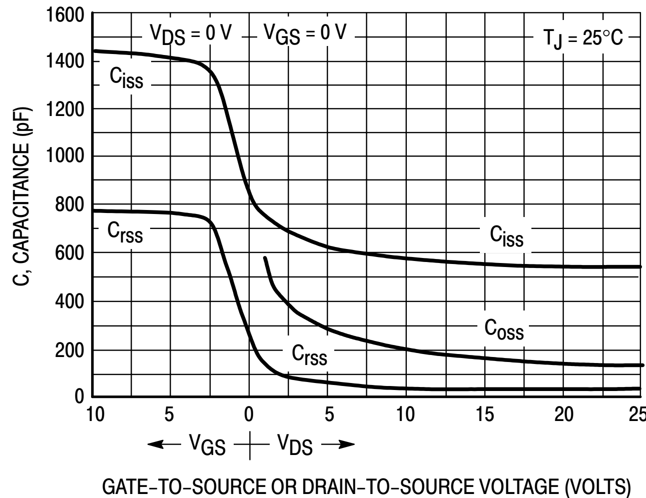



**Figure 7. Capacitance Variation**

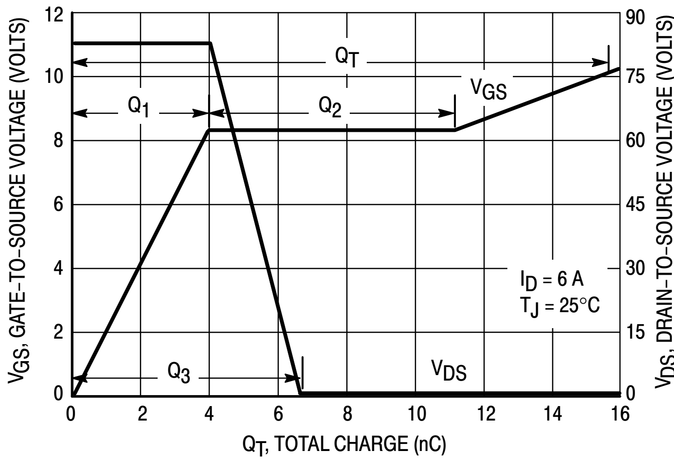



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

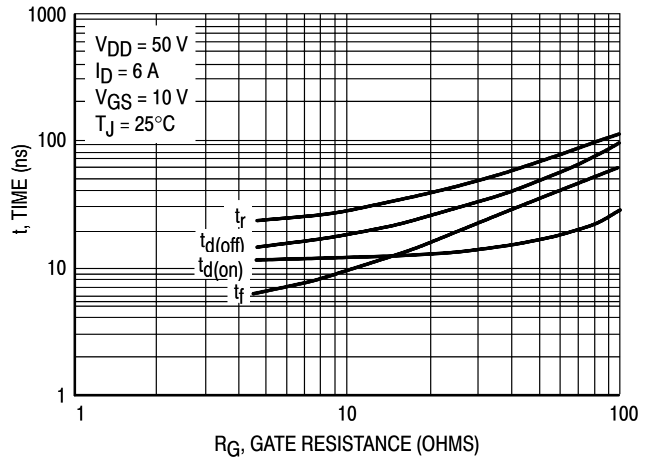



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

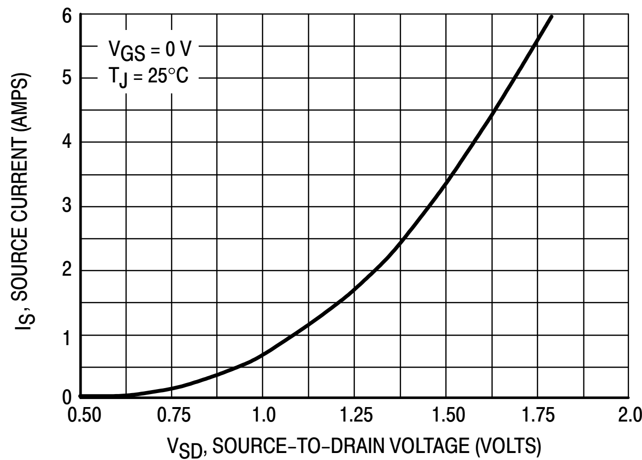



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

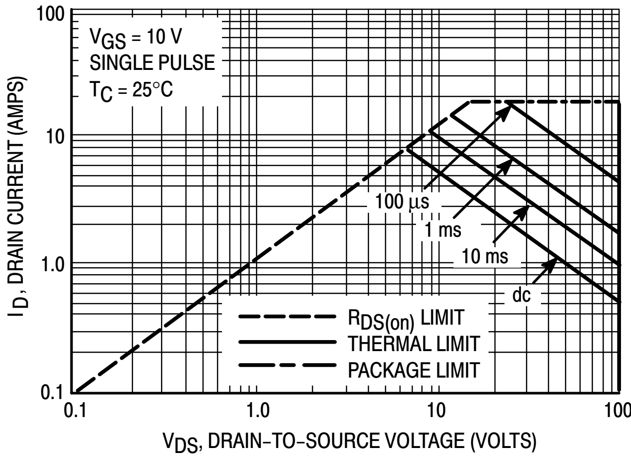



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

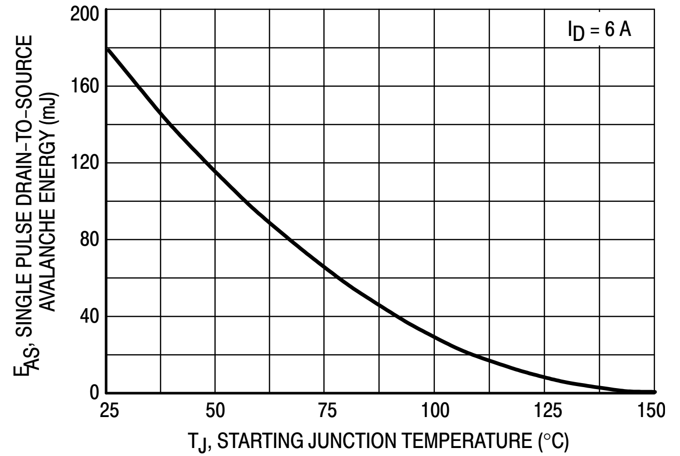



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

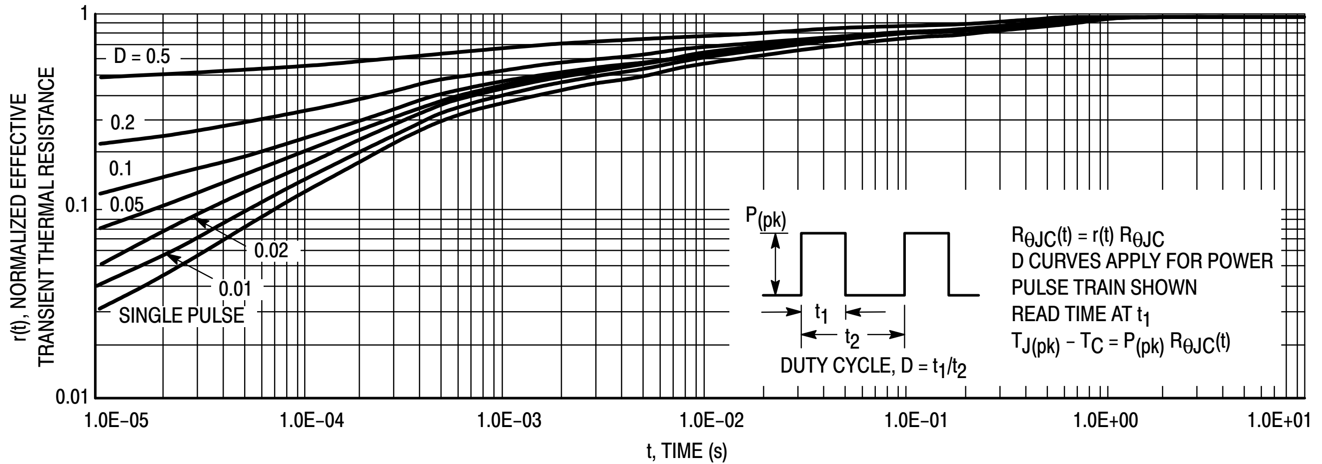



**Figure 13. Thermal Response**

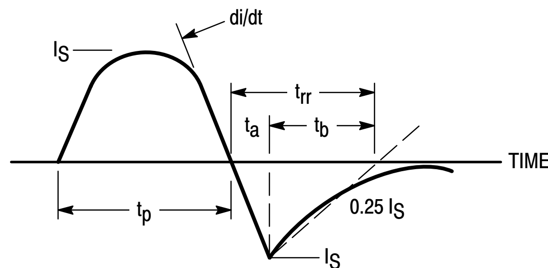
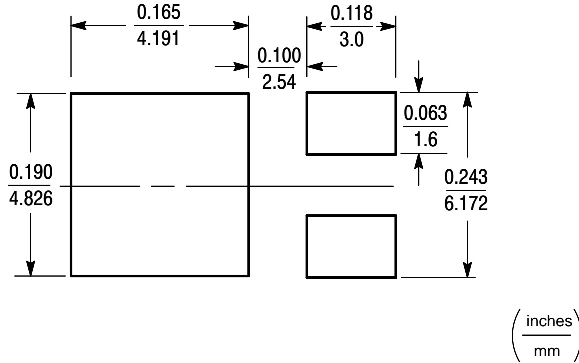



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

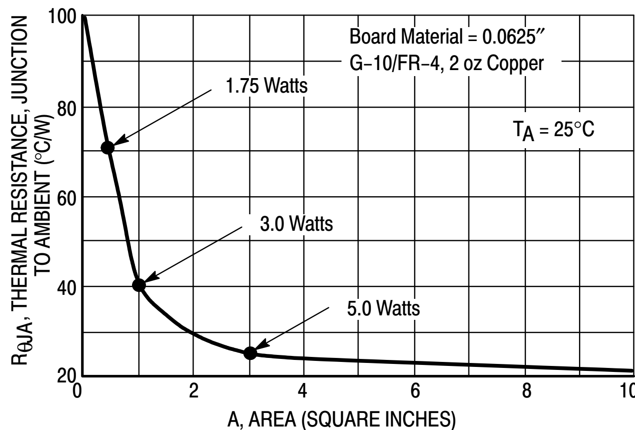



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

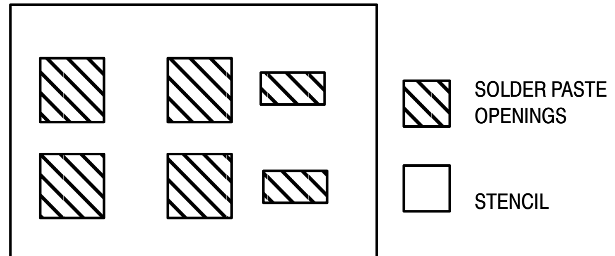



**Figure 16. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

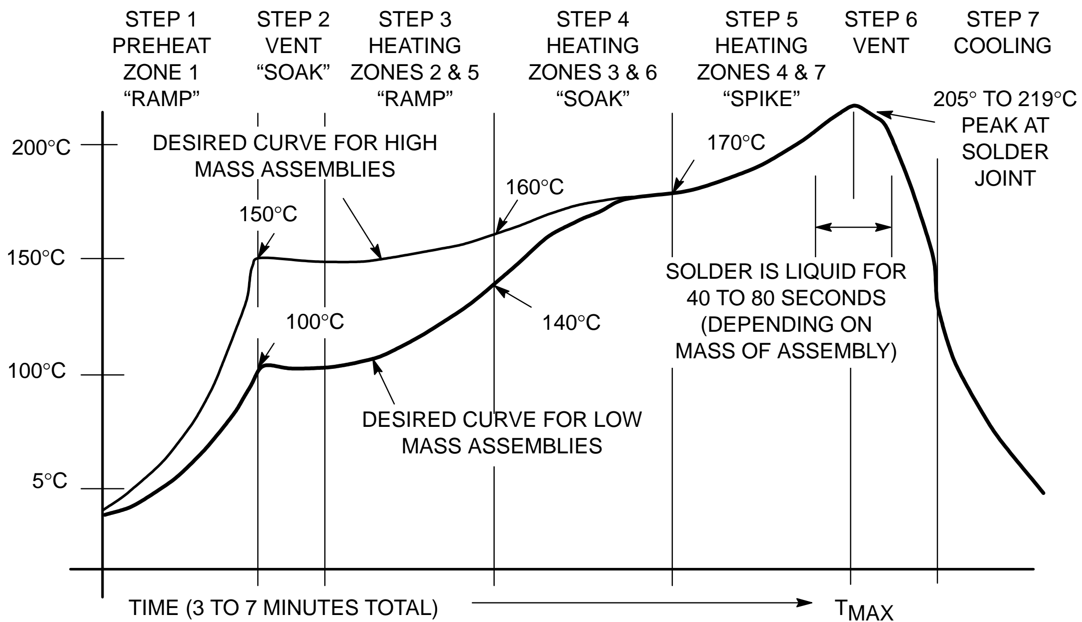



**Figure 17. Typical Solder Heating Profile**

# MTD9N10E

**Preferred Device**

# Power MOSFET 9 Amps, 100 Volts

## N–Channel DPAK

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Replaces MTD6N10

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

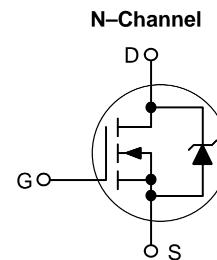
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 9.0<br>5.0<br>27 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C<br>Total Power Dissipation @ $T_A$ = 25°C, when mounted to minimum recommended pad size | $P_D$ | 40<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 9.0 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 40 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient, when mounted to minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor**™

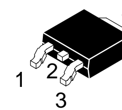
**http://onsemi.com**

**9 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 250 mΩ**

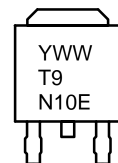
**N–Channel**




**MARKING DIAGRAM**

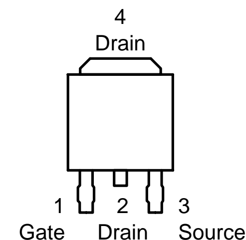



**CASE 369A**
**DPAK**
**STYLE 2**




Y = Year
WW = Work Week
T9 = MOSFET

**PIN ASSIGNMENT**




**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTD9N10E | DPAK | 75 Units/Rail |
| MTD9N10E1 | DPAK | 75 Units/Rail |
| MTD9N10ET4 | DPAK | 2500 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 100 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 103 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 6.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 4.5 Adc) | | $R_{DS(on)}$ | – | 0.17 | 0.25 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 9.0 Adc) | | $V_{DS(on)}$ | – | – | 2.43 | Vdc |
| ($I_D$ = 4.5 Adc, $T_J$ = 125°C) | | | – | – | 2.40 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 4.5 Adc) | | $g_{FS}$ | 4.0 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 610 | 1200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 176 | 400 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 14 | 30 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 50 Vdc, $I_D$ = 9.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 8.8 | 20 | ns |
| Rise Time | | $t_r$ | – | 28 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 16 | 30 | |
| Fall Time | | $t_f$ | – | 4.8 | 10 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 9.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 14 | 21 | nC |
| | | $Q_1$ | – | 5.2 | – | |
| | | $Q_2$ | – | 3.2 | – | |
| | | $Q_3$ | – | 6.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 9.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.98 | 1.8 | Vdc |
| | ($I_S$ = 9.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.9 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 9.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 91 | – | ns |
| | | $t_a$ | – | 71 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.4 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

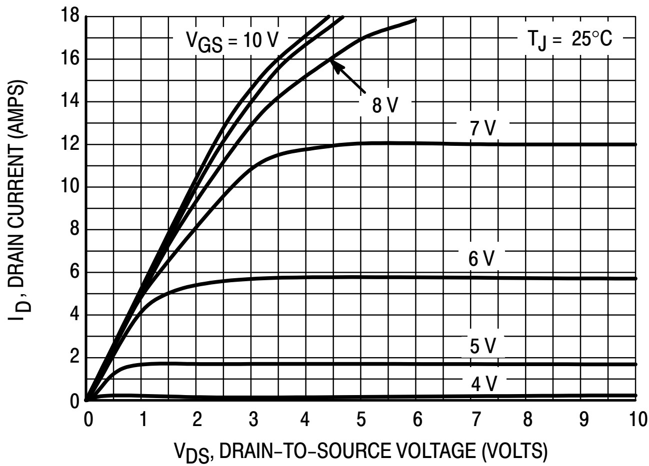



**Figure 1. On–Region Characteristics**

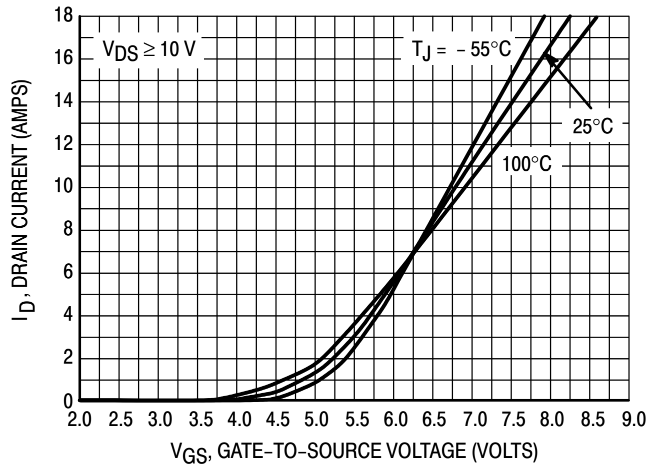



**Figure 2. Transfer Characteristics**

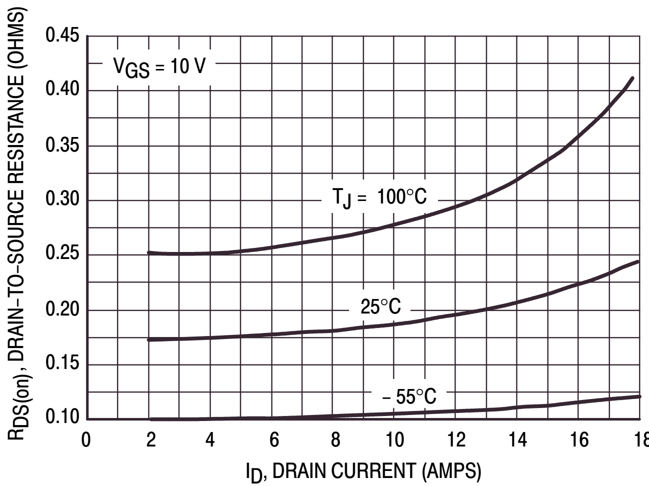



**Figure 3. On–Resistance versus Drain Current and Temperature**

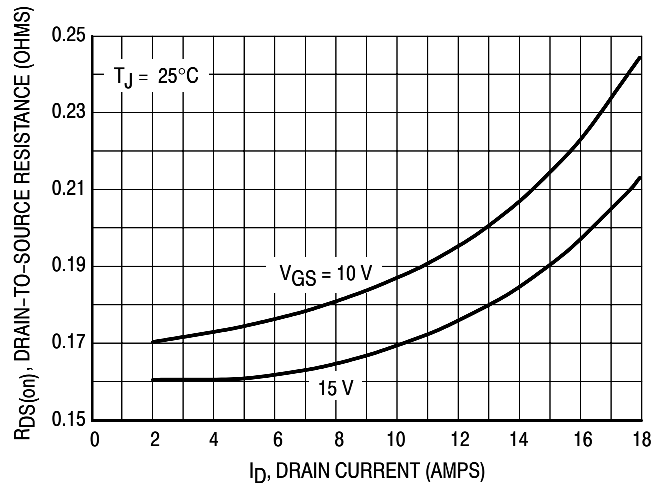



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

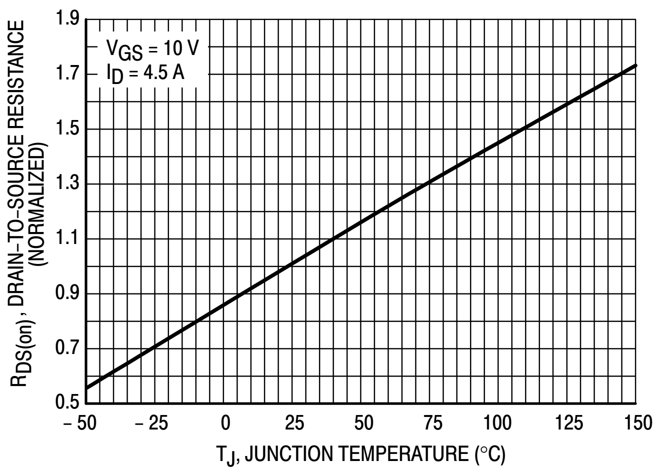



**Figure 5. On–Resistance Variation with Temperature**

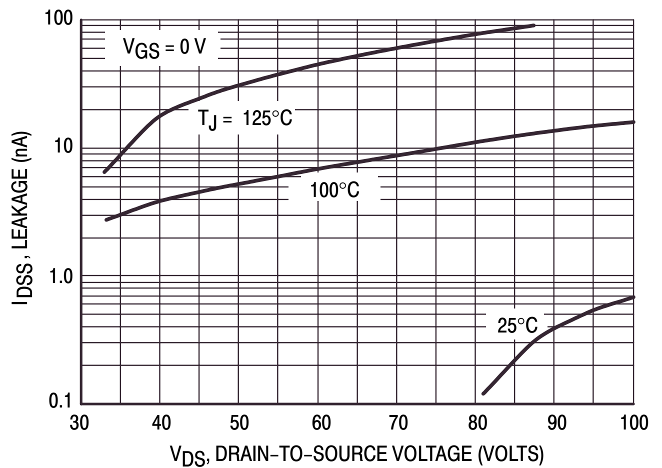



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

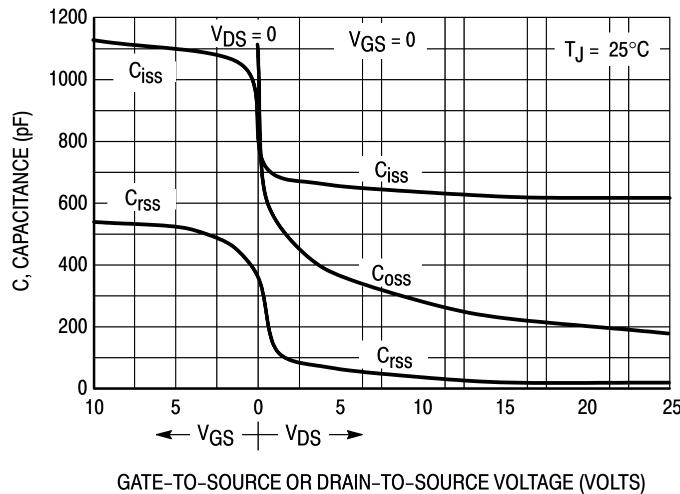



**Figure 7. Capacitance Variation**

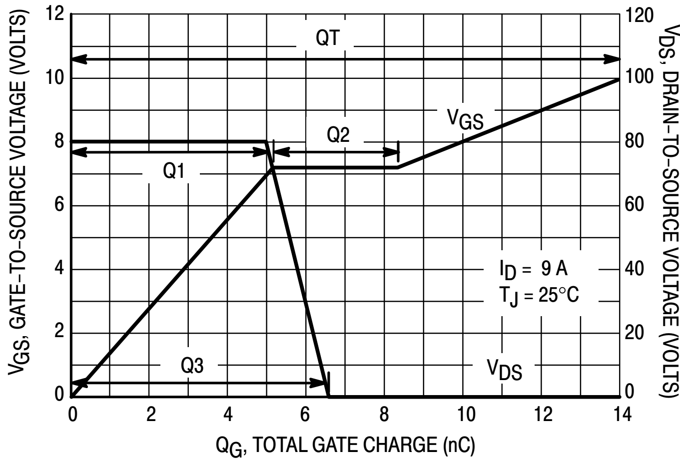



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

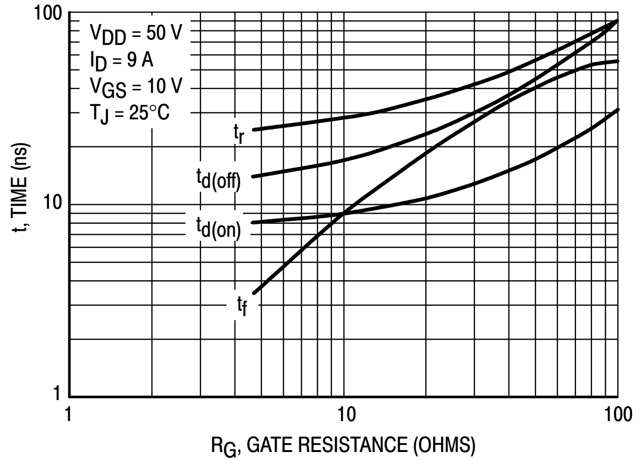



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

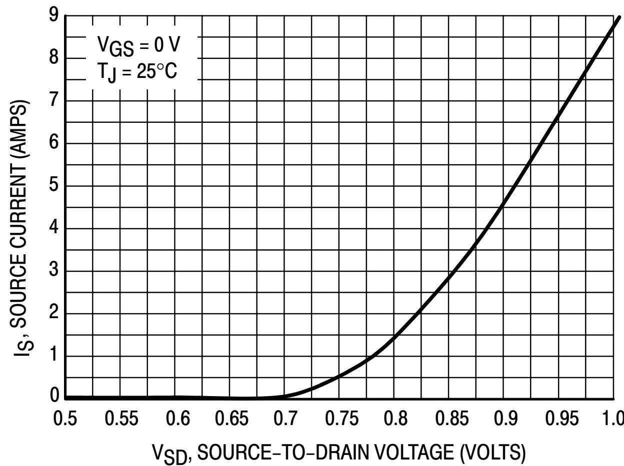



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

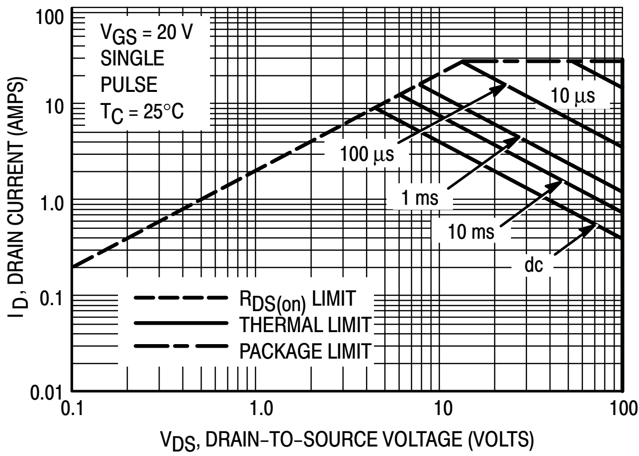



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

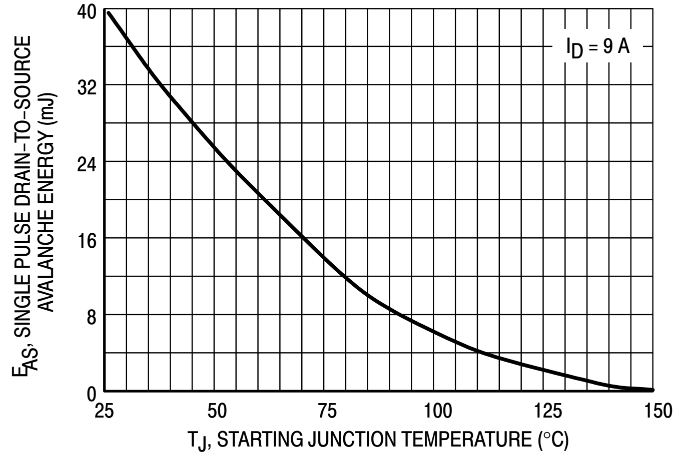



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

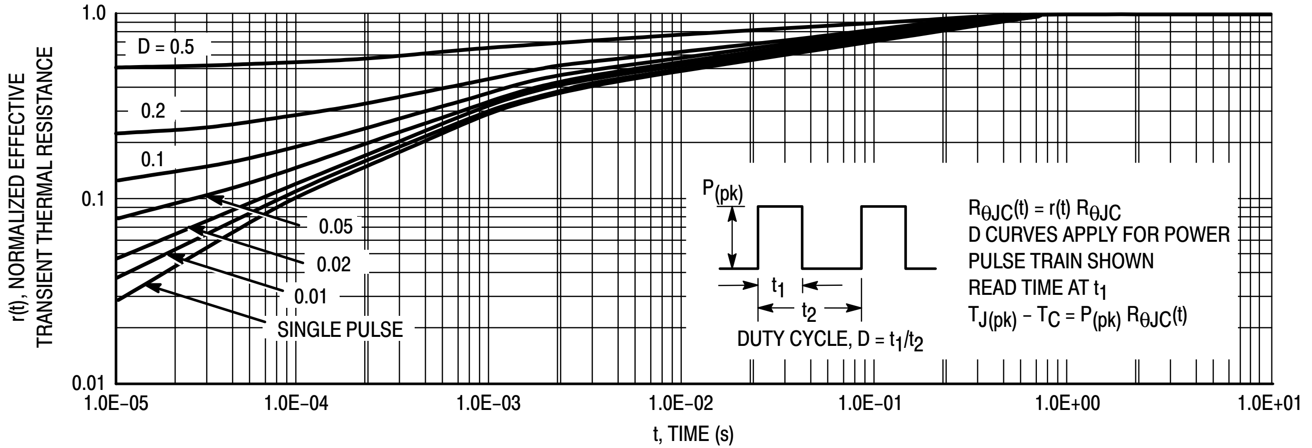



**Figure 13. Thermal Response**

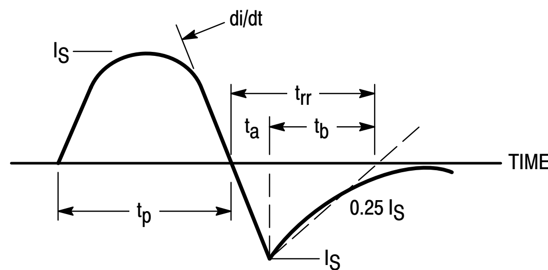
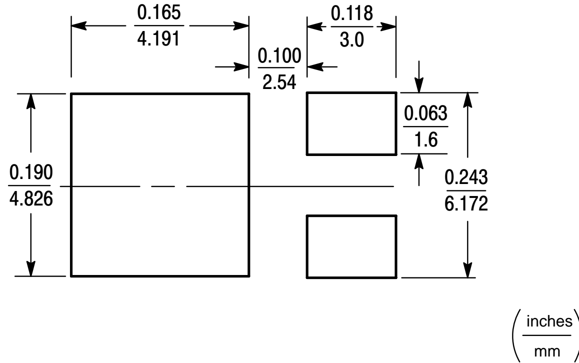



**Figure 14. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE DPAK SURFACE MOUNT PACKAGE

## RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.




## POWER DISSIPATION FOR A SURFACE MOUNT DEVICE

The power dissipation for a surface mount device is a function of the drain pad size. These can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient, and the operating temperature, $T_A$. Using the values provided on the data sheet, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device. For a DPAK device, $P_D$ is calculated as follows.

$$P_D = \frac{150°C - 25°C}{71.4°C/W} = 1.75 \text{ Watts}$$

The 71.4°C/W for the DPAK package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.75 Watts. There are other alternatives to achieving higher power dissipation from the surface mount packages. One is to increase the area of the drain pad. By increasing the area of the drain pad, the power dissipation can be increased. Although one can almost double the power dissipation with this method, one will be giving up area on the printed circuit board which can defeat the purpose of using surface mount technology. For example, a graph of $R_{\theta JA}$ versus drain pad area is shown in Figure 15.

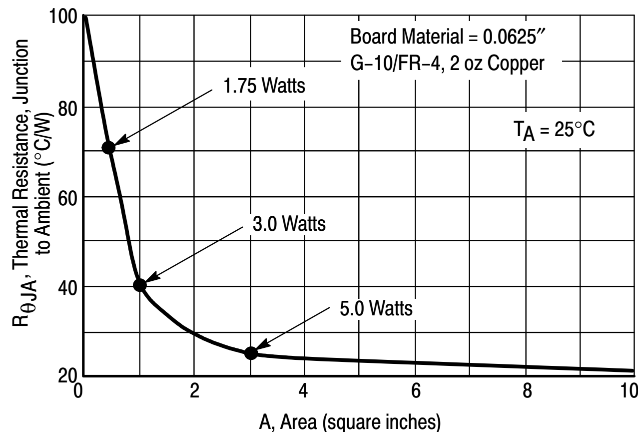



**Figure 15. Thermal Resistance versus Drain Pad Area for the DPAK Package (Typical)**

Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

## SOLDER STENCIL GUIDELINES

Prior to placing surface mount components onto a printed circuit board, solder paste must be applied to the pads. Solder stencils are used to screen the optimum amount. These stencils are typically 0.008 inches thick and may be made of brass or stainless steel. For packages such as the SC–59, SC–70/SOT–323, SOD–123, SOT–23, SOT–143, SOT–223, SO–8, SO–14, SO–16, and SMB/SMC diode packages, the stencil opening should be the same as the pad size or a 1:1 registration. This is not the case with the DPAK and $D^2PAK$ packages. If one uses a 1:1 opening to screen solder onto the drain pad, misalignment and/or "tombstoning" may occur due to an excess of solder. For these two packages, the opening in the stencil for the paste should be approximately 50% of the tab area. The opening for the leads is still a 1:1 registration. Figure 16 shows a typical stencil for the DPAK and $D^2PAK$ packages. The pattern of the opening in the stencil for the drain pad is not critical as long as it allows approximately 50% of the pad to be covered with paste.

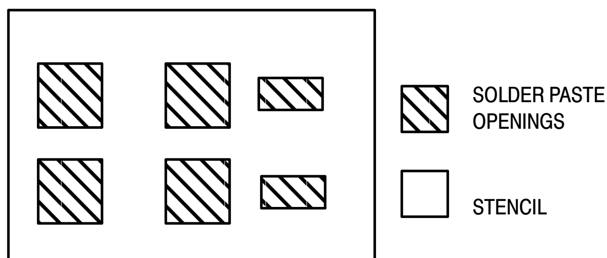



**Figure 16. Typical Stencil for DPAK and $D^2PAK$ Packages**

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

* Due to shadowing and the inability to set the wave height to incorporate other surface mount components, the $D^2PAK$ is not recommended for wave soldering.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones, and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 17 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

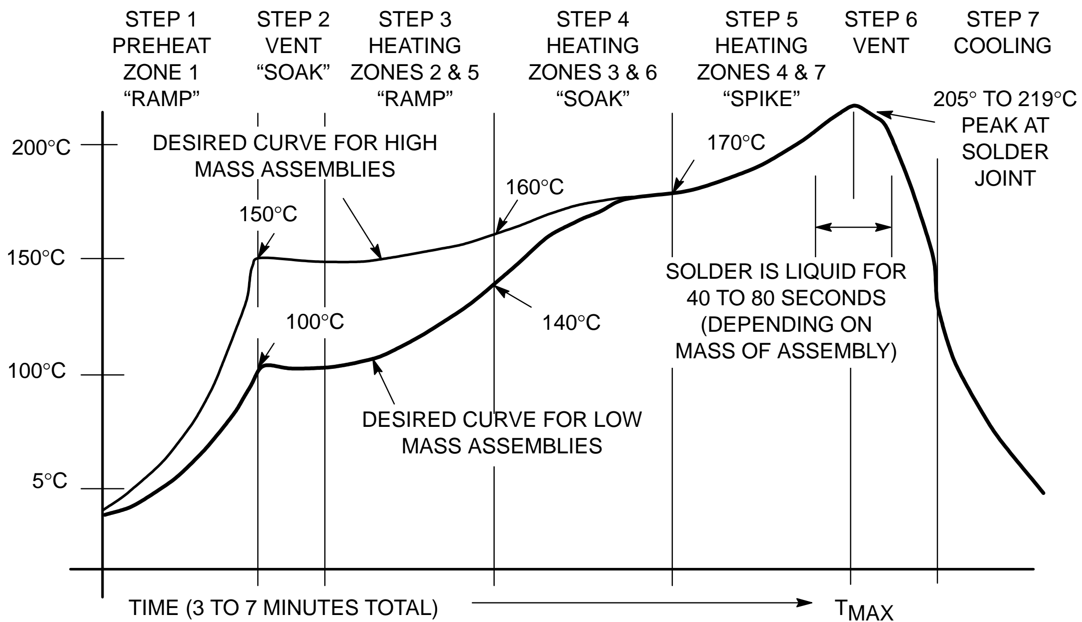



**Figure 17. Typical Solder Heating Profile**

# MTDF1N02HD

**Preferred Device**

# Power MOSFET 1 Amp, 20 Volts

## N–Channel Micro8™, Dual

These Power MOSFET devices are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8 devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

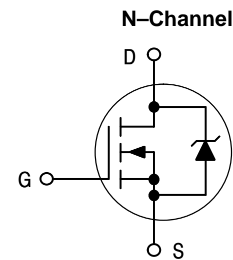
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Extremely Low Profile (<1.1 mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

**ON Semiconductor™**

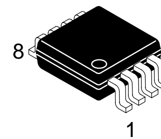
**http://onsemi.com**

**1 AMPERE**
**20 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

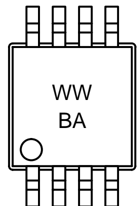
**N–Channel**




**MARKING DIAGRAM**

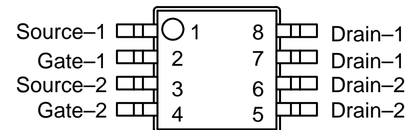



**Micro8, Dual**
**CASE 846A**
**STYLE 2**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTDF1N02HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Typical | Max | Unit |
|---|---|---|---|---|---|
| Drain–to–Source Voltage | | $V_{DSS}$ | – | 20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | | $V_{DGR}$ | – | 20 | V |
| Gate–to–Source Voltage – Continuous | | $V_{GS}$ | – | ± 8.0 | V |
| 1″ SQ. | Thermal Resistance – Junction to Ambient | $R_{THJA}$ | 80 | 100 | °C/W |
| FR–4 or G–10 PCB | Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | – | 1.25 | Watts |
| Figure 1 below | Linear Derating Factor | | – | 10 | mW/°C |
| | Drain Current – Continuous @ $T_A$ = 25°C | $I_D$ | – | 2.8 | A |
| 1 die operating | Continuous @ $T_A$ = 70°C | $I_D$ | – | 2.3 | A |
| Steady State | Pulsed Drain Current (Note 1.) | $I_{DM}$ | – | 23 | A |
| Minimum | Thermal Resistance – Junction to Ambient | $R_{THJA}$ | 160 | 200 | °C/W |
| FR–4 or G–10 PCB | Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | – | 0.63 | Watts |
| Figure 2 below | Linear Derating Factor | | – | 5.0 | mW/°C |
| | Drain Current – Continuous @ $T_A$ = 25°C | $I_D$ | – | 1.7 | A |
| 1 die operating | Continuous @ $T_A$ = 70°C | $I_D$ | – | 1.6 | A |
| Steady State | Pulsed Drain Current (Note 1.) | $I_{DM}$ | – | 16 | A |
| Minimum | Thermal Resistance – Junction to Ambient | $R_{THJA}$ | 240 | 300 | °C/W |
| FR–4 or G–10 PCB | Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | – | 0.42 | Watts |
| Figure 2 below | Linear Derating Factor | | – | 3.33 | mW/°C |
| | Drain Current – Continuous @ $T_A$ = 25°C | $I_D$ | – | 1.6 | A |
| 2 die operating | Continuous @ $T_A$ = 70°C | $I_D$ | – | 1.3 | A |
| Steady State | Pulsed Drain Current (Note 1.) | $I_{DM}$ | – | 13 | A |
| Operating and Storage Temperature Range | | $T_J$, $T_{stg}$ | – | – 55 to 150 | °C |

1. Repetitive rating; pulse width limited by maximum junction temperature.

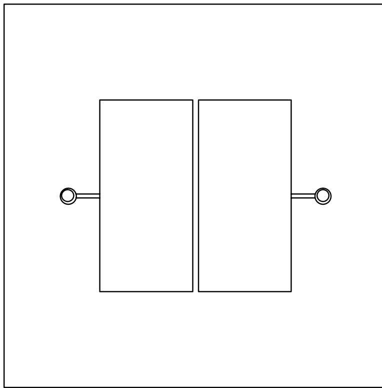


**Figure 1. 1″ Square FR–4 or G–10 PCB**

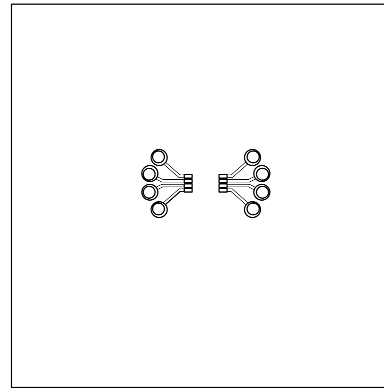


**Figure 2. Minimum FR–4 or G–10 PCB**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>20<br>– | <br>–<br>5.0 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>0.7<br>– | <br>0.9<br>2.5 | <br>1.1<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.7 Adc)<br>($V_{GS}$ = 2.7 Vdc, $I_D$ = 0.85 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>99<br>133 | <br>120<br>160 | mΩ |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 0.85 Adc) | | $g_{FS}$ | 2.0 | – | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 145 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 90 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 38 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 8.0 | – | ns |
| Rise Time | | $t_r$ | – | 27 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 23 | – | |
| Fall Time | | $t_f$ | – | 34 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 0.85 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 16 | – | ns |
| Rise Time | | $t_r$ | – | 79 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 24 | – | |
| Fall Time | | $t_f$ | – | 31 | – | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 3.9 | 5.5 | nC |
| | | $Q_1$ | – | 0.4 | – | |
| | | $Q_2$ | – | 1.7 | – | |
| | | $Q_3$ | – | 1.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.84<br>0.71 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 29 | – | ns |
| | | $t_a$ | – | 14 | – | |
| | | $t_b$ | – | 15 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.018 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

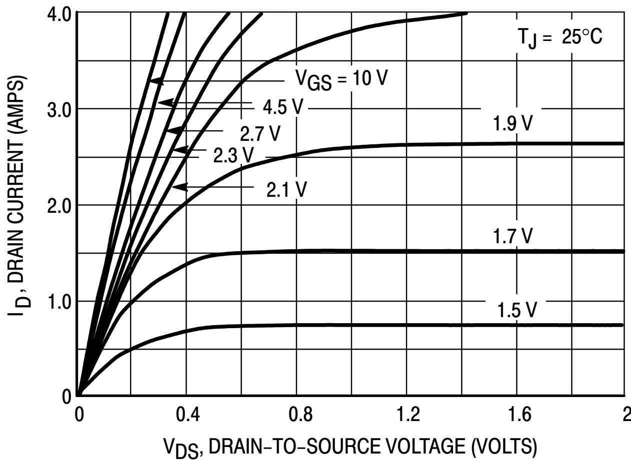



**Figure 3. On–Region Characteristics**

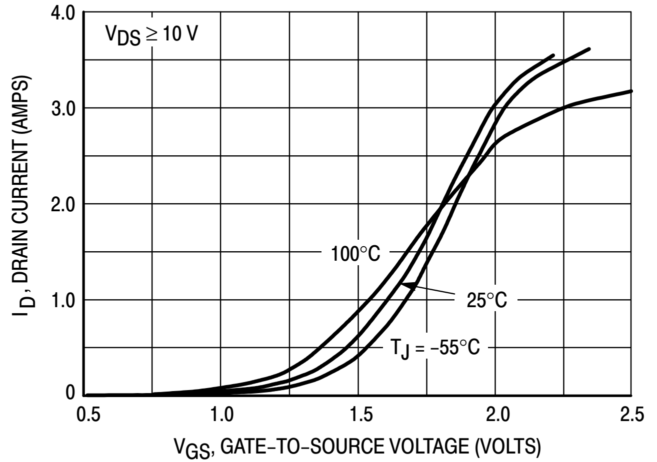



**Figure 4. Transfer Characteristics**

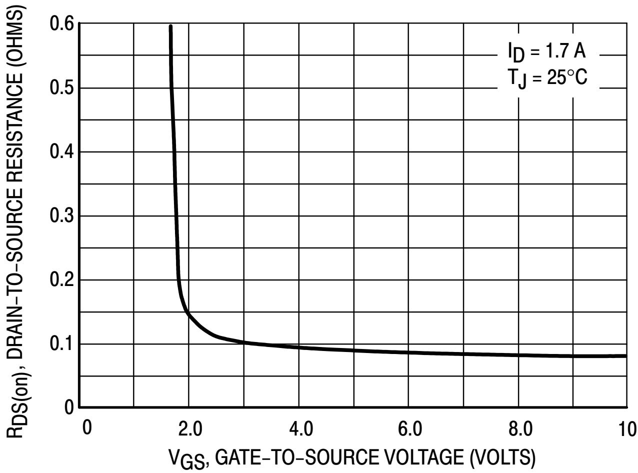



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

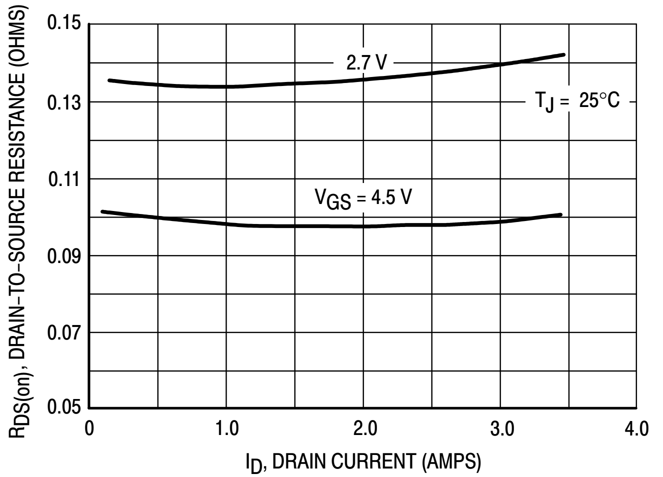



**Figure 6. On–Resistance versus Drain Current and Gate Voltage**

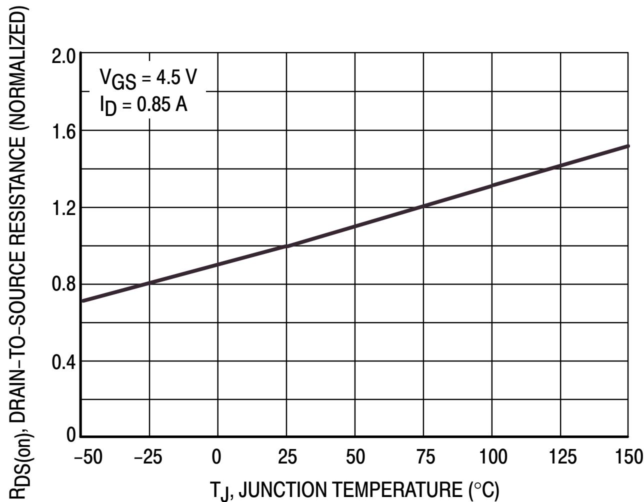



**Figure 7. On–Resistance Variation with Temperature**

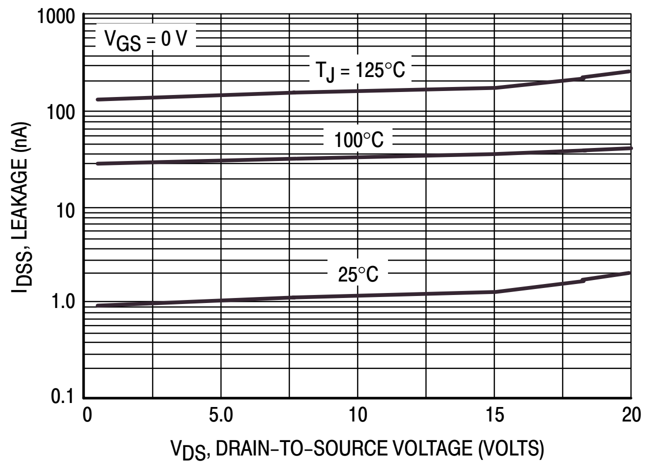



**Figure 8. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

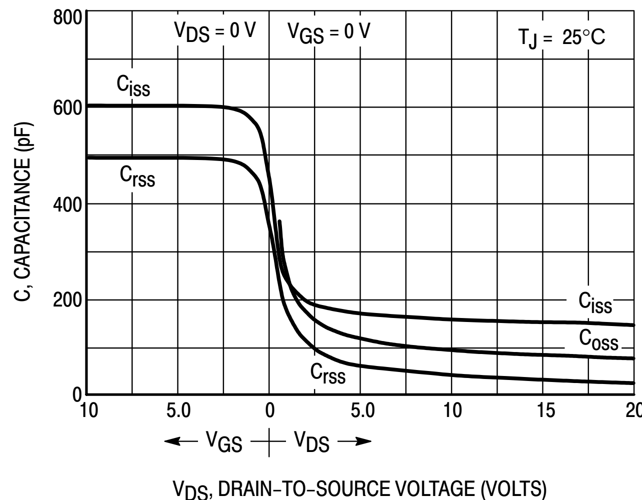



**Figure 9. Capacitance Variation**

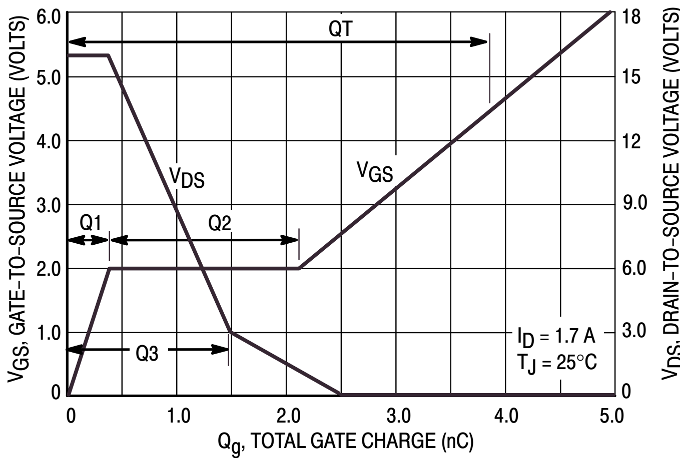



**Figure 10. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

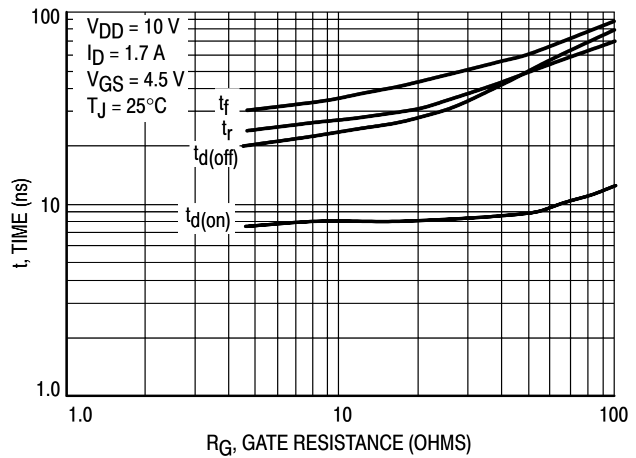



**Figure 11. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 13. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

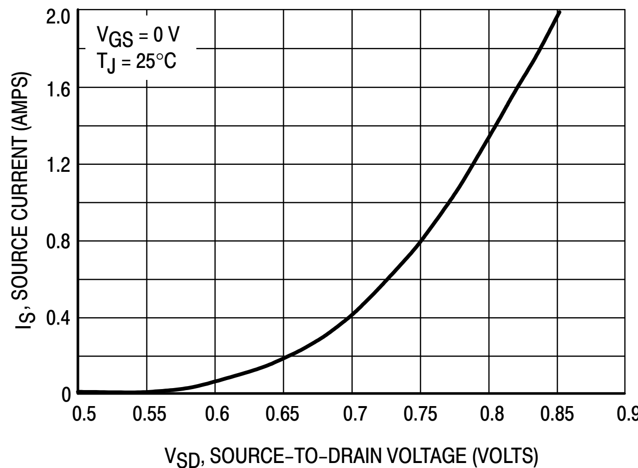



**Figure 12. Diode Forward Voltage versus Current**

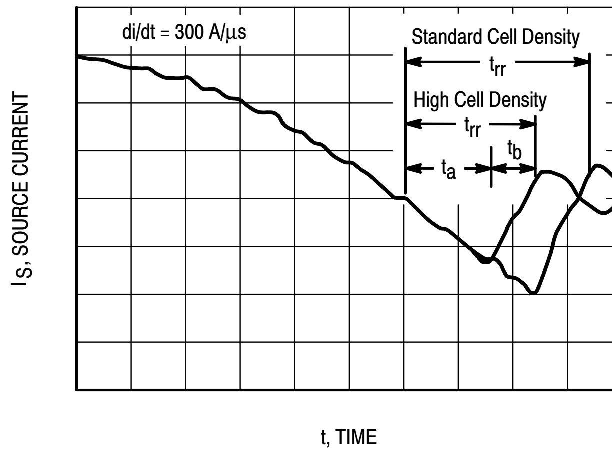



**Figure 13. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 14) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{θJC}$).

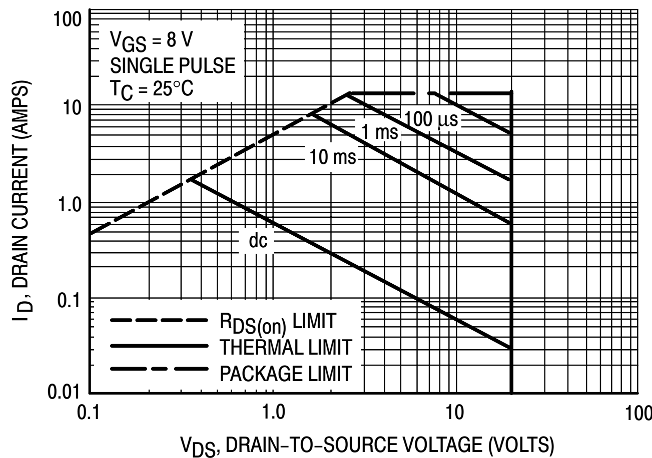



**Figure 14. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

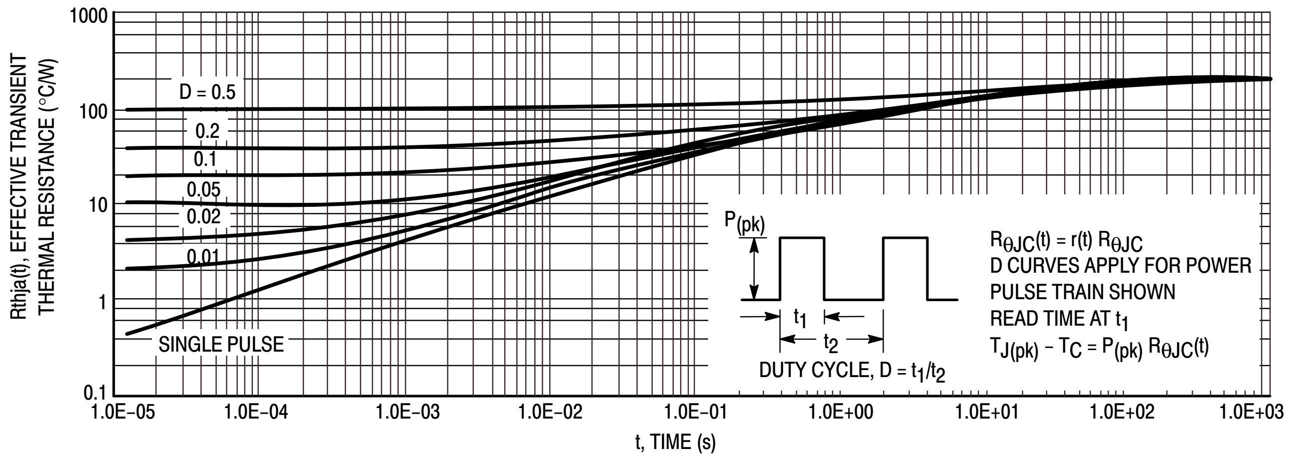



**Figure 15. Thermal Response**

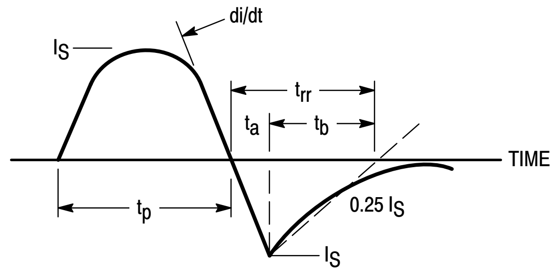
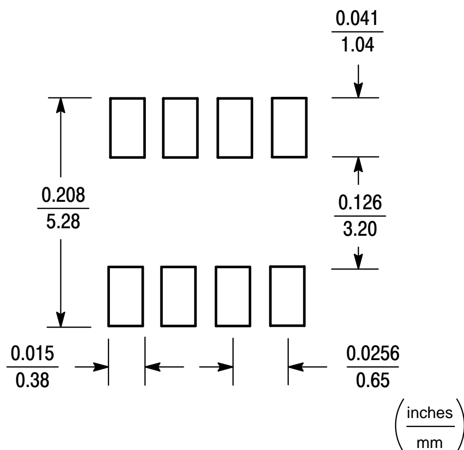



**Figure 16. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.63 Watts.

$$P_D = \frac{150°C - 25°C}{200°C/W} = 0.63 \text{ Watts}$$

The 200°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.63 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 15 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

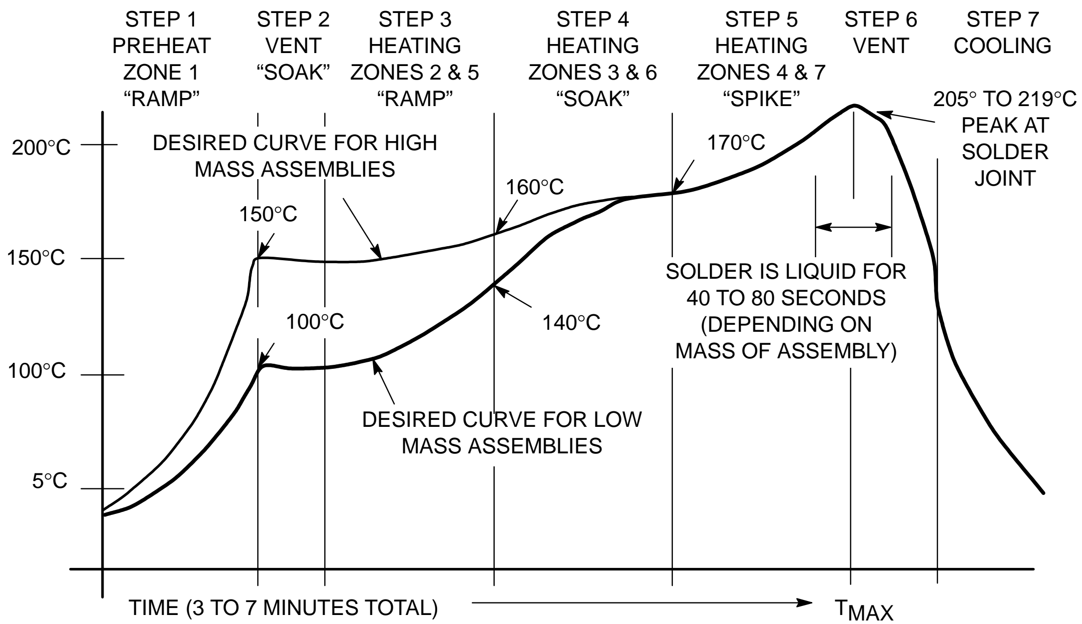
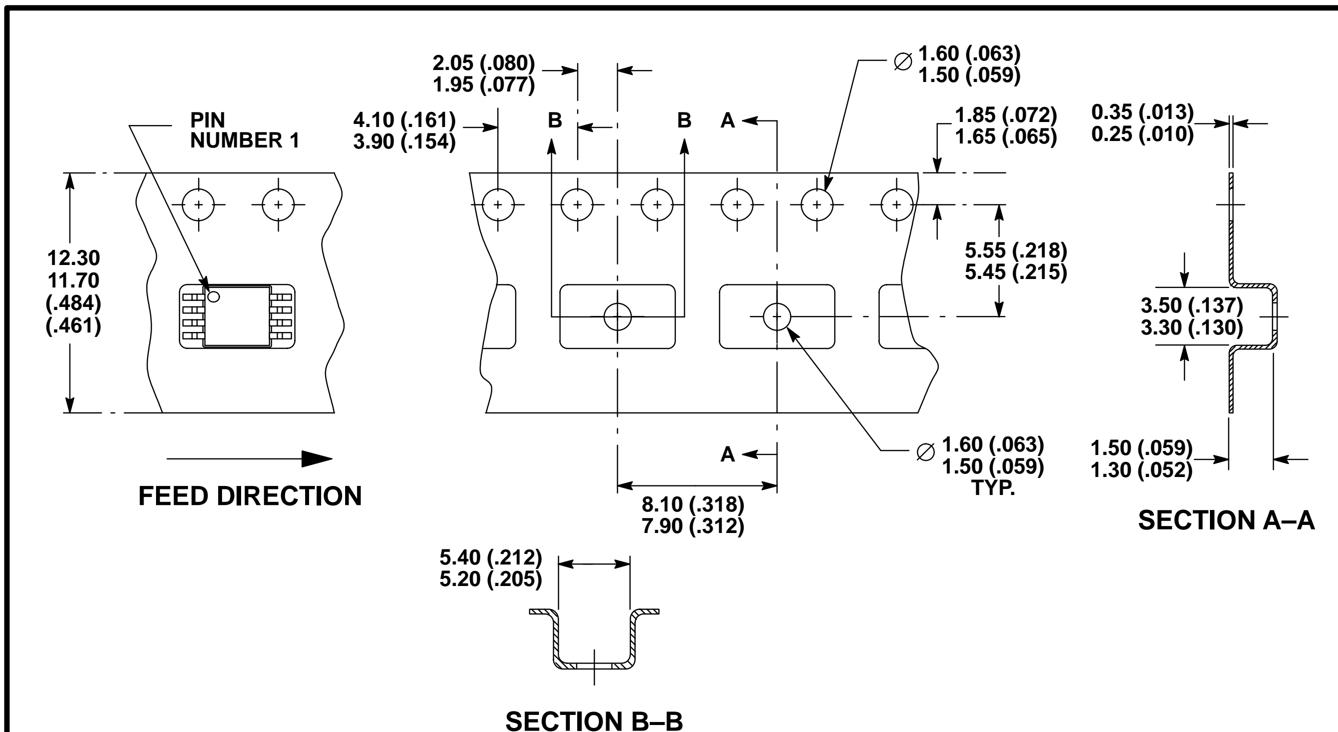


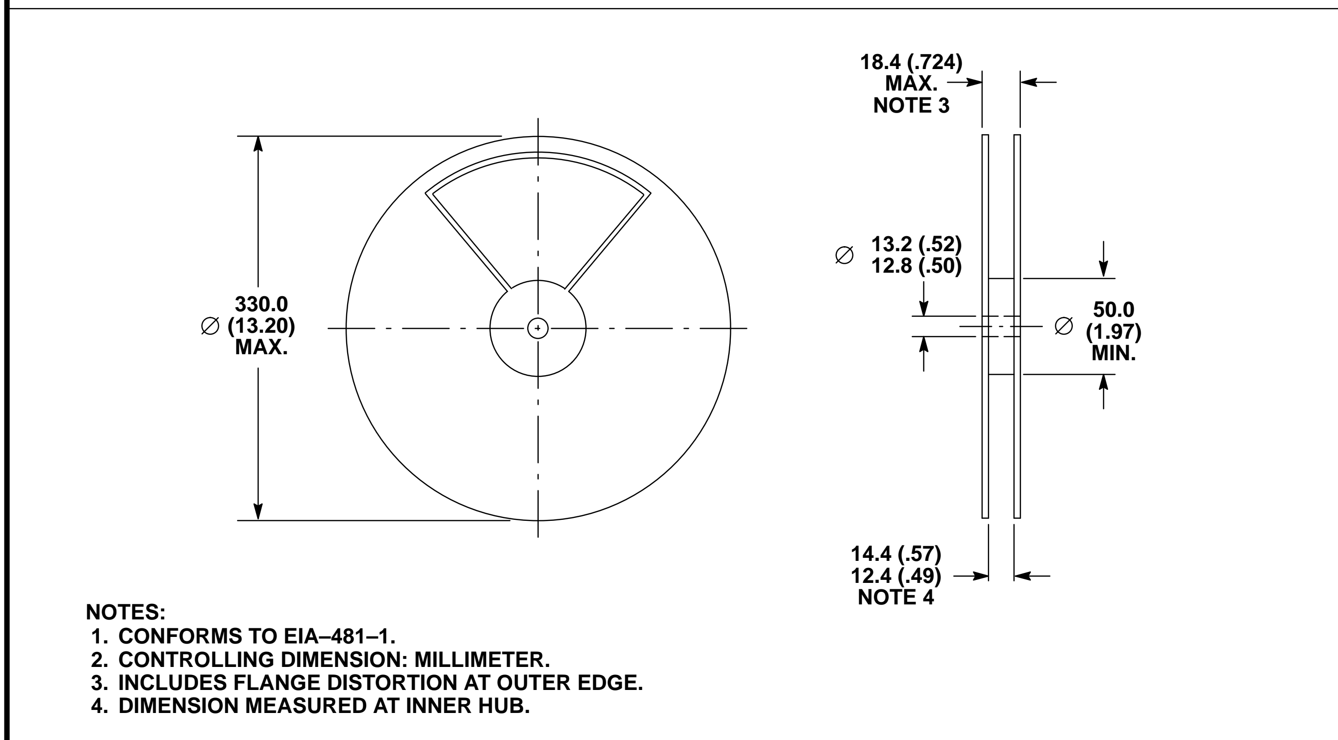

**Figure 17. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro8**

Dimensions are shown in millimeters (inches)



# MTDF1N03HD

**Preferred Device**

# Power MOSFET 1 Amp, 30 Volts

## N–Channel Micro8™, Dual

These Power MOSFET devices are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8 devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

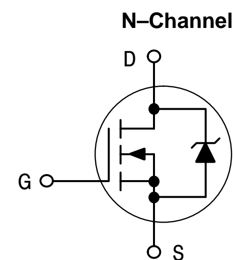
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

**ON Semiconductor™**

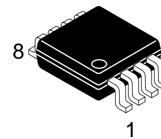
**http://onsemi.com**

**1 AMPERE**
**30 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

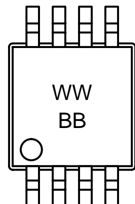
**N–Channel**




**MARKING DIAGRAM**

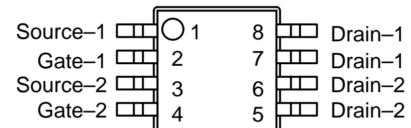



**Micro8, Dual**
**CASE 846A**
**STYLE 2**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTDF1N03HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)
**Negative sign for P–Channel devices omitted for clarity**

| Rating | | Symbol | Max | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | | $V_{DSS}$ | 30 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | | $V_{DGR}$ | 30 | V |
| Gate–to–Source Voltage – Continuous | | $V_{GS}$ | ± 20 | V |
| 1″ SQ.<br>FR–4 or G–10 PCB<br>Figure 1 below<br><br><br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 100<br>1.25<br>10<br>2.8<br>2.2<br>23 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Minimum<br>FR–4 or G–10 PCB<br>Figure 2 below<br><br>1 die operating<br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 200<br>0.63<br>5.0<br>2.0<br>1.6<br>16 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Minimum<br>FR–4 or G–10 PCB<br>Figure 2 below<br><br>2 die operating<br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 300<br>0.42<br>3.33<br>1.6<br>1.3<br>13 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Operating and Storage Temperature Range | | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 2.4 Apk, L = 69 mH, $R_G$ = 25 Ω) | | $E_{AS}$ | 200 | mJ |

1. Repetitive rating; pulse width limited by maximum junction temperature.

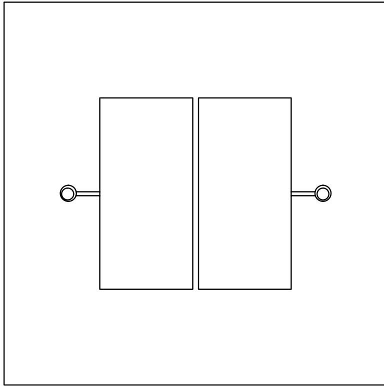


**Figure 1. 1″ Square FR–4 or G–10 PCB**

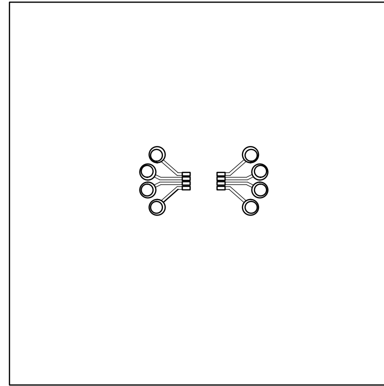


**Figure 2. Minimum FR–4 or G–10 PCB**

## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>29 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.6<br>3.7 | <br>–<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 1.7 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 0.85 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>96<br>135 | <br>120<br>160 | mΩ |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 0.85 Adc) (Note 2.) | | $g_{FS}$ | 1.0 | 2.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 140 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 70 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 30 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 15 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 7.5 | – | ns |
| Rise Time | | $t_r$ | – | 10 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 22 | – | |
| Fall Time | | $t_f$ | – | 18 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 0.85 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 7.0 | – | ns |
| Rise Time | | $t_r$ | – | 8.2 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 22 | – | |
| Fall Time | | $t_f$ | – | 14.5 | – | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 1.7 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 5.0 | 7.0 | nC |
| | | $Q_1$ | – | 0.5 | – | |
| | | $Q_2$ | – | 1.65 | – | |
| | | $Q_3$ | – | 1.3 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.84<br>0.7 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 1.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 20 | – | ns |
| | | $t_a$ | – | 12 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.012 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

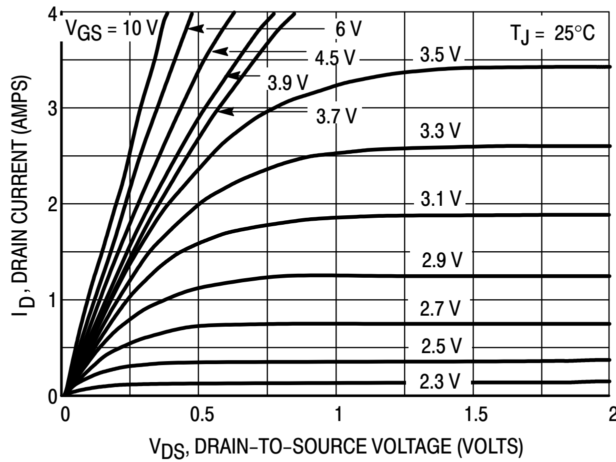



**Figure 3. On–Region Characteristics**

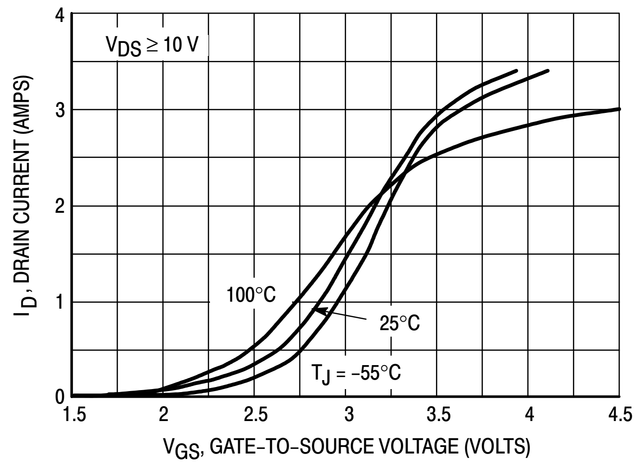



**Figure 4. Transfer Characteristics**

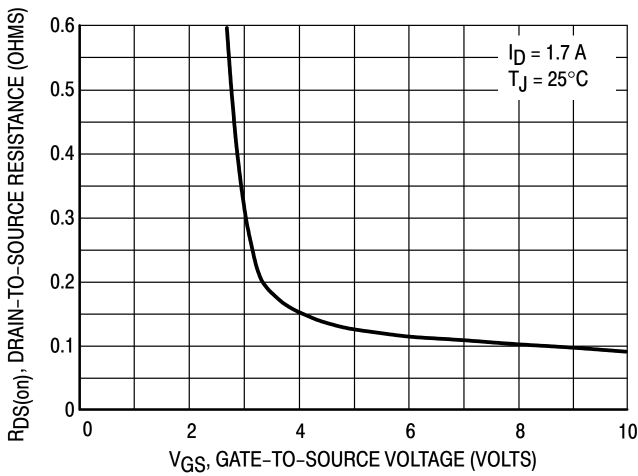



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

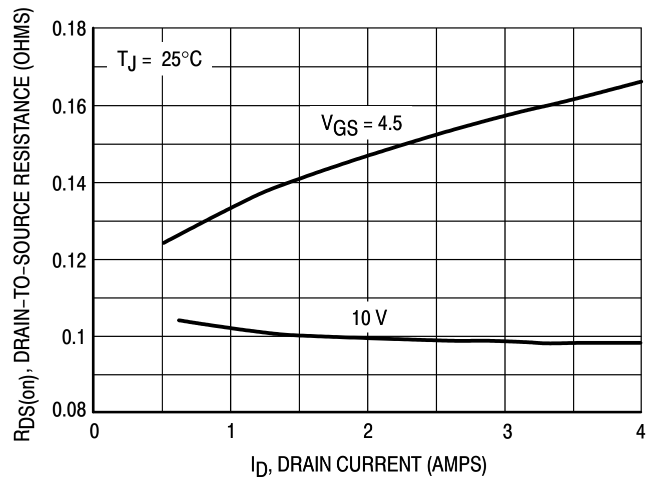



**Figure 6. On–Resistance versus Drain Current and Gate Voltage**

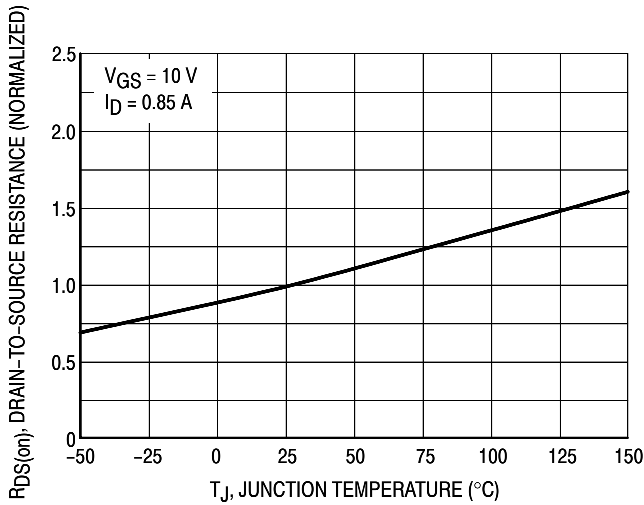



**Figure 7. On–Resistance Variation with Temperature**

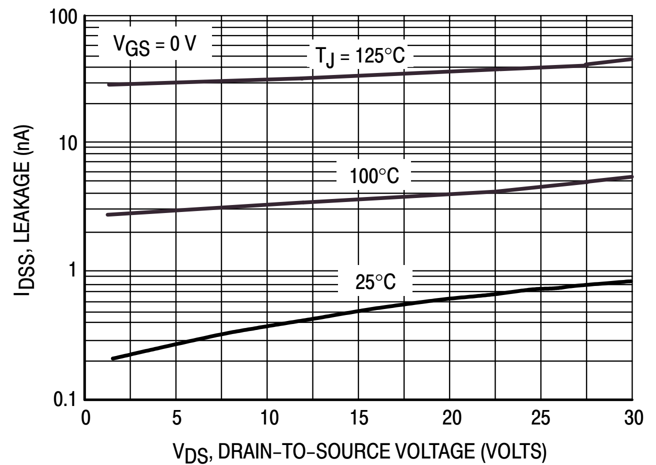



**Figure 8. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 11) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

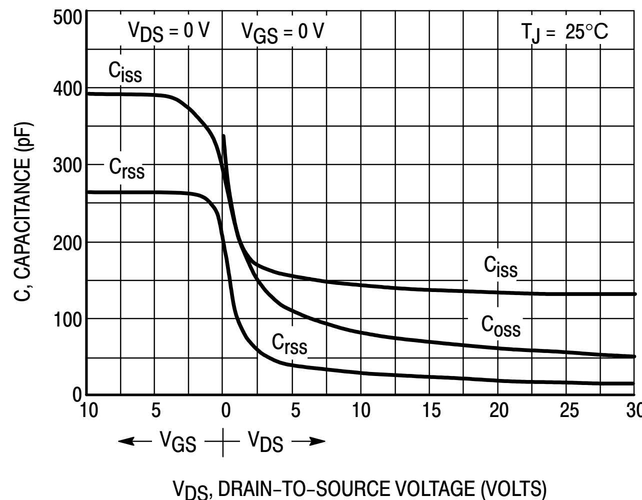



**Figure 9. Capacitance Variation**

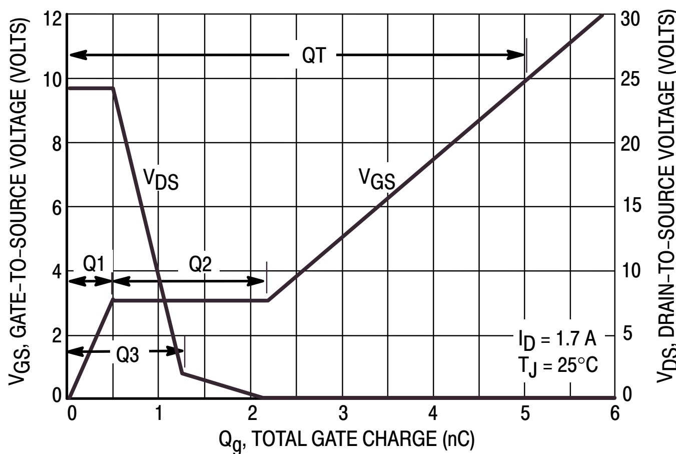



**Figure 10. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

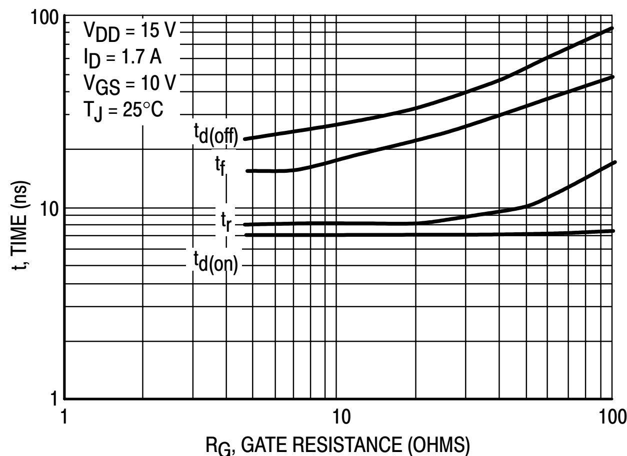



**Figure 11. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 13. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

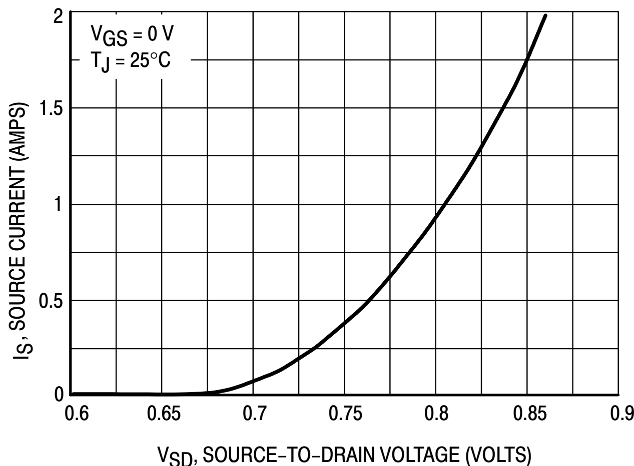



**Figure 12. Diode Forward Voltage versus Current**

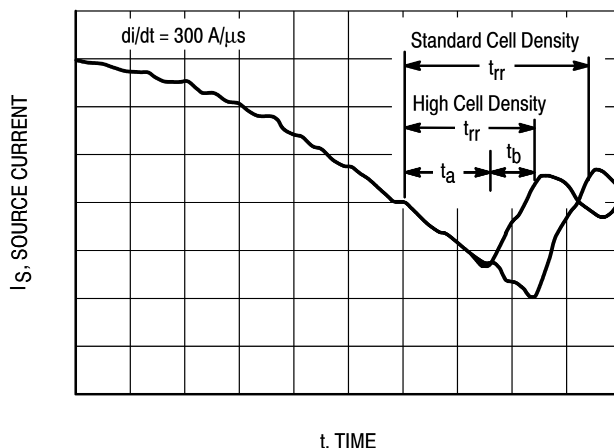



**Figure 13. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 14) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 16). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

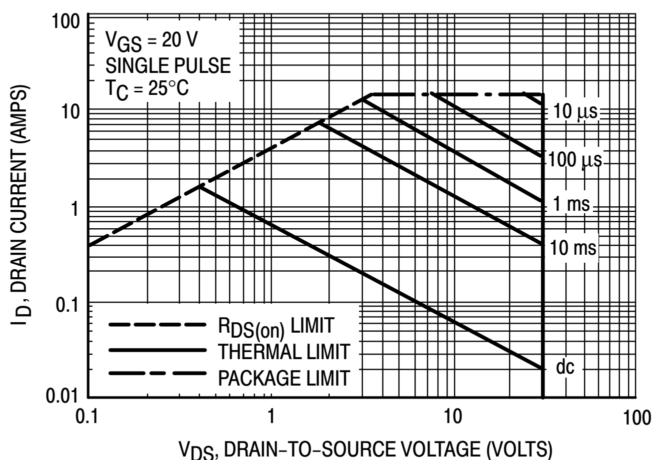



**Figure 14. Maximum Rated Forward Biased Safe Operating Area**

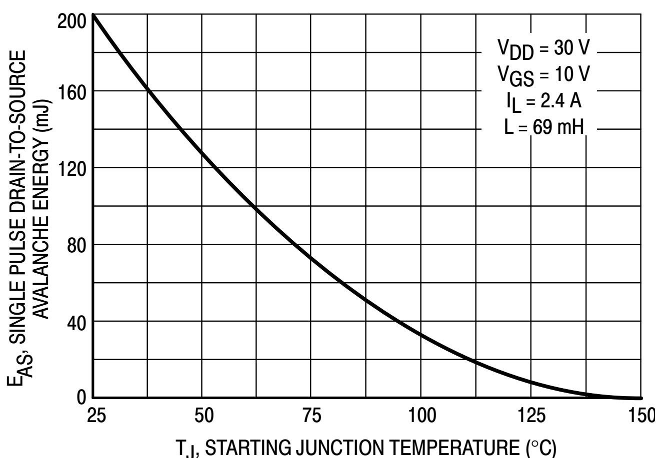



**Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

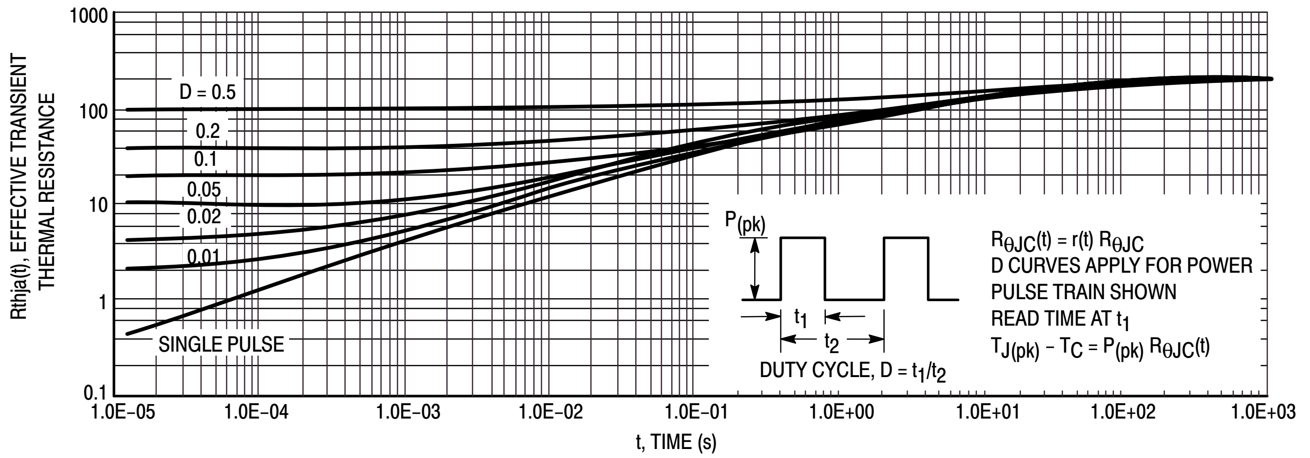



**Figure 16. Thermal Response**

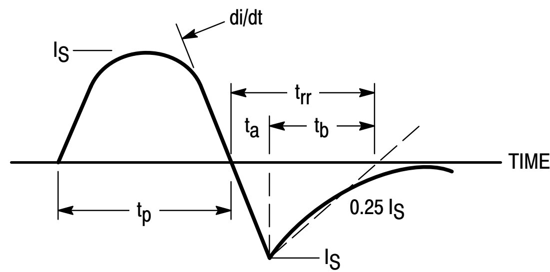
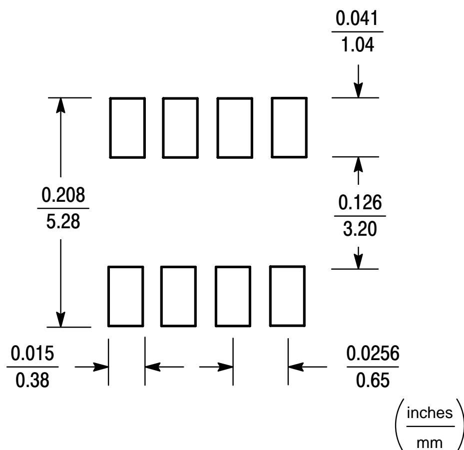



**Figure 17. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.63 Watts.

$$P_D = \frac{150°C - 25°C}{200°C/W} = 0.63 \text{ Watts}$$

The 200°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.63 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

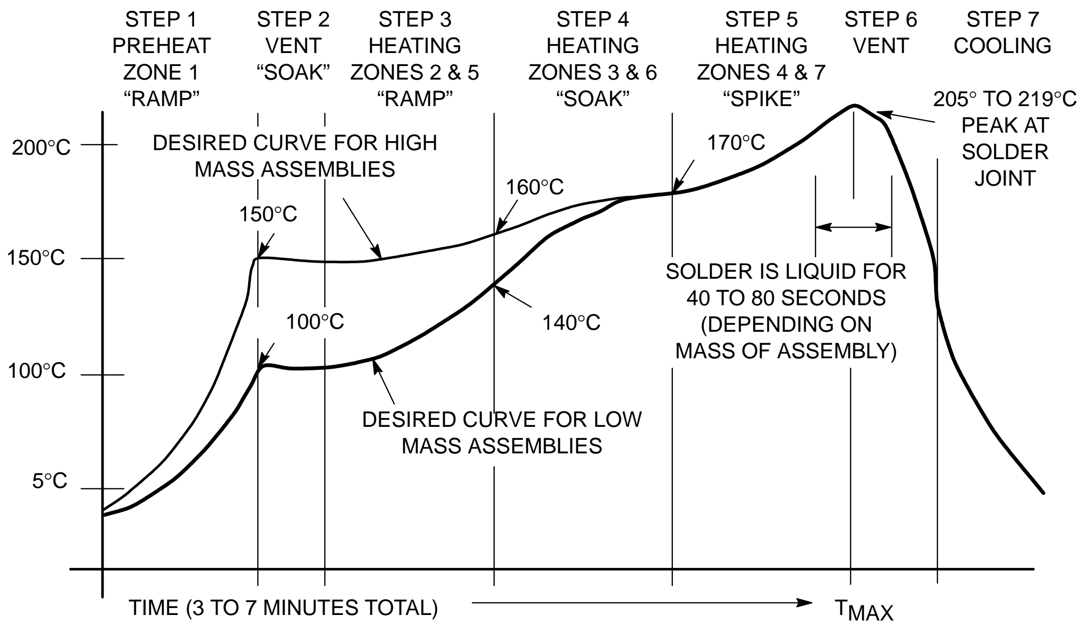
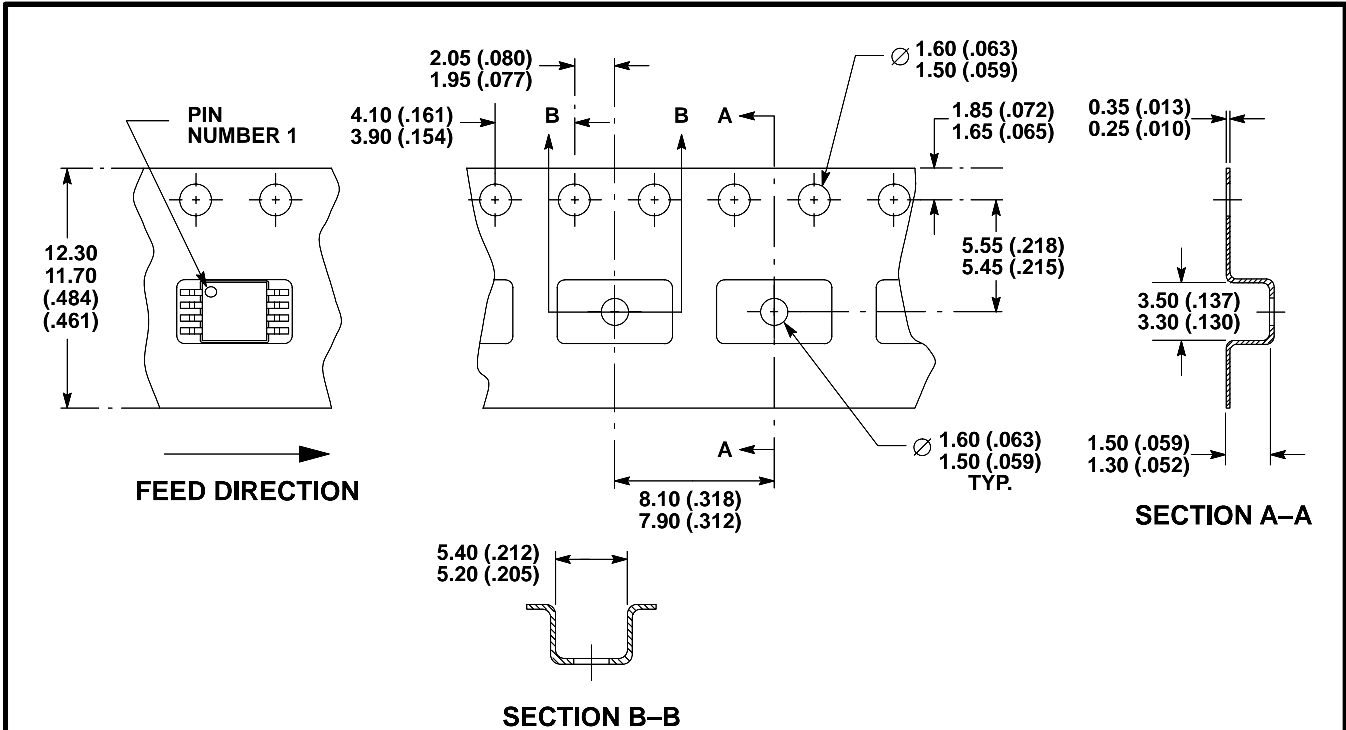


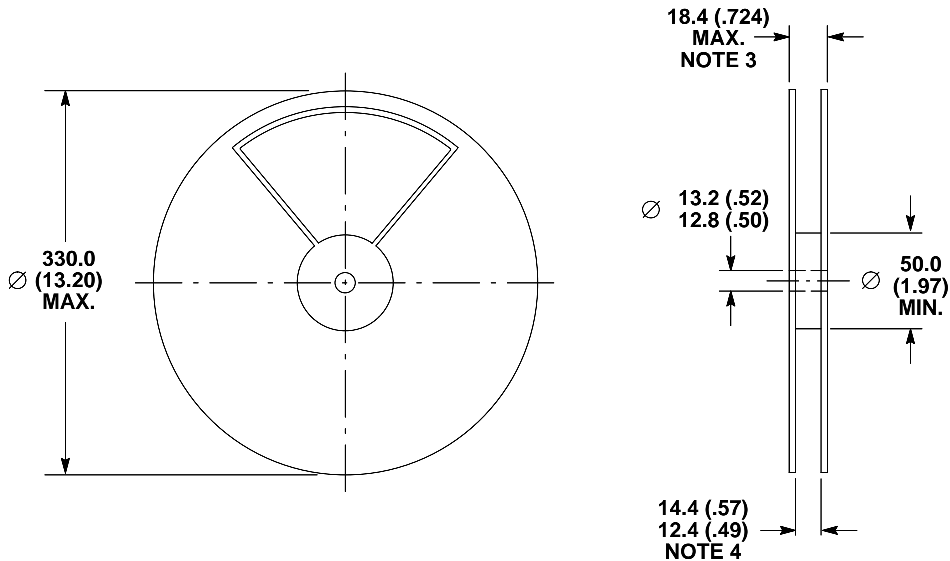

**Figure 18. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro8**
Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# MTDF2N06HD

**Preferred Device**

# Power MOSFET 2 Amps, 60 Volts

## N–Channel Micro8™, Dual

Micro8 devices are an advanced series of Power MOSFETs that contain monolithic back–to–back zener diodes. These zener diodes provide protection against ESD and unexpected transients. These miniature surface mount MOSFETs feature ultra low $R_{DS(on)}$ and true logic level performance. They are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives.

- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Mounting Information for Micro8 Package Provided

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 20 | Vdc |
| Continuous Drain Current @ $T_A$ = 25°C (Note 1.)<br>Pulsed Drain Current (Note 2.) | $I_D$<br>$I_{DM}$ | 1.5<br>12 | Adc |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.) | $P_D$ | 1.25 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Continuous Source Current (Diode Conduction) (Note 3.) | $I_S$ | 0.9 | Adc |

**THERMAL RESISTANCE**

| Parameter | Symbol | Max | Unit |
|---|---|---|---|
| Junction–to–Ambient (Note 1.) | $R_{θJA}$ | 100 | °C/W |

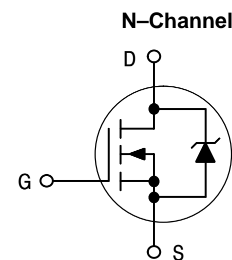
1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 10 V, @ 10 Seconds)
2. Repetitive rating; pulse width limited by maximum junction temperature.
3. When mounted on FR–4 board, t ≤ 10 seconds

ON Semiconductor™

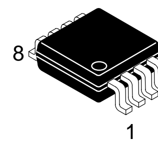
http://onsemi.com

**2 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 220 mΩ**

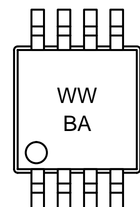
**N–Channel**




**MARKING DIAGRAM**

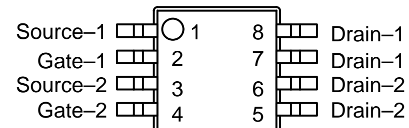



**Micro8, Dual**
**CASE 846A**
**STYLE 2**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTDF2N06HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 4.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | | $V_{GS(th)}$ | 1.0 | 1.6 | 3.0 | Vdc |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Notes 4. & 6.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 0.75 Adc) | | $R_{DS(on)}$ | –<br>– | 180<br>220 | 220<br>260 | mΩ |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 1.0 Adc) (Note 4.) | | $g_{FS}$ | 0.5 | 2.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 V, f = 1.0 MHz) | $C_{iss}$ | – | 140 | 200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 40 | 60 | |
| Transfer Capacitance | | $C_{rss}$ | – | 12 | 18 | |
| **SWITCHING CHARACTERISTICS** (Note 5.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 1.5 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.0 Ω) (Note 4.) | $t_{d(on)}$ | – | 7.5 | 15 | ns |
| Rise Time | | $t_r$ | – | 8.0 | 16 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 25 | 50 | |
| Fall Time | | $t_f$ | – | 14.5 | 29 | |
| Gate Charge<br>(See Figure 8) | ($V_{GS}$ = 10 Vdc, $I_D$ = 1.5 Adc, $V_{DD}$ = 30 Vdc) (Note 4.) | $Q_T$ | – | 18 | 26 | nC |
| | | $Q_1$ | – | 3.1 | – | |
| | | $Q_2$ | – | 6.8 | – | |
| | | $Q_3$ | – | 5.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc) (Note 4.)<br>($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.9<br>0.83 | 1.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 1.5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4.) | $t_{rr}$ | – | 24 | – | ns |
| | | $t_a$ | – | 18 | – | |
| | | $t_b$ | – | 6.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.02 | – | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperatures.
6. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

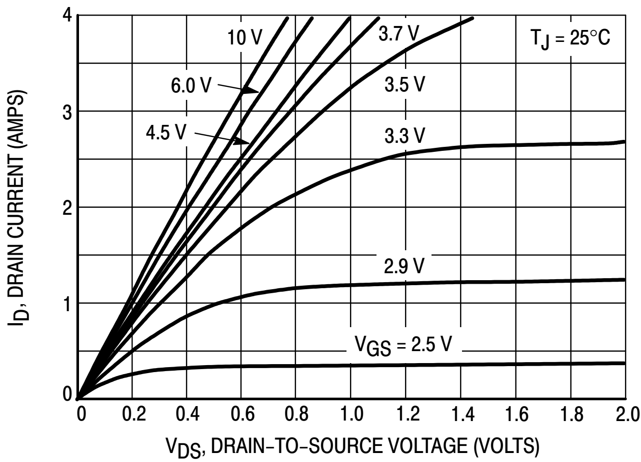



**Figure 1. On–Region Characteristics**

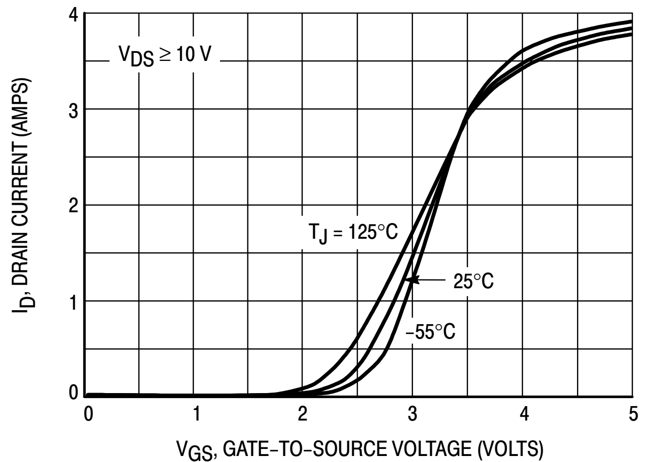



**Figure 2. Transfer Characteristics**

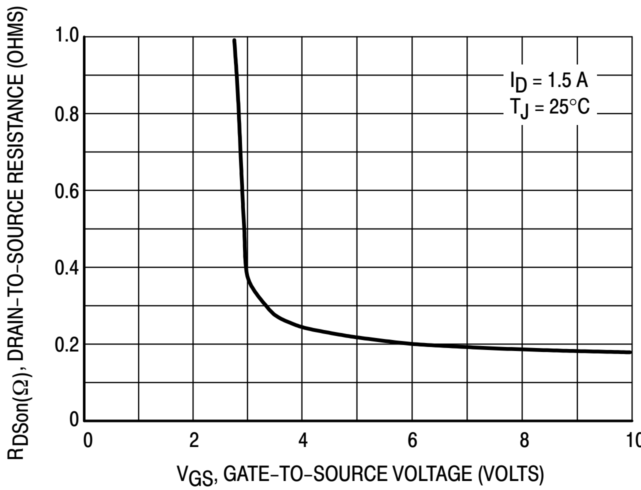



**Figure 3. On–Resistance versus Drain Current**

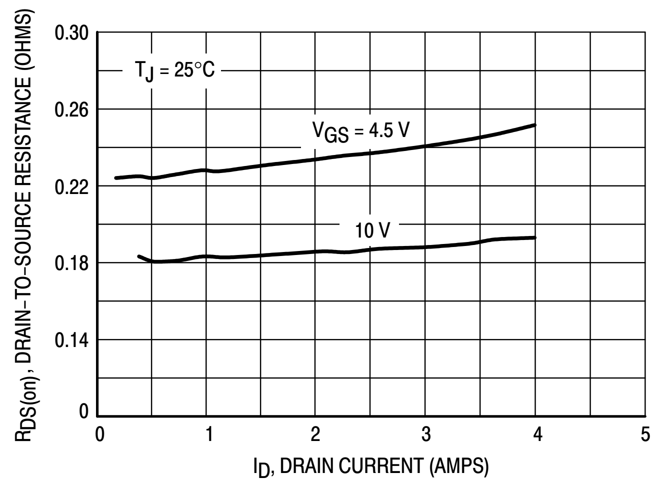



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

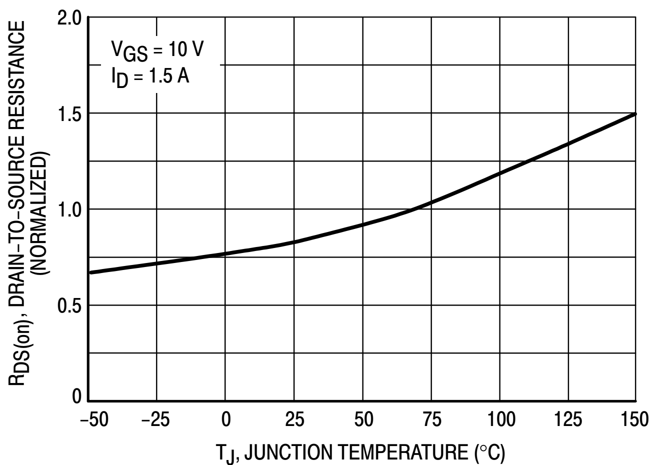



**Figure 5. On–Resistance Variation with Temperature**

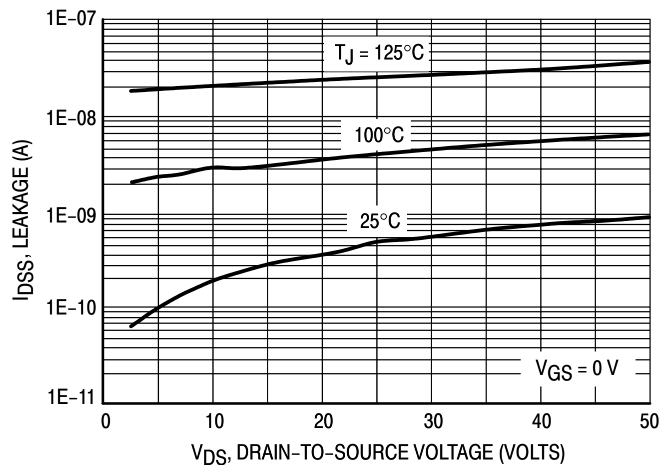



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

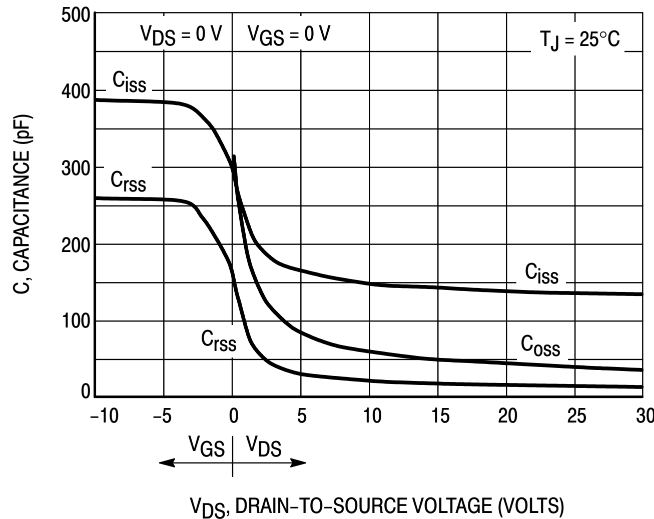



**Figure 7. Capacitance Variation**

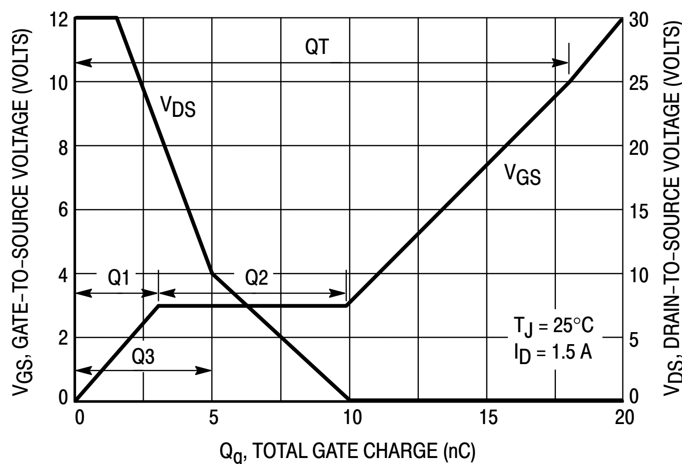



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

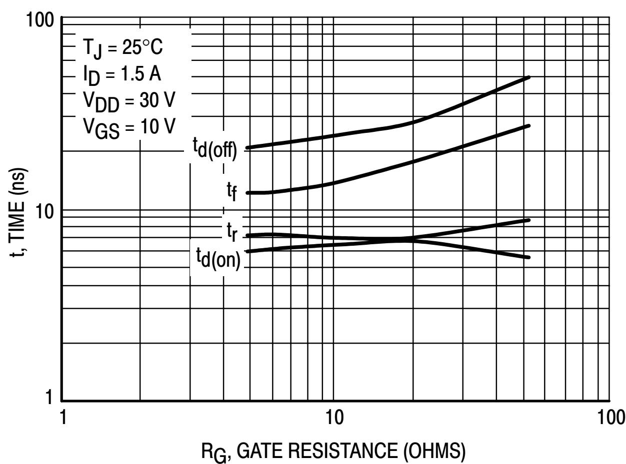



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

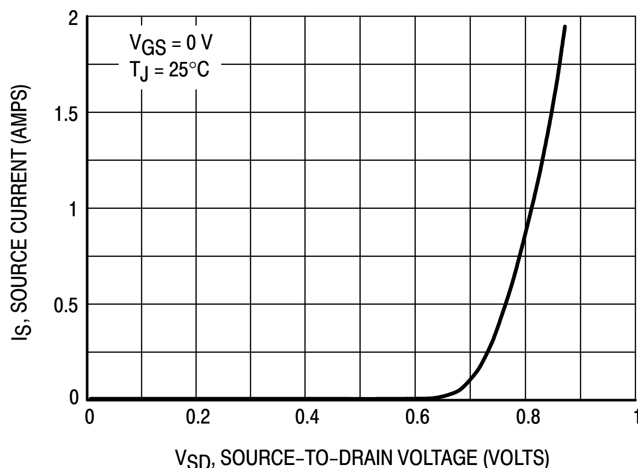



**Figure 10. Diode Forward Voltage versus Current**

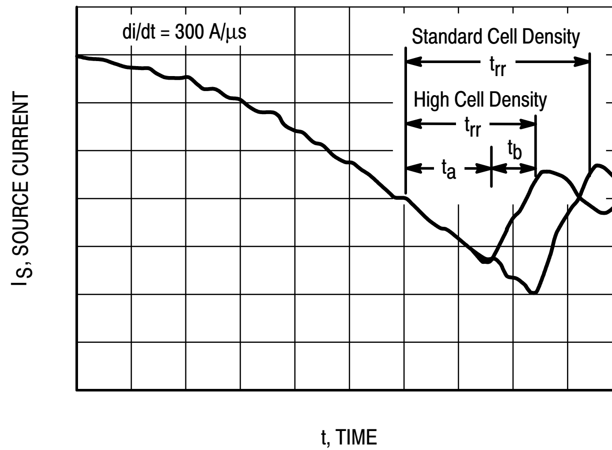



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

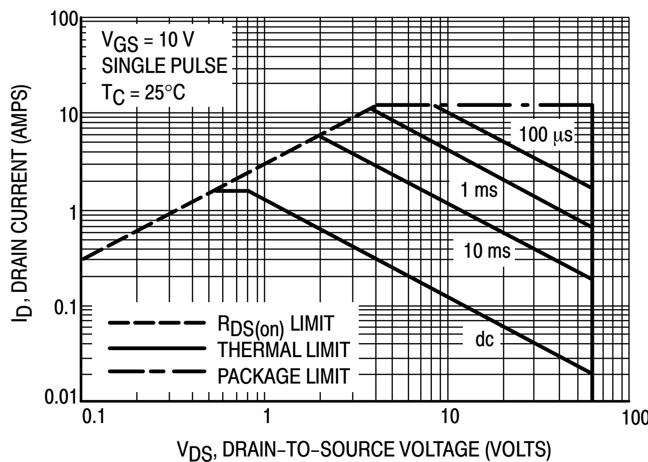
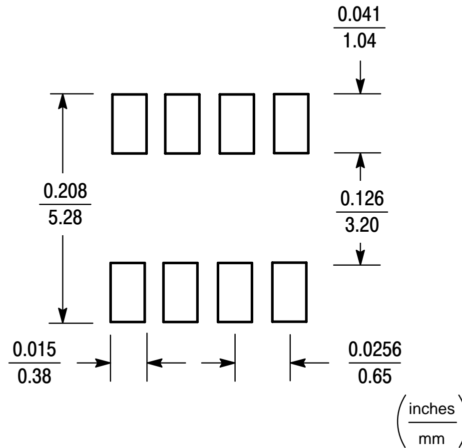



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 1.25 Watts.

$$P_D = \frac{150°C - 25°C}{100°C/W} = 1.25 \text{ Watts}$$

The 100°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.25 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 13 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

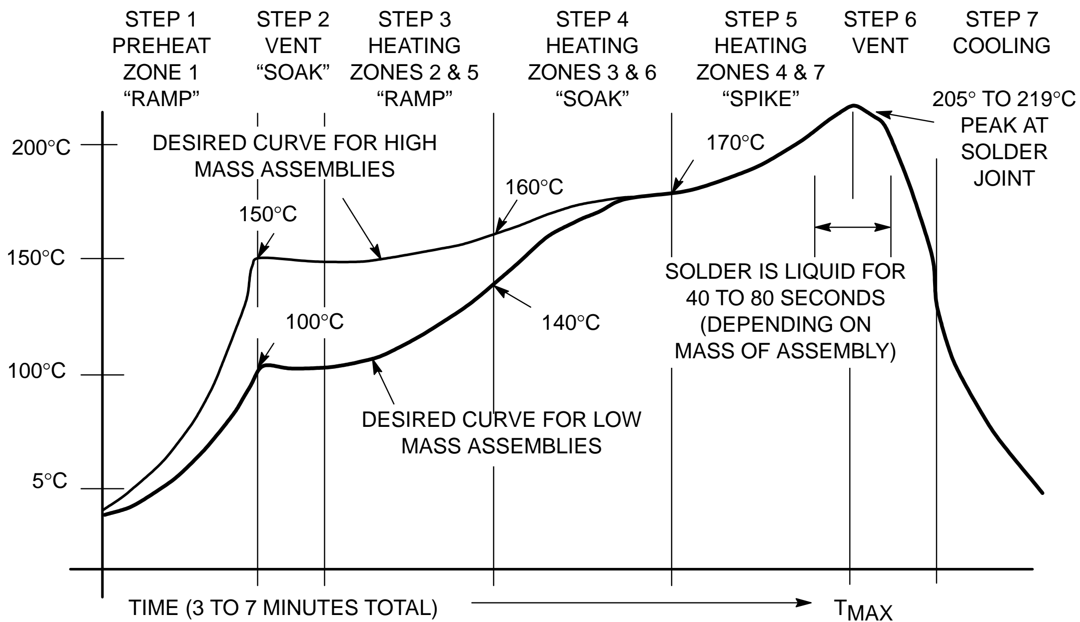



**Figure 13. Typical Solder Heating Profile**

# MTP10N10E

**Preferred Device**

# Power MOSFET 10 Amps, 100 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers drain–to–source diodes with fast recovery times. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical, and offer additional safety margin against unexpected voltage transients.

- Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor – Absorbs High Energy in the Avalanche Mode – Unclamped Inductive Switching (UIS) Energy Capability Specified at 100°C
- Commutating Safe Operating Area (CSOA) Specified for Use in Half and Full Bridge Circuits
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

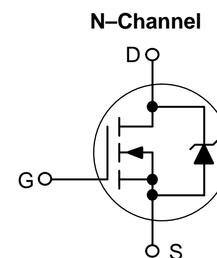
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–Source Voltage | $V_{GS}$ | ±20 | Vdc |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 10<br>25 | Adc |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 5 seconds | $T_L$ | 275 | °C |

**ON Semiconductor™**

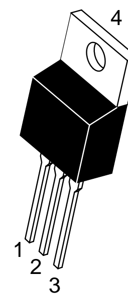
**http://onsemi.com**

**10 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 250 mΩ**

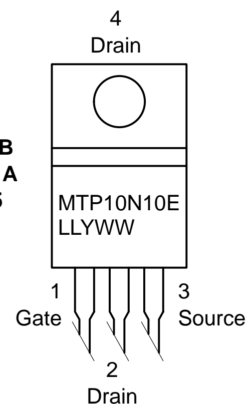
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP10N10E = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP10N10E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 0.25 mA) | | $V_{(BR)DSS}$ | 100 | – | Vdc |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | μA |
| ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0) | | | – | 10 | |
| ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $V_{GS}$ = 0, $T_J$ = 125°C) | | | – | 80 | |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | – | 100 | nAdc |
| Gate–Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSR}$ | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage | | $V_{GS(th)}$ | | | Vdc |
| ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | | | 2.0 | 4.5 | |
| $T_J$ = 100°C | | | 1.5 | 4.0 | |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 5.0 Adc) | | $R_{DS(on)}$ | – | 0.25 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 V) | | $V_{DS(on)}$ | | | Vdc |
| ($I_D$ = 10 Adc) | | | – | 2.7 | |
| ($I_D$ = 5.0 Adc, $T_J$ = 100°C) | | | – | 2.4 | |
| Forward Transconductance ($V_{DS}$ = 15 V, $I_D$ = 5.0 A) | | $g_{FS}$ | 4.0 | – | mhos |
| **DRAIN–TO–SOURCE AVALANCHE CHARACTERISTICS** | | | | | |
| Unclamped Drain–to–Source Avalanche Energy See Figures 14 and 15 | | $W_{DSR}$ | | | mJ |
| ($I_D$ = 25 A, $V_{DD}$ = 25 V, $T_C$ = 25°C, Single Pulse, Non–repetitive) | | | – | 60 | |
| ($I_D$ = 10 A, $V_{DD}$ = 25 V, $T_C$ = 25°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) | | | – | 100 | |
| ($I_D$ = 4.0 A, $V_{DD}$ = 25 V, $T_C$ = 100°C, P.W. ≤ 200 μs, Duty Cycle ≤ 1%) | | | – | 40 | |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) See Figure 16 | $C_{iss}$ | – | 600 | pF |
| Output Capacitance | | $C_{oss}$ | – | 400 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 1.) ($T_J$ = 100°C) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 5.0 A, $R_G$ = 50 Ω) See Figure 9 | $t_{d(on)}$ | – | 50 | ns |
| Rise Time | | $t_r$ | – | 80 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 100 | |
| Fall Time | | $t_f$ | – | 80 | |
| Total Gate Charge | ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $I_D$ = Rated $I_D$, $V_{GS}$ = 10 V) See Figures 17 and 18 | $Q_g$ | 15 (Typ) | 30 | nC |
| Gate–Source Charge | | $Q_{gs}$ | 8.0 (Typ) | – | |
| Gate–Drain Charge | | $Q_{gd}$ | 7.0 (Typ) | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** (Note 1.) | | | | | |
| Forward On–Voltage | ($I_S$ = Rated $I_D$ $V_{GS}$ = 0) | $V_{SD}$ | 1.4 (Typ) | 1.7 | Vdc |
| Forward Turn–On Time | | $t_{on}$ | Limited by stray inductance | | |
| Reverse Recovery Time | | $t_{rr}$ | 70 (Typ) | – | ns |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance | | $L_d$ | | | nH |
| (Measured from the contact screw on tab to center of die) | | | 3.5 (Typ) | – | |
| (Measured from the drain lead 0.25″ from package to center of die) | | | 4.5 (Typ) | – | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_s$ | 7.5 (Typ) | – | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

## TYPICAL ELECTRICAL CHARACTERISTICS

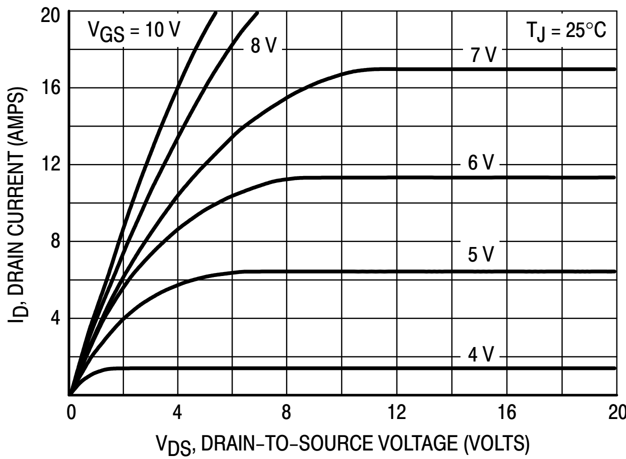


**Figure 1. On–Region Characteristics**

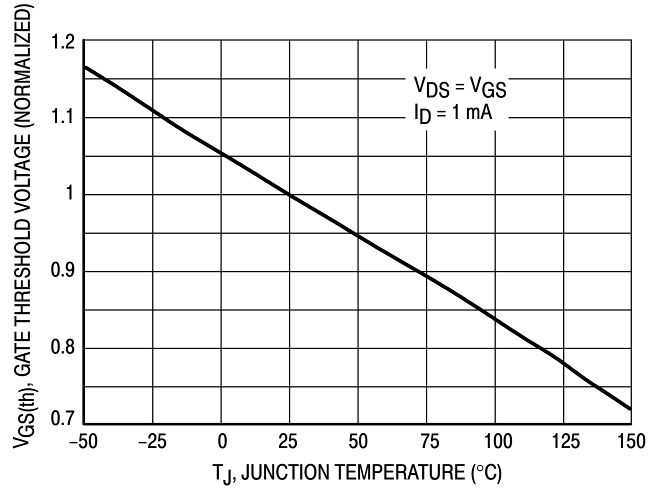


**Figure 2. Gate–Threshold Voltage Variation With Temperature**

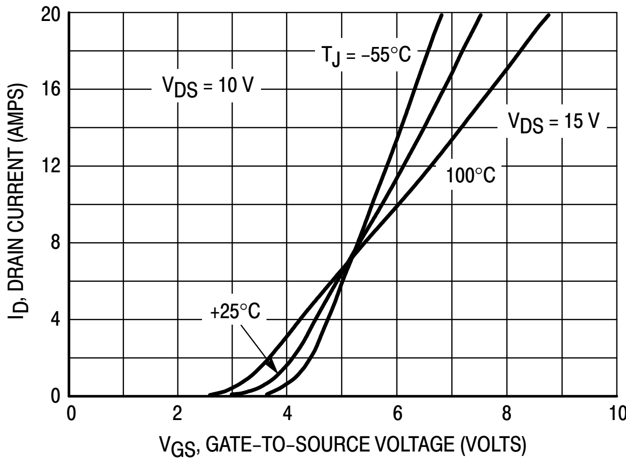


**Figure 3. Transfer Characteristics**

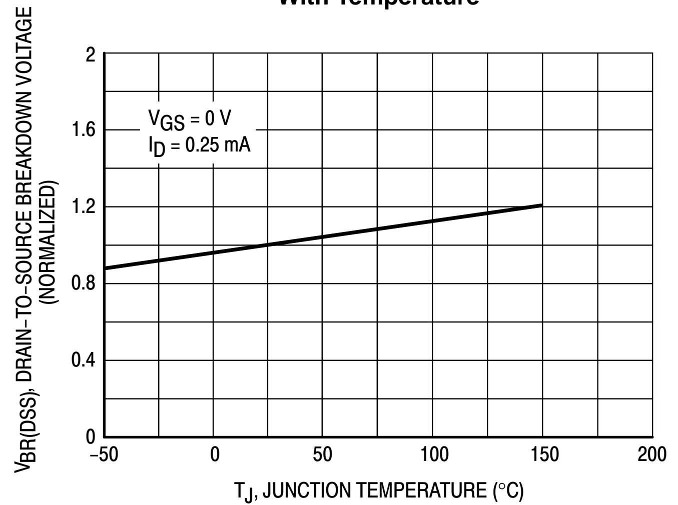


**Figure 4. Breakdown Voltage Variation With Temperature**

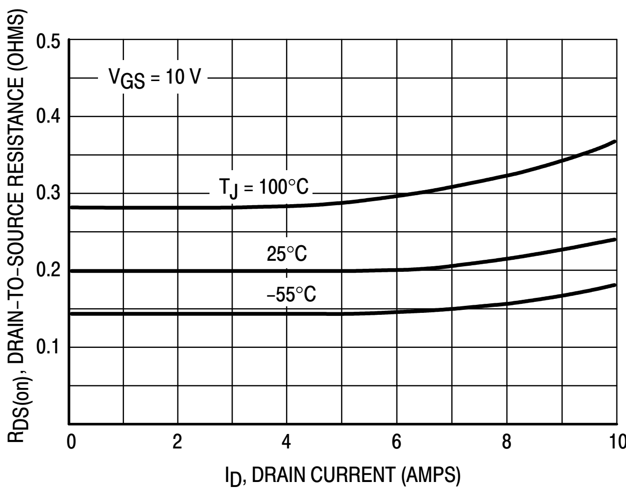


**Figure 5. On–Resistance versus Drain Current**

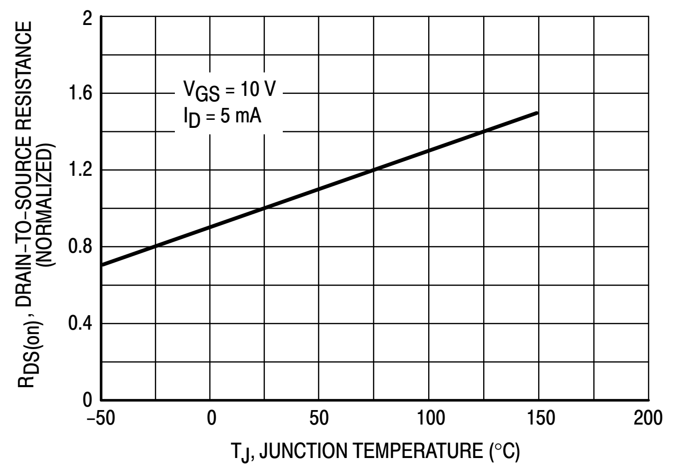


**Figure 6. On–Resistance Variation With Temperature**

## SAFE OPERATING AREA INFORMATION

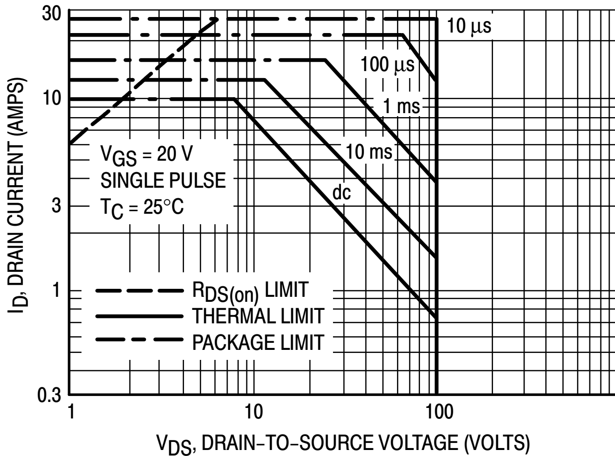


**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

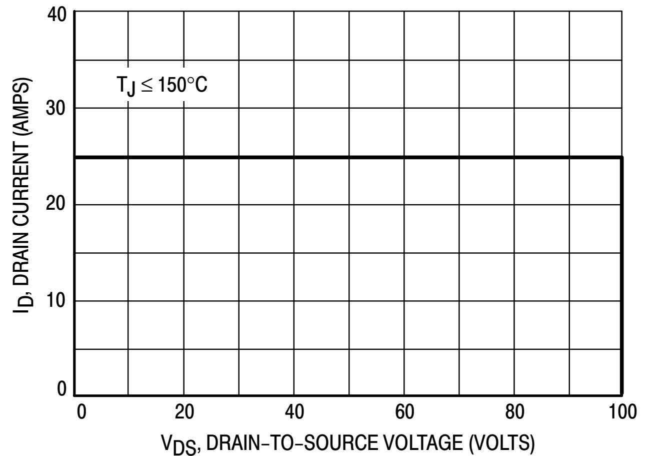


**Figure 8. Maximum Rated Switching Safe Operating Area**

## FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, “Transient Thermal Resistance–General Data and Its Use” provides detailed instructions.

## SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

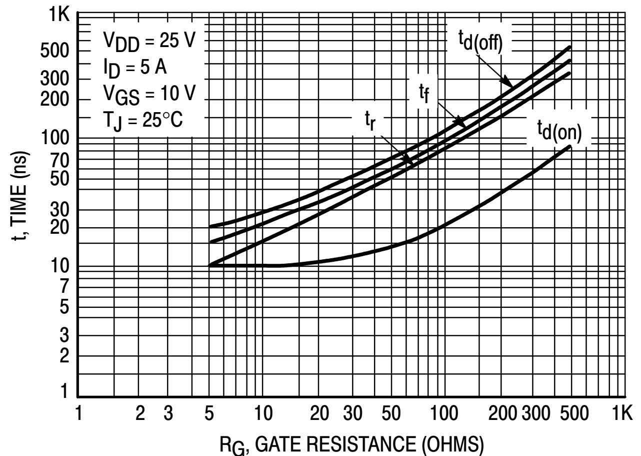


**Figure 9. Resistive Switching Time versus Gate Resistance**

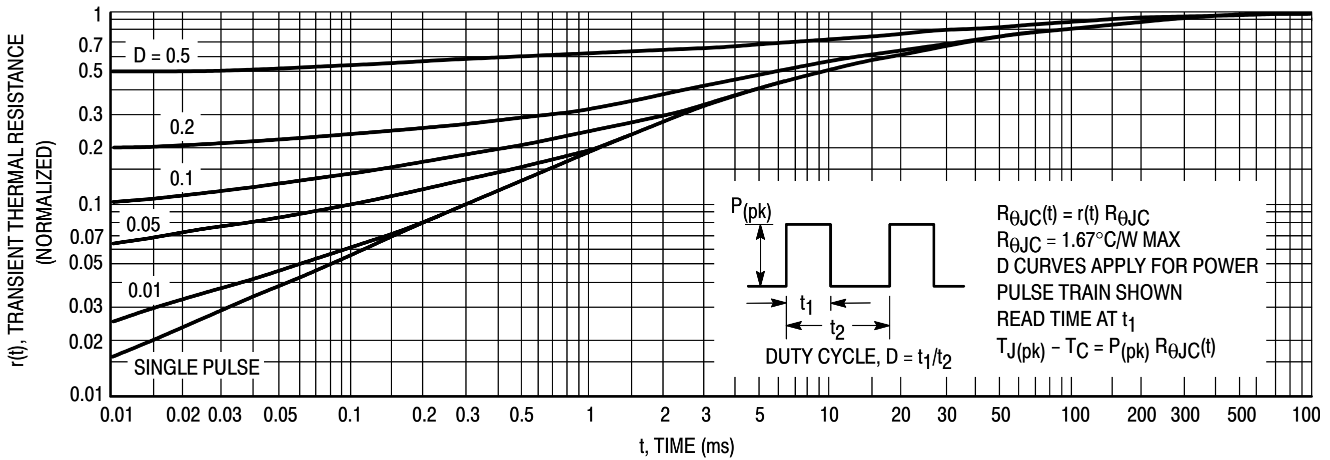


**Figure 10. Thermal Response**

## COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of $I_{FM}$ and peak $V_{DS}$ for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increase with increasing rate of change of source current so $dI_S/dt$ is specified with a maximum value. Higher values of $dI_S/dt$ require an appropriate derating of $I_{FM}$, peak $V_{DS}$ or both. Ultimately $dI_S/dt$ is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during $t_{rr}$ as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain–to–source voltage that the device must sustain during commutation; $I_{FM}$ is the maximum forward source-drain diode current just prior to the onset of commutation.

$V_R$ is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as $I_S$ decays from $I_{RM}$ to zero.

$R_{GS}$ should be minimized during commutation. $T_J$ has only a second order effect on CSOA.

Stray inductances in ON Semiconductor's test circuit are assumed to be practical minimums. $dV_{DS}/dt$ in excess of 10 V/ns was attained with $dI_S/dt$ of 400 A/μs.

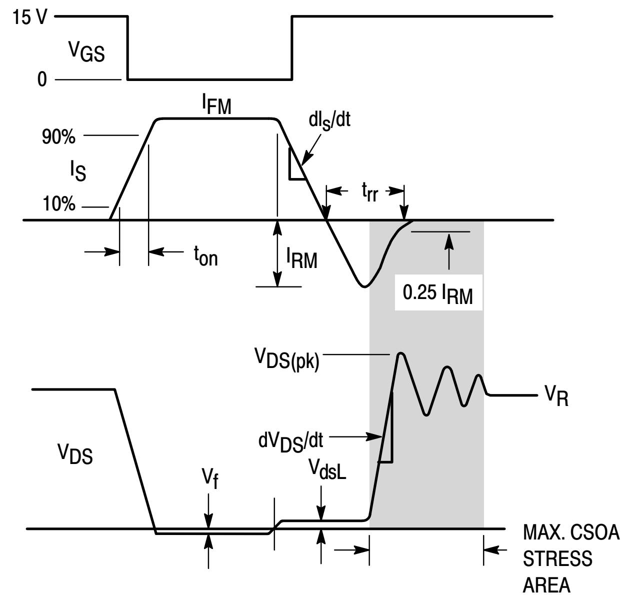


**Figure 11. Commutating Waveforms**

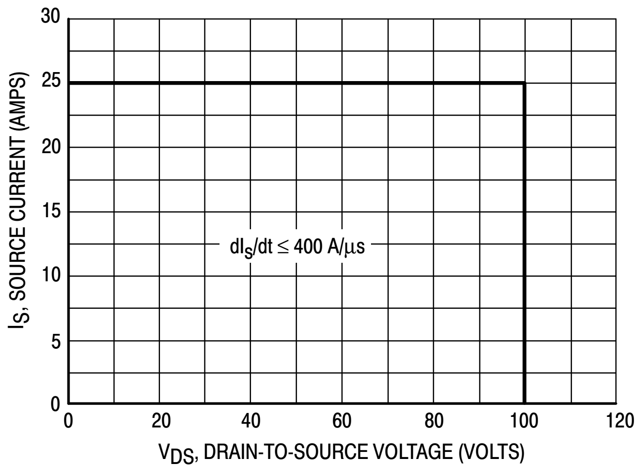


Figure 12. Commutating Safe Operating Area (CSOA)

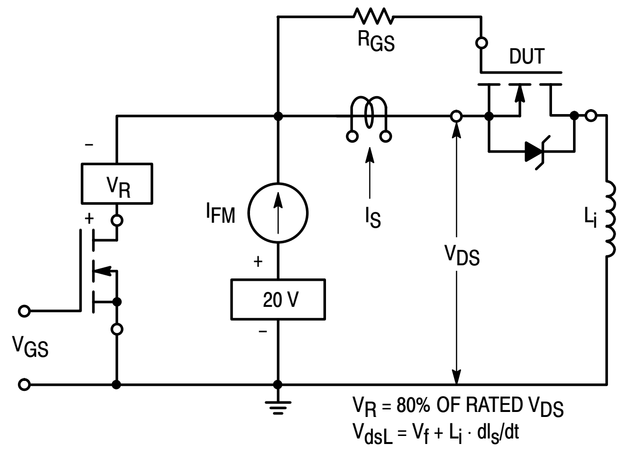


Figure 13. Commutating Safe Operating Area Test Circuit

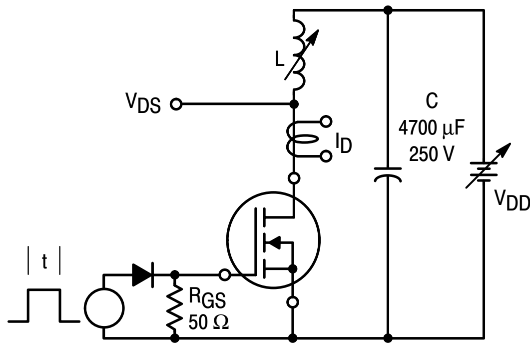


Figure 14. Unclamped Inductive Switching Test Circuit

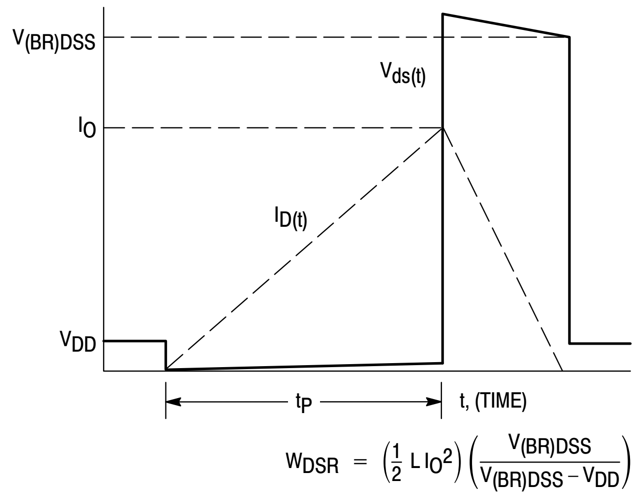


Figure 15. Unclamped Inductive Switching Waveforms

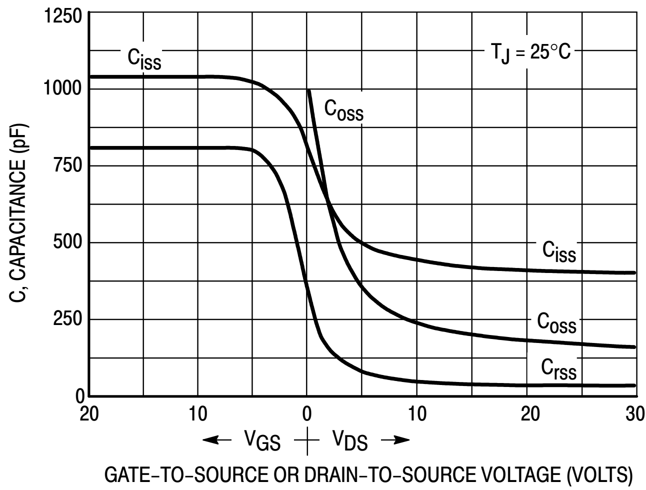


**Figure 16. Capacitance Variation**

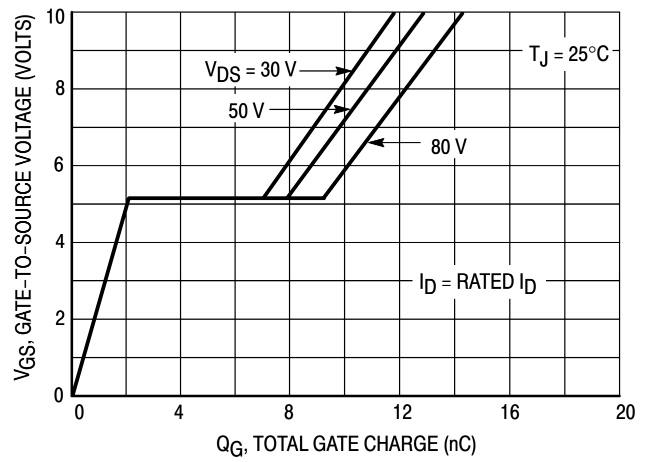


**Figure 17. Gate Charge versus Gate–To–Source Voltage**

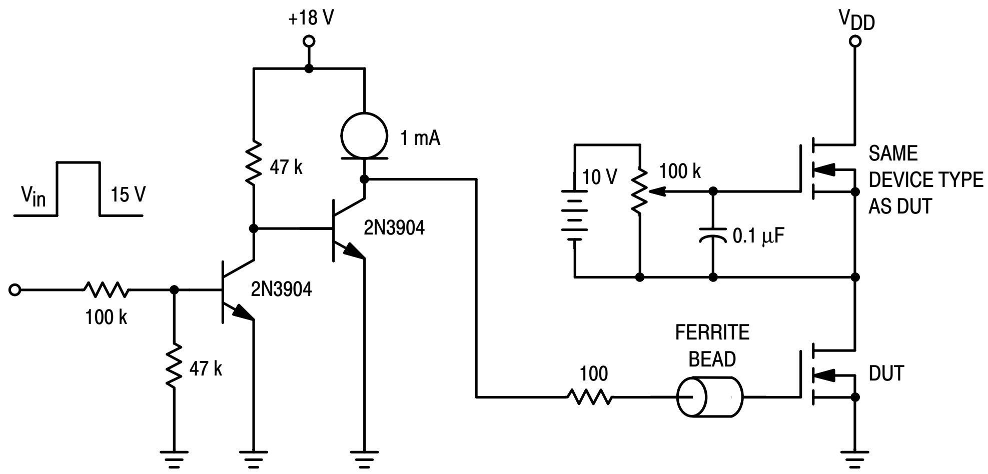


**Figure 18. Gate Charge Test Circuit**

# MTP10N10EL

**Preferred Device**

# Power MOSFET 10 Amps, 100 Volts, Logic Level

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>±20 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous @ $T_C$ = 25°C<br>– Continuous @ $T_C$ = 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>10<br>6.0<br>35 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C<br>Total Power Dissipation @ $T_C$ = 25°C (Note 1.) | $P_D$ | 40<br>0.32<br>1.75 | Watts<br>W/°C<br>Watts |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 10 Adc, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 50 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient<br>– Junction to Ambient (Note 1.) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>3.13<br>100<br>71.4 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

1. When surface mounted to an FR4 board using the minimum recommended pad size.

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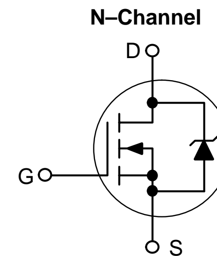
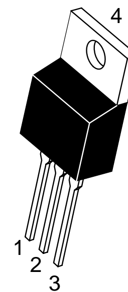
**10 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 22 mΩ**

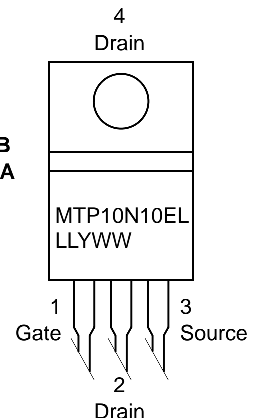
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




MTP10N10EL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP10N10EL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 100 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 115 | – | mV/°C |
| Zero Gate Voltage Drain Current | | $I_{DSS}$ | | | | μAdc |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | | | – | – | 10 | |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.45 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 5.0 Adc) | | $R_{DS(on)}$ | – | 0.17 | 0.22 | Ohm |
| Drain–to–Source On–Voltage | | $V_{DS(on)}$ | | | | Vdc |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 10 Adc) | | | – | 1.85 | 2.6 | |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 5.0 Adc, $T_J$ = 125°C) | | | – | – | 2.3 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 5.0 Adc) | | $g_{FS}$ | 5.0 | 7.9 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 741 | 1040 | pF |
| Output Capacitance | | $C_{oss}$ | – | 175 | 250 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 18.9 | 40 | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 50 Vdc, $I_D$ = 10 Adc, $V_{GS}$ = 5.0 Vdc, $R_g$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 74 | 150 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 30 | |
| Fall Time | | $t_f$ | – | 38 | 80 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 10 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 9.3 | 15 | nC |
| | | $Q_1$ | – | 2.56 | | |
| | | $Q_2$ | – | 4.4 | – | |
| | | $Q_3$ | – | 4.6 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 2.) | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.98 | 1.6 | Vdc |
| | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.898 | – | |
| Reverse Recovery Time | ($I_S$ = 10 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 124.7 | – | ns |
| | | $t_a$ | – | 86 | – | |
| | | $t_b$ | – | 38.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.539 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_d$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad.) | | $L_s$ | – | 7.5 | – | |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
3. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

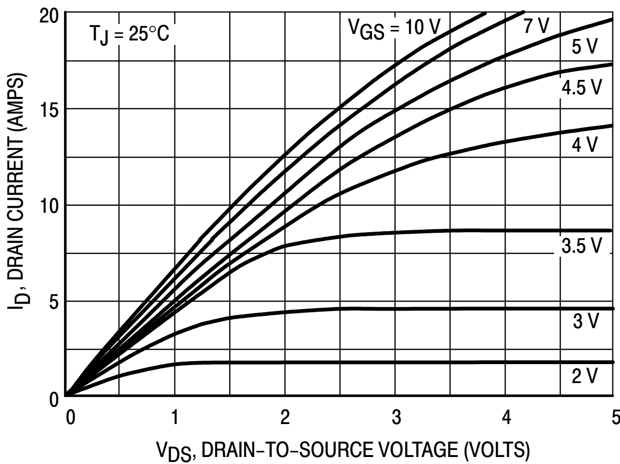



**Figure 1. On–Region Characteristics**

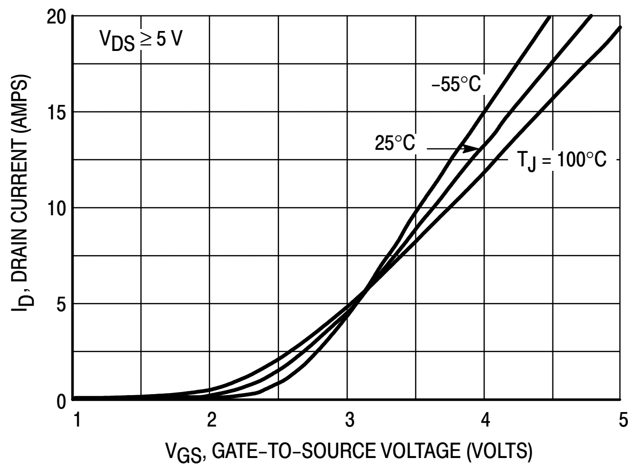



**Figure 2. Transfer Characteristics**

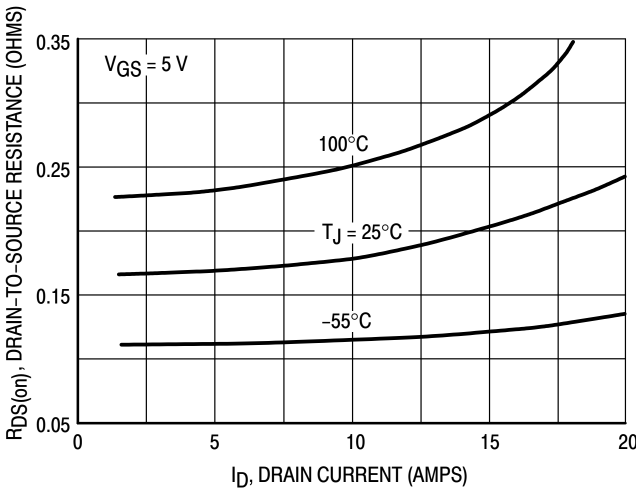



**Figure 3. On–Resistance versus Drain Current and Temperature**

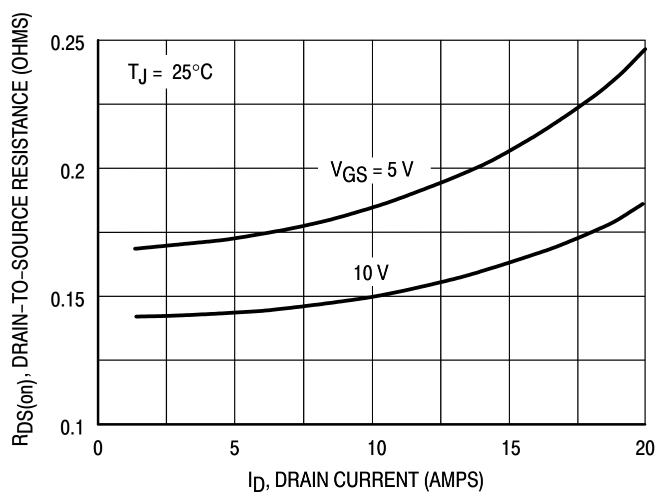



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

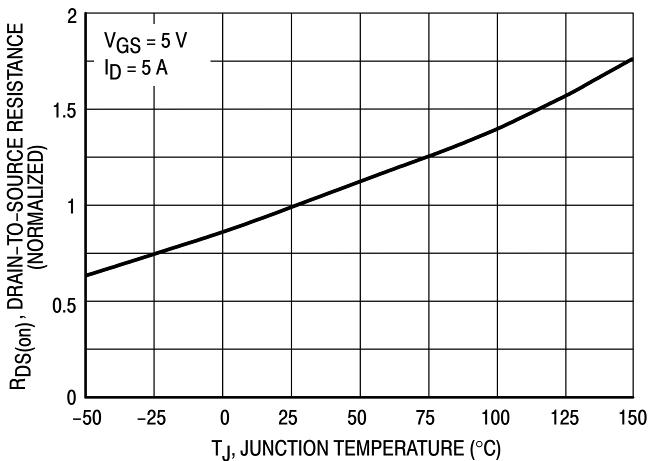



**Figure 5. On–Resistance Variation with Temperature**

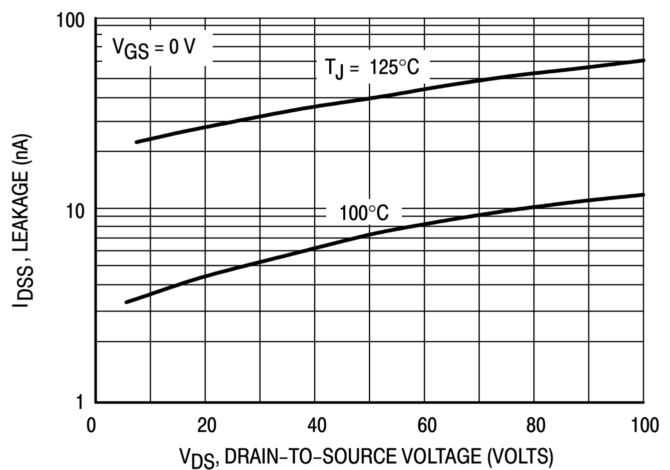



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

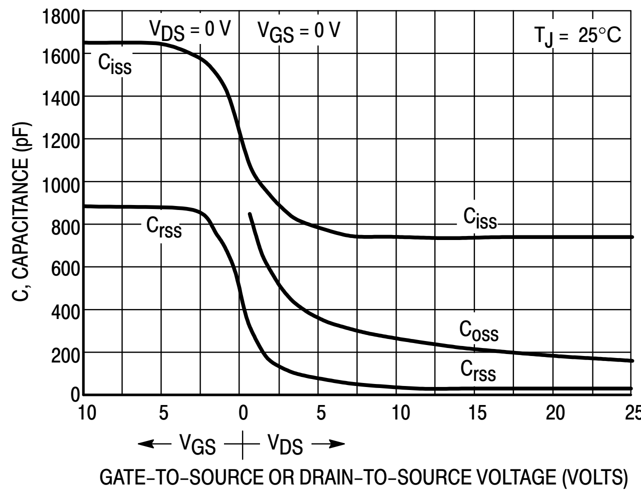



**Figure 7. Capacitance Variation**

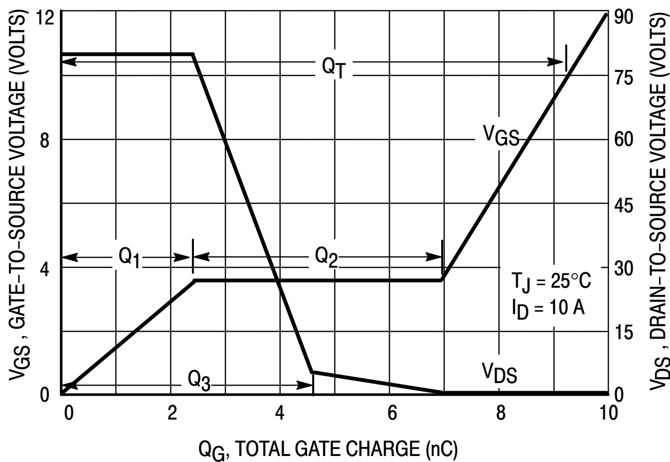



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

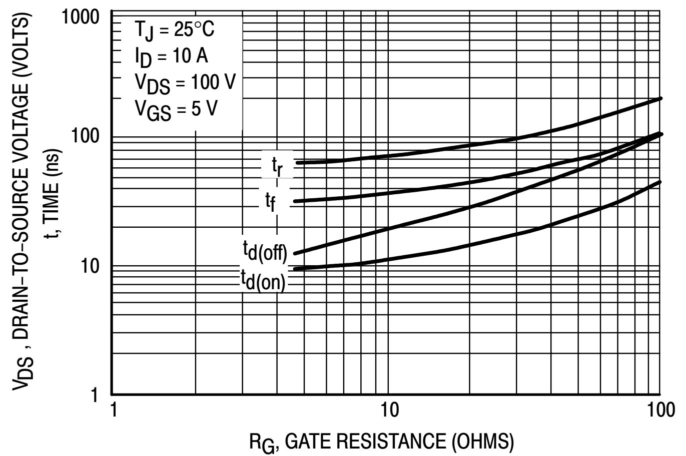



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

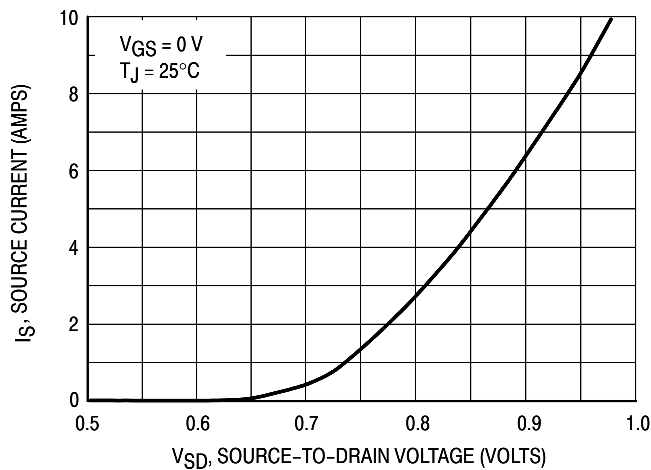



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

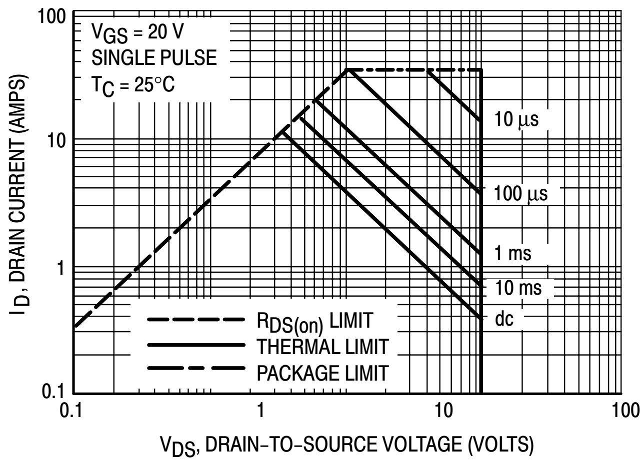



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

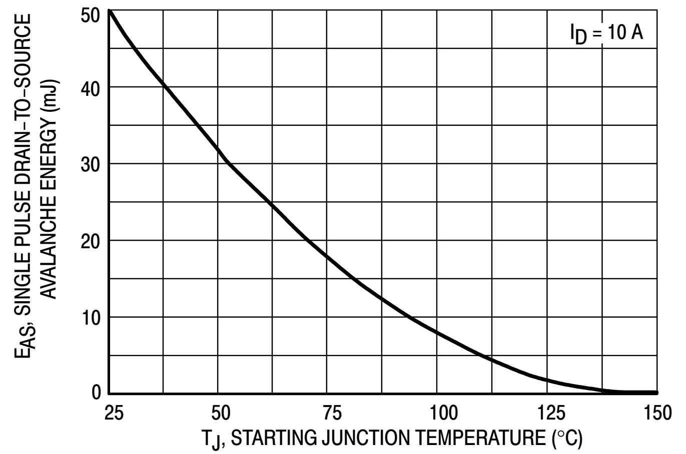



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

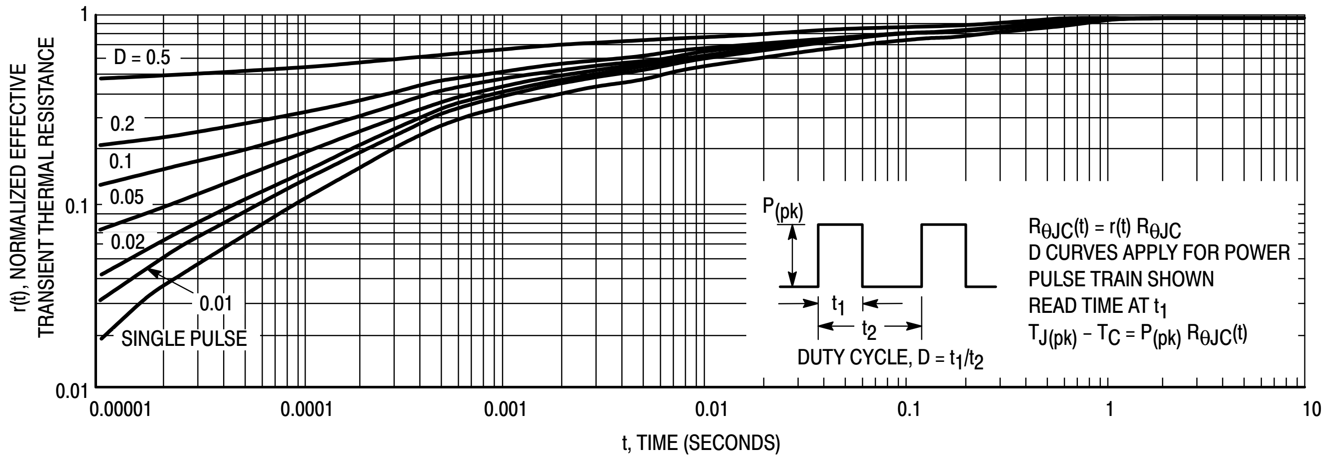



**Figure 13. Thermal Response**

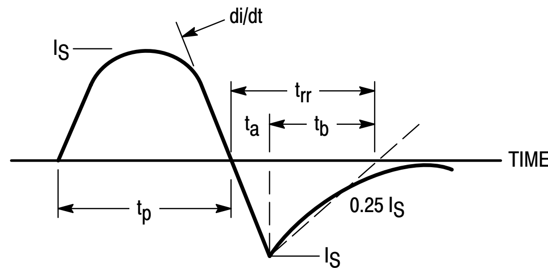



**Figure 14. Diode Reverse Recovery Waveform**

# MTP12P10

**Preferred Device**

# Power MOSFET 12 Amps, 100 Volts

## P–Channel TO–220

**ON Semiconductor™**

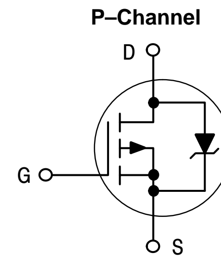
**http://onsemi.com**

This Power MOSFET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds – Switching Times Specified at 100°C
- Designer's Data – $I_{DSS}$, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged – SOA is Power Dissipation Limited
- Source–to–Drain Diode Characterized for Use With Inductive Loads

**12 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 300 mΩ**

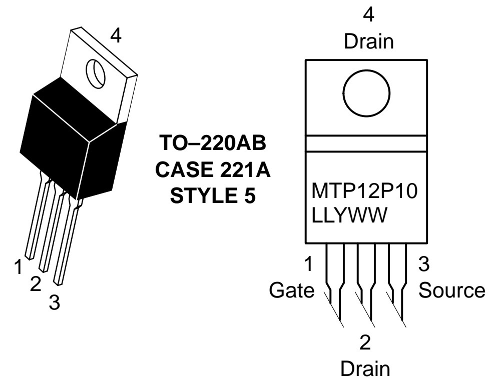
**P–Channel**




**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–Source Voltage – Continuous<br>– Non–repetitive ($t_p$ ≤ 50 μs) | $V_{GS}$<br>$V_{GSM}$ | ±20<br>±40 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Pulsed | $I_D$<br>$I_{DM}$ | 12<br>28 | Adc |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –65 to 150 | °C |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTP12P10 | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP12P10 | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 0.25 mA) | | $V_{(BR)DSS}$ | 100 | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0) ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | – | 100 | nAdc |
| Gate–Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSR}$ | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) $T_J$ = 100°C | | $V_{GS(th)}$ | 2.0<br>1.5 | 4.5<br>4.0 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.3 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 V) ($I_D$ = 12 Adc) ($I_D$ = 6.0 Adc, $T_J$ = 100°C) | | $V_{DS(on)}$ | –<br>– | 4.2<br>3.8 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 V, $I_D$ = 6.0 A) | | $g_{FS}$ | 2.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) See Figure 10 | $C_{iss}$ | – | 920 | pF |
| Output Capacitance | | $C_{oss}$ | – | 575 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 200 | |
| **SWITCHING CHARACTERISTICS** (Note 1.) ($T_J$ = 100°C) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 0.5 Rated $I_D$, $R_G$ = 50 Ω) See Figures 12 and 13 | $t_{d(on)}$ | – | 50 | ns |
| Rise Time | | $t_r$ | – | 150 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 150 | |
| Fall Time | | $t_f$ | – | 150 | |
| Total Gate Charge | ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $I_D$ = Rated $I_D$, $V_{GS}$ = 10 V) See Figure 11 | $Q_g$ | 33 (Typ) | 50 | nC |
| Gate–Source Charge | | $Q_{gs}$ | 16 (Typ) | – | |
| Gate–Drain Charge | | $Q_{gd}$ | 17 (Typ) | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** (Note 1.) | | | | | |
| Forward On–Voltage | ($I_S$ = Rated $I_D$, $V_{GS}$ = 0) | $V_{SD}$ | 4.0 (Typ) | 5.5 | Vdc |
| Forward Turn–On Time | | $t_{on}$ | Limited by stray inductance | | |
| Reverse Recovery Time | | $t_{rr}$ | 300 (Typ) | – | ns |
| **INTERNAL PACKAGE INDUCTANCE (TO–204)** | | | | | |
| Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and the center of the die) | | $L_d$ | 5.0 (Typ) | – | nH |
| Internal Source Inductance (Measured from the source pin, 0.25″ from the package to the source bond pad) | | $L_s$ | 12.5 (Typ) | – | |
| **INTERNAL PACKAGE INDUCTANCE (TO–220)** | | | | | |
| Internal Drain Inductance (Measured from the contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die) | | $L_d$ | 3.5 (Typ)<br>4.5 (Typ) | –<br>– | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_s$ | 7.5 (Typ) | – | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.

## TYPICAL ELECTRICAL CHARACTERISTICS

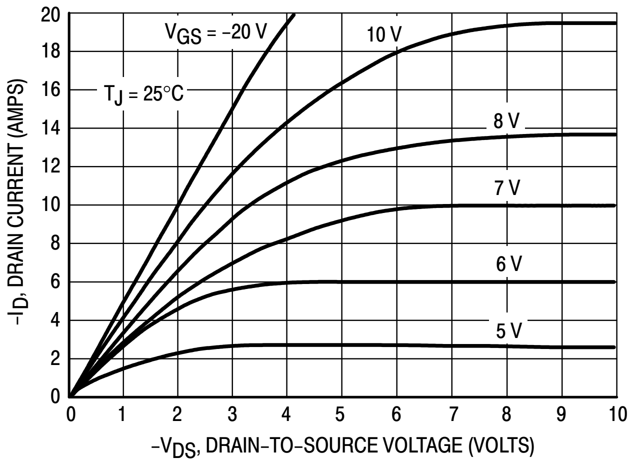



**Figure 1. On−Region Characteristics**

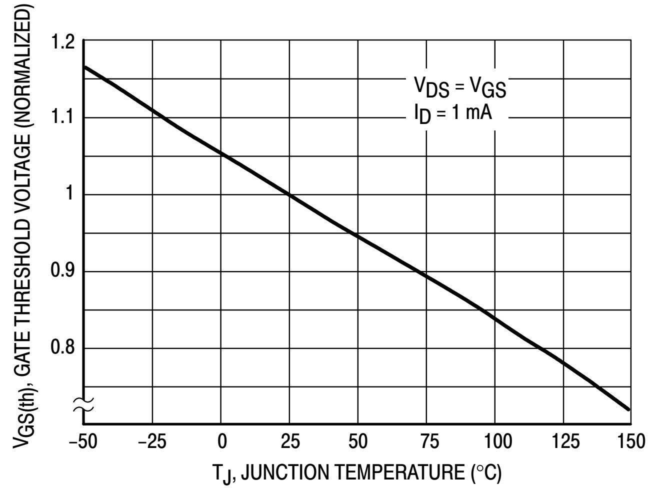



**Figure 2. Gate−Threshold Voltage Variation With Temperature**

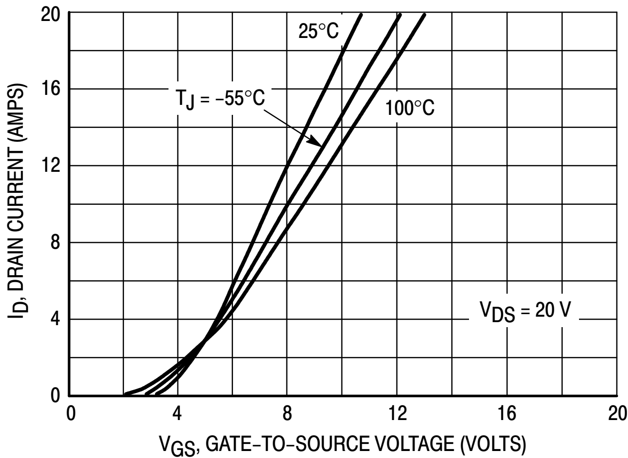



**Figure 3. Transfer Characteristics**

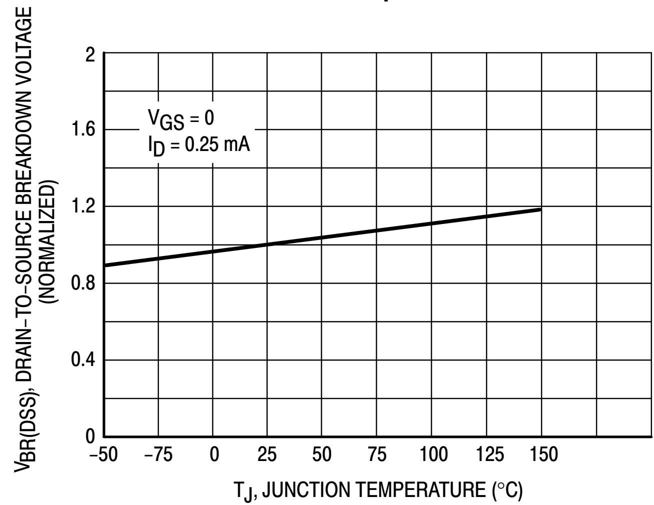



**Figure 4. Normalized Breakdown Voltage versus Temperature**

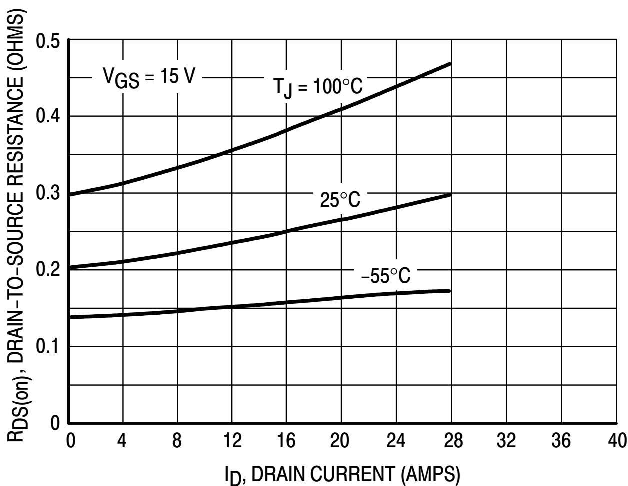



**Figure 5. On−Resistance versus Drain Current**

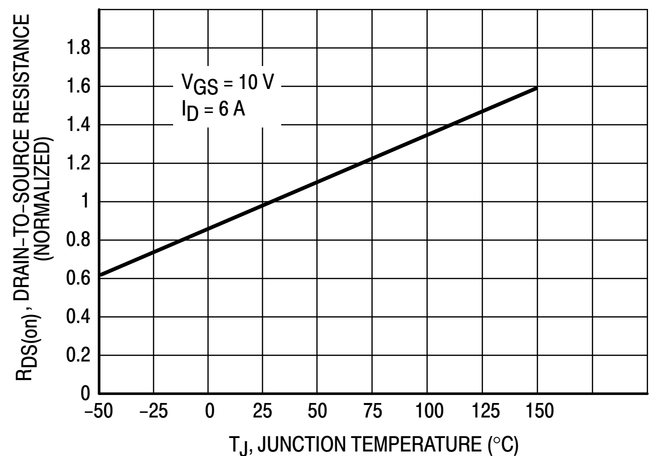



**Figure 6. On−Resistance Variation With Temperature**

## SAFE OPERATING AREA INFORMATION

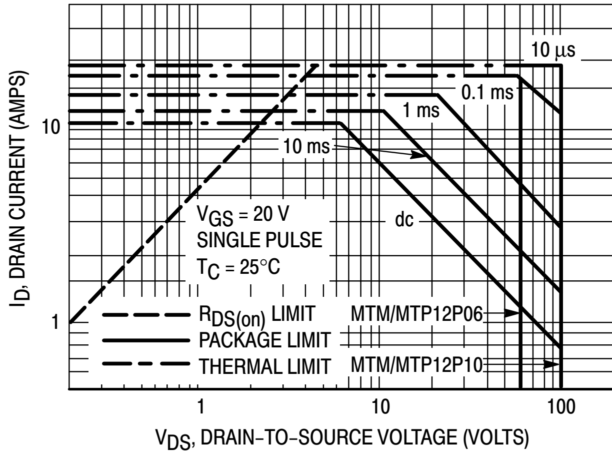



**Figure 7. Maximum Rated Forward Biased Safe Operating Area**

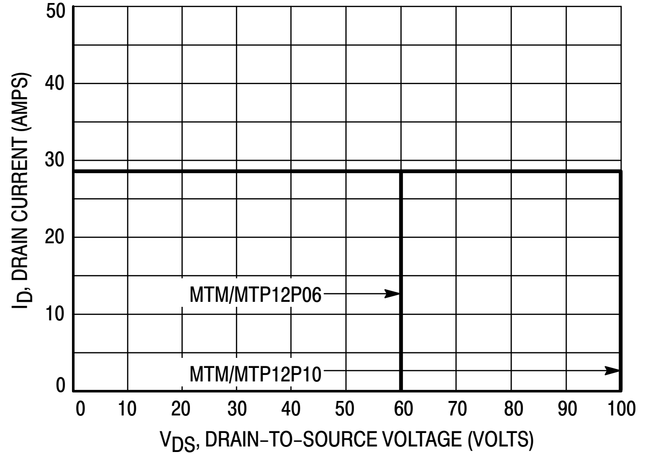



**Figure 8. Maximum Rated Switching Safe Operating Area**

### FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain–to–source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. ON Semiconductor Application Note, AN569, "Transient Thermal Resistance–General Data and Its Use" provides detailed instructions.

### SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn–on and turn–off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

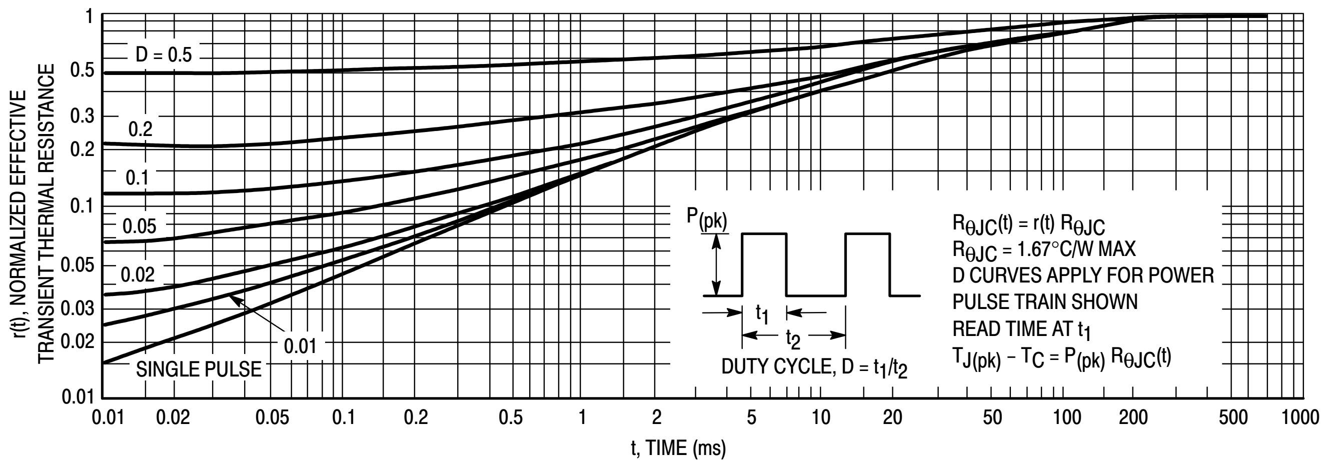



**Figure 9. Thermal Response**

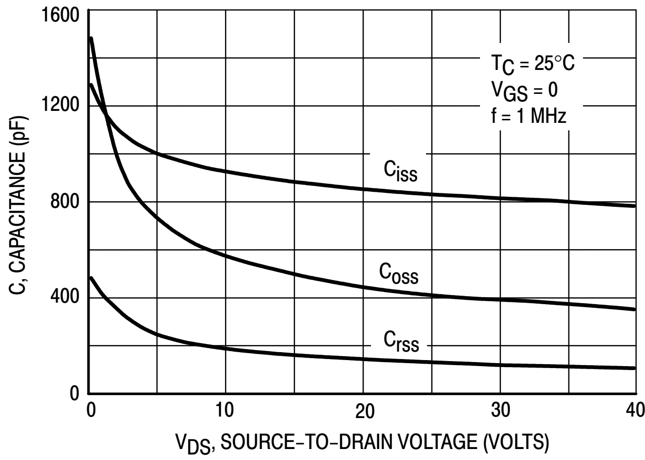



**Figure 10. Capacitance Variation**

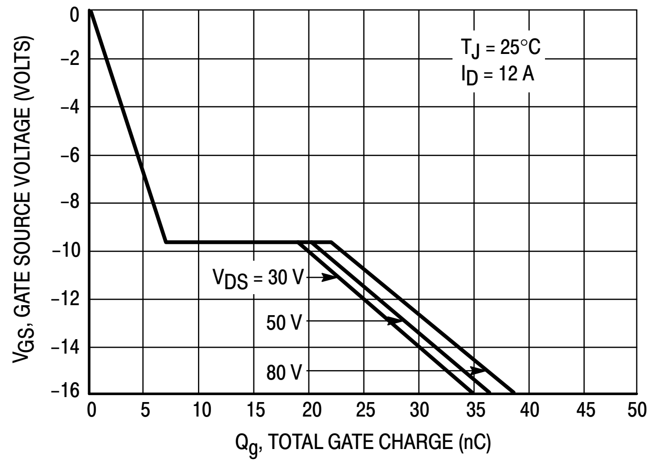



**Figure 11. Gate Charge versus Gate–To–Source Voltage**

## RESISTIVE SWITCHING

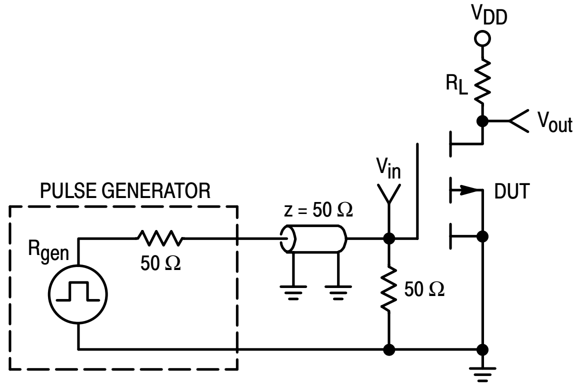



**Figure 12. Switching Test Circuit**

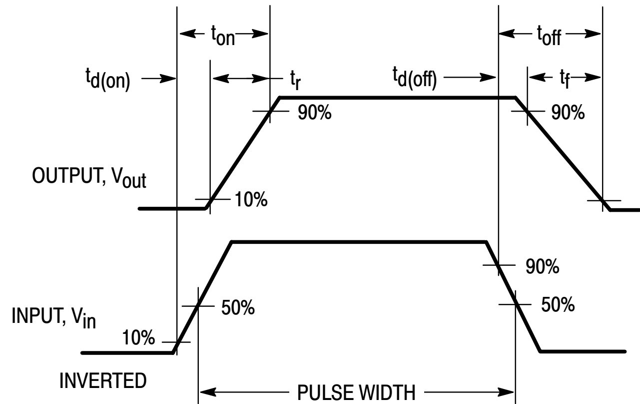



**Figure 13. Switching Waveforms**

# MTP1302

**Preferred Device**

# Power MOSFET 42 Amps, 30 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode Is Characterized for Use In Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

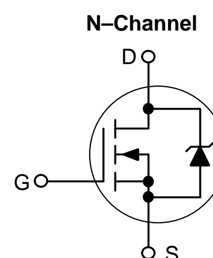
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive (tp ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 42<br>20<br>126 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 74<br>0.592 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 42 Apk, L = 0.25 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 220 | mJ |
| Thermal Resistance<br>Junction to Case<br>Junction–to–Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

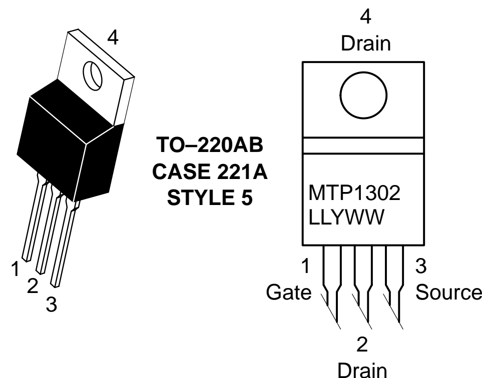
**http://onsemi.com**

**42 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 22 mΩ**

**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTP1302 | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP1302 | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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November, 2000 – Rev. 1
Publication Order Number:
MTP1302/D

**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 5.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 42 Adc) | | $R_{DS(on)}$ | –<br>–<br>– | 19<br>26<br>19.5 | 22<br>29<br>– | mΩ |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc, $T_J$ = 150°C)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 42 Adc) | | $V_{DS(on)}$ | –<br>–<br>– | 0.38<br>–<br>0.82 | 0.5<br>0.33<br>– | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 10 | 16 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 755 | 1162 | pF |
| Output Capacitance | | $C_{oss}$ | – | 370 | 518 | |
| Transfer Capacitance | | $C_{rss}$ | – | 102 | 204 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.2 | 15 | ns |
| Rise Time | | $t_r$ | – | 52 | 104 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 45 | 90 | |
| Fall Time | | $t_f$ | – | 73 | 146 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 14.5 | 21.8 | nC |
| | | $Q_1$ | – | 2.2 | – | |
| | | $Q_2$ | – | 8.8 | – | |
| | | $Q_3$ | – | 6.8 | – | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 27 | 40.5 | nC |
| | | $Q_1$ | – | 2.2 | – | |
| | | $Q_2$ | – | 10 | – | |
| | | $Q_3$ | – | 7.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 0.83<br>0.79 | 1.1<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 38 | – | ns |
| | | $t_a$ | – | 19 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 36 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

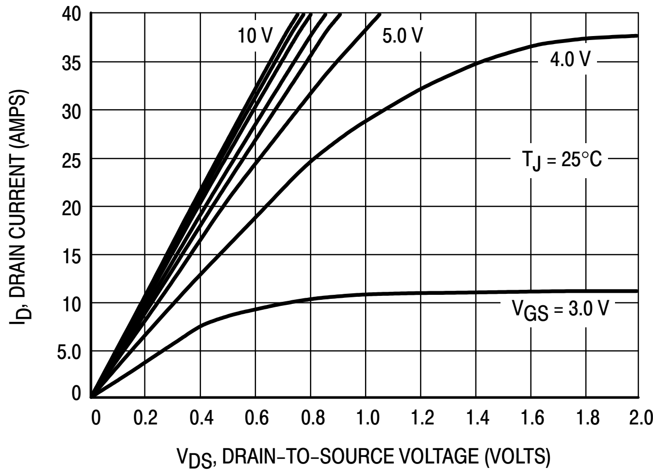



**Figure 1. On–Region Characteristics**

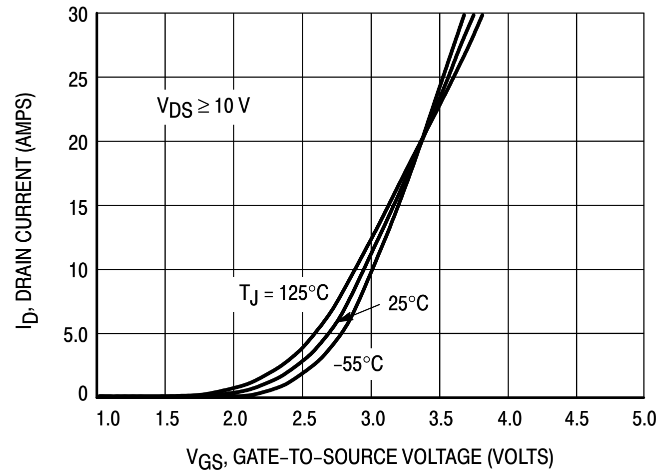



**Figure 2. Transfer Characteristics**

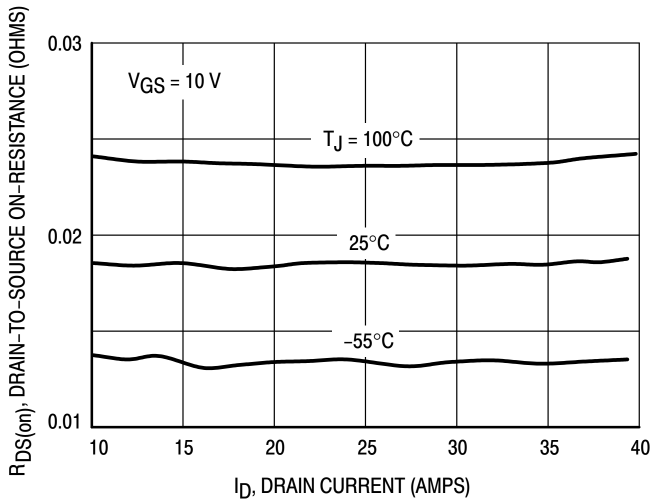



**Figure 3. On–Resistance versus Drain Current and Temperature**

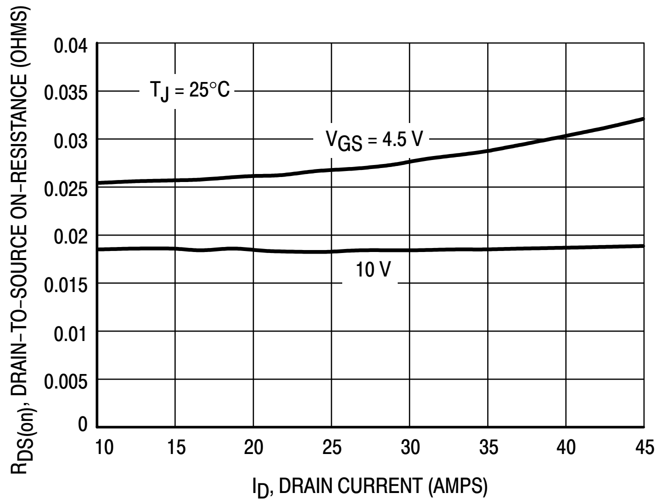



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

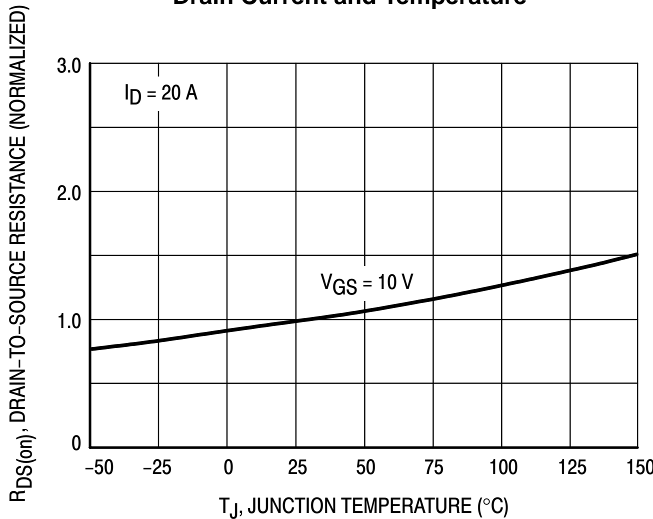



**Figure 5. On–Resistance Variation with Temperature**

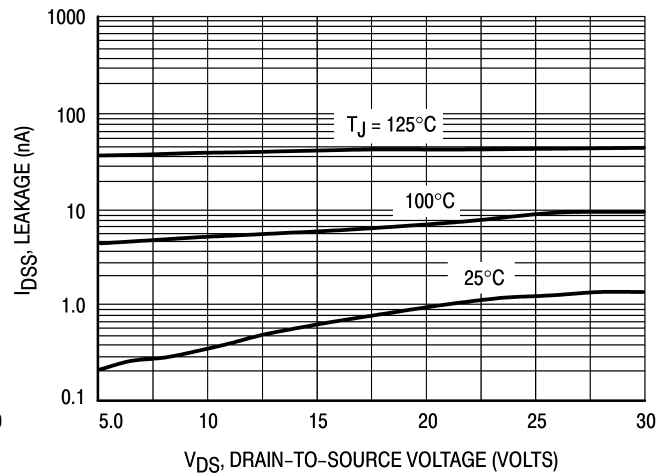



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

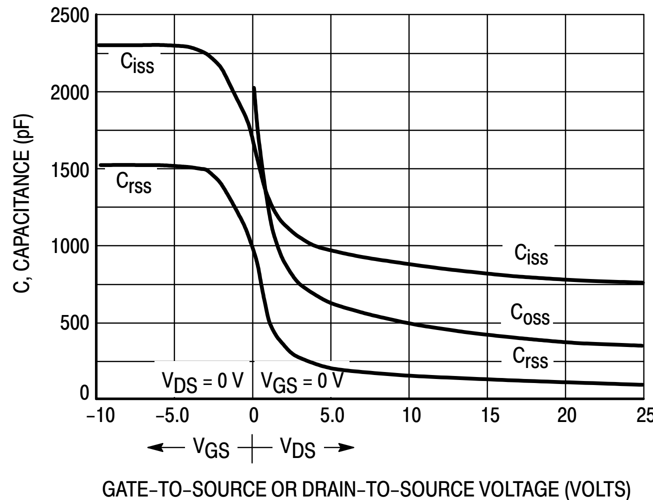



**Figure 7. Capacitance Variation**

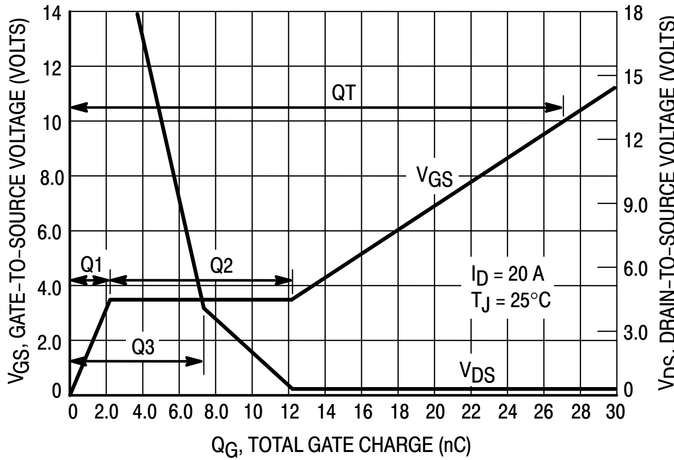



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

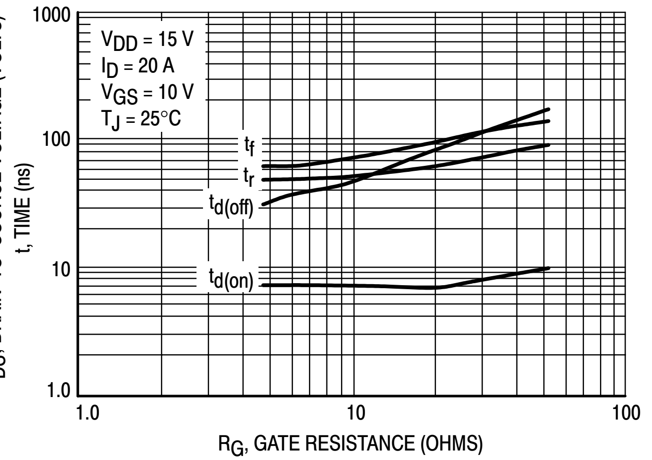



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

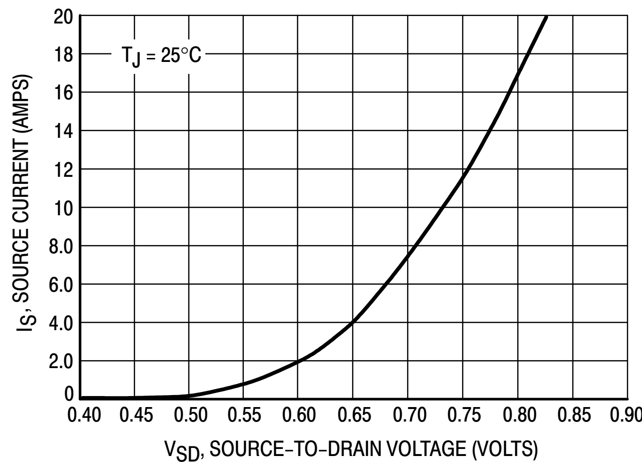



**Figure 10. Diode Forward Voltage versus Current**

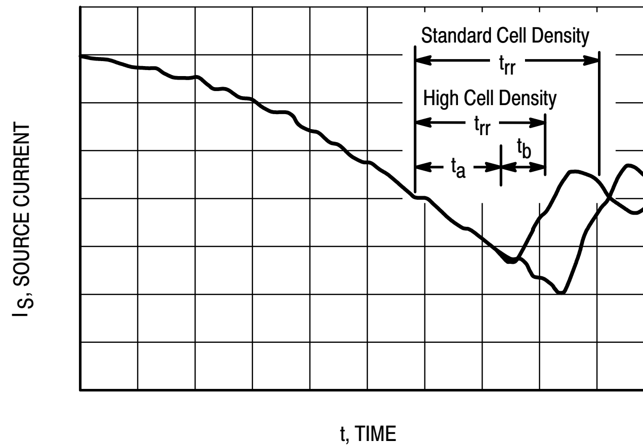



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

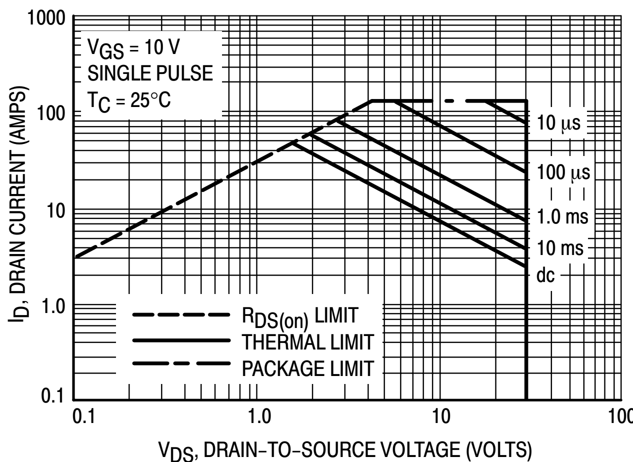



Figure 12. Maximum Rated Forward Biased Safe Operating Area

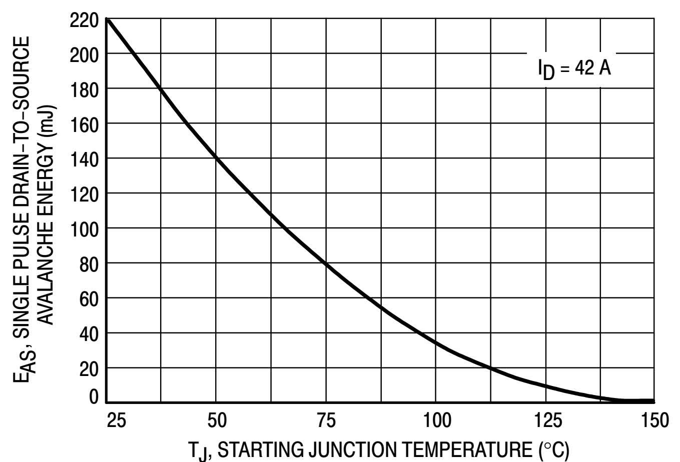



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

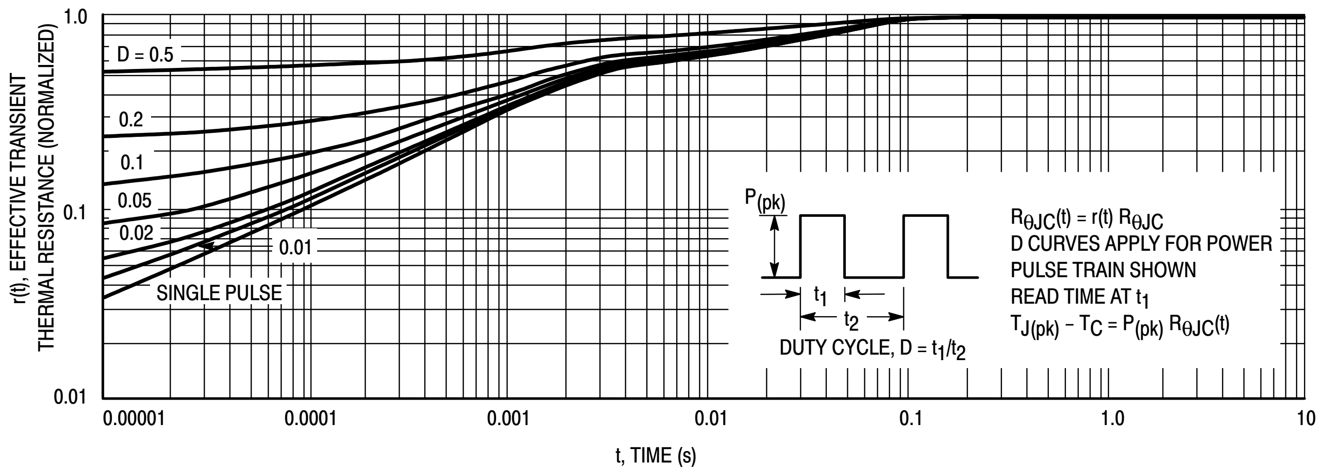



**Figure 14. Thermal Response**

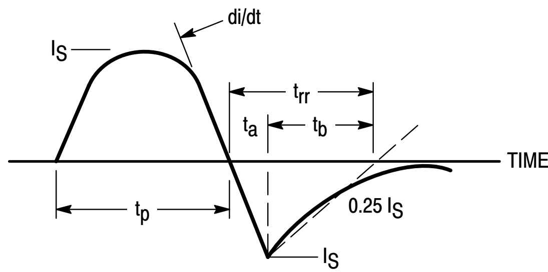



**Figure 15. Diode Reverse Recovery Waveform**

# MTP1306

Preferred Device

# Power MOSFET 75 Amps, 30 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating area are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

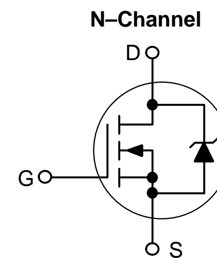
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±20 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>75<br>59<br>225 | <br>Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1.2 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 75 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 280 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient | <br>$R_{θJC}$<br>$R_{θJA}$ | <br>0.8<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 5.0 seconds | $T_L$ | 260 | °C |

ON Semiconductor™

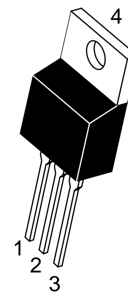
http://onsemi.com

**75 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 6.5 mΩ**

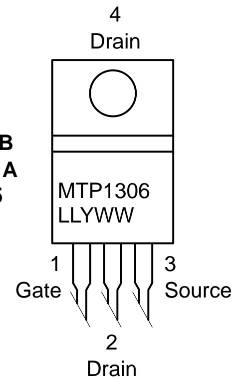
N–Channel




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




| | |
|---|---|
| MTP1306 | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP1306 | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 30 | – | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | µAdc |
| ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 38 Adc) | | $R_{DS(on)}$ | – | 5.8 | 6.5 | mΩ |
| ($V_{GS}$ = 5.0 Vdc, $I_D$ = 38 Adc) | | | – | 7.4 | 8.5 | |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 75 Adc) | | $V_{DS(on)}$ | – | 0.44 | 0.5 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 38 Adc, $T_J$ = 150°C) | | | – | – | 0.38 | |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 15 | 55 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2560 | 3584 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1305 | 1827 | |
| Transfer Capacitance | | $C_{rss}$ | – | 386 | 772 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | – | 17 | 35 | ns |
| Rise Time | | $t_r$ | – | 170 | 340 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 68 | 136 | |
| Fall Time | | $t_f$ | – | 145 | 290 | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 50 | 70 | nC |
| | | $Q_1$ | – | 8.3 | – | |
| | | $Q_2$ | – | 25.3 | – | |
| | | $Q_3$ | – | 17.2 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.75 | 1.1 | Vdc |
| | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.64 | – | |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 84 | – | ns |
| | | $t_a$ | – | 35 | – | |
| | | $t_b$ | – | 53 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.13 | – | µC |

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

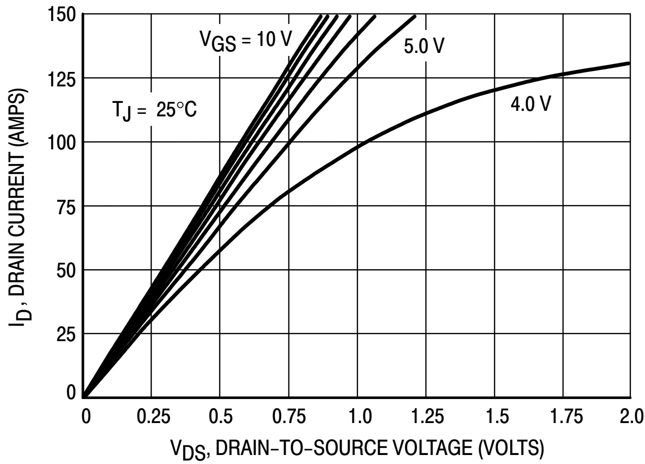


**Figure 1. On–Region Characteristics**

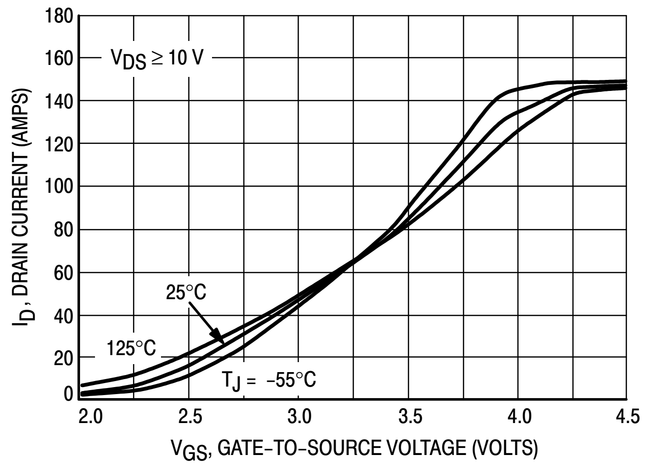


**Figure 2. Transfer Characteristics**

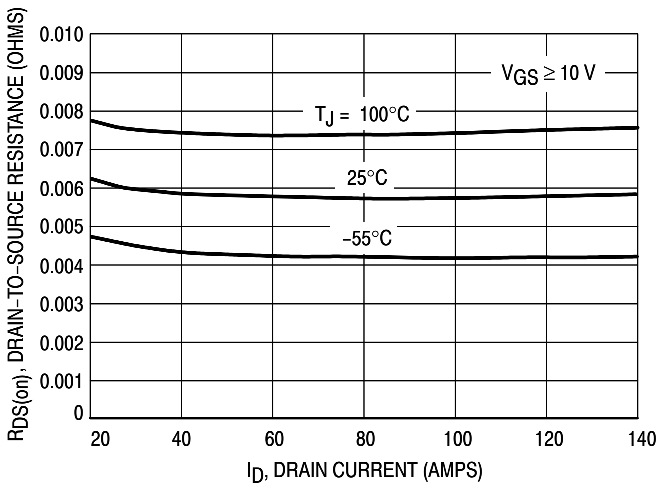


**Figure 3. On–Resistance versus Drain Current and Temperature**

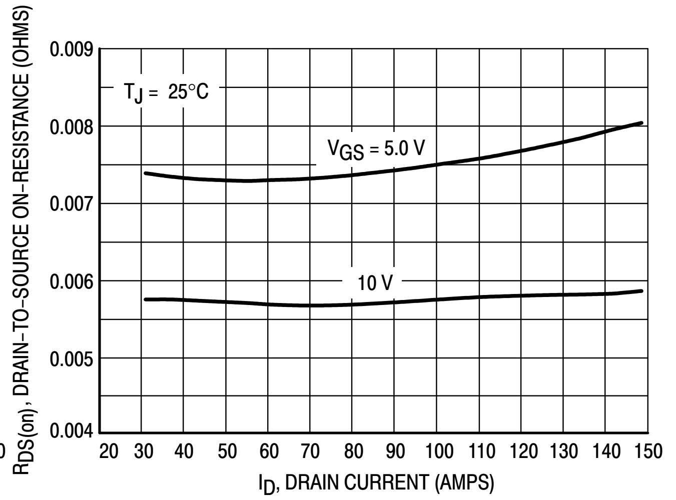


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

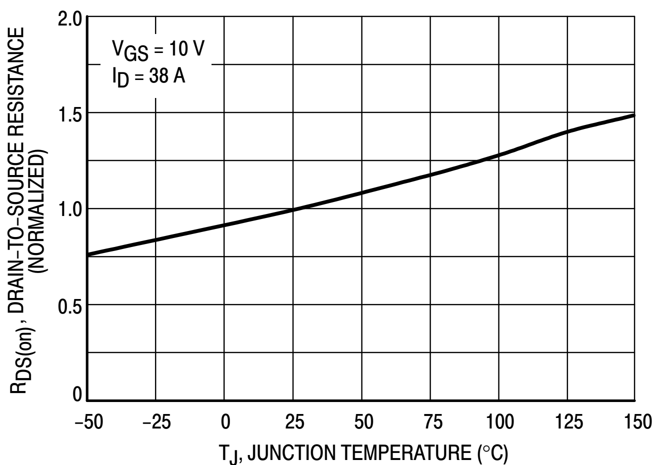


**Figure 5. On–Resistance Variation with Temperature**

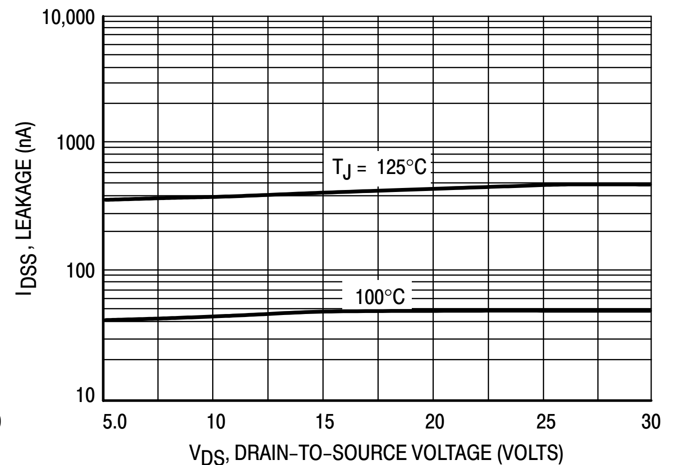


**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

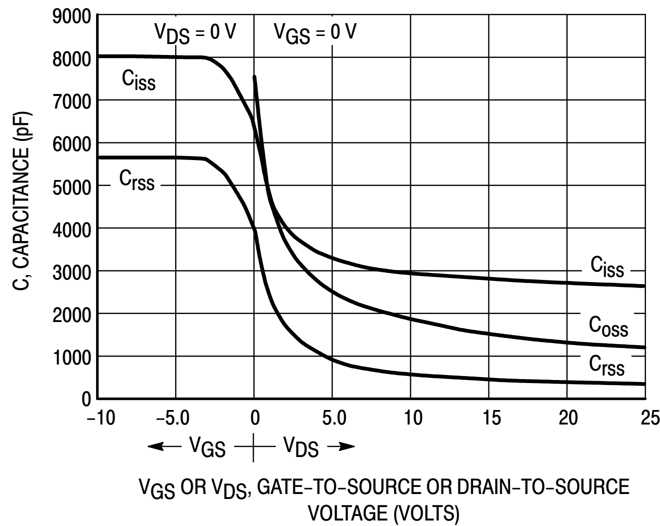


**Figure 7. Capacitance Variation**

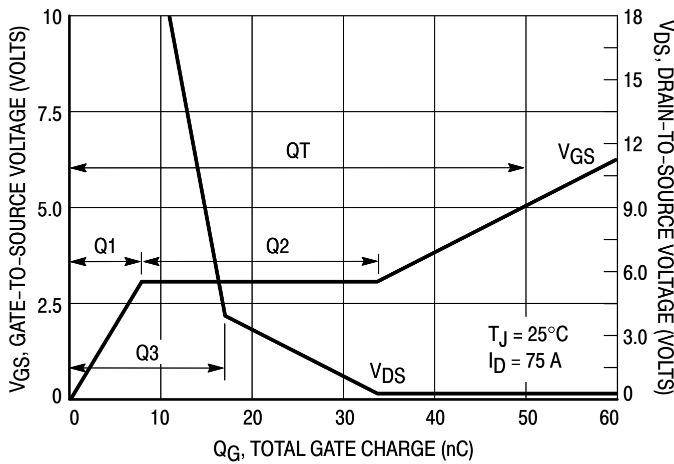


**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

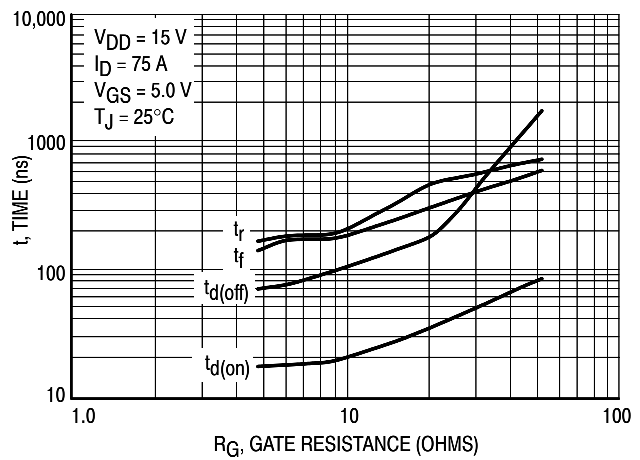


**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

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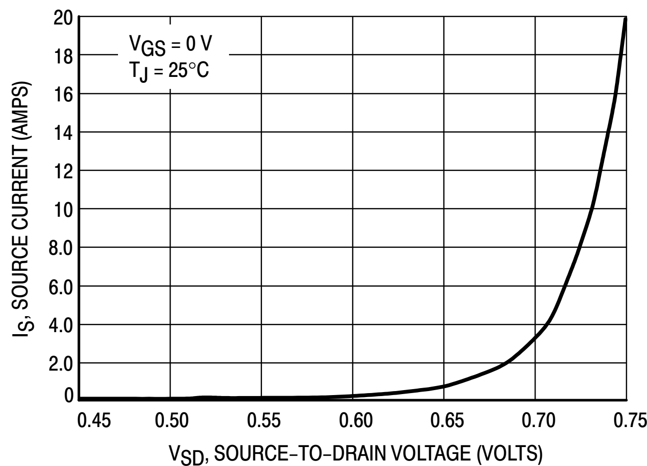


**Figure 10. Diode Forward Voltage versus Current**

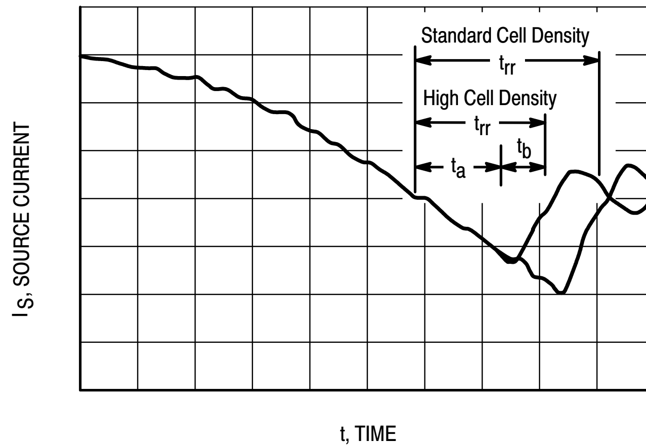


**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

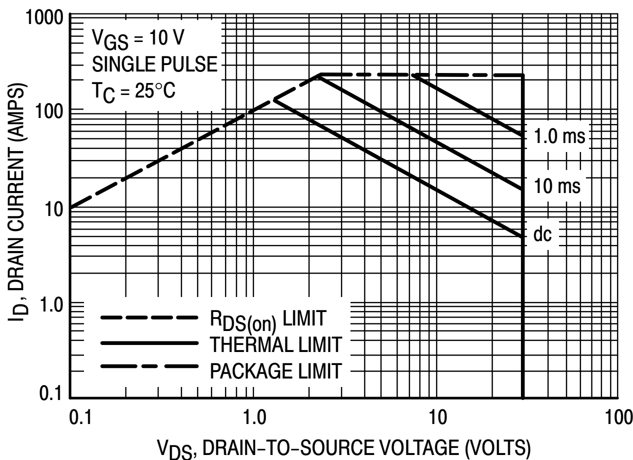



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

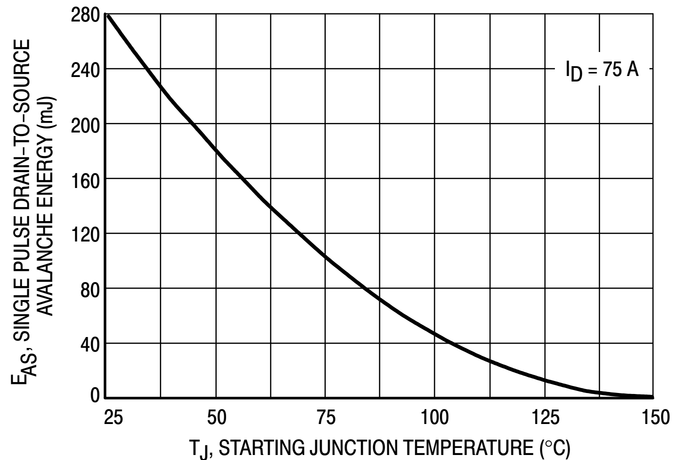



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

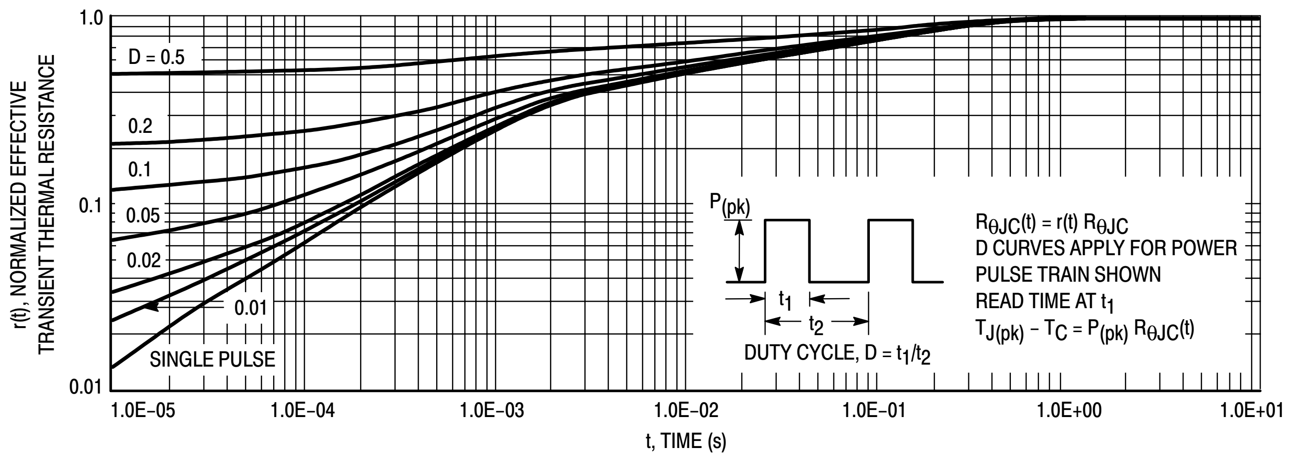



**Figure 14. Thermal Response**

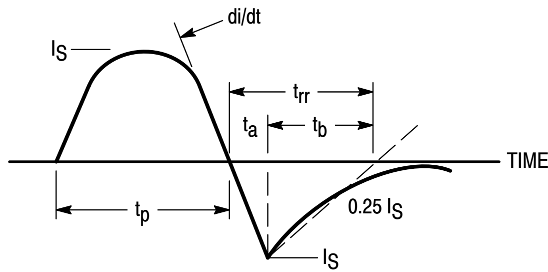



**Figure 15. Diode Reverse Recovery Waveform**

# MTP15N06V

**Preferred Device**

# Power MOSFET 15 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

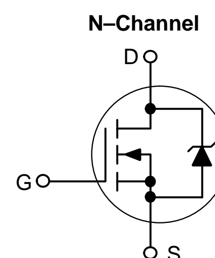
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Single Pulse ($t_p \le 50\ \mu s$) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le 10\ \mu s$) | $I_D$<br>$I_D$<br>$I_{DM}$ | 15<br>8.7<br>45 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 55<br>0.5 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 15 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 113 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 2.73<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor**™

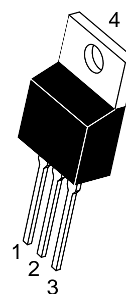
http://onsemi.com

**15 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

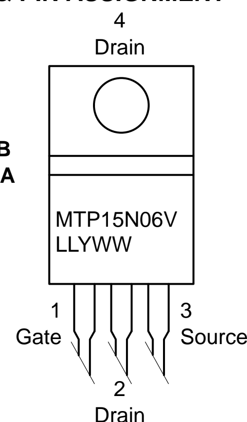
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP15N06V = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP15N06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 67 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 2.7 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 5.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 7.5 Adc) | | $R_{DS(on)}$ | – | 0.08 | 0.12 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 15 Adc) | | $V_{DS(on)}$ | – | 2.0 | 2.2 | Vdc |
| ($I_D$ = 7.5 Adc, $T_J$ = 150°C) | | | – | – | 1.9 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 7.5 Adc) | | $g_{FS}$ | 4.0 | 6.2 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 469 | 660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 148 | 200 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 35 | 60 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.6 | 20 | ns |
| Rise Time | | $t_r$ | – | 51 | 100 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 18 | 40 | |
| Fall Time | | $t_f$ | – | 33 | 70 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 14.4 | 20 | nC |
| | | $Q_1$ | – | 2.8 | – | |
| | | $Q_2$ | – | 6.4 | – | |
| | | $Q_3$ | – | 6.1 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.05 | 1.6 | Vdc |
| | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 1.5 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 59.3 | – | ns |
| | | $t_a$ | – | 46 | – | |
| | | $t_b$ | – | 13.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.165 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

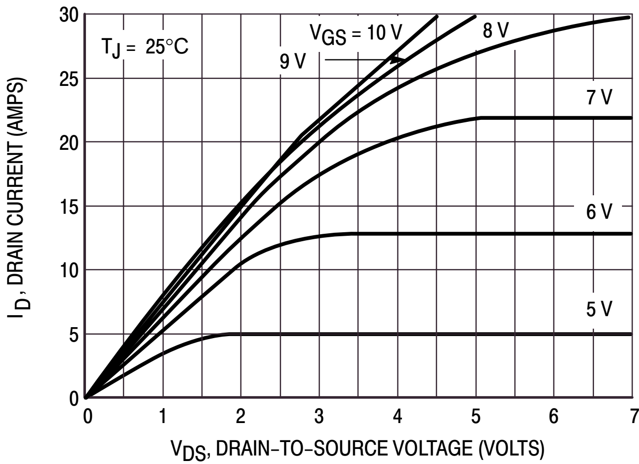



**Figure 1. On–Region Characteristics**

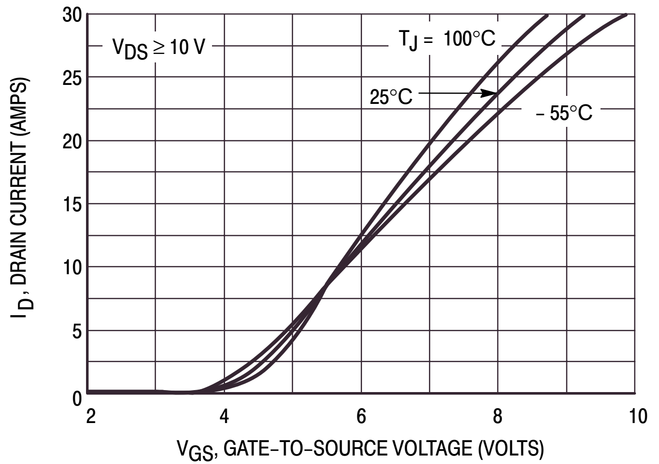



**Figure 2. Transfer Characteristics**

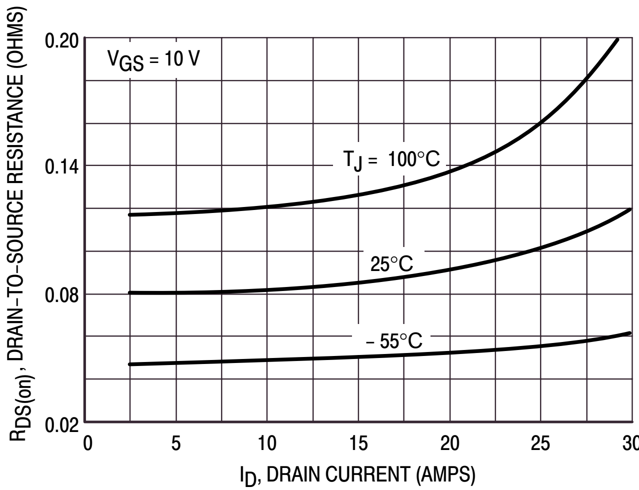



**Figure 3. On–Resistance versus Drain Current and Temperature**

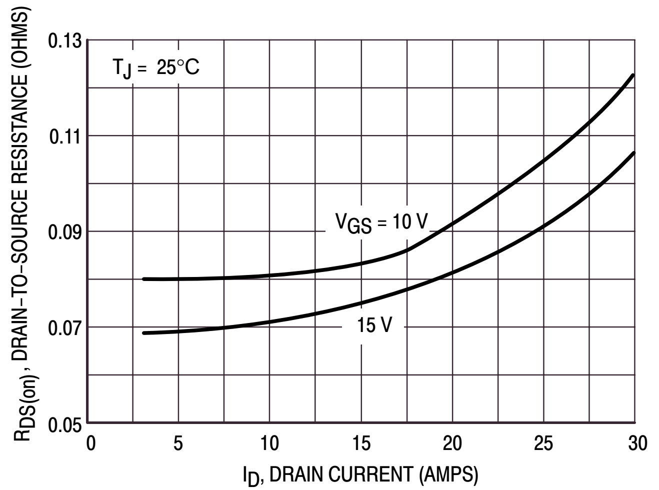



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

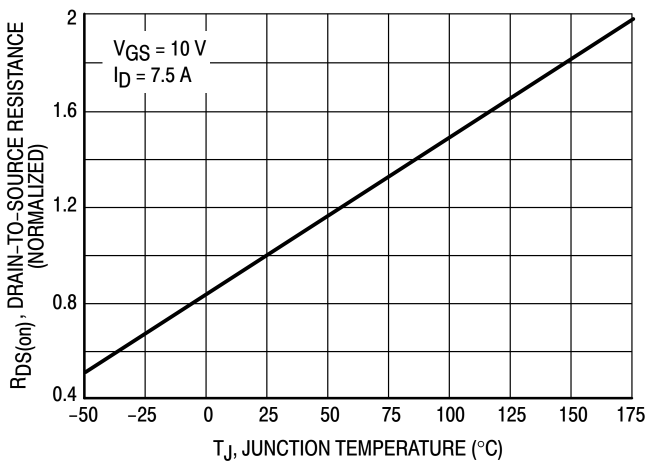



**Figure 5. On–Resistance Variation with Temperature**

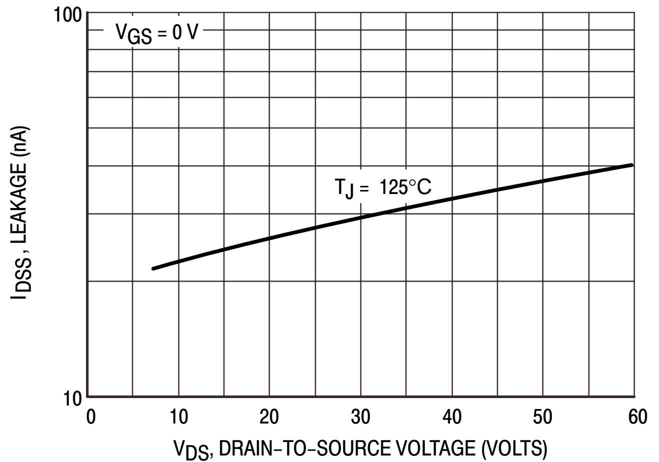



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

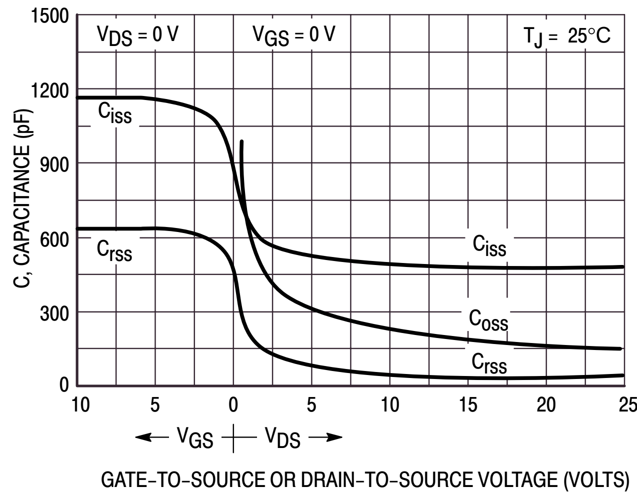



**Figure 7. Capacitance Variation**

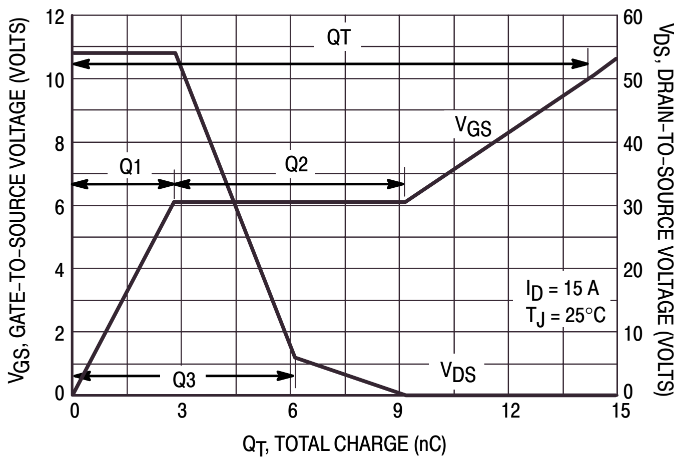



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

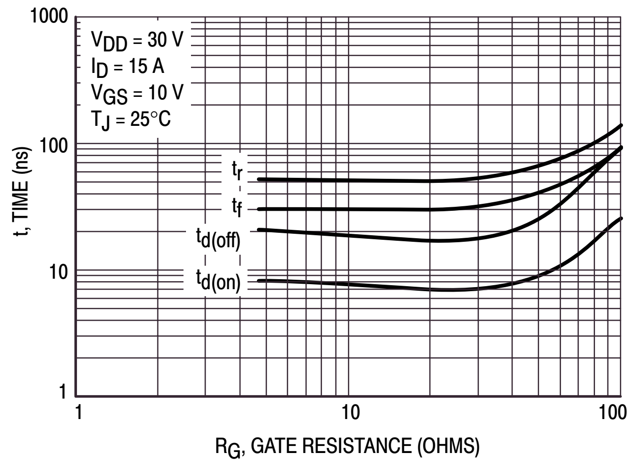



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

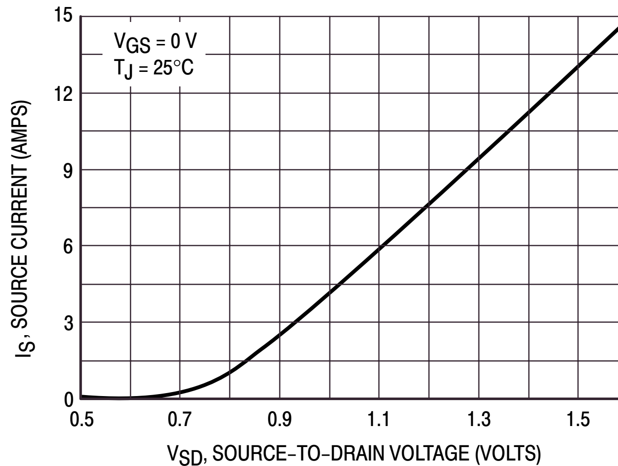



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

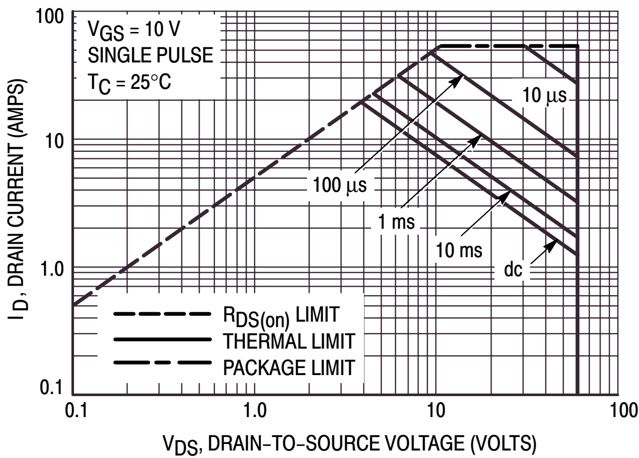



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

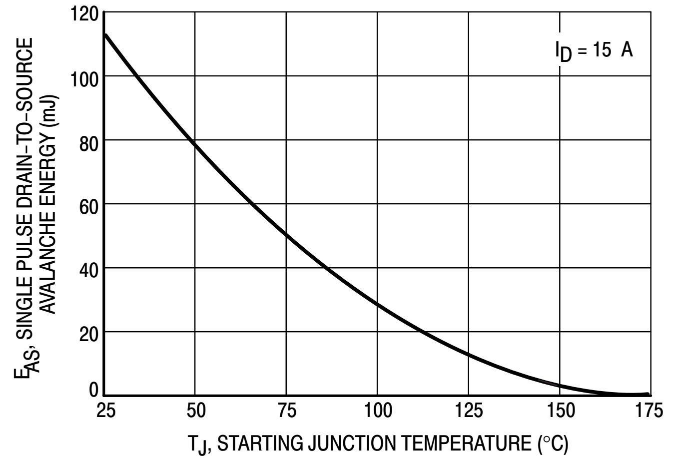



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

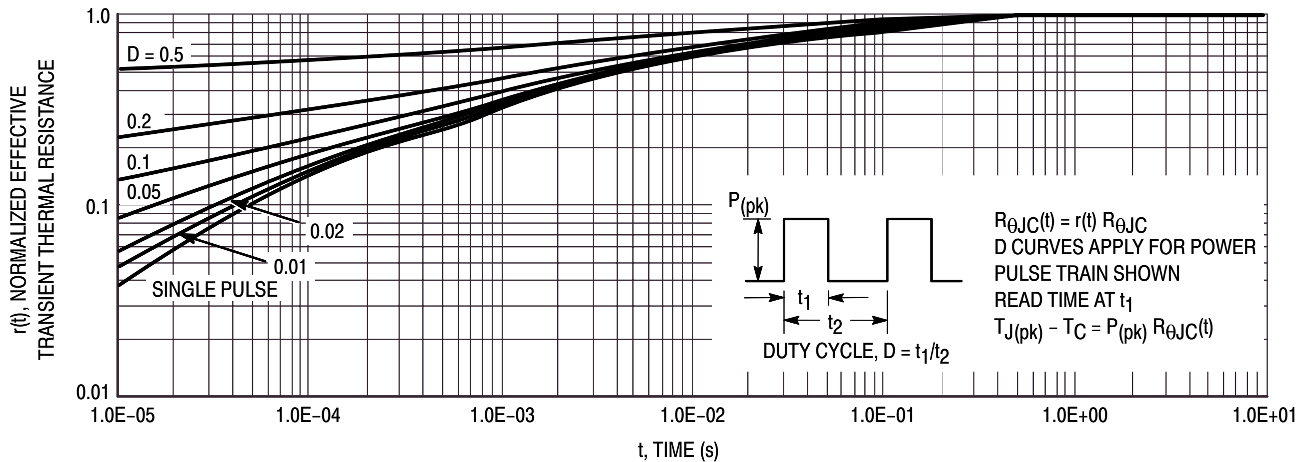



**Figure 13. Thermal Response**

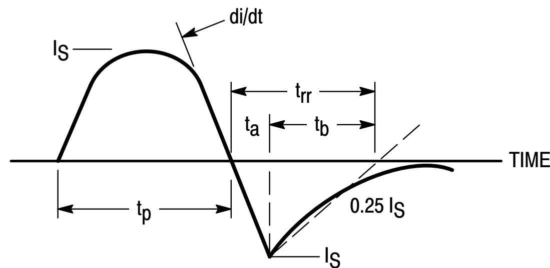



**Figure 14. Diode Reverse Recovery Waveform**

# MTP15N06VL

**Preferred Device**

# Power MOSFET 15 Amps, 60 Volts, Logic Level

## N–Channel TO–220

**ON Semiconductor**™

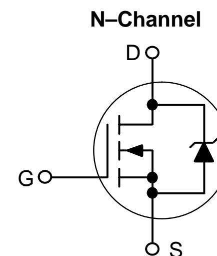
**http://onsemi.com**

**15 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 85 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

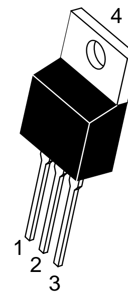
**N–Channel**



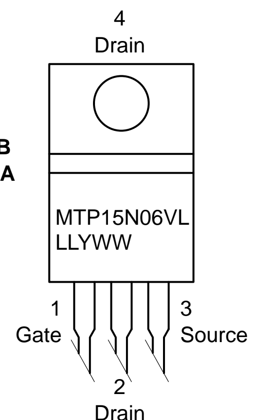

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 15<br>12<br>53 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 60<br>0.40 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 15 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 113 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 2.5<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP15N06VL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP15N06VL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>68 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.0 | <br>2.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 7.5 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.075 | <br>0.085 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 15 Adc)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 7.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.5<br>1.3 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 7.5 Adc) | | $g_{FS}$ | 8.0 | 10 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 570 | 800 | pF |
| Output Capacitance | | $C_{oss}$ | – | 180 | 250 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 45 | 90 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 150 | 300 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 27 | 50 | |
| Fall Time | | $t_f$ | – | 70 | 140 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 15 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 32 | 40 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 7.0 | – | |
| | | $Q_3$ | – | 11 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 0.96<br>0.85 | 1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 15 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 63 | – | ns |
| | | $t_a$ | – | 42 | – | |
| | | $t_b$ | – | 21 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.140 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die.)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

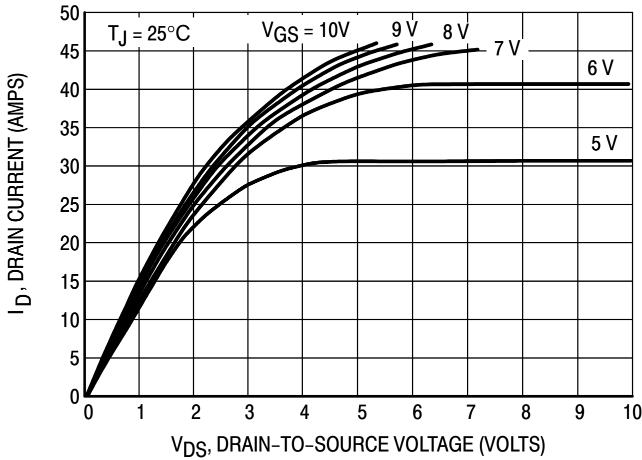



**Figure 1. On–Region Characteristics**

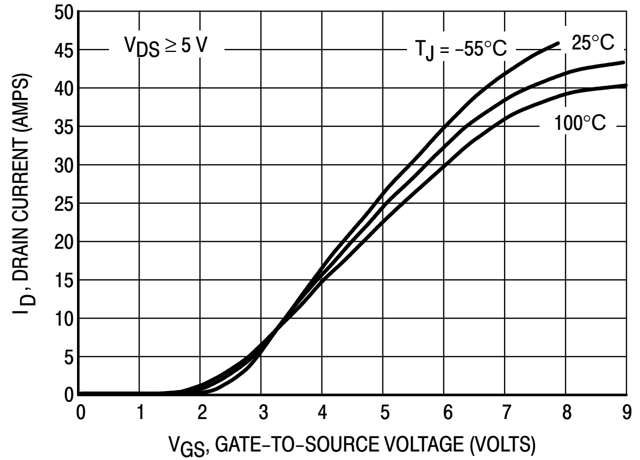



**Figure 2. Transfer Characteristics**

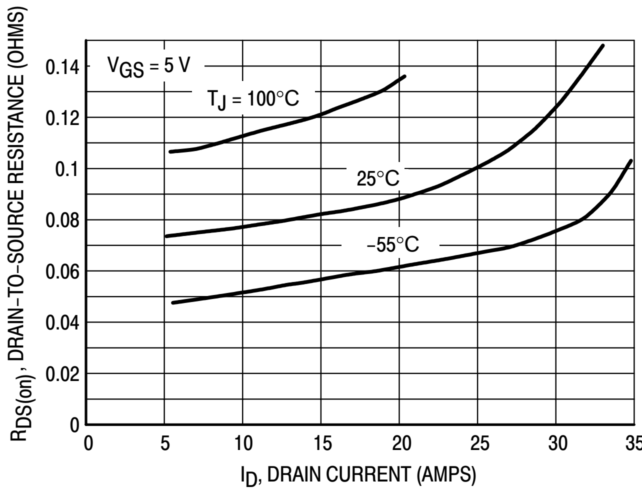



**Figure 3. On–Resistance versus Drain Current and Temperature**

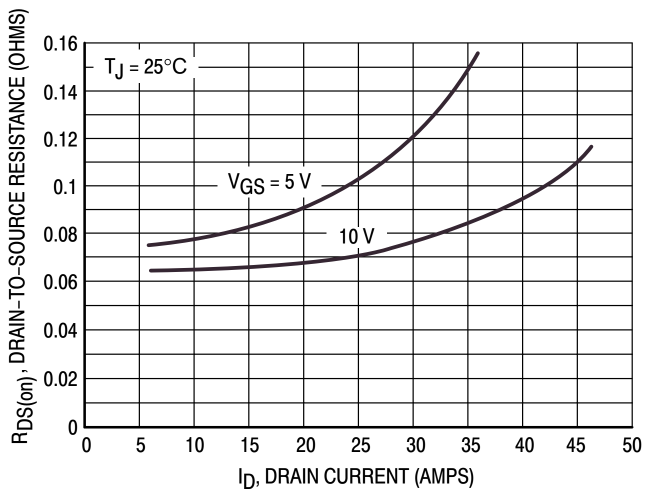



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

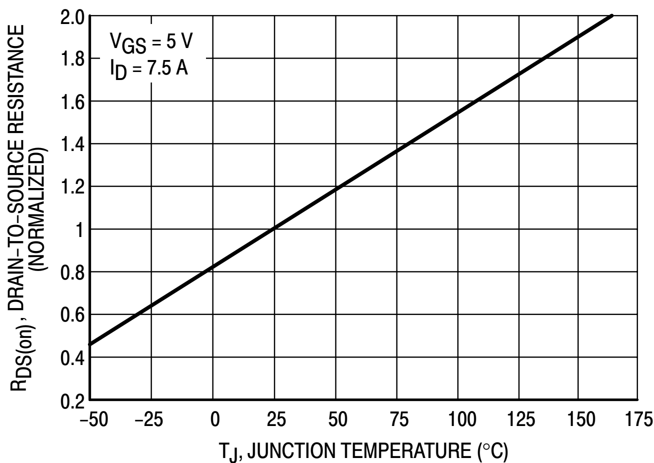



**Figure 5. On–Resistance Variation with Temperature**

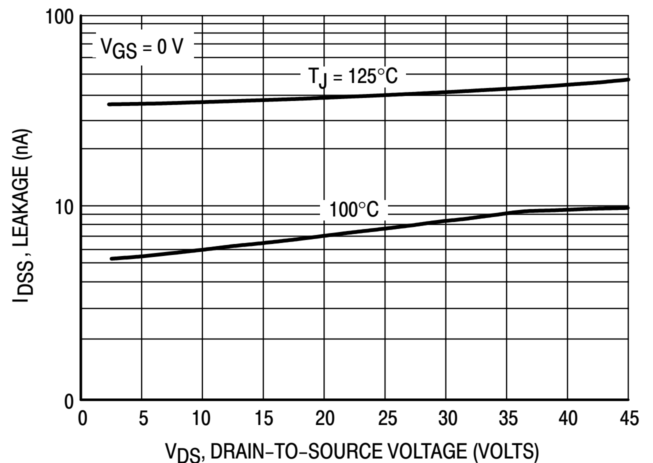



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

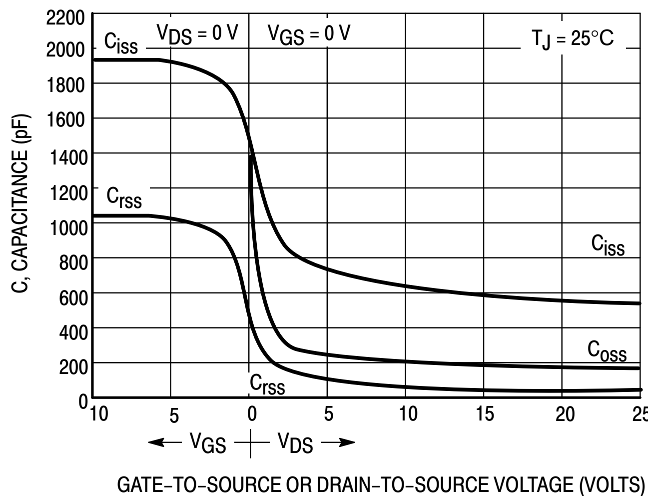



**Figure 7. Capacitance Variation**

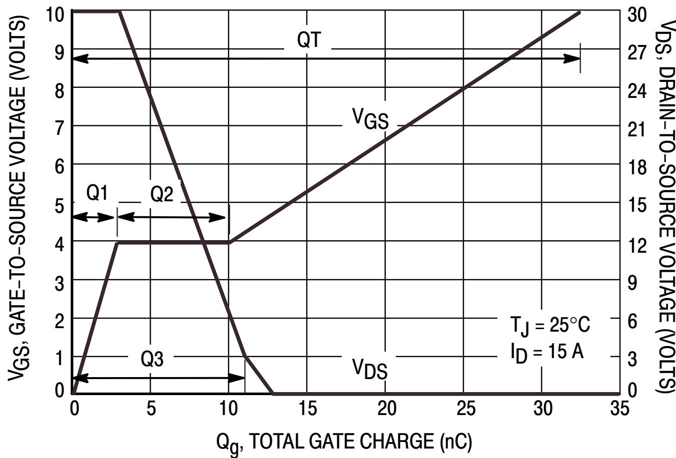



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

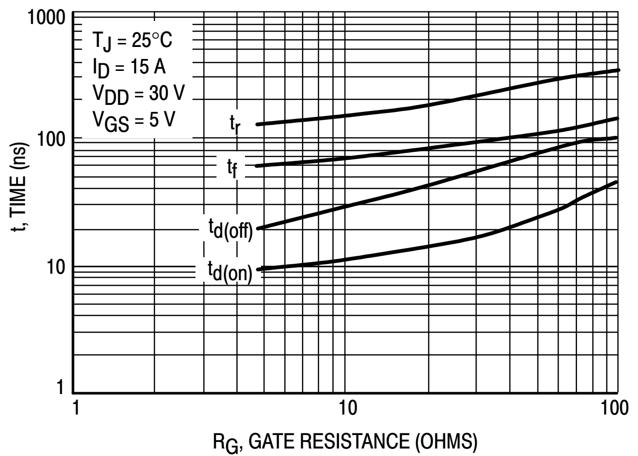



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

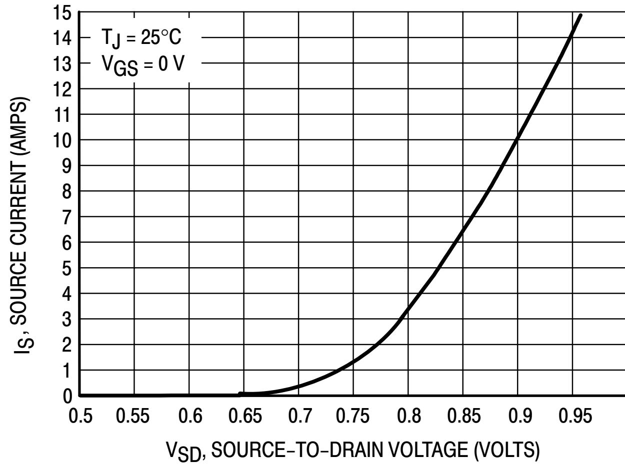



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

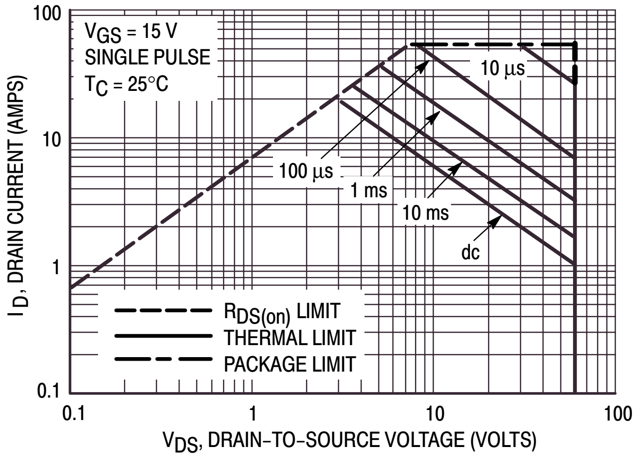



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

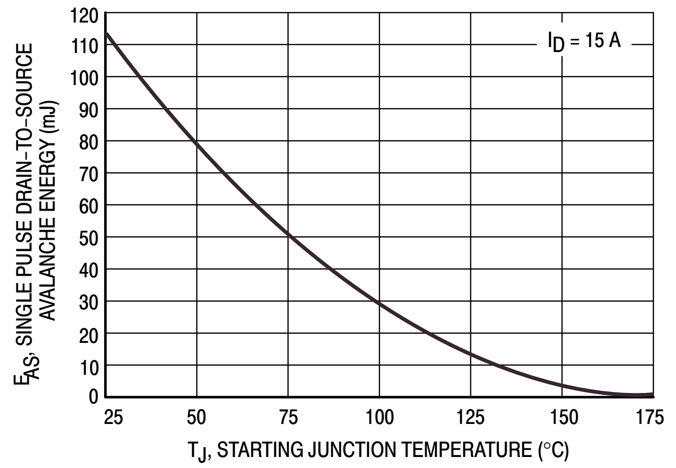



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

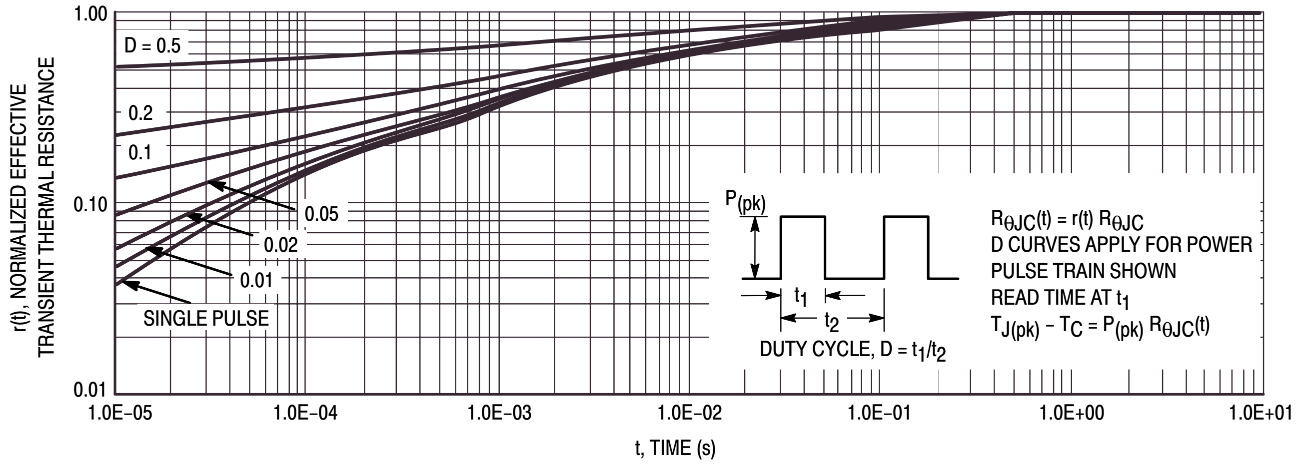



**Figure 13. Thermal Response**

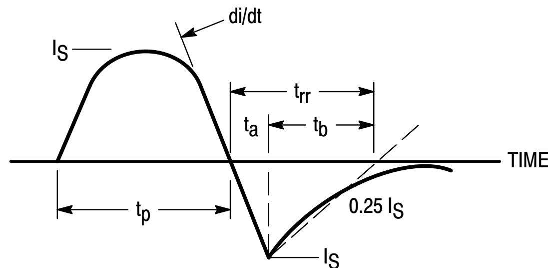



**Figure 14. Diode Reverse Recovery Waveform**

# MTP20N06V

Preferred Device

# Power MOSFET 20 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

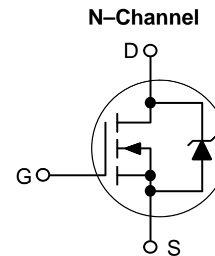
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>13<br>70 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 60<br>0.40 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 20 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 200 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>2.5<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

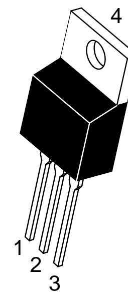
http://onsemi.com

**20 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 80 mΩ**

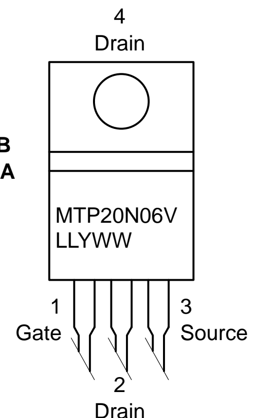
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP20N06V | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP20N06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>69 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.8<br>5.0 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.065 | <br>0.080 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>2.0<br>1.9 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.0 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 6.0 | 8.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 590 | 830 | pF |
| Output Capacitance | | $C_{oss}$ | – | 180 | 250 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 40 | 80 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 8.7 | 20 | ns |
| Rise Time | | $t_r$ | – | 77 | 150 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 26 | 50 | |
| Fall Time | | $t_f$ | – | 46 | 90 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 28 | 40 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 9.0 | – | |
| | | $Q_3$ | – | 8.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>–<br>– | <br>1.05<br>0.96 | <br>1.6<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 60 | – | ns |
| | | $t_a$ | – | 52 | – | |
| | | $t_b$ | – | 8.0 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.172 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

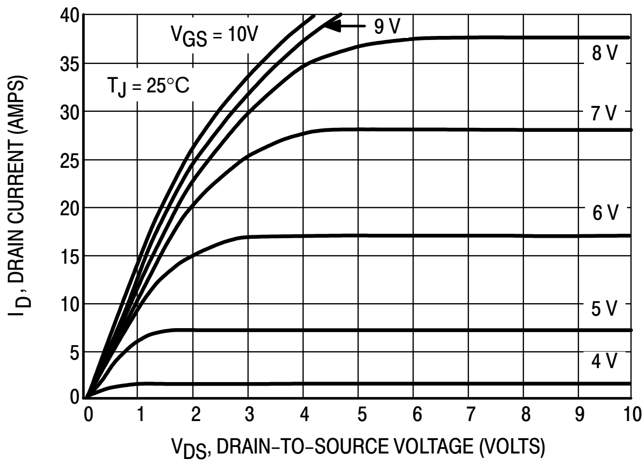



**Figure 1. On–Region Characteristics**

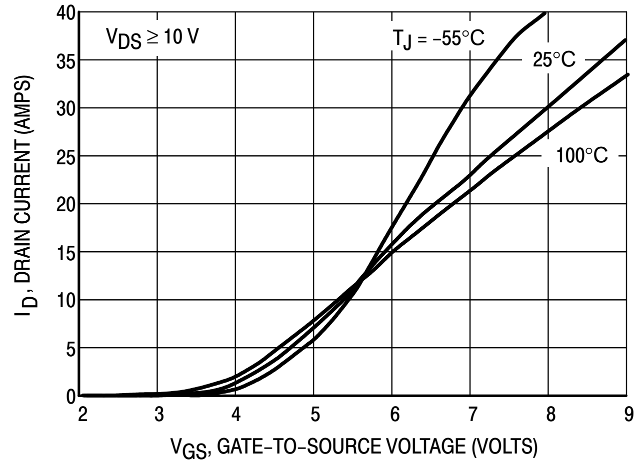
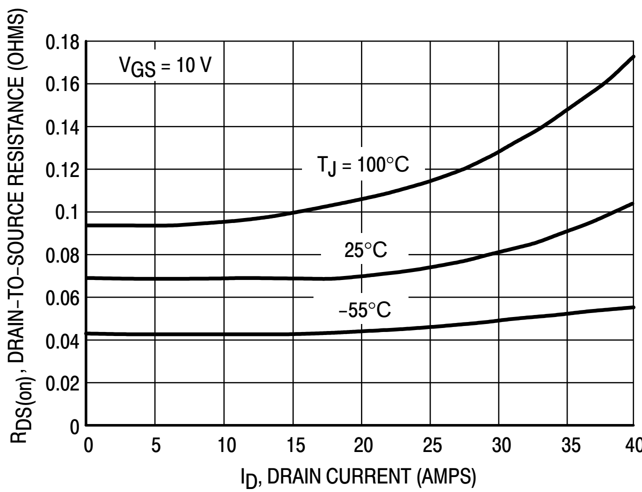



**Figure 2. Transfer Characteristics**

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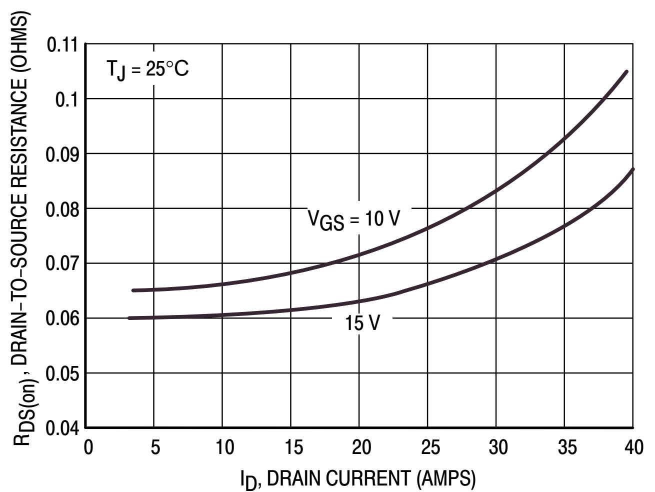


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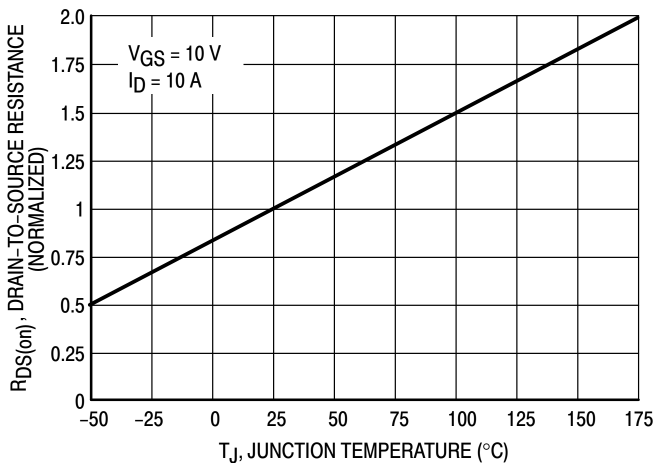


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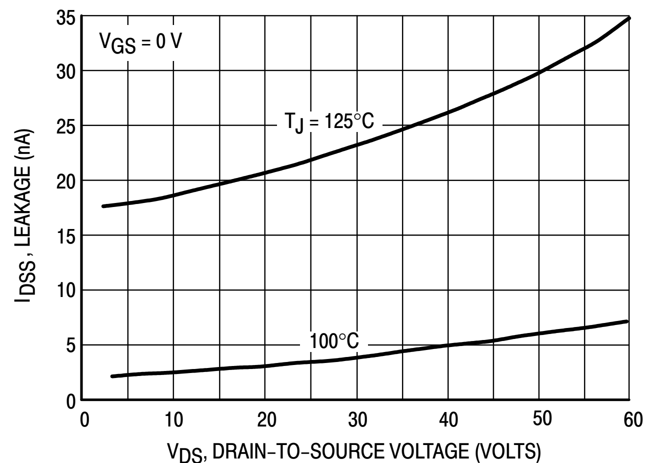


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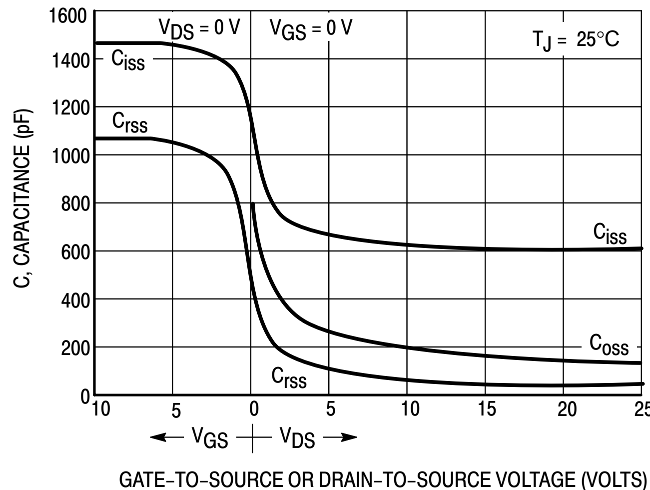


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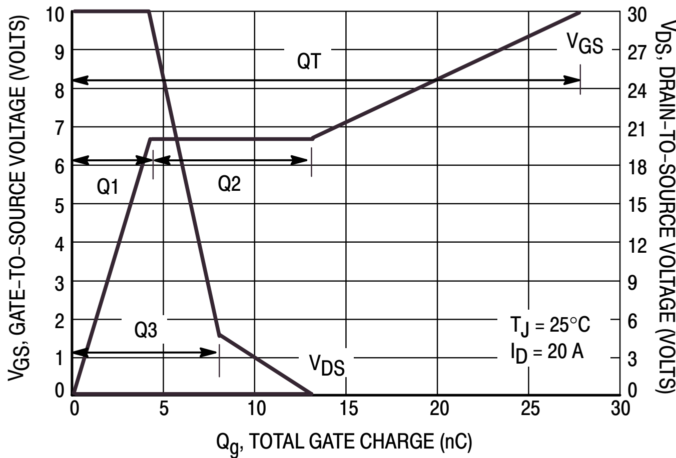


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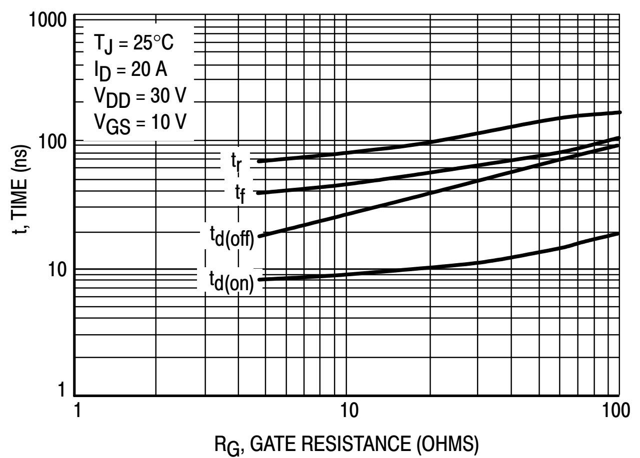
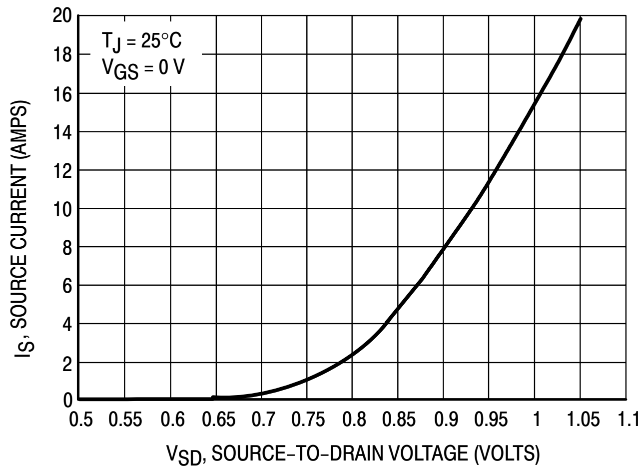



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

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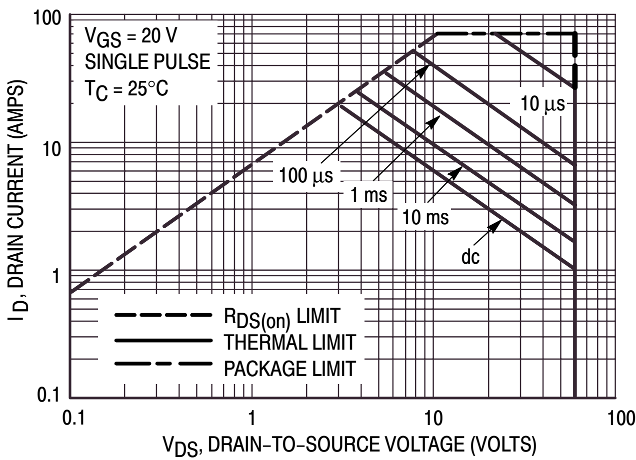



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

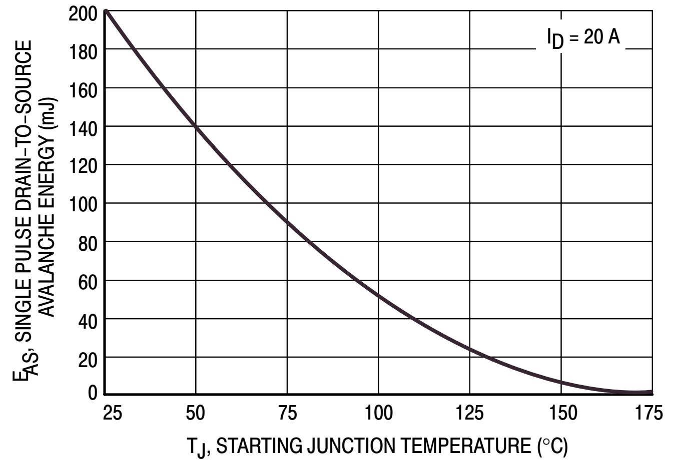



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

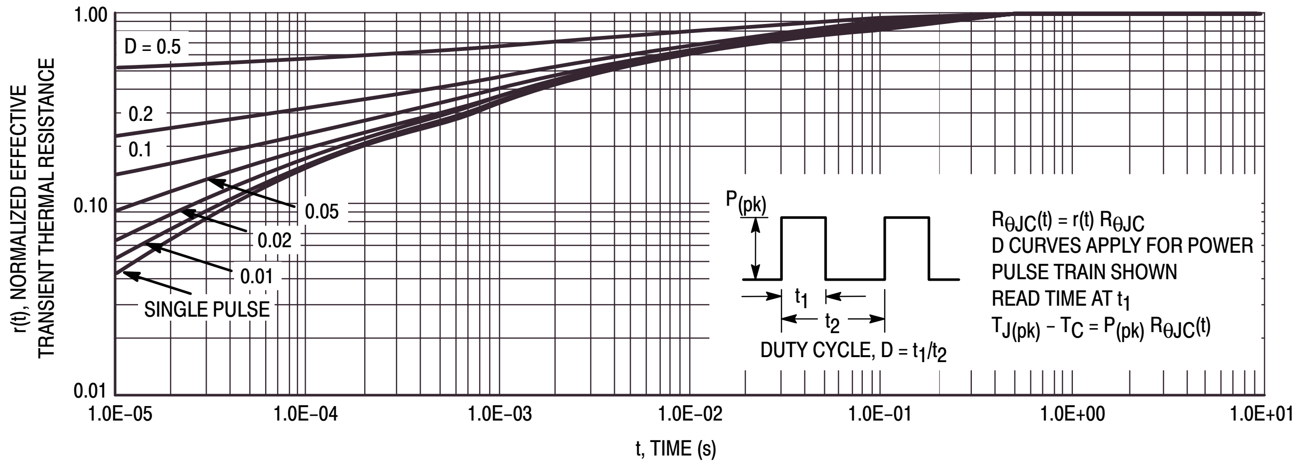



**Figure 13. Thermal Response**

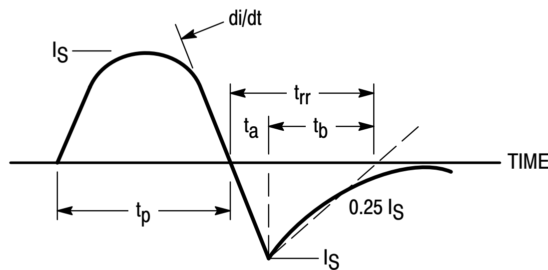



**Figure 14. Diode Reverse Recovery Waveform**

# MTP20N15E

**Preferred Device**

# Power MOSFET
# 20 Amps, 150 Volts
## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

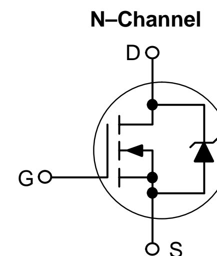
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 150 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 150 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 32 | Vdc |
| Drain – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>12<br>60 | Adc |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 112<br>0.9 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 120 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 20 Apk, L = 0.3 mH) | $E_{AS}$ | 60 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.1<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

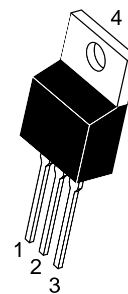
**http://onsemi.com**

**20 AMPERES**
**150 VOLTS**
**$R_{DS(on)}$ = 130 mΩ**

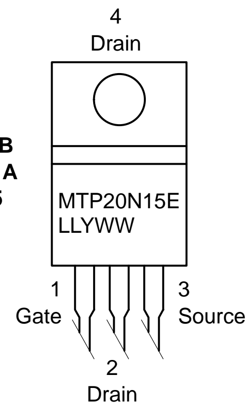
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP20N15E | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP20N15E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | $V_{(BR)DSS}$ | 150 | – | – | Vdc |
| Temperature Coefficient (Positive) | | – | TBD | – | mV/°C |
| Zero Gate Voltage Collector Current ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | $I_{GSS(f)}$ | – | – | 100 | nAdc |
| | $I_{GSS(r)}$ | – | – | 100 | |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mAdc) | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | – | TBD | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | $R_{DS(on)}$ | – | 0.12 | 0.13 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 20 Adc) | $V_{DS(on)}$ | – | – | 2.8 | Vdc |
| ($I_D$ = 10 Adc, $T_J$ = 125°C) | | – | – | 2.6 | |
| Forward Transconductance ($V_{DS}$ = 13 Vdc, $I_D$ = 10 Adc) | $g_{FS}$ | 8.0 | 11 | – | mhos |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1133 | 1627 | pF |
| Output Capacitance | | $C_{oss}$ | – | 332 | 474 | |
| Transfer Capacitance | | $C_{rss}$ | – | 105 | 174 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 75 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 25 | ns |
| Rise Time | | $t_r$ | – | 77 | 153 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 33 | 67 | |
| Fall Time | | $t_f$ | – | 49 | 97 | |
| Gate Charge | ($V_{DS}$ = 120 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 39.1 | 55.9 | nC |
| | | $Q_1$ | – | 7.5 | – | |
| | | $Q_2$ | – | 22 | – | |
| | | $Q_3$ | – | 17 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | – | 1.5 | Vdc |
| | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | – | – | |
| Reverse Recovery Time | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 160 | – | ns |
| | | $t_a$ | – | 123 | – | |
| | | $t_b$ | – | 36.5 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.1 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

# MTP20N20E

Preferred Device

# Power MOSFET
# 20 Amps, 200 Volts
## N–Channel TO–220

**ON Semiconductor**™

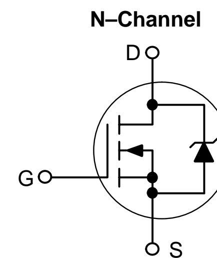
http://onsemi.com

**20 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 160 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

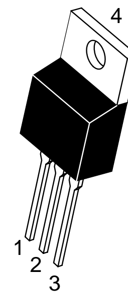
**N–Channel**



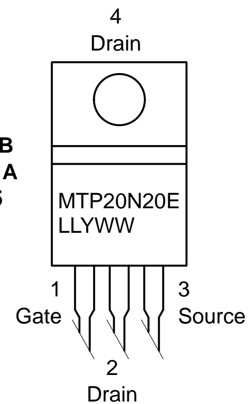

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 20<br>12<br>60 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 125<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc,<br>$I_L$ = 20 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 600 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.00<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP20N20E | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP20N20E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 µAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 200<br>– | –<br>263 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | –<br>7.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 10 Adc) | | $R_{DS(on)}$ | – | 0.12 | 0.16 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 20 Adc)<br>($I_D$ = 10 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 3.84<br>3.36 | Vdc |
| Forward Transconductance ($V_{DS}$ = 13 Vdc, $I_D$ = 10 Adc) | | $g_{FS}$ | 8.0 | 11 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1880 | 2700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 378 | 535 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 68 | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 17 | 40 | ns |
| Rise Time | | $t_r$ | – | 86 | 180 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | 100 | |
| Fall Time | | $t_f$ | – | 60 | 120 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 20 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 54 | 75 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 24 | – | |
| | | $Q_3$ | – | 22 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.0<br>0.82 | 1.35<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 20 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 239 | – | ns |
| | | $t_a$ | – | 136 | – | |
| | | $t_b$ | – | 103 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 2.09 | – | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 µs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

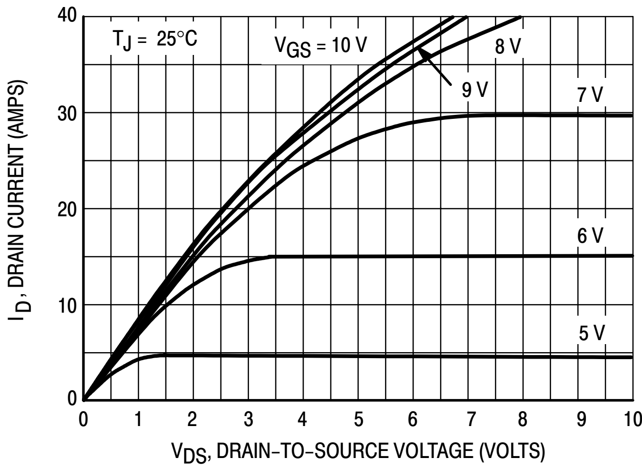



**Figure 1. On–Region Characteristics**

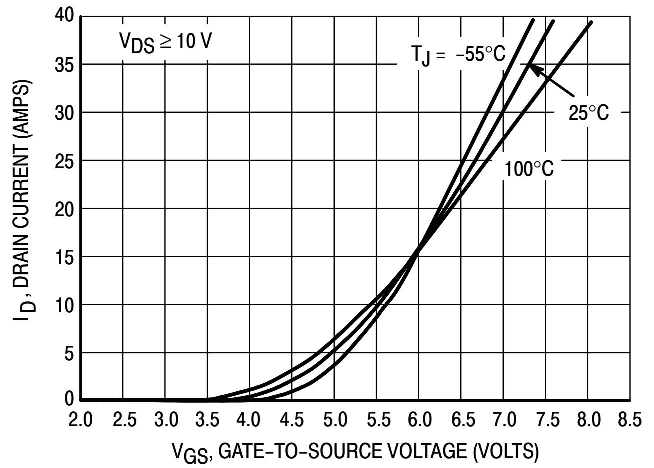



**Figure 2. Transfer Characteristics**

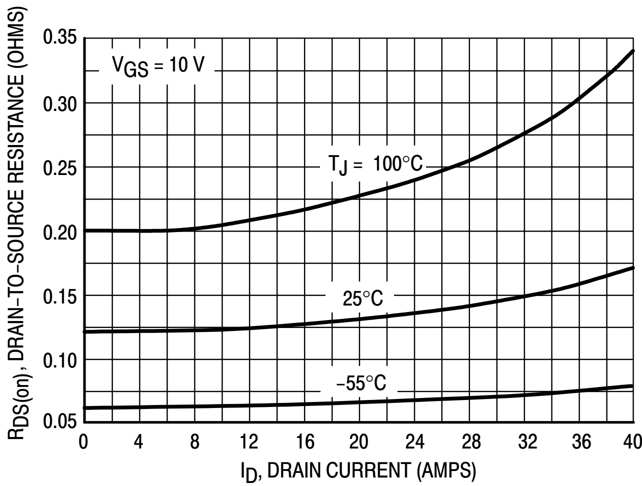



**Figure 3. On–Resistance versus Drain Current and Temperature**

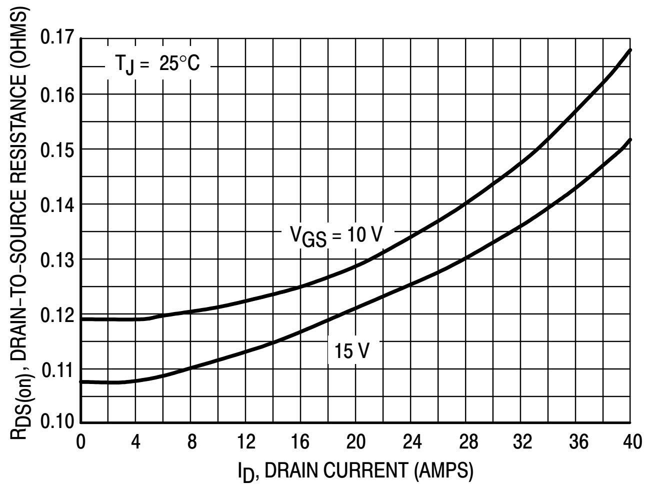



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

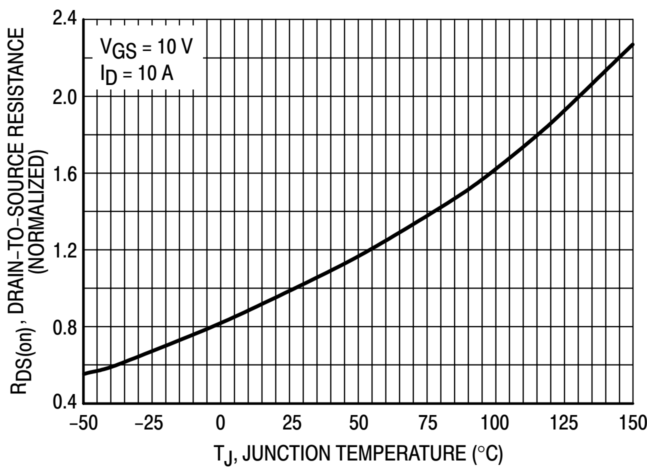



**Figure 5. On–Resistance Variation with Temperature**

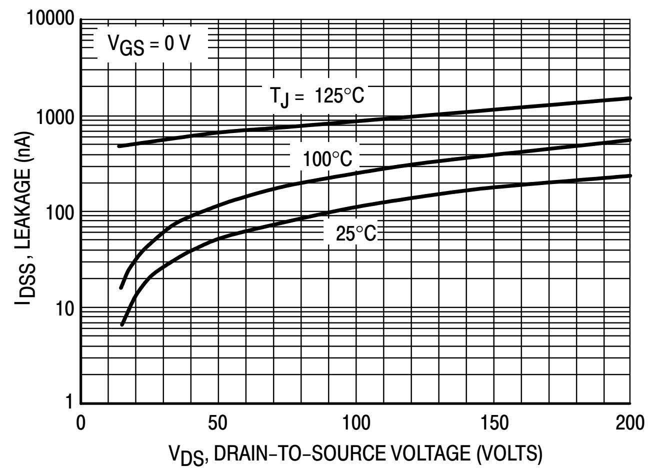



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

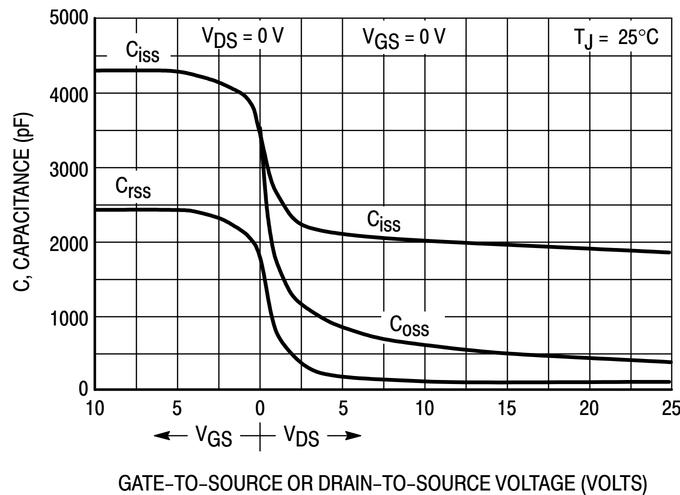



**Figure 7. Capacitance Variation**

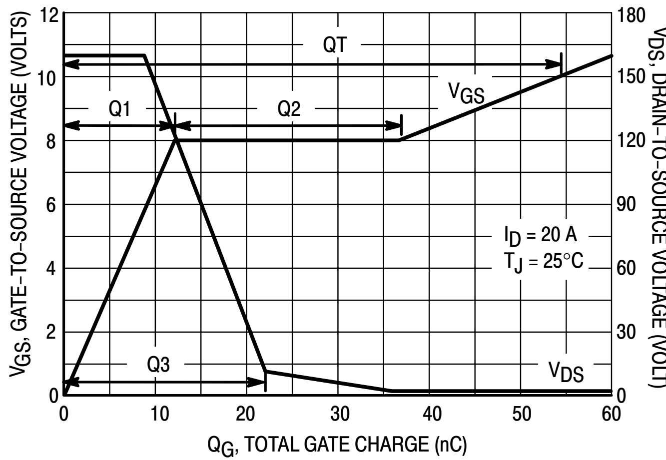



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

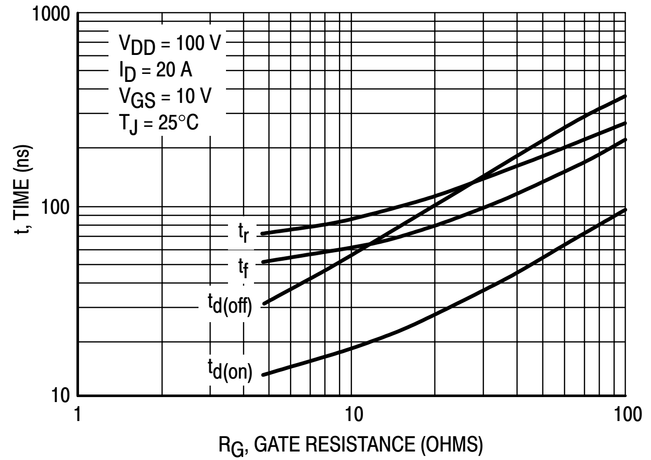



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

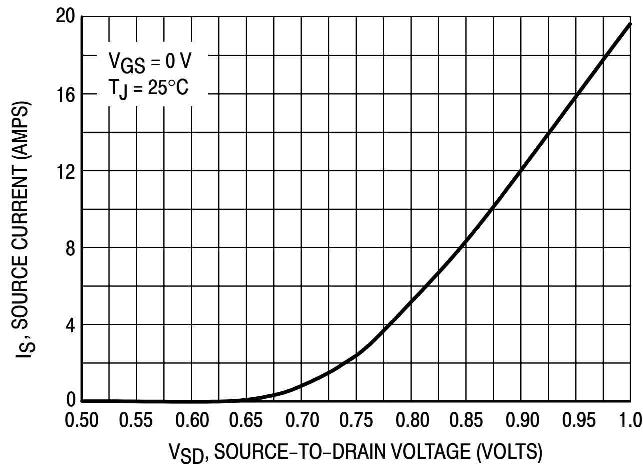



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

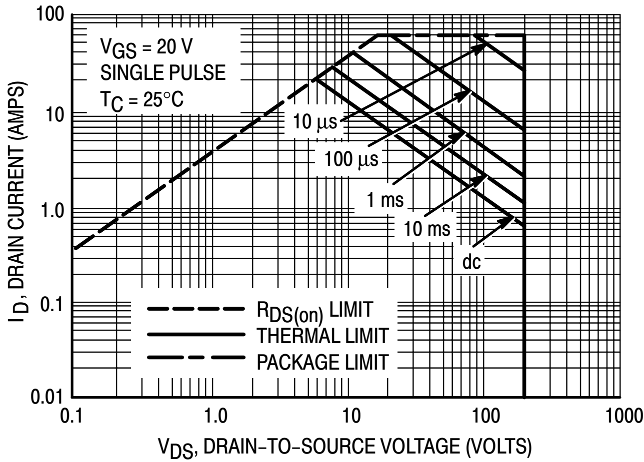



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

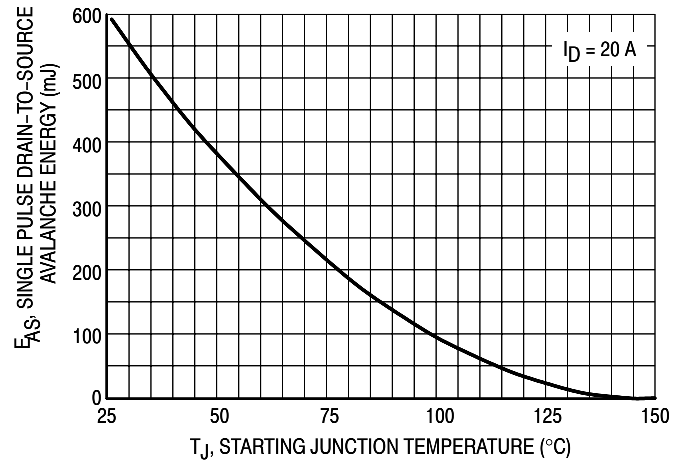



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

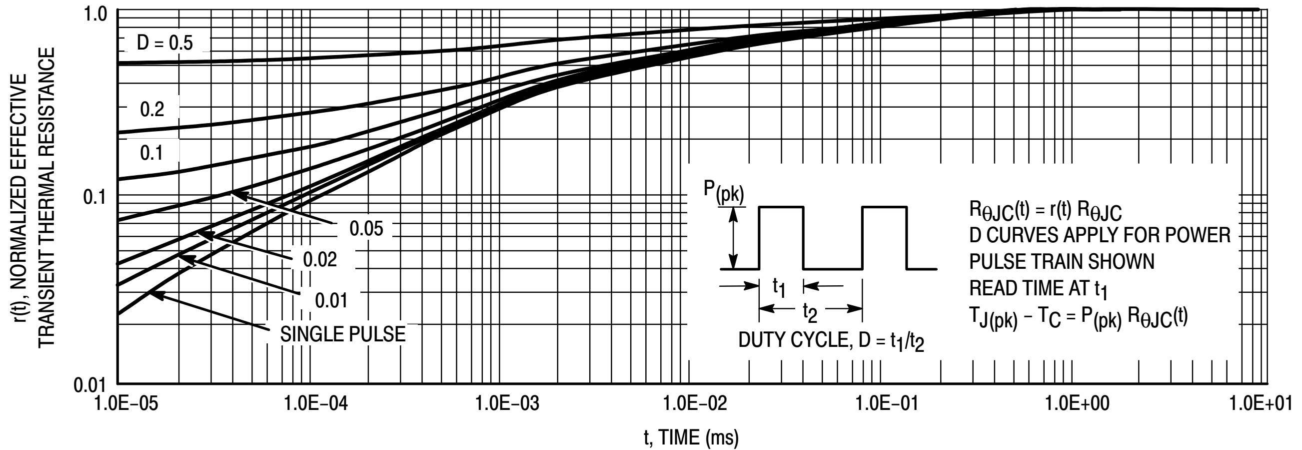



**Figure 13. Thermal Response**

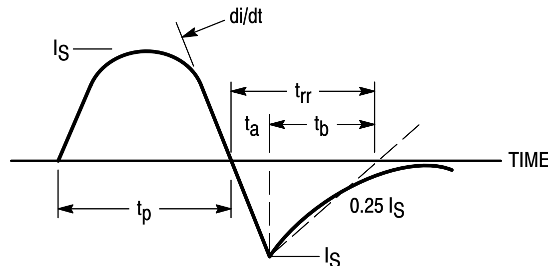



**Figure 14. Diode Reverse Recovery Waveform**

# MTP23P06V

**Preferred Device**

# Power MOSFET 23 Amps, 60 Volts

## P–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

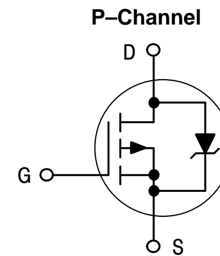
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

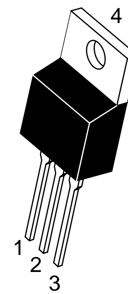
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 23<br>15<br>81 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 90<br>0.60 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 23 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 794 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**23 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 120 mΩ**

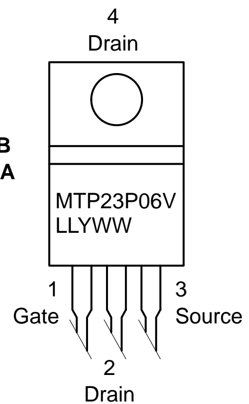
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP23P06V | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP23P06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>60.5 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>5.3 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 11.5 Adc) | | $R_{DS(on)}$ | – | 0.093 | 0.12 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 23 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 11.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 3.3<br>3.2 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 10.9 Vdc, $I_D$ = 11.5 Adc) | | $g_{FS}$ | 5.0 | 11.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1160 | 1620 | pF |
| Output Capacitance | | $C_{oss}$ | – | 380 | 530 | |
| Transfer Capacitance | | $C_{rss}$ | – | 105 | 210 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 23 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 13.8 | 30 | ns |
| Rise Time | | $t_r$ | – | 98.3 | 200 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 41 | 80 | |
| Fall Time | | $t_f$ | – | 62 | 120 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 23 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 38 | 50 | nC |
| | | $Q_1$ | – | 7.0 | – | |
| | | $Q_2$ | – | 18 | – | |
| | | $Q_3$ | – | 14 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 2.2<br>1.8 | 3.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 23 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 142.2 | – | ns |
| | | $t_a$ | – | 100.5 | – | |
| | | $t_b$ | – | 41.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.804 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

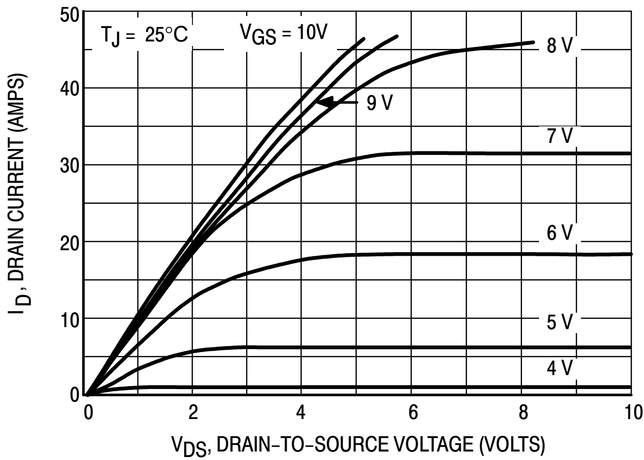



**Figure 1. On–Region Characteristics**

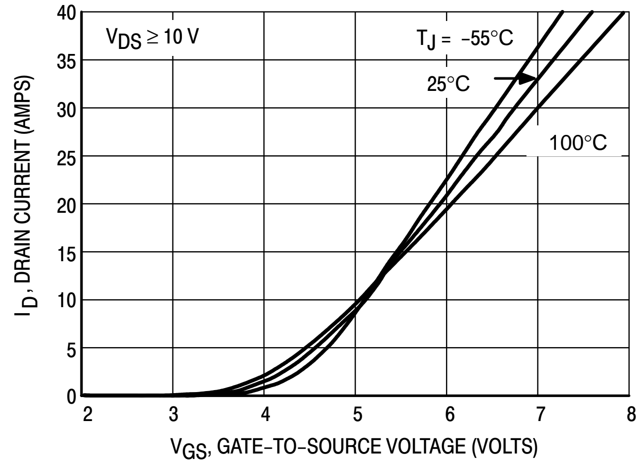



**Figure 2. Transfer Characteristics**

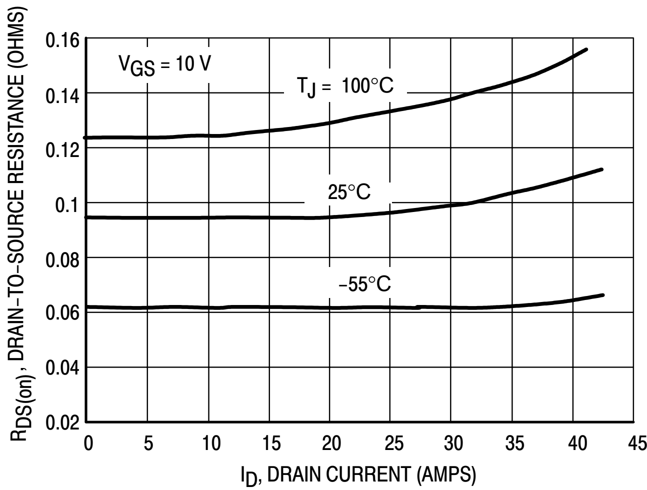



**Figure 3. On–Resistance versus Drain Current and Temperature**

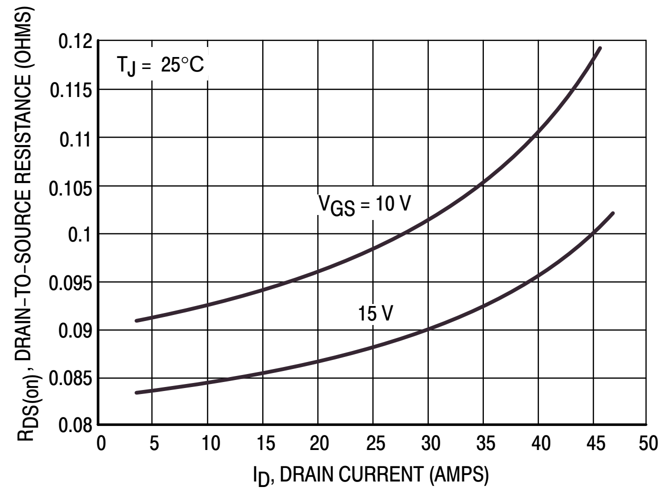



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

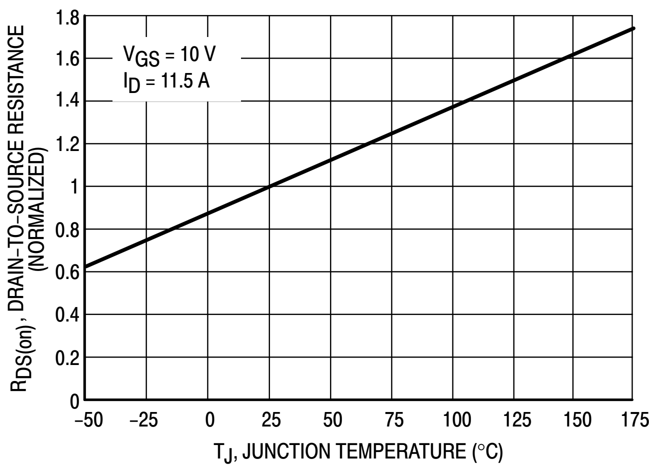



**Figure 5. On–Resistance Variation with Temperature**

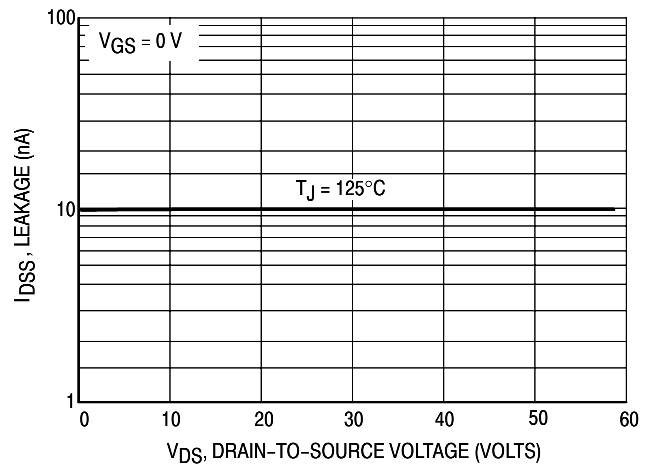



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

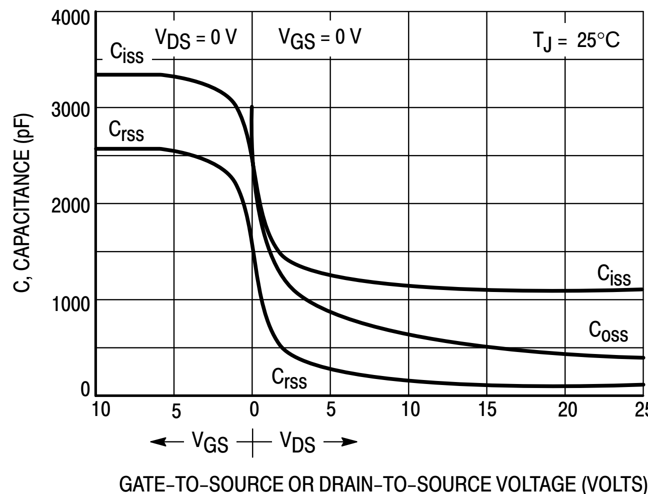



**Figure 7. Capacitance Variation**

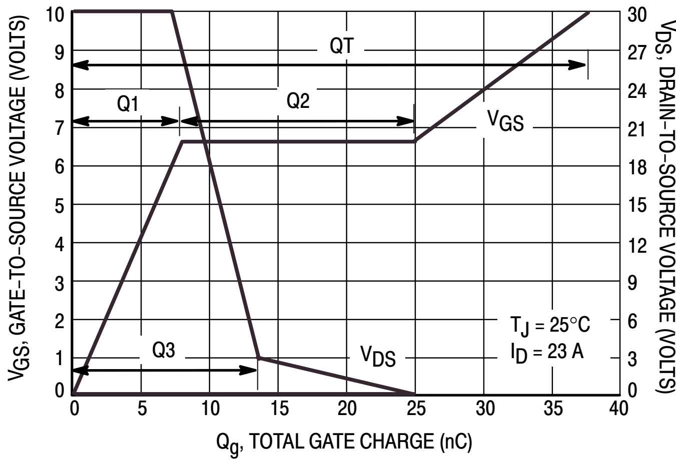



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

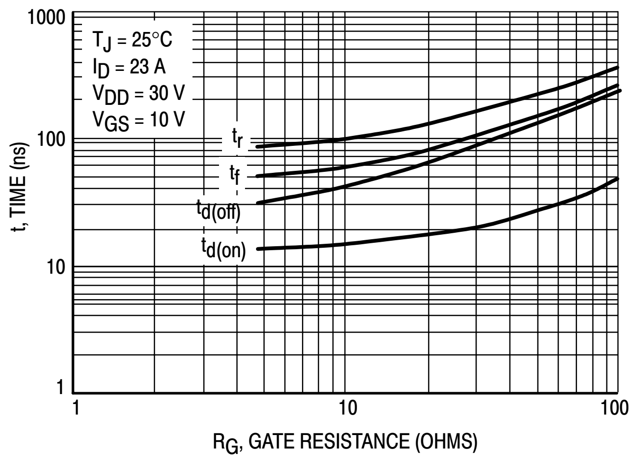



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

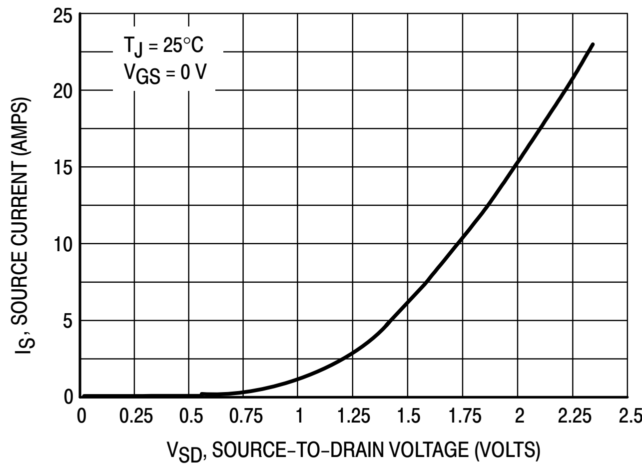



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

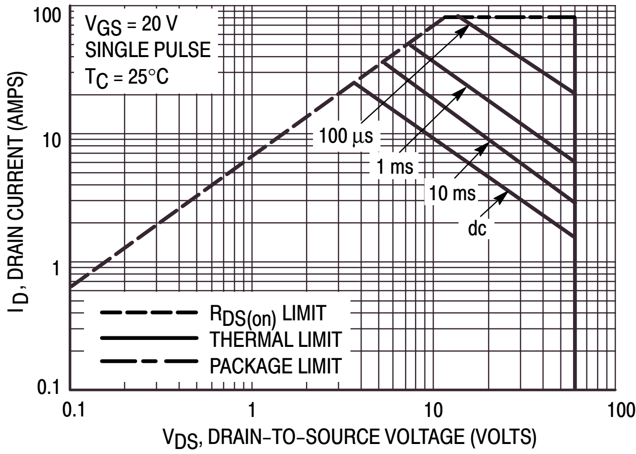



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

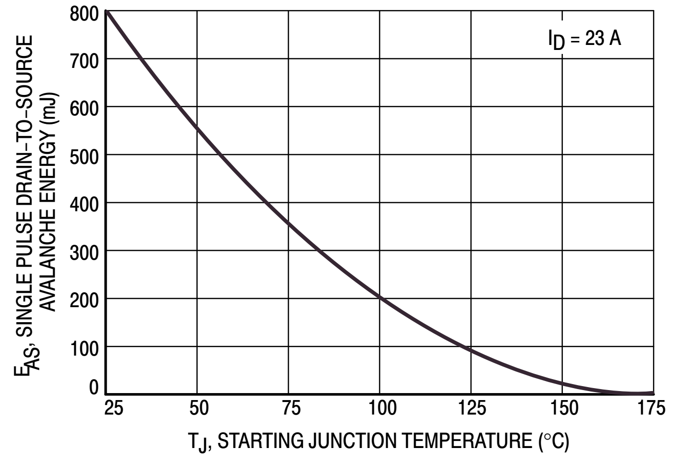



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

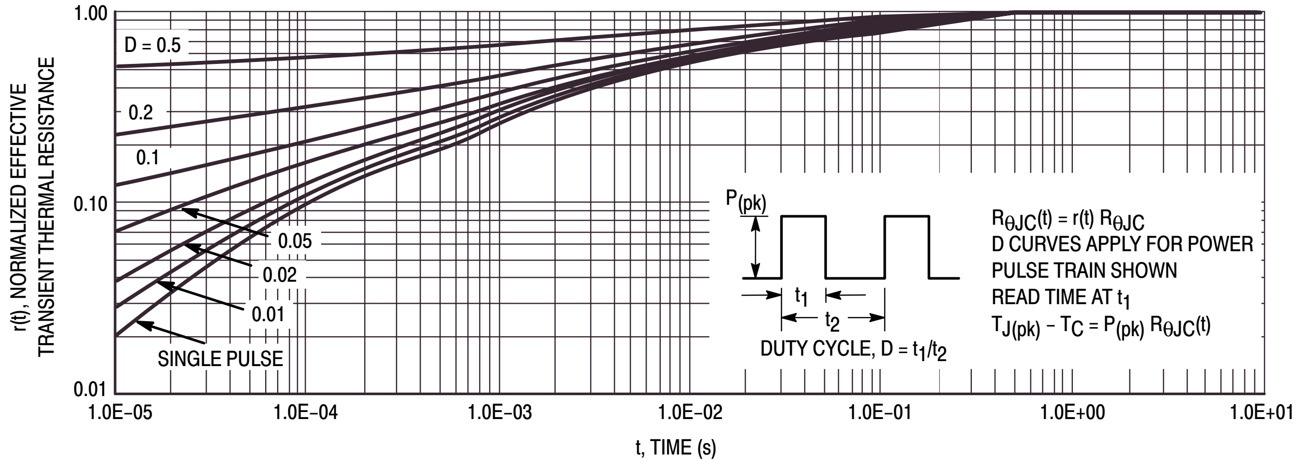



**Figure 13. Thermal Response**

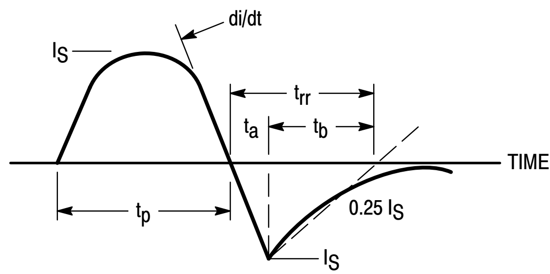



**Figure 14. Diode Reverse Recovery Waveform**

# MTP27N10E

Preferred Device

# Power MOSFET 27 Amps, 100 Volts

## N–Channel TO–220

**ON Semiconductor™**

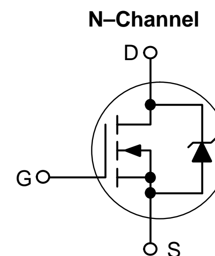
http://onsemi.com

**27 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 70 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

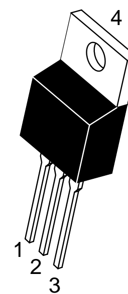
**N–Channel**



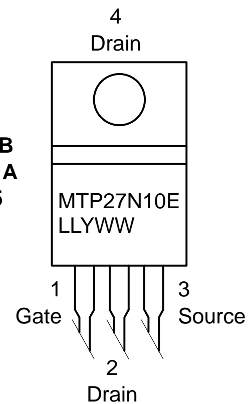

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage – Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ± 20<br>± 40 | Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 27<br>17<br>95 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 104<br>0.83 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 75 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 27 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 109 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.2<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




TO–220AB
CASE 221A
STYLE 5




MTP27120E = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP27N10E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>100<br>– | <br>–<br>120 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.1<br>7.0 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 13.5 Adc) | $R_{DS(on)}$ | <br>– | <br>0.058 | <br>0.07 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 27 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 13.5 Adc, $T_J$ = 125°C) | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>2.3<br>2.0 | Vdc |
| Forward Transconductance ($V_{DS}$ = 7.7 Vdc, $I_D$ = 13.5 Adc) | $g_{FS}$ | 6.0 | 11 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1131 | 1580 | pF |
| Output Capacitance | $C_{oss}$ | – | 468 | 660 | |
| Transfer Capacitance | $C_{rss}$ | – | 186 | 370 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | |
| Turn–On Delay Time ($V_{DD}$ = 50 Vdc, $I_D$ = 27 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 13 | 30 | ns |
| Rise Time | $t_r$ | – | 142 | 280 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 29 | 60 | |
| Fall Time | $t_f$ | – | 59 | 120 | |
| Gate Charge (See Figure 8) ($V_{DS}$ = 80 Vdc, $I_D$ = 27 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 41 | 60 | nC |
| | $Q_1$ | – | 9.0 | – | |
| | $Q_2$ | – | 25 | – | |
| | $Q_3$ | – | 22 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>1.0<br>0.94 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time ($I_S$ = 27 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 126 | – | ns |
| | $t_a$ | – | 98 | – | |
| | $t_b$ | – | 28 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.685 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_D$ | <br>– | <br>3.5<br>4.5 | <br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

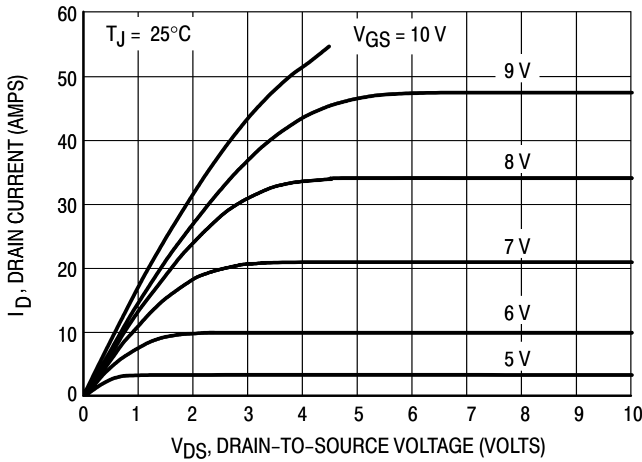



**Figure 1. On–Region Characteristics**

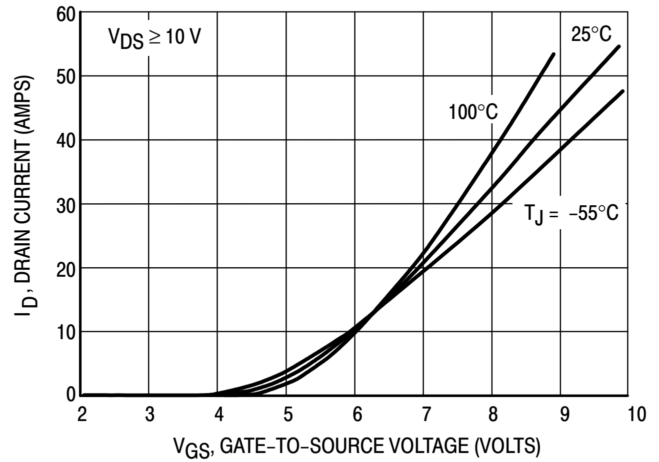



**Figure 2. Transfer Characteristics**

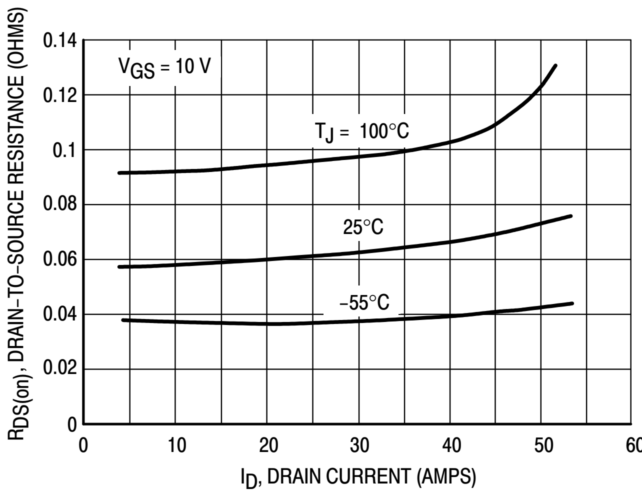



**Figure 3. On–Resistance versus Drain Current and Temperature**

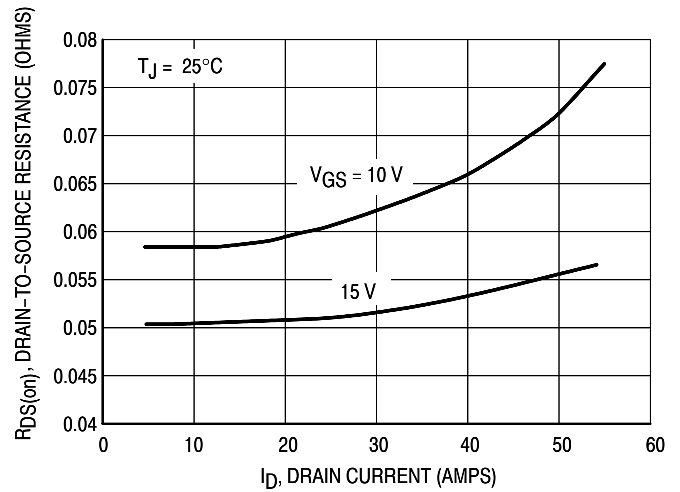



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

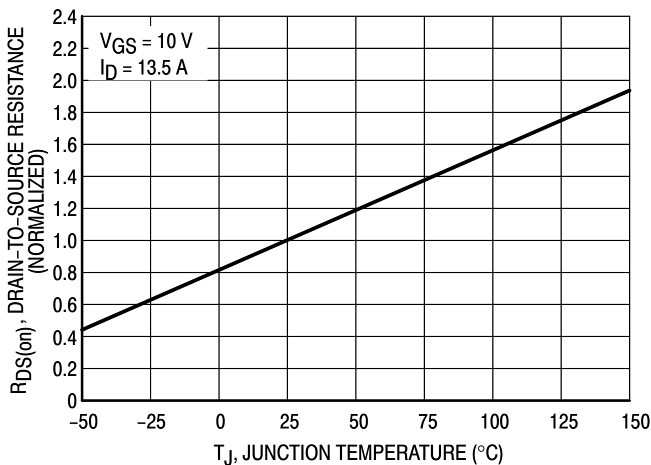



**Figure 5. On–Resistance Variation with Temperature**

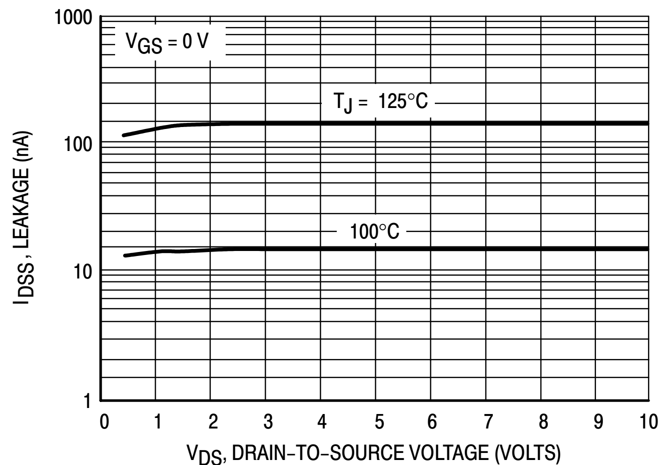



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \ C_{iss} \ In \ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \ C_{iss} \ In \ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

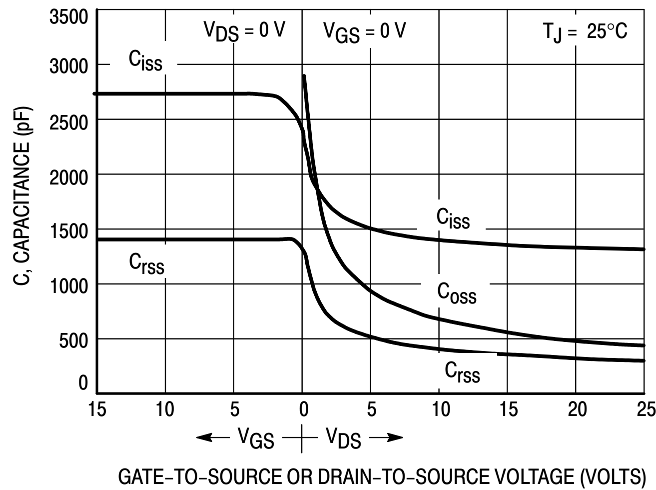



**Figure 7. Capacitance Variation**

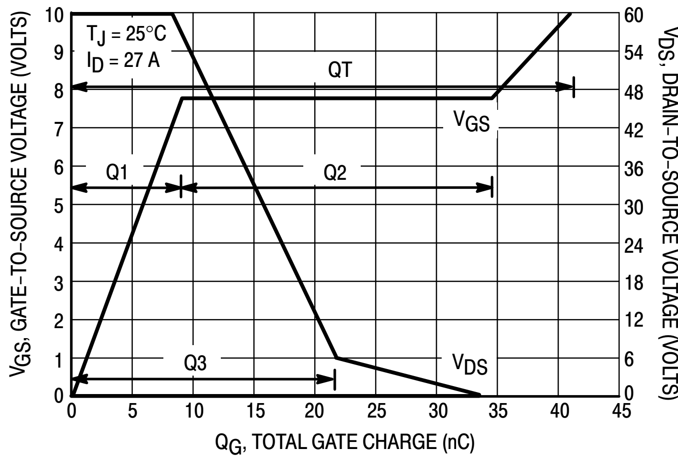



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

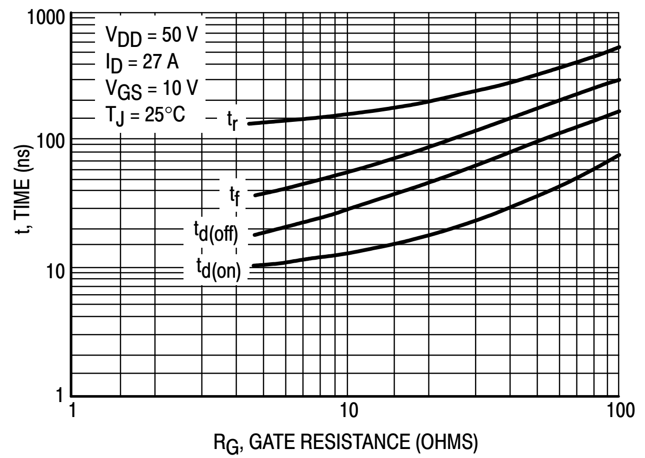



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

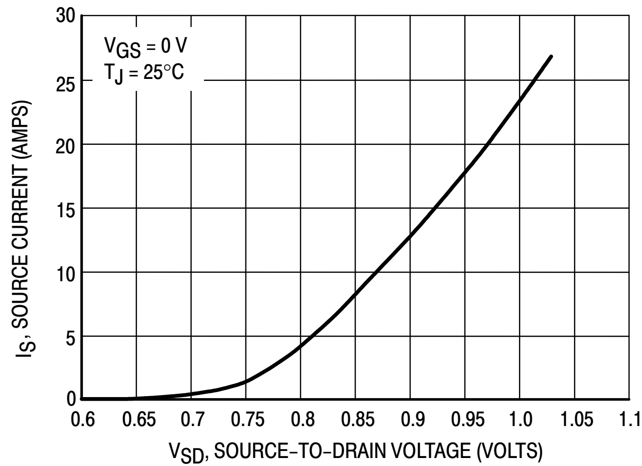



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

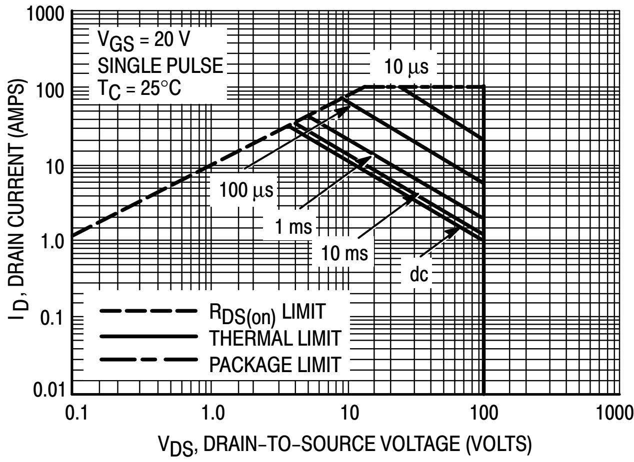



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

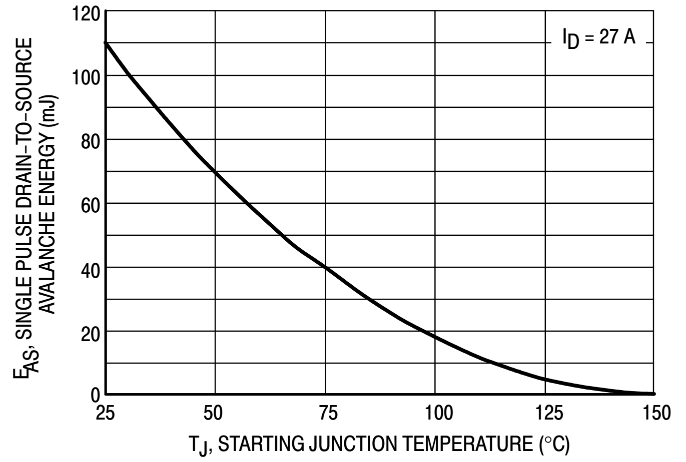



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

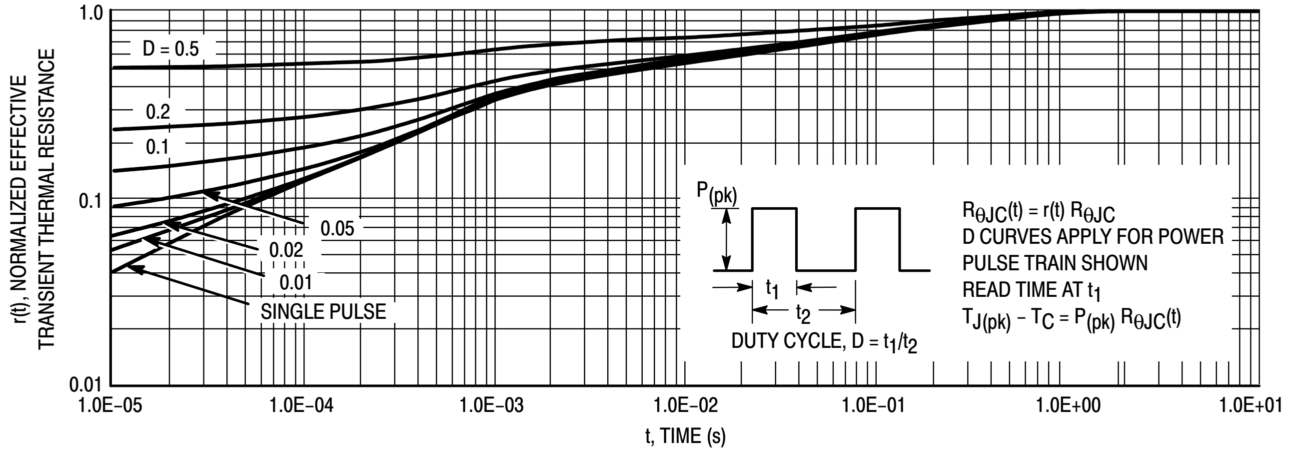



**Figure 13. Thermal Response**

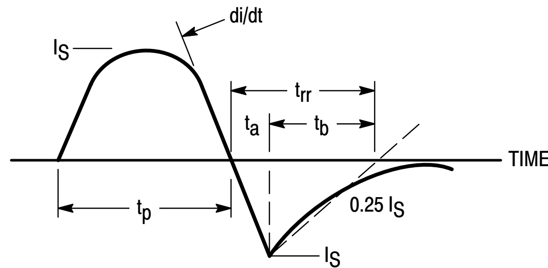



**Figure 14. Diode Reverse Recovery Waveform**

# MTP2955V

Preferred Device

# Power MOSFET 12 Amps, 60 Volts

## P–Channel TO–220

**ON Semiconductor**™

http://onsemi.com

**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 230 mΩ**

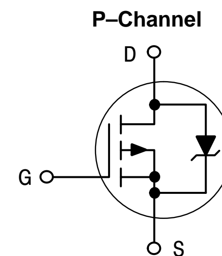
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

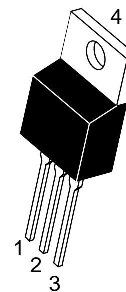
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>8.0<br>42 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 60<br>0.40 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 12 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 216 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>2.5<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

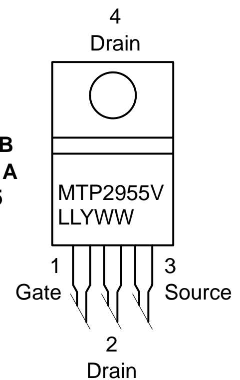
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP2955V | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP2955V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>58 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | µAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 µAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.8<br>5.0 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 1.5) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.185 | 0.230 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 12 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>2.9<br>2.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 3.0 | 5.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 550 | 700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 200 | 280 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 50 | 100 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 50 | 100 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 24 | 50 | |
| Fall Time | | $t_f$ | – | 39 | 80 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 19 | 30 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 9.0 | – | |
| | | $Q_3$ | – | 7.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>–<br>– | <br>1.8<br>1.5 | <br>3.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/µs) | $t_{rr}$ | – | 115 | – | ns |
| | | $t_a$ | – | 90 | – | |
| | | $t_b$ | – | 25 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.53 | – | µC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

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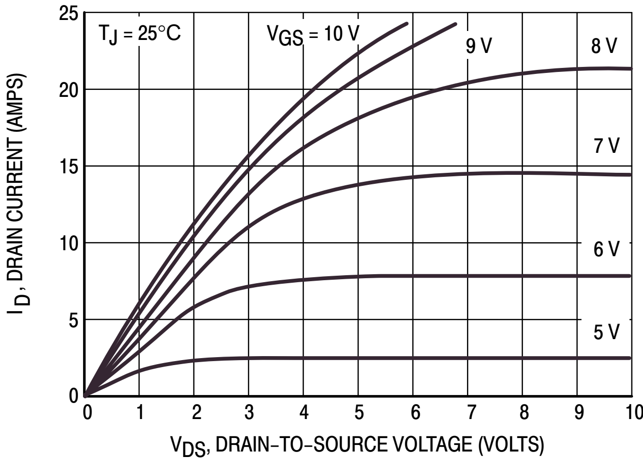


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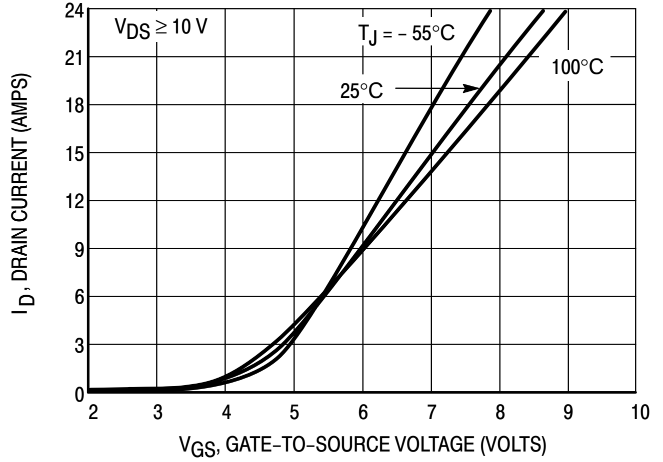


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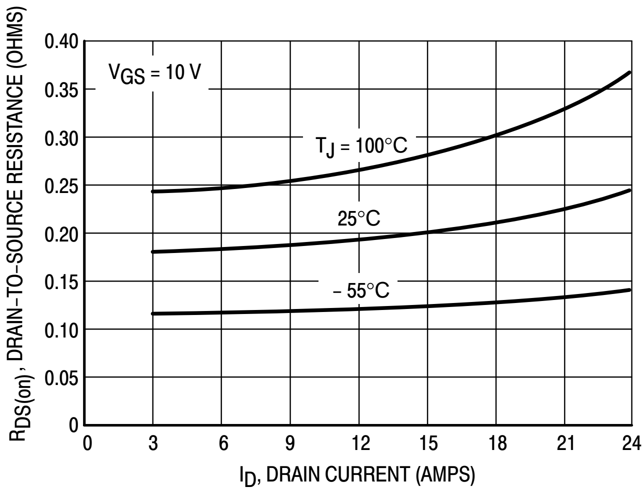
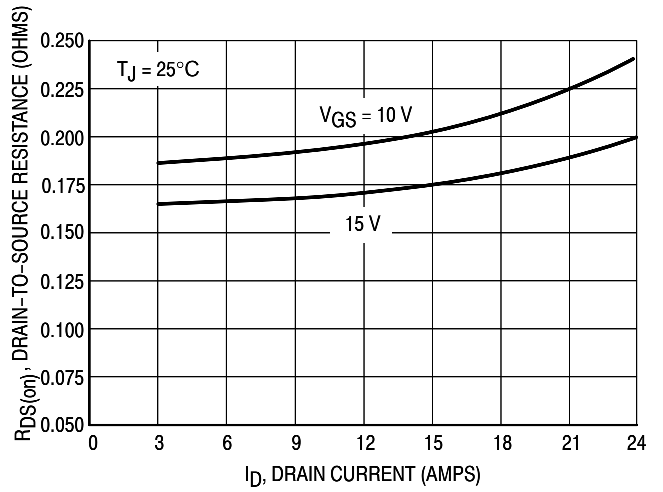



**Figure 3. On–Resistance versus Drain Current and Temperature**

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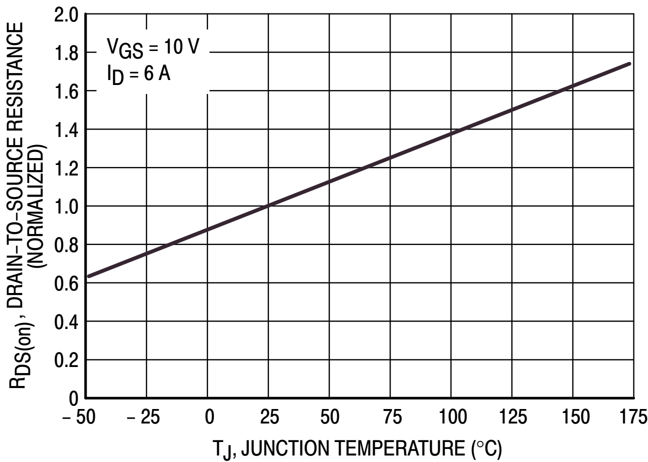


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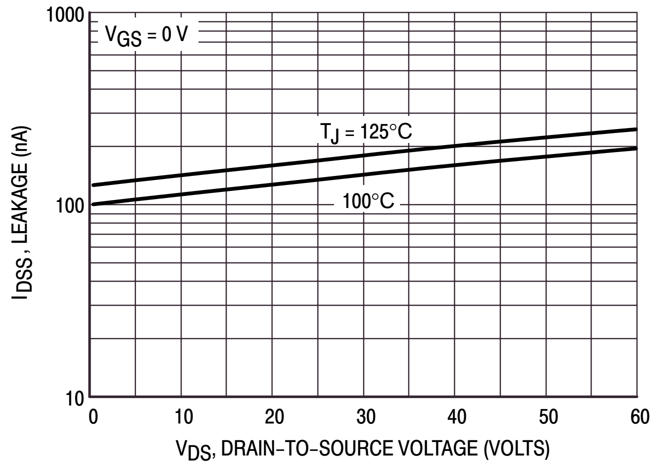


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$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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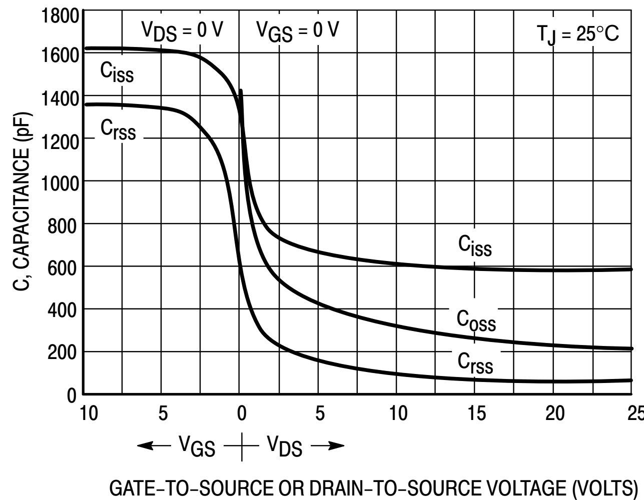


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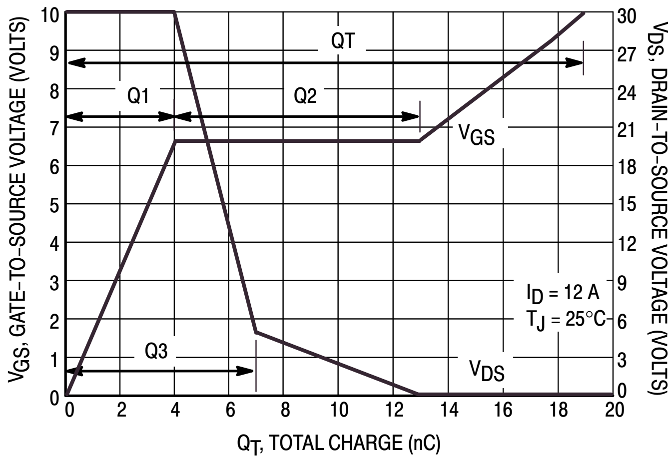



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

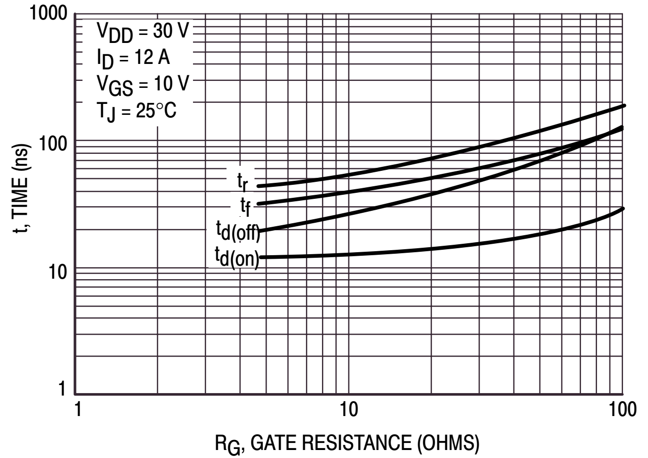



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

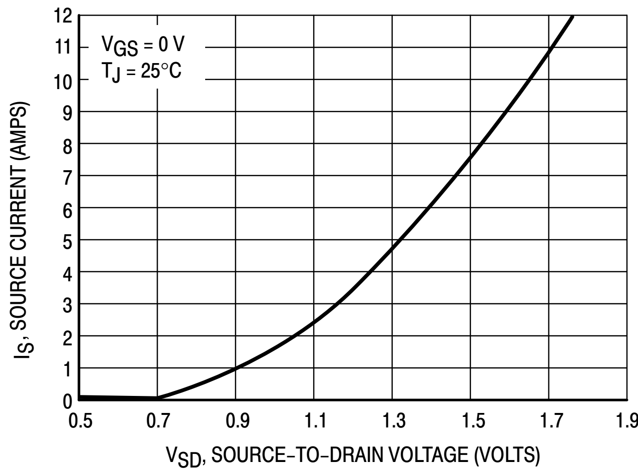



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

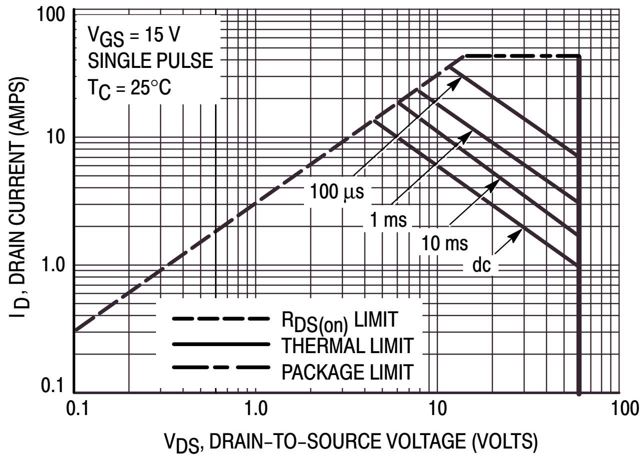



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

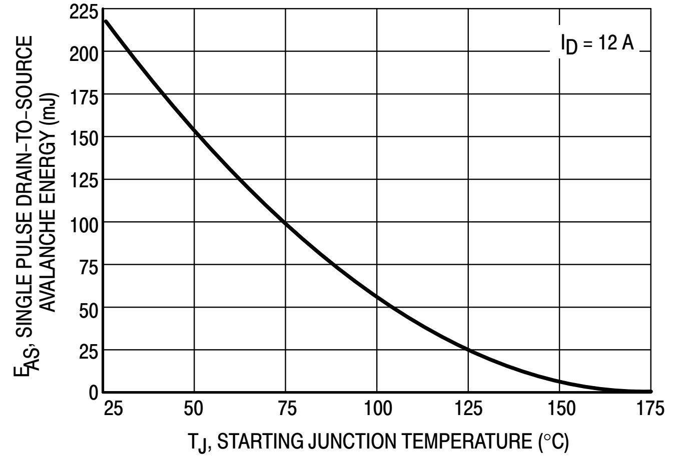



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

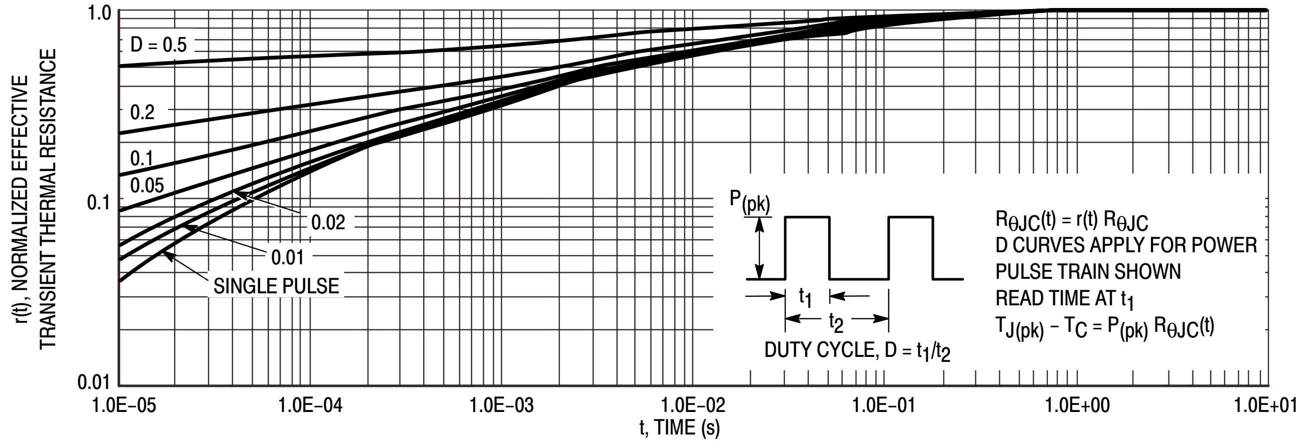



**Figure 13. Thermal Response**

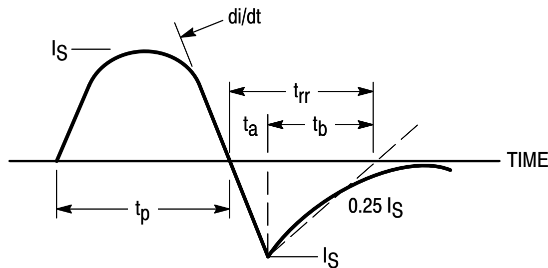



**Figure 14. Diode Reverse Recovery Waveform**

# MTP29N15E

**Preferred Device**

# Power MOSFET 29 Amps, 150 Volts

## N–Channel TO–220

**ON Semiconductor™**

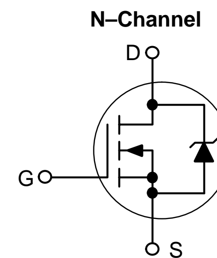
**http://onsemi.com**

**29 AMPERES**
**150 VOLTS**
**$R_{DS(on)}$ = 70 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls. These devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

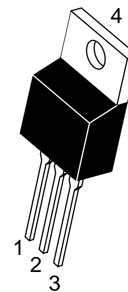
**N–Channel**



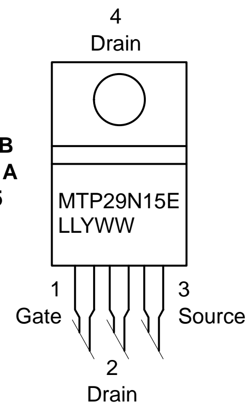

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 150 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 150 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 29<br>19<br>102 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 125<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 29 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 421 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP29N15E = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP29N15E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 150 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 151 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ =125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 2.7 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 5.4 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 14.5 Adc) | | $R_{DS(on)}$ | – | 0.054 | 0.07 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 29 Adc) | | $V_{DS(on)}$ | – | – | 2.4 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 14.5 Adc, $T_J$ = 125°C) | | | – | – | 2.1 | |
| Forward Transconductance ($V_{DS}$ = 8.6 Vdc, $I_D$ = 14.5 Adc) | | $g_{FS}$ | 10 | 20 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2300 | 3220 | pF |
| Output Capacitance | | $C_{oss}$ | – | 450 | 630 | |
| Transfer Capacitance | | $C_{rss}$ | – | 130 | 260 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 75 Vdc, $I_D$ = 29 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 19 | 40 | ns |
| Rise Time | | $t_r$ | – | 95 | 190 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 90 | 180 | |
| Fall Time | | $t_f$ | – | 85 | 170 | |
| Gate Charge | ($V_{DS}$ = 120 Vdc, $I_D$ = 29 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 83 | 120 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 37 | – | |
| | | $Q_3$ | – | 23 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.92 | 1.3 | Vdc |
| | ($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.84 | – | |
| Reverse Recovery Time | ($I_S$ = 29 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 174 | – | ns |
| | | $t_a$ | – | 126 | – | |
| | | $t_b$ | – | 48 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.4 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) | | $L_D$ | – | 3.5 | – | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | – | 4.5 | – | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

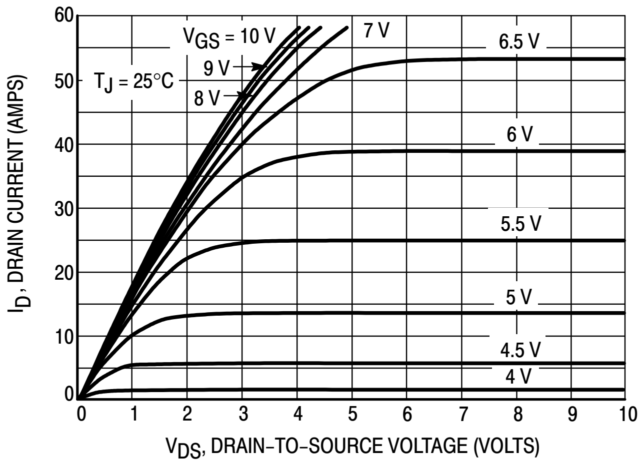



**Figure 1. On–Region Characteristics**

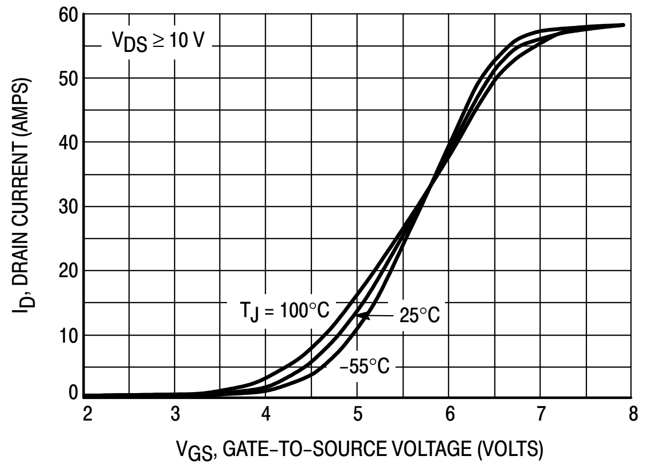



**Figure 2. Transfer Characteristics**

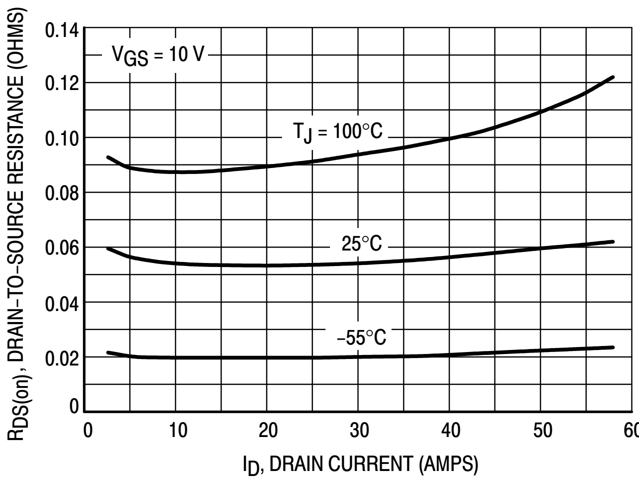



**Figure 3. On–Resistance versus Drain Current and Temperature**

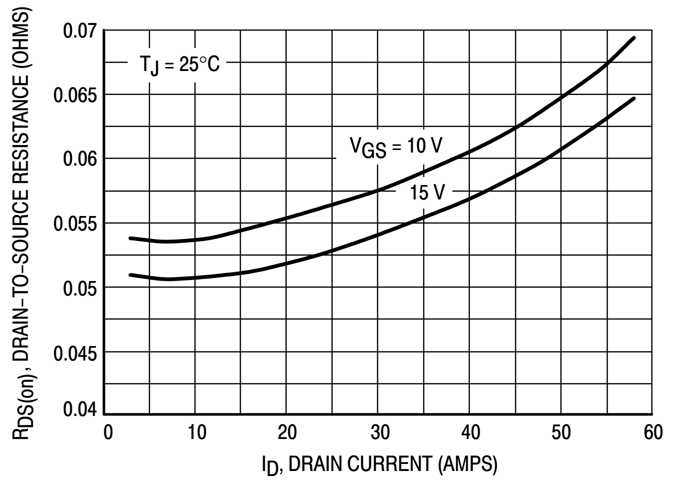



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

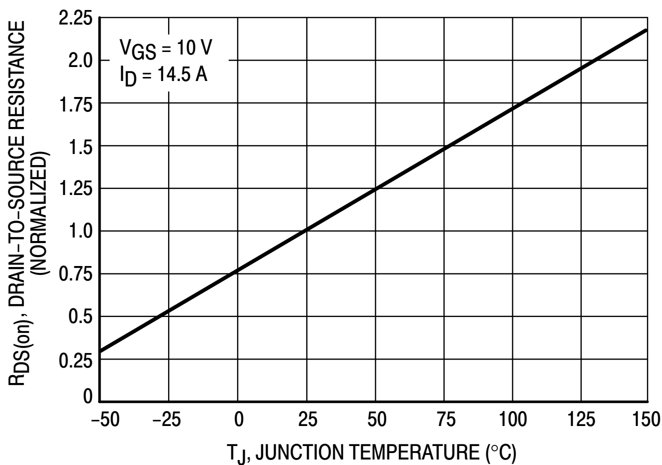



**Figure 5. On–Resistance Variation with Temperature**

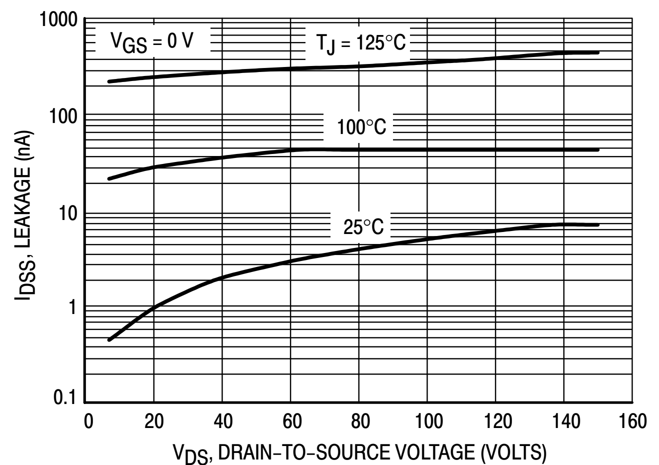



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

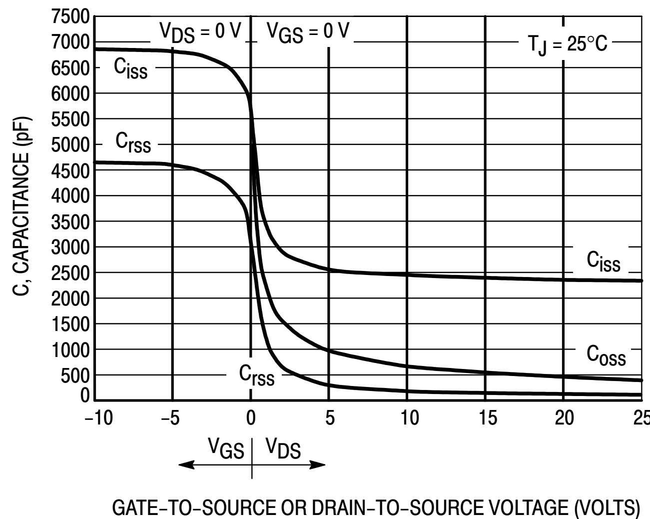



**Figure 7. Capacitance Variation**

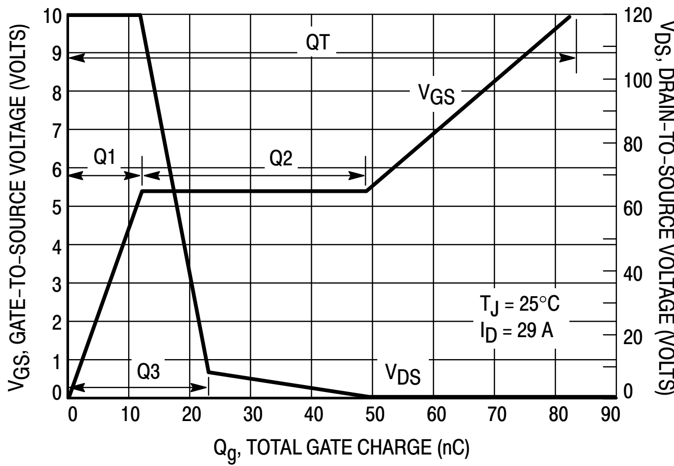



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

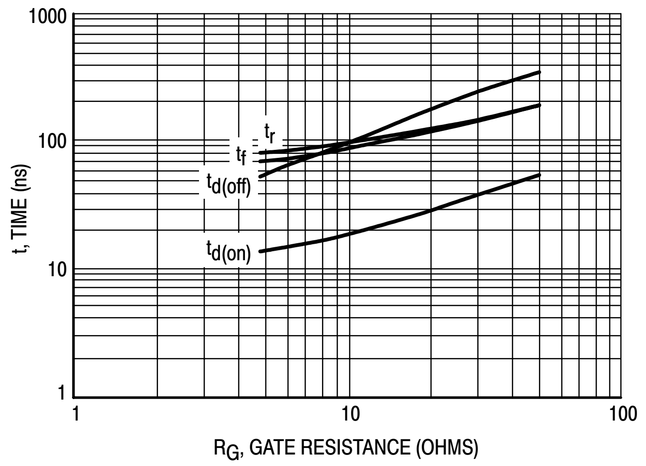



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 15. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

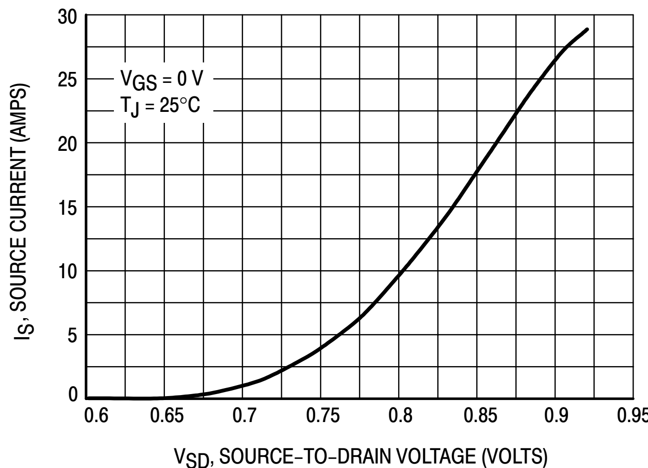



**Figure 10. Diode Forward Voltage versus Current**

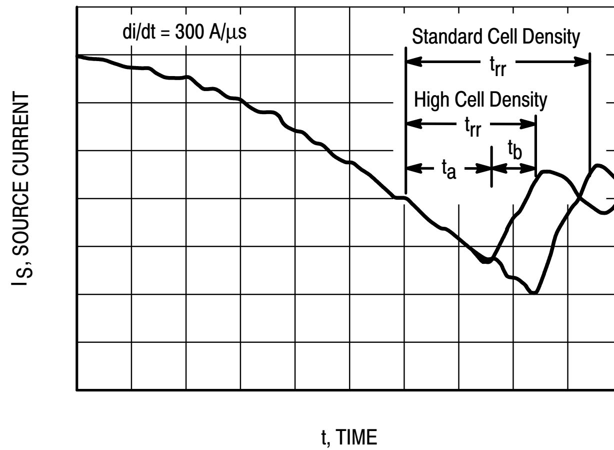



Figure 11. Reverse Recovery Time ($t_{rr}$)

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

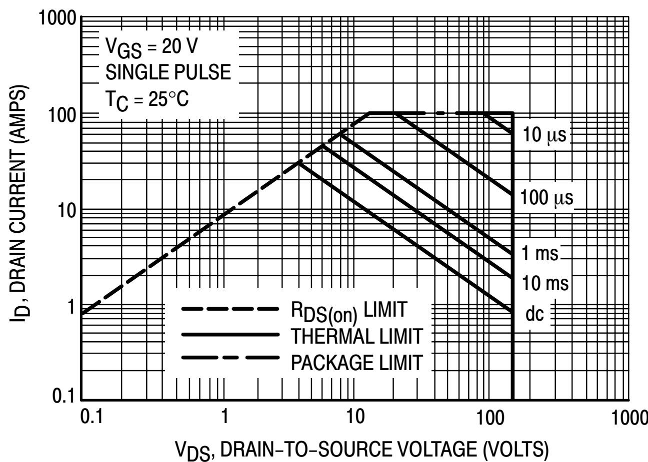



Figure 12. Maximum Rated Forward Biased Safe Operating Area

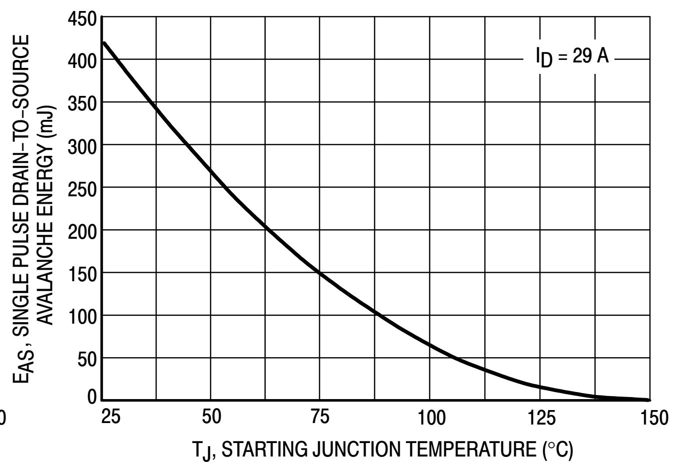



Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature

## TYPICAL ELECTRICAL CHARACTERISTICS

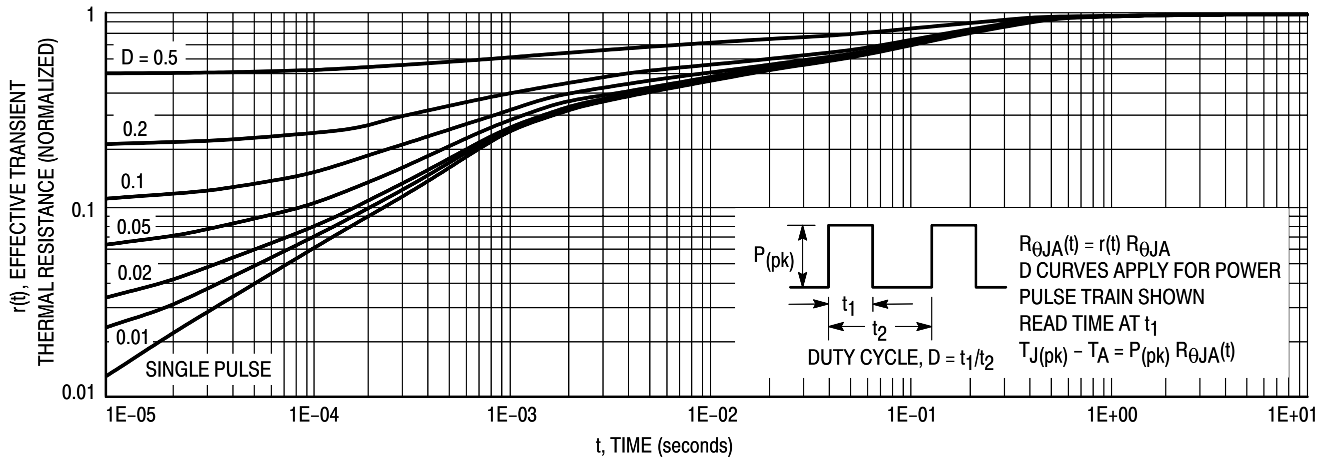



**Figure 14. Thermal Response**

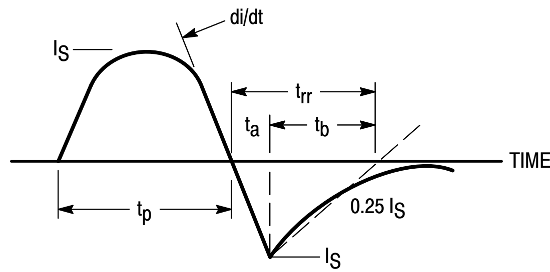



**Figure 15. Diode Reverse Recovery Waveform**

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

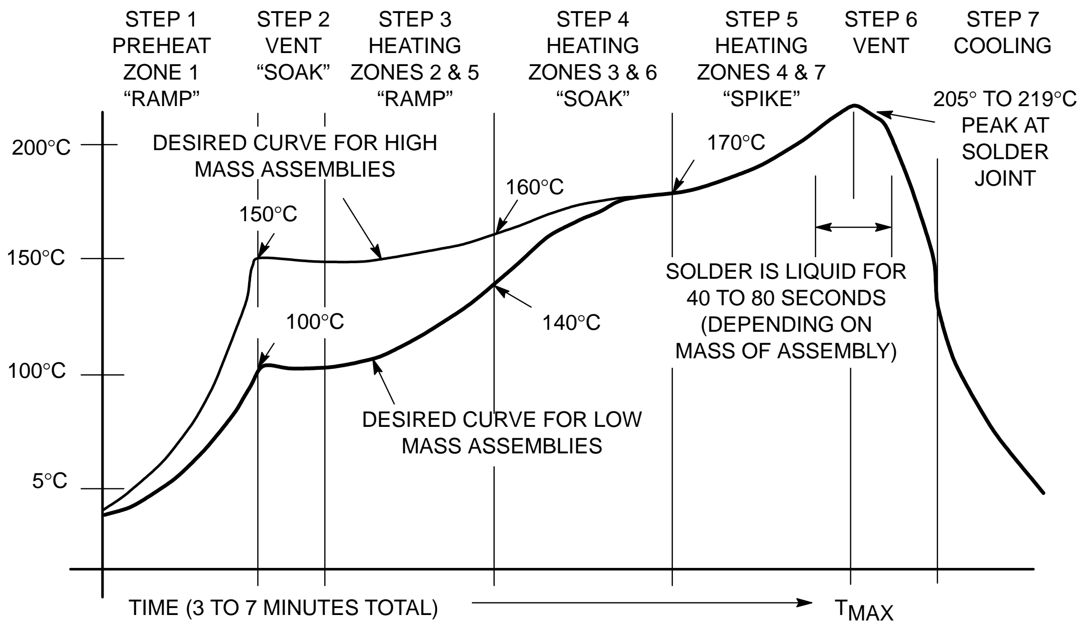



**Figure 16. Typical Solder Heating Profile**

# MTP2P50E

Preferred Device

# Power MOSFET 2 Amps, 500 Volts

## P–Channel TO–220

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

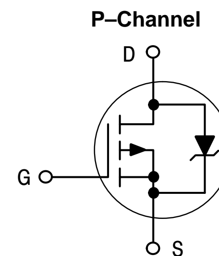
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 500 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 500 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 2.0<br>1.6<br>6.0 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 100 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 4.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 80 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

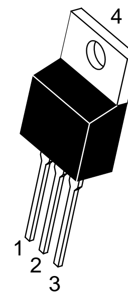
http://onsemi.com

**2 AMPERES**
**500 VOLTS**
**$R_{DS(on)}$ = 6 Ω**

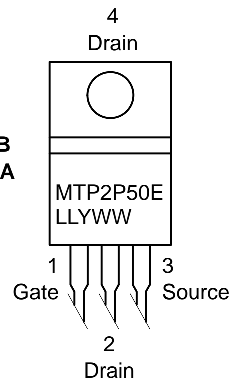
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP2P50E | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP2P50E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 500<br>– | –<br>564 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 500 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 500 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 3.0<br>4.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 1.0 Adc) | | $R_{DS(on)}$ | – | 4.5 | 6.0 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 2.0 Adc)<br>($I_D$ = 1.0 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 9.5<br>– | 14.4<br>12.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 1.0 Adc) | | $g_{FS}$ | 0.5 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 845 | 1183 | pF |
| Output Capacitance | | $C_{oss}$ | – | 100 | 140 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 26 | 52 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 250 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 24 | ns |
| Rise Time | | $t_r$ | – | 14 | 28 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 21 | 42 | |
| Fall Time | | $t_f$ | – | 19 | 38 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 400 Vdc, $I_D$ = 2.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 19 | 27 | nC |
| | | $Q_1$ | – | 3.7 | – | |
| | | $Q_2$ | – | 7.9 | – | |
| | | $Q_3$ | – | 9.9 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 2.3<br>1.85 | 3.5<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 2.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 223 | – | ns |
| | | $t_a$ | – | 161 | – | |
| | | $t_b$ | – | 62 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.92 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

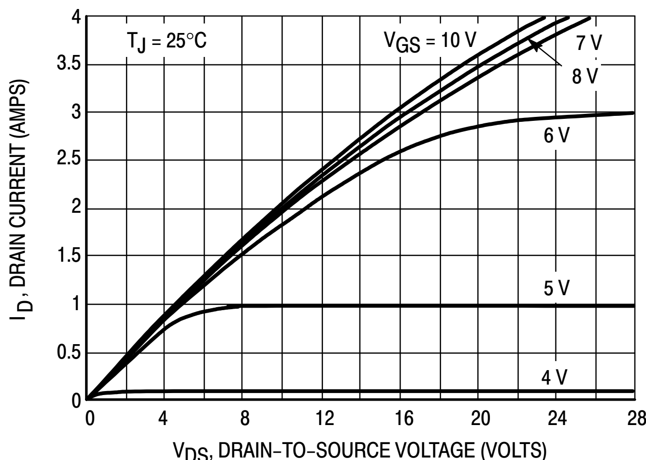



**Figure 1. On–Region Characteristics**

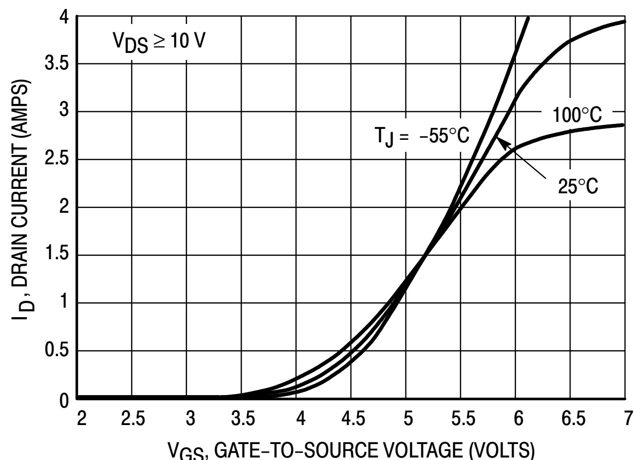



**Figure 2. Transfer Characteristics**

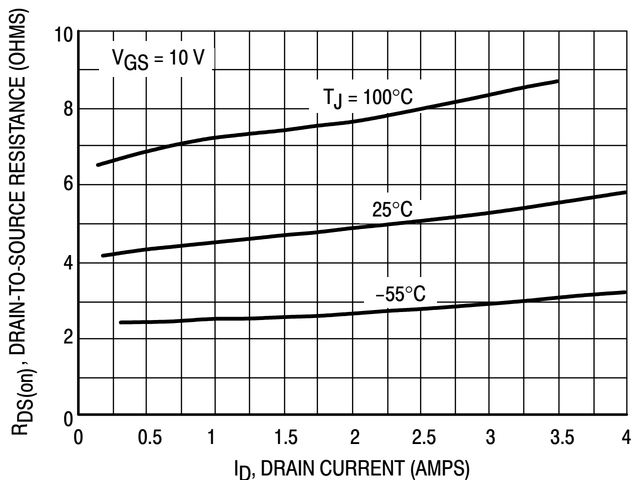



**Figure 3. On–Resistance versus Drain Current and Temperature**

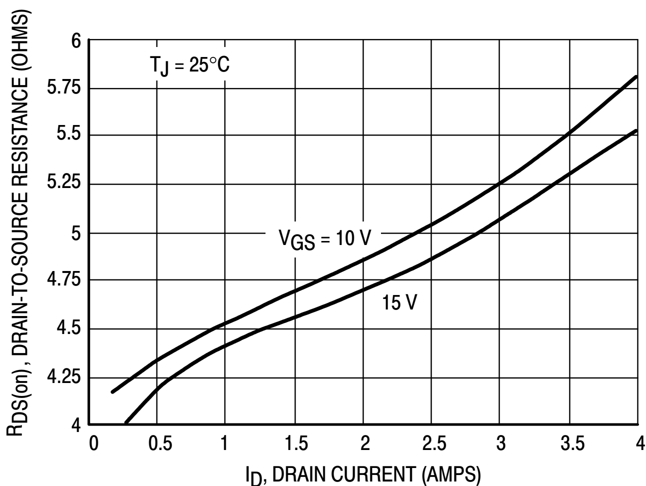



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

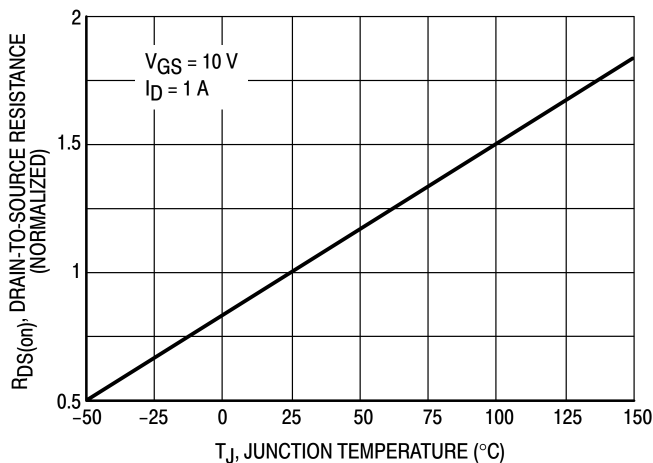



**Figure 5. On–Resistance Variation with Temperature**

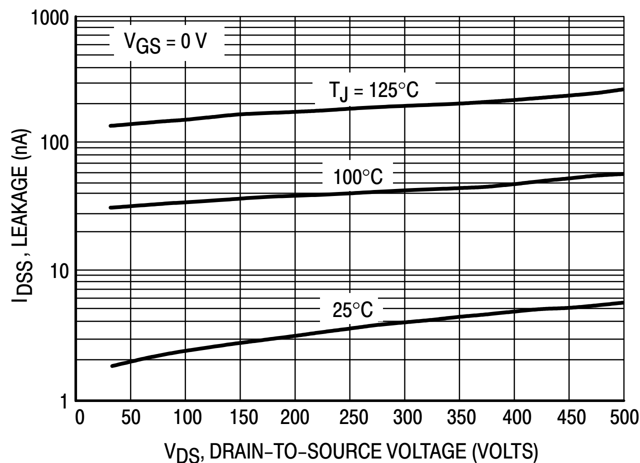



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

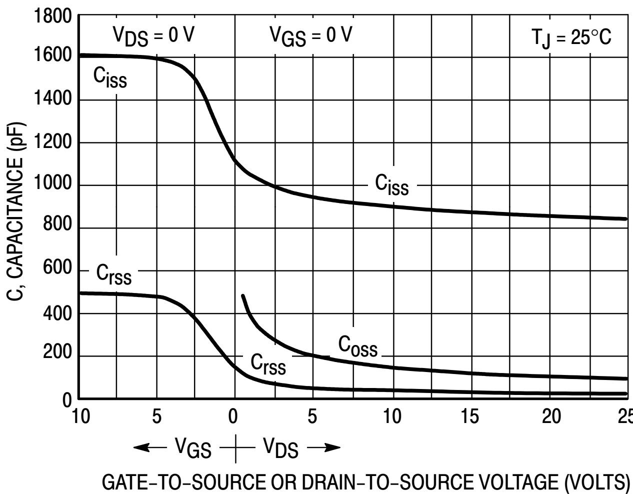



**Figure 7a. Capacitance Variation**

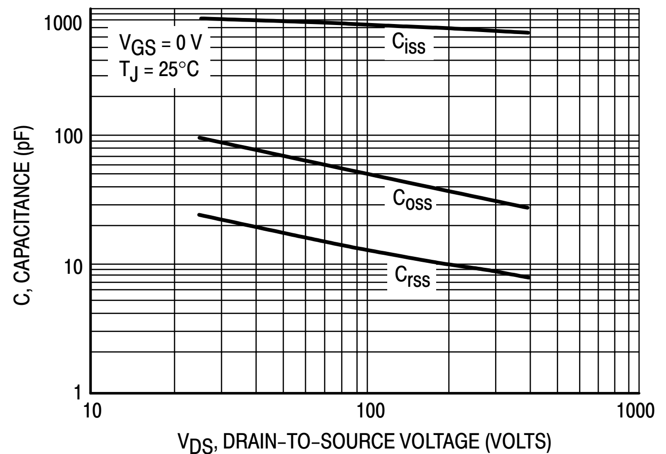



**Figure 7b. High Voltage Capacitance Variation**

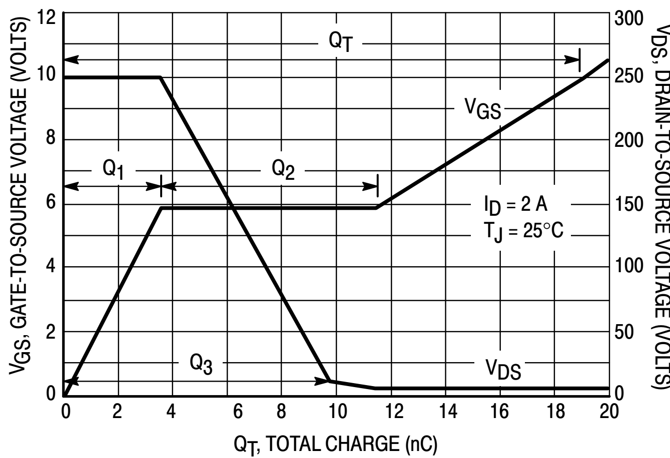



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

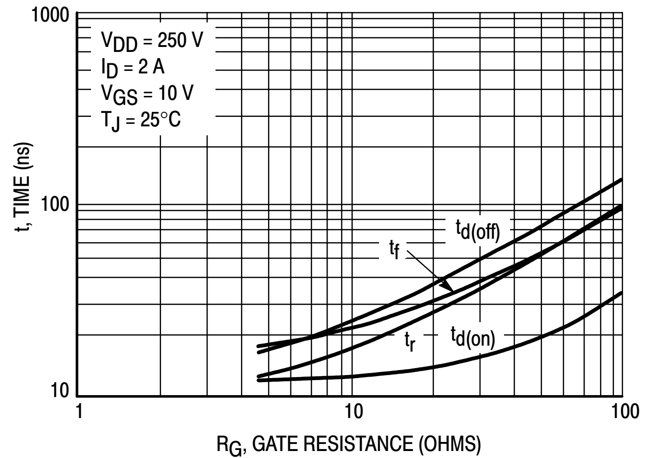



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

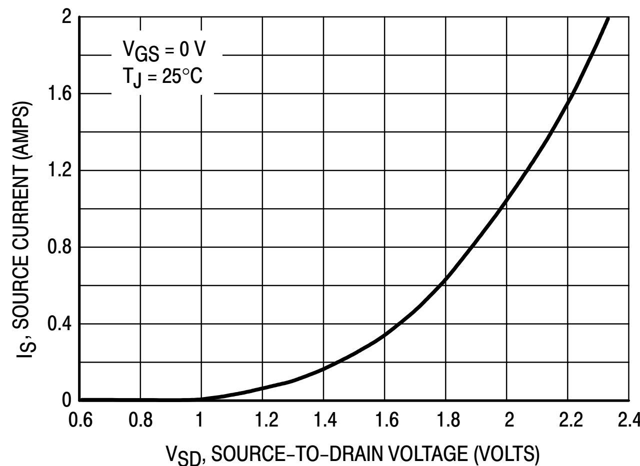



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

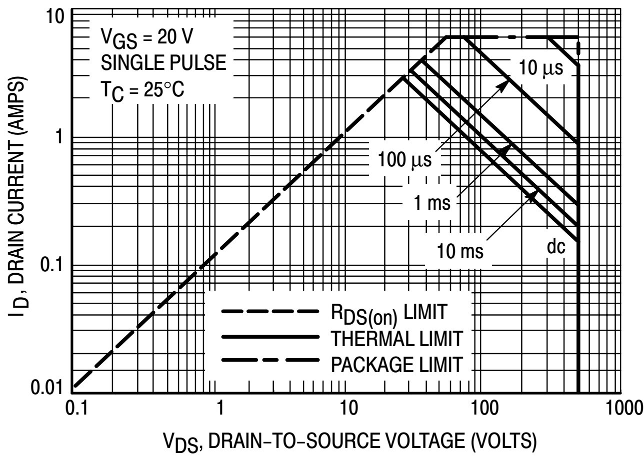



Figure 11. Maximum Rated Forward Biased Safe Operating Area

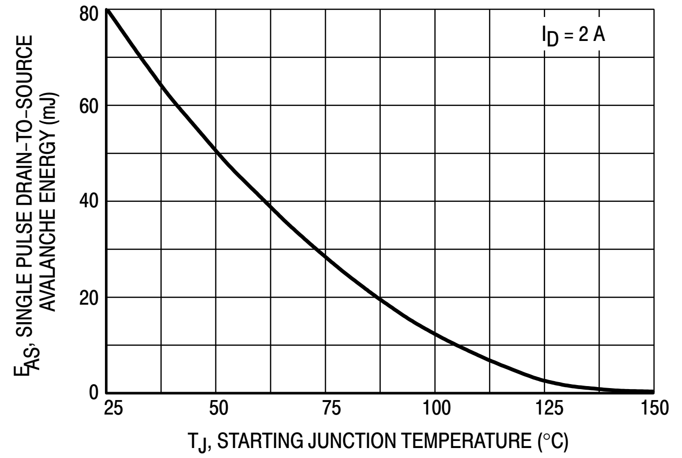



Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

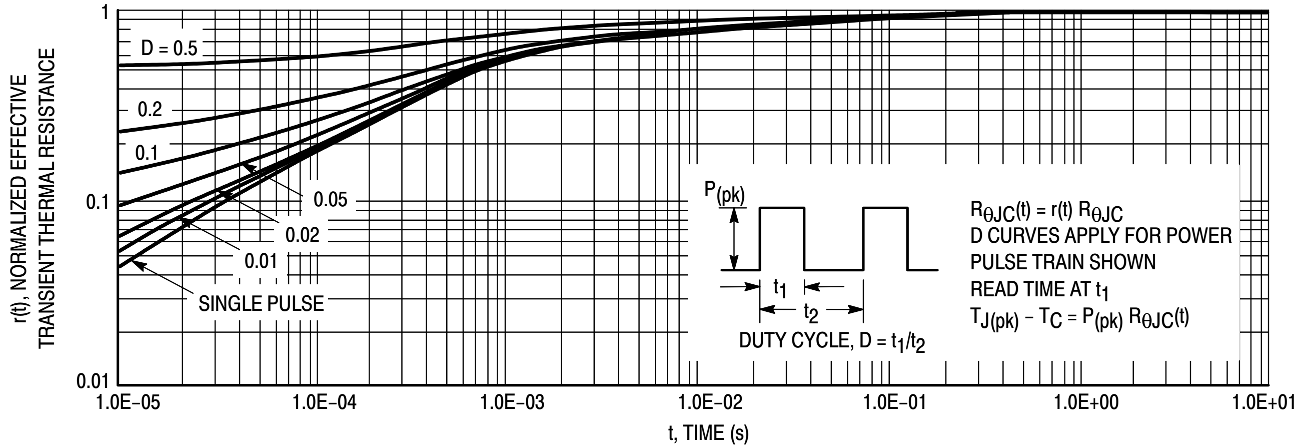



Figure 13. Thermal Response

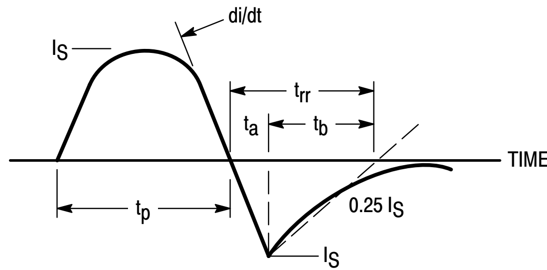



Figure 14. Diode Reverse Recovery Waveform

# MTP3055V

**Preferred Device**

# Power MOSFET 12 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

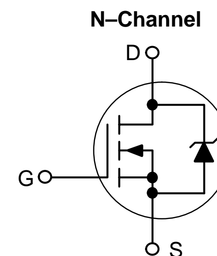
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>7.3<br>37 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 48<br>0.32 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 12 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 72 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 3.13<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

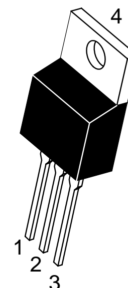
**http://onsemi.com**

**12 AMPERES**
**50 VOLTS**
**$R_{DS(on)}$ = 150 mΩ**

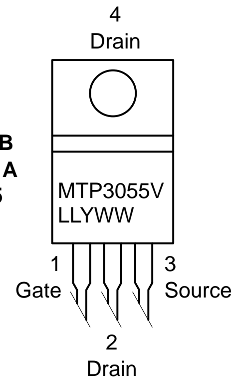
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




TO–220AB
CASE 221A
STYLE 5




| | |
|---|---|
| MTP3055V | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP3055V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>65 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>5.4 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.10 | 0.15 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 12 Adc)<br>($I_D$ = 6.0 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.3<br>– | 2.2<br>1.9 | Vdc |
| Forward Transconductance ($V_{DS}$ = 7.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 4.0 | 5.0 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 410 | 500 | pF |
| Output Capacitance | | $C_{oss}$ | – | 130 | 180 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 25 | 50 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 7.0 | 10 | ns |
| Rise Time | | $t_r$ | – | 34 | 60 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 30 | |
| Fall Time | | $t_f$ | – | 18 | 50 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 12.2 | 17 | nC |
| | | $Q_1$ | – | 3.2 | – | |
| | | $Q_2$ | – | 5.2 | – | |
| | | $Q_3$ | – | 5.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.0<br>0.91 | 1.6<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 15) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 40 | – | |
| | | $t_b$ | – | 16 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.128 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

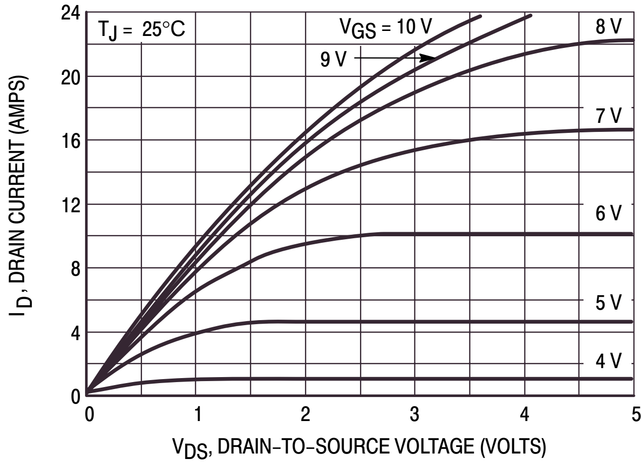



**Figure 1. On–Region Characteristics**

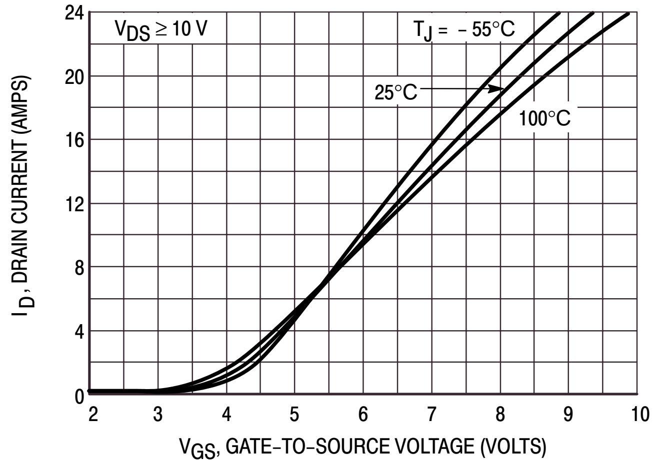



**Figure 2. Transfer Characteristics**

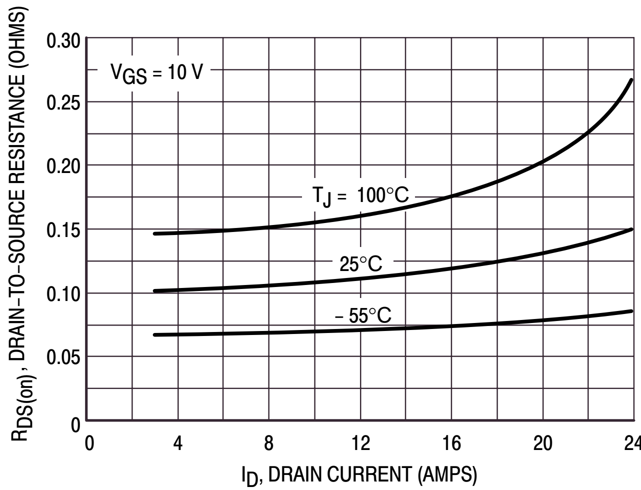



**Figure 3. On–Resistance versus Drain Current and Temperature**

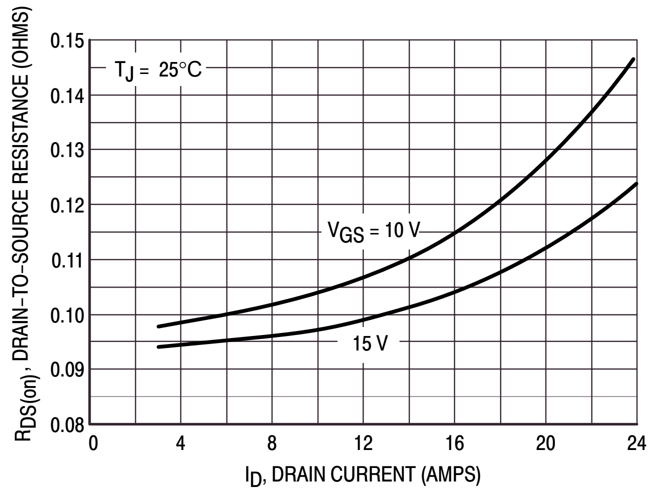



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

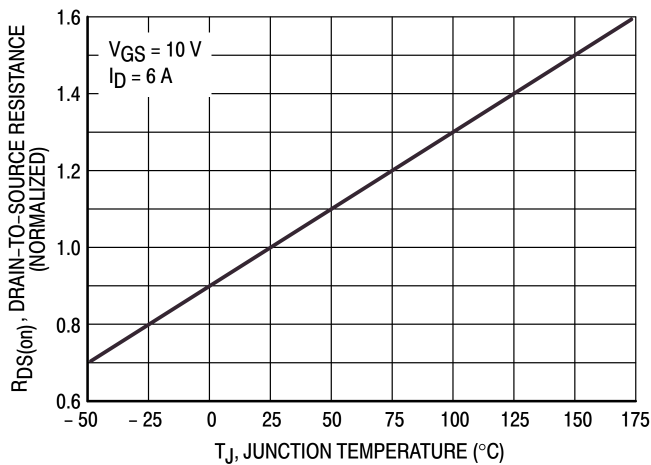



**Figure 5. On–Resistance Variation with Temperature**

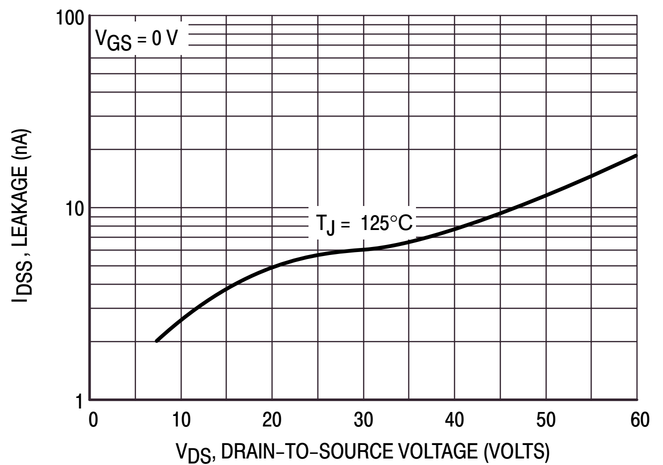



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

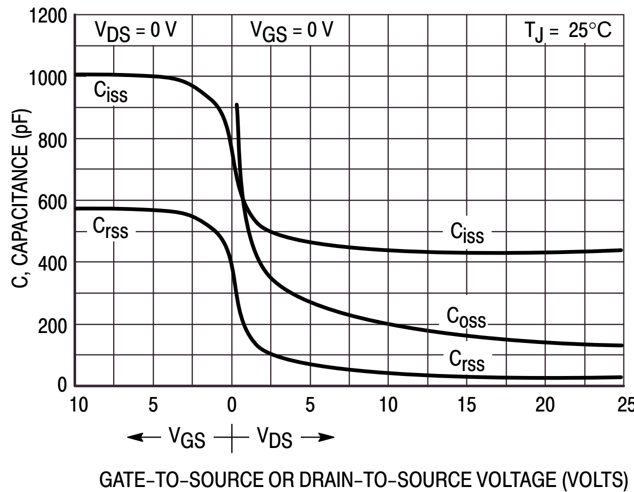



**Figure 7. Capacitance Variation**

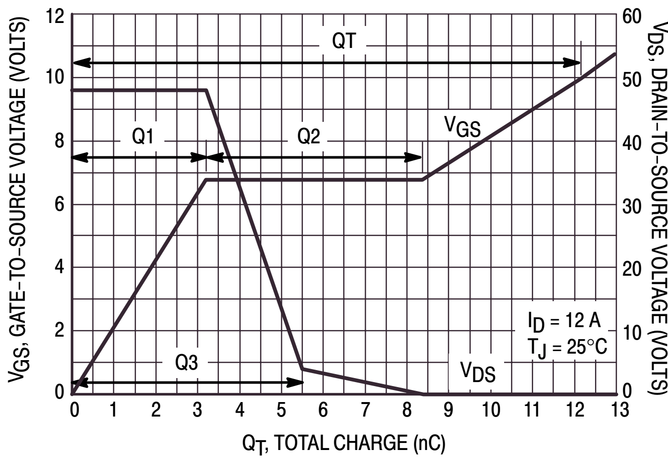



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

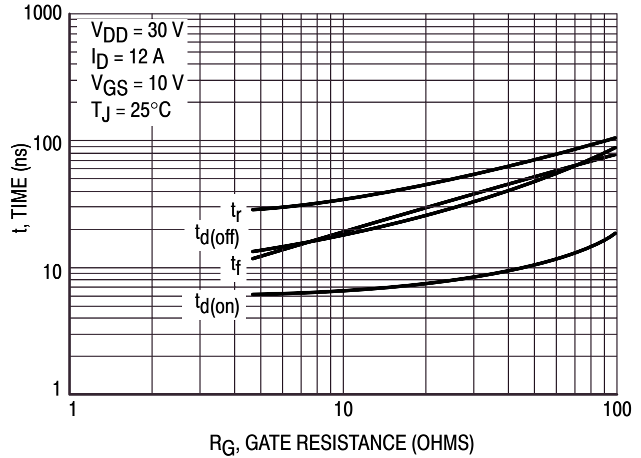



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

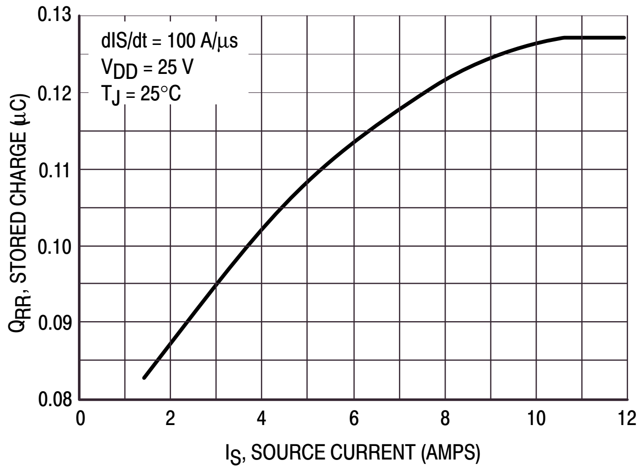



**Figure 10. Stored Charge**

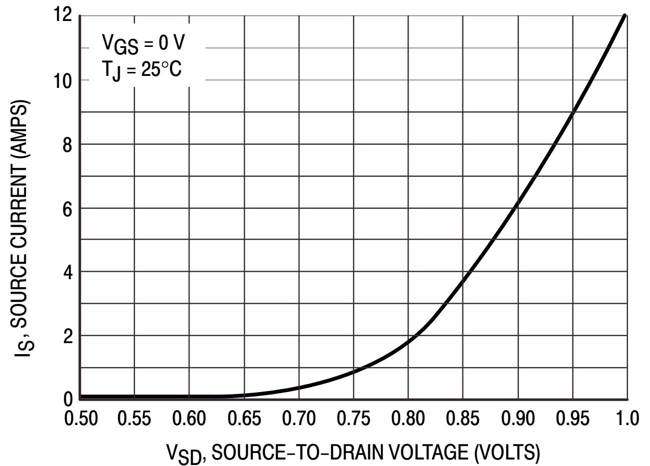



**Figure 11. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

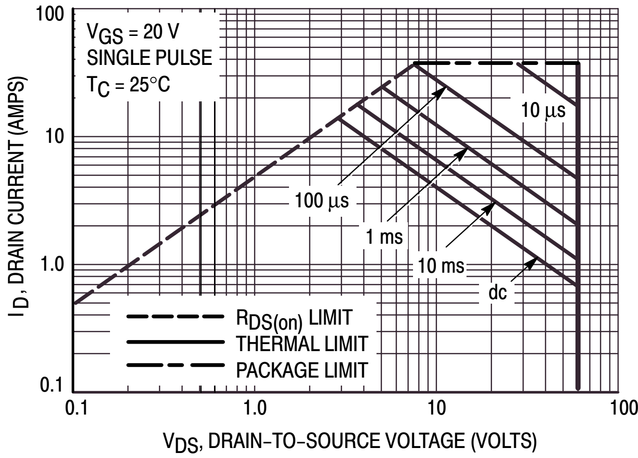



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

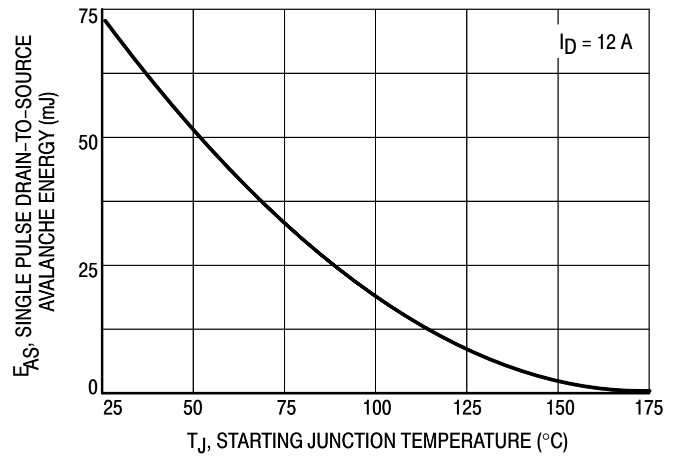



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

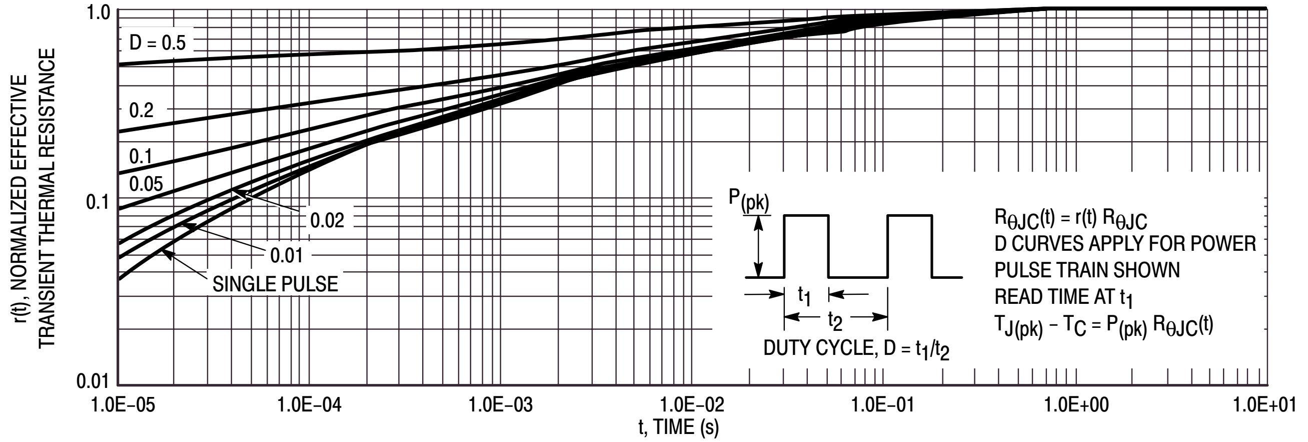



**Figure 14. Thermal Response**

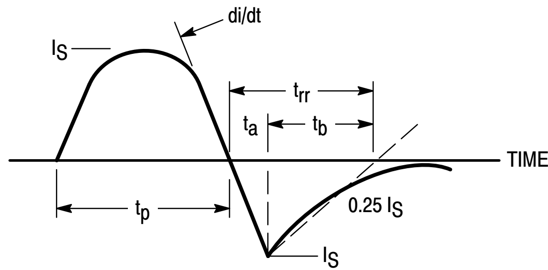



**Figure 15. Diode Reverse Recovery Waveform**

# MTP3055VL

Preferred Device

# Power MOSFET 12 Amps, 60 Volts, Logic Level

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

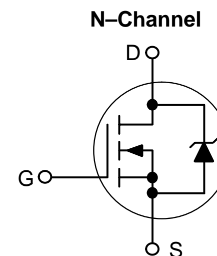
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Single Pulse ($t_p \leq 50\ \mu s$) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq 10\ \mu s$) | $I_D$<br>$I_D$<br>$I_{DM}$ | 12<br>8.0<br>42 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 48<br>0.32 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc,<br>$I_L$ = 12 Apk, L = 1.0 mH, $R_G$ =25 Ω) | $E_{AS}$ | 72 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>3.13<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

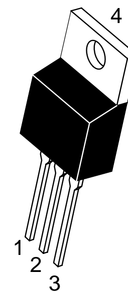
http://onsemi.com

**12 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 180 mΩ**

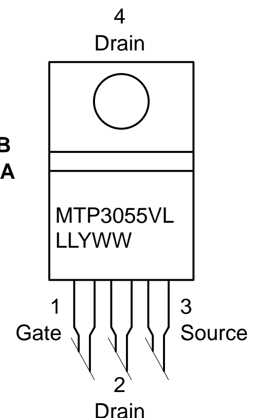
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP3055VL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP3055VL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 62 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±15 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.6 | 2.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 3.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 6.0 Adc) | | $R_{DS(on)}$ | – | 0.12 | 0.18 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc) ($I_D$ = 12 Adc) | | $V_{DS(on)}$ | – | 1.6 | 2.6 | Vdc |
| ($I_D$ = 6.0 Adc, $T_J$ = 150°C) | | | – | – | 2.5 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 6.0 Adc) | | $g_{FS}$ | 5.0 | 8.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 410 | 570 | pF |
| Output Capacitance | | $C_{oss}$ | – | 114 | 160 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 21 | 40 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 9.0 | 20 | ns |
| Rise Time | | $t_r$ | – | 85 | 190 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 14 | 30 | |
| Fall Time | | $t_f$ | – | 43 | 90 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 12 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 8.1 | 10 | nC |
| | | $Q_1$ | – | 1.8 | – | |
| | | $Q_2$ | – | 4.2 | – | |
| | | $Q_3$ | – | 3.8 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.97 | 1.3 | Vdc |
| | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | – | 0.86 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 12 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 55.7 | – | ns |
| | | $t_a$ | – | 37 | – | |
| | | $t_b$ | – | 18.7 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.116 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) | | $L_D$ | – | 3.5 | – | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | | 4.5 | | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

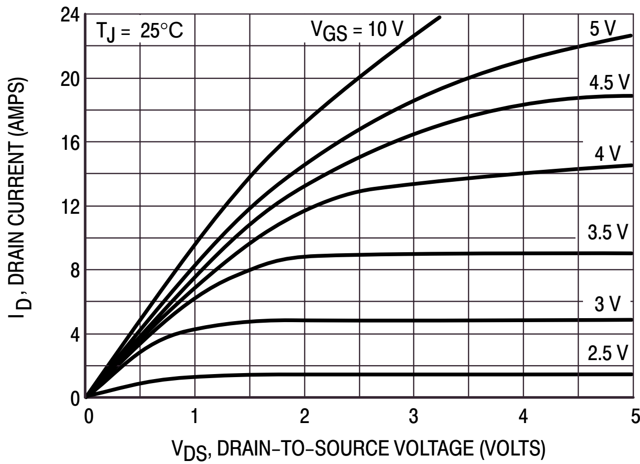



**Figure 1. On–Region Characteristics**

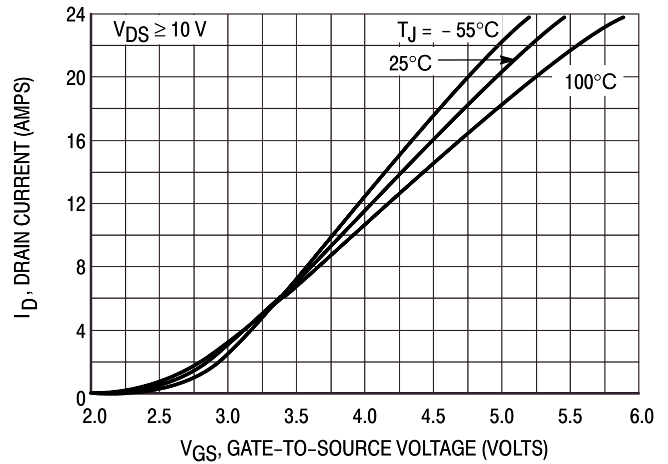



**Figure 2. Transfer Characteristics**

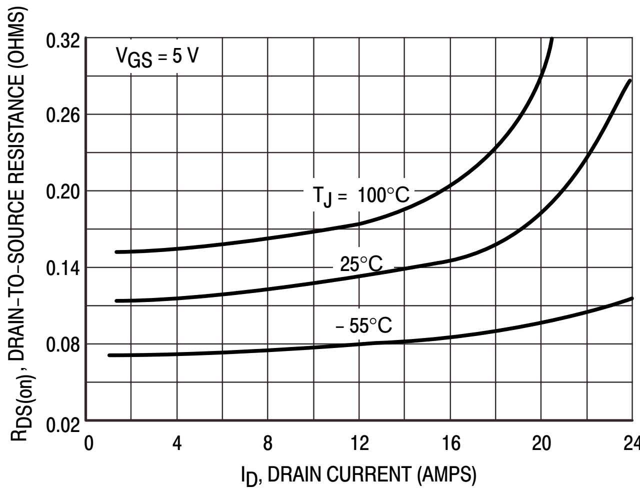
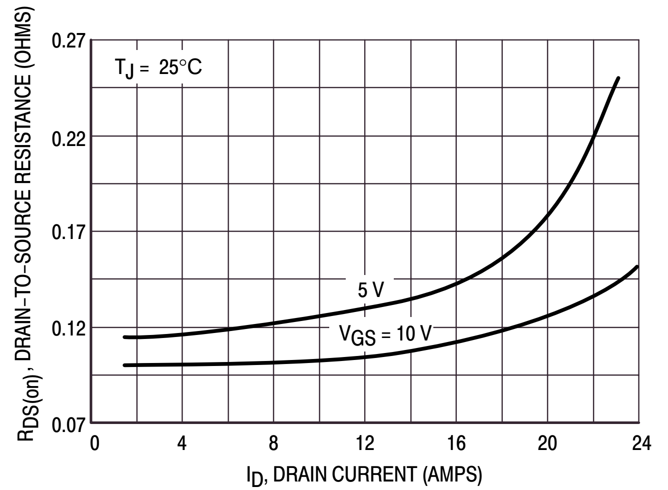



**Figure 3. On–Resistance versus Drain Current and Temperature**

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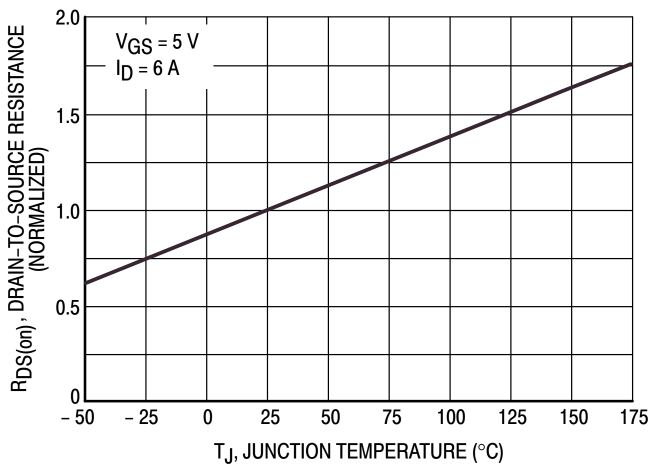
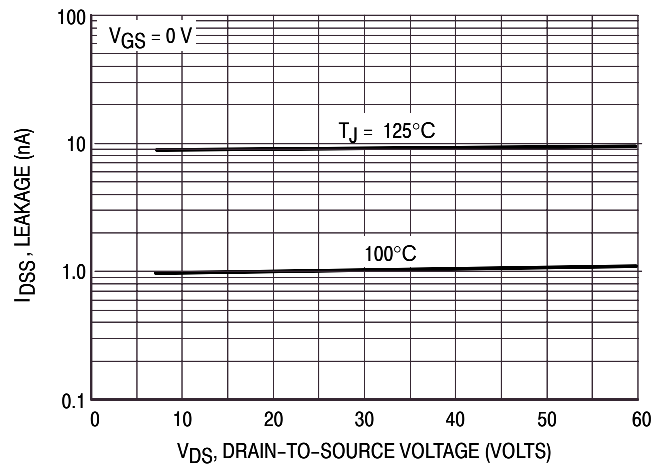



**Figure 5. On–Resistance Variation with Temperature**

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$t_{d(off)} = R_G C_{iss} \ln (V_{GG}/V_{GSP})$

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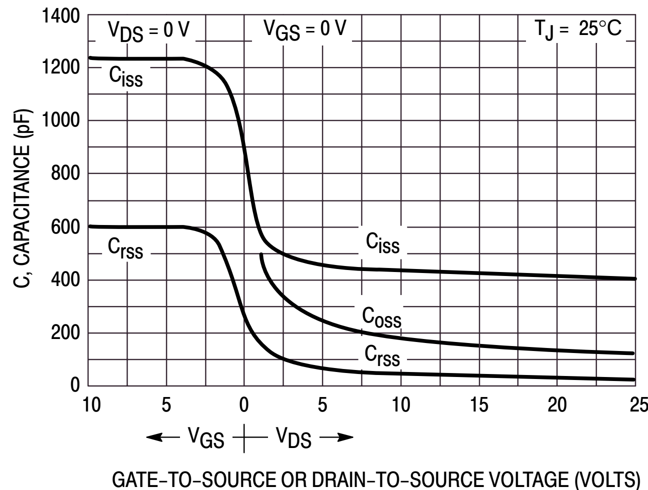


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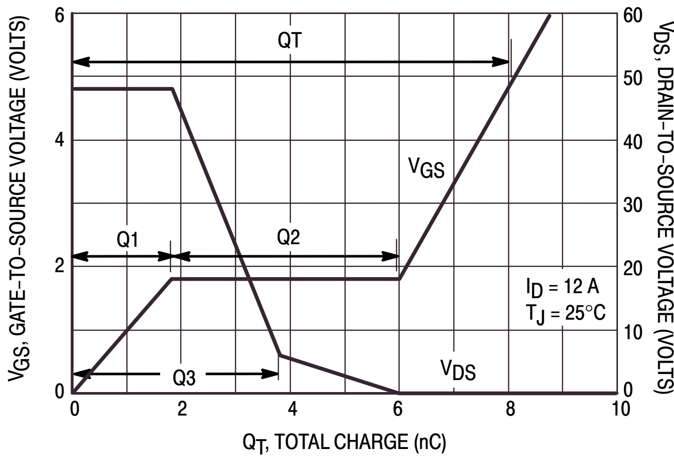


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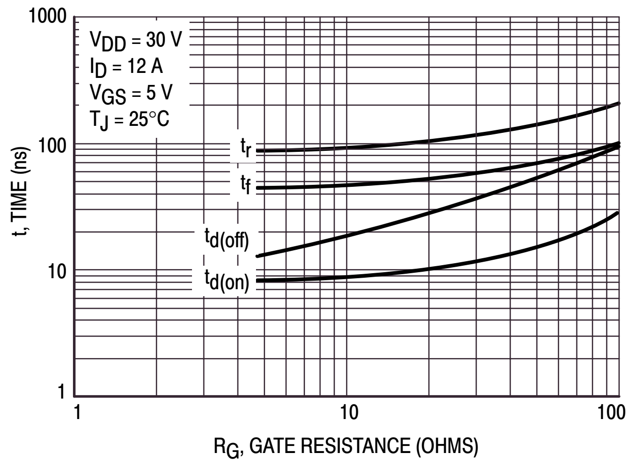
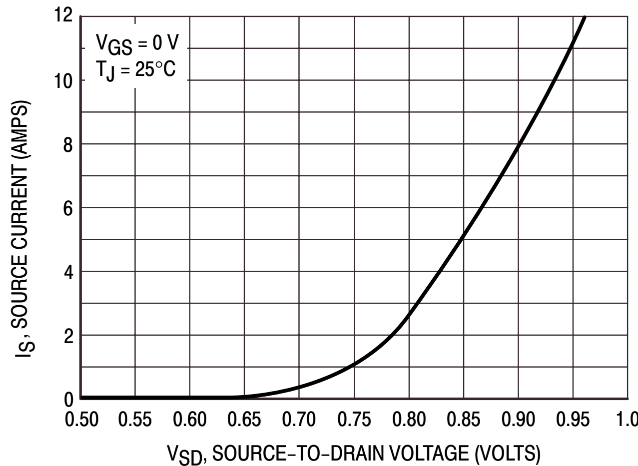



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

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## SAFE OPERATING AREA

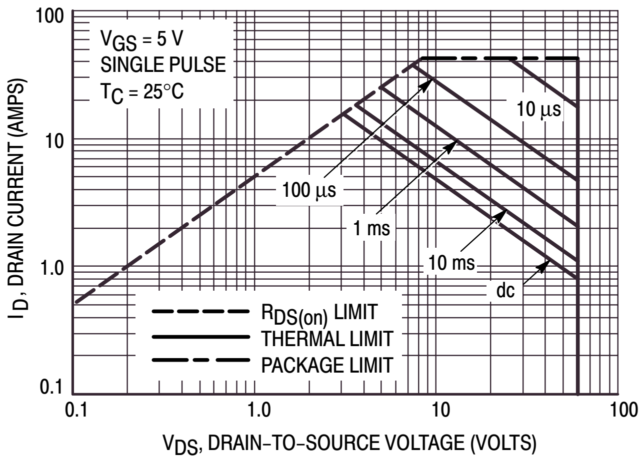
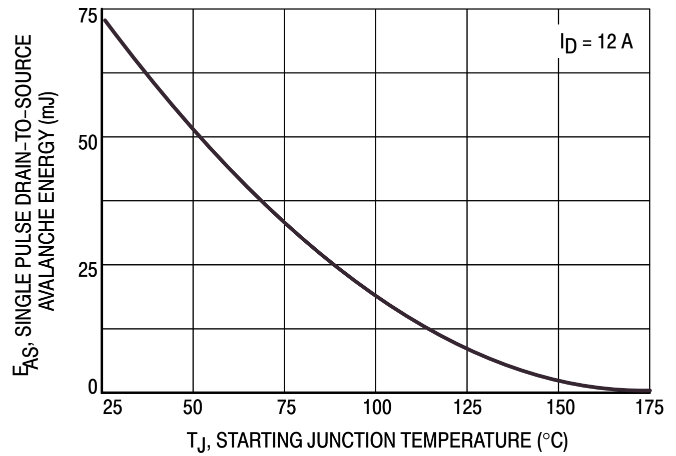



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

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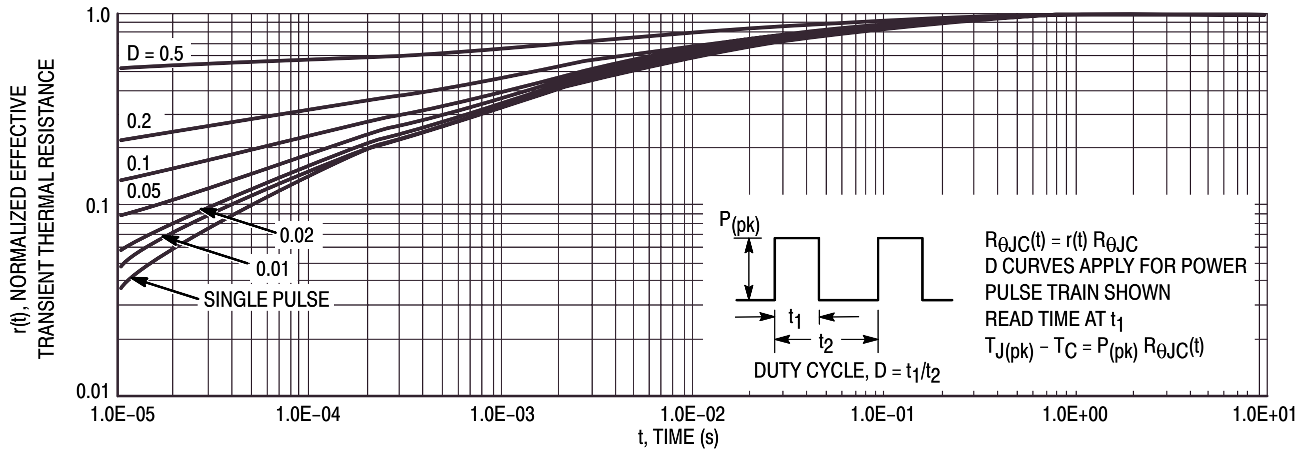


**Figure 13. Thermal Response**

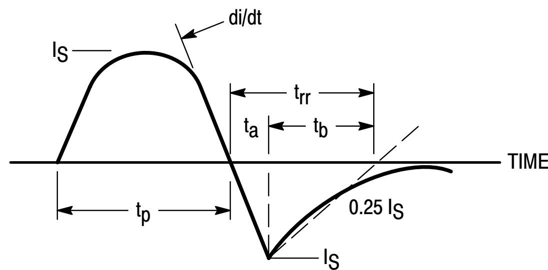


**Figure 14. Diode Reverse Recovery Waveform**

# MTP30N06VL

**Preferred Device**

# Power MOSFET 30 Amps, 60 Volts, Logic Level

## N–Channel TO–220

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**30 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 50 mΩ**

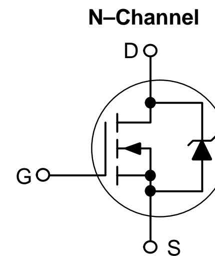
This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

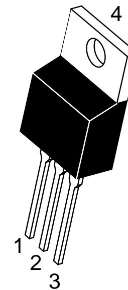
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 30<br>20<br>105 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 90<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 30 Apk, L = 0.342 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 154 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

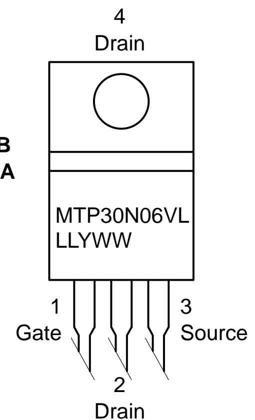
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP30N06VL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP30N06VL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 63 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 1.0 | 1.5 | 2.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5 Vdc, $I_D$ = 15 Adc) | | $R_{DS(on)}$ | – | 0.033 | 0.05 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 5 Vdc, $I_D$ = 30 Adc) | | $V_{DS(on)}$ | – | – | 1.8 | Vdc |
| ($V_{GS}$ = 5 Vdc, $I_D$ = 15 Adc, $T_J$ = 150 °C) | | | – | – | 1.73 | |
| Forward Transconductance ($V_{DS}$ = 6.25 Vdc, $I_D$ = 15 Adc) | | $g_{FS}$ | 13 | 21 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1130 | 1580 | pF |
| Output Capacitance | | $C_{oss}$ | – | 360 | 500 | |
| Transfer Capacitance | | $C_{rss}$ | – | 95 | 190 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 30 | ns |
| Rise Time | | $t_r$ | – | 260 | 520 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 54 | 110 | |
| Fall Time | | $t_f$ | – | 108 | 220 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 27 | 40 | nC |
| | | $Q_1$ | – | 5 | – | |
| | | $Q_2$ | – | 17 | – | |
| | | $Q_3$ | – | 15 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.98 | 1.6 | Vdc |
| | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | | – | 0.89 | – | |
| Reverse Recovery Time | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 86.4 | – | ns |
| | | $t_a$ | – | 49.6 | – | |
| | | $t_b$ | – | 36.8 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.228 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

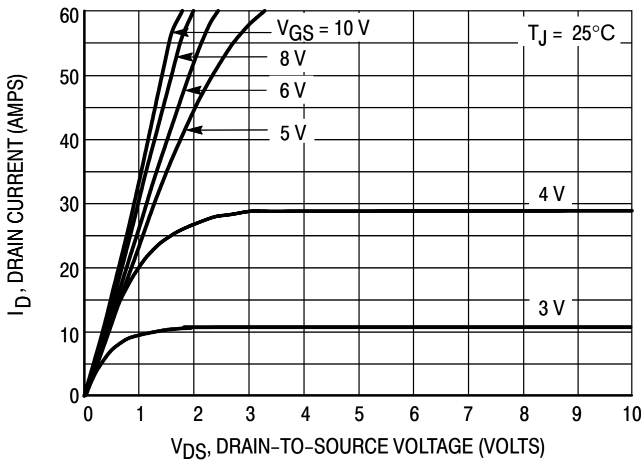



**Figure 1. On–Region Characteristics**

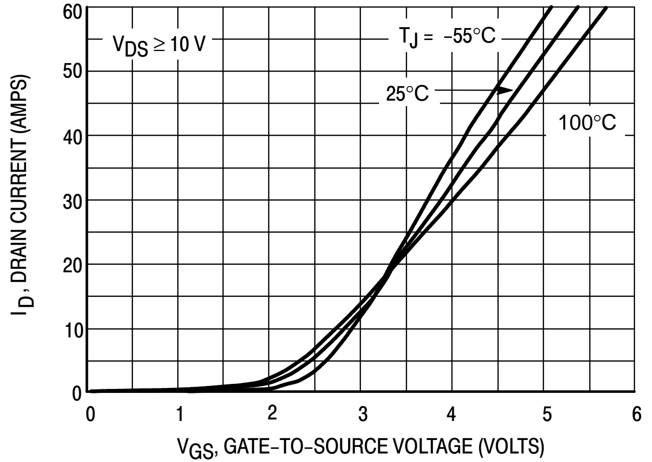



**Figure 2. Transfer Characteristics**

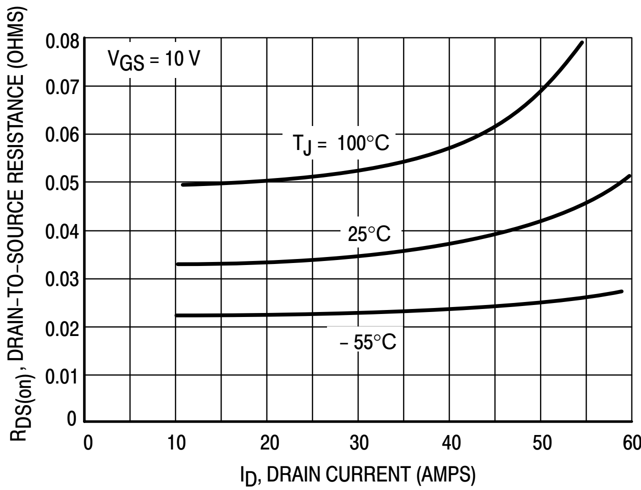



**Figure 3. On–Resistance versus Drain Current and Temperature**

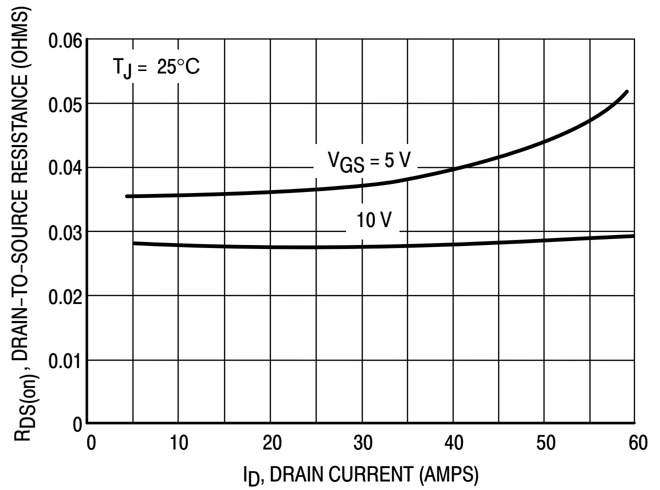



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

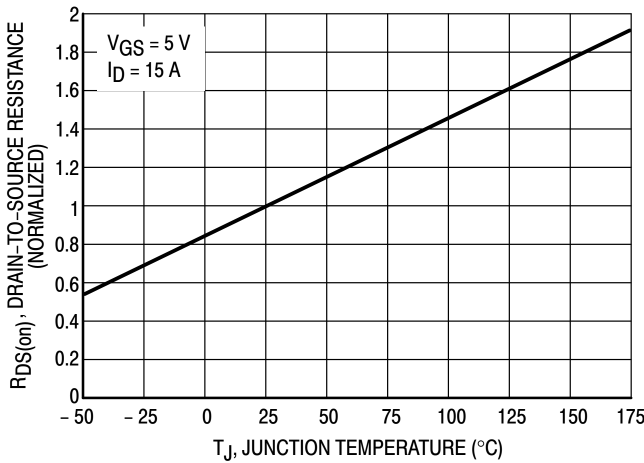



**Figure 5. On–Resistance Variation with Temperature**

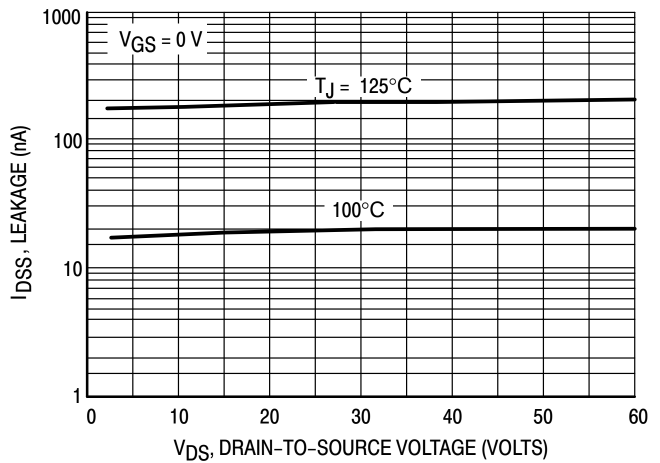



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

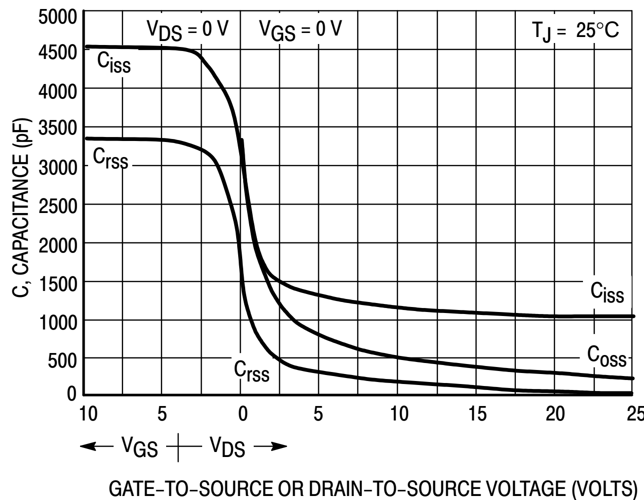



**Figure 7. Capacitance Variation**

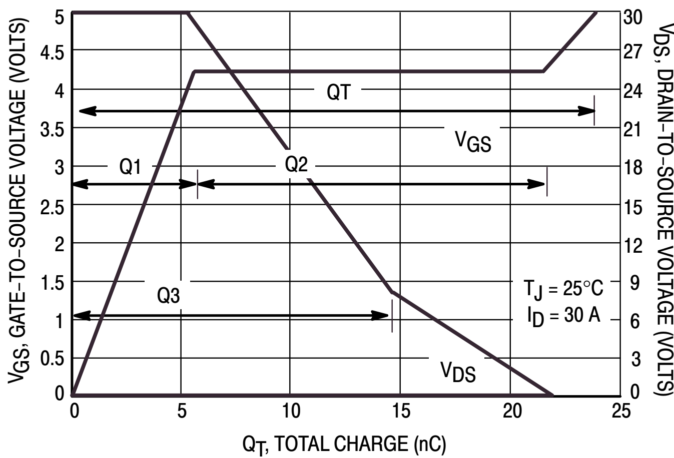



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

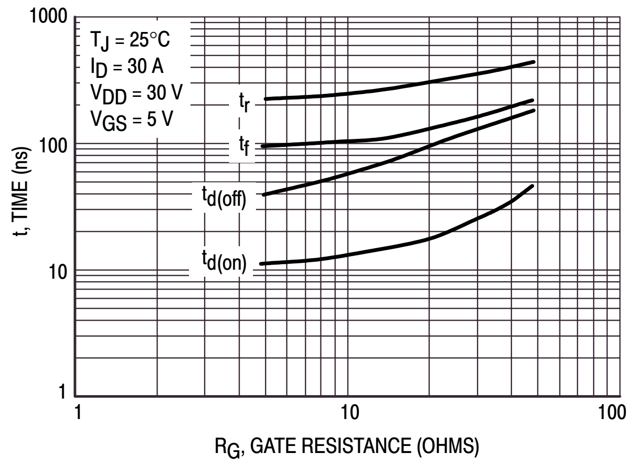



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

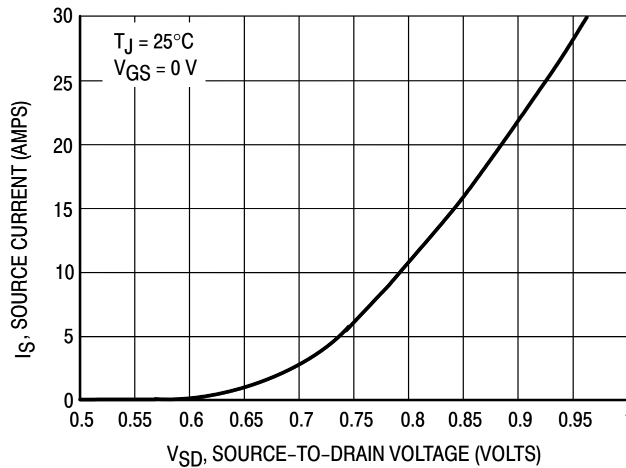



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

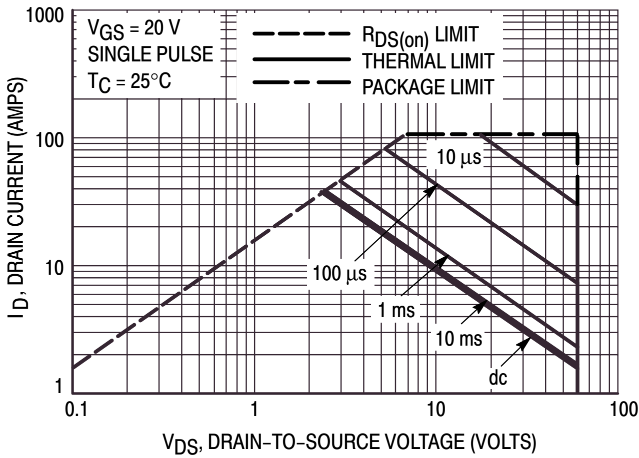



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

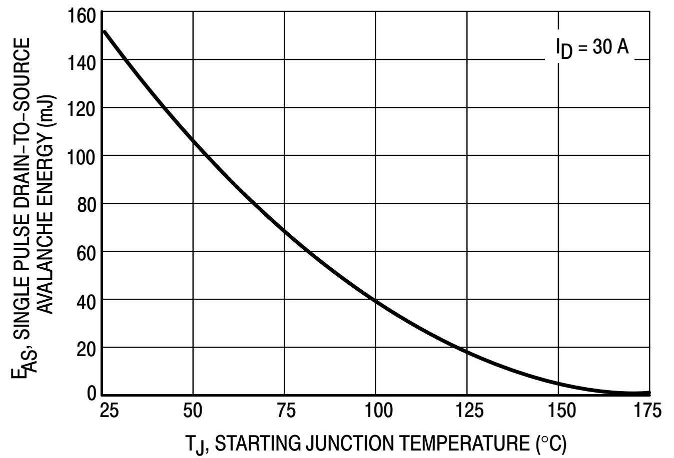



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

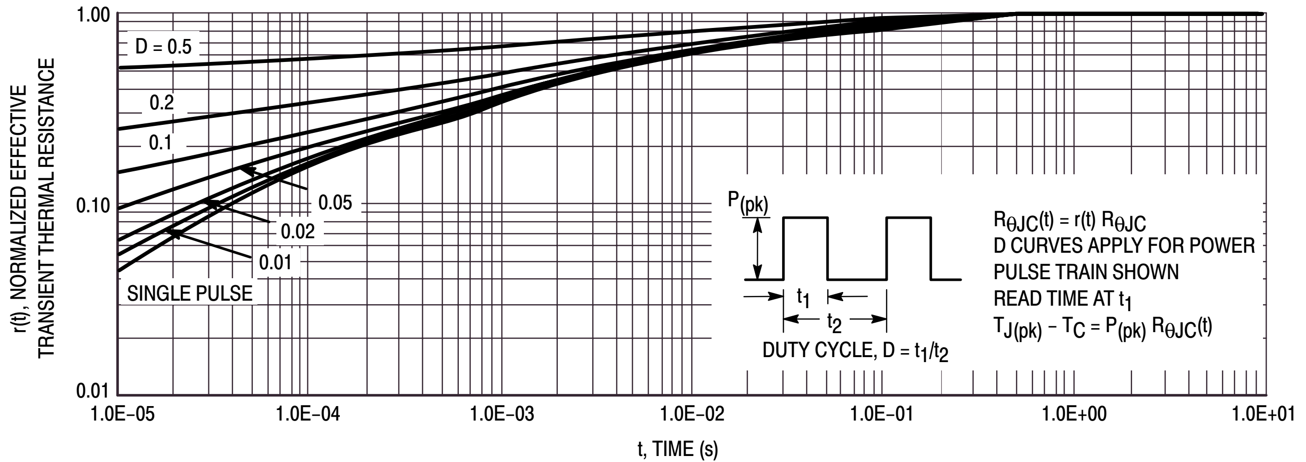



**Figure 13. Thermal Response**

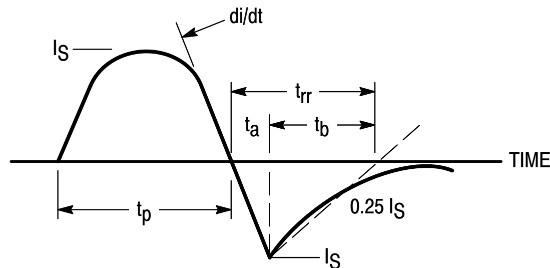



**Figure 14. Diode Reverse Recovery Waveform**

# MTP30P06V

**Preferred Device**

# Power MOSFET
# 30 Amps, 60 Volts
## P–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

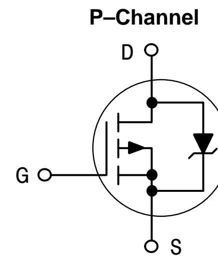
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

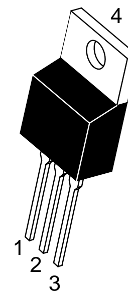
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 30<br>19<br>105 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 125<br>0.83 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 30 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 450 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.2<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**30 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 80 mΩ**

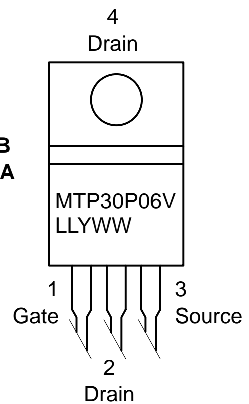
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP30P06V = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP30P06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>62 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.6<br>5.3 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc) | | $R_{DS(on)}$ | – | 0.067 | 0.08 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 30 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 15 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 2.0<br>– | 2.9<br>2.8 | Vdc |
| Forward Transconductance ($V_{DS}$ = 8.3 Vdc, $I_D$ = 15 Adc) | | $g_{FS}$ | 5.0 | 7.9 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1562 | 2190 | pF |
| Output Capacitance | | $C_{oss}$ | – | 524 | 730 | |
| Transfer Capacitance | | $C_{rss}$ | – | 154 | 310 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14.7 | 30 | ns |
| Rise Time | | $t_r$ | – | 25.9 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 98 | 200 | |
| Fall Time | | $t_f$ | – | 52.4 | 100 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 30 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 54 | 80 | nC |
| | | $Q_1$ | – | 9.0 | – | |
| | | $Q_2$ | – | 26 | – | |
| | | $Q_3$ | – | 20 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 2.3<br>1.9 | 3.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 30 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 175 | – | ns |
| | | $t_a$ | – | 107 | – | |
| | | $t_b$ | – | 68 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.965 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

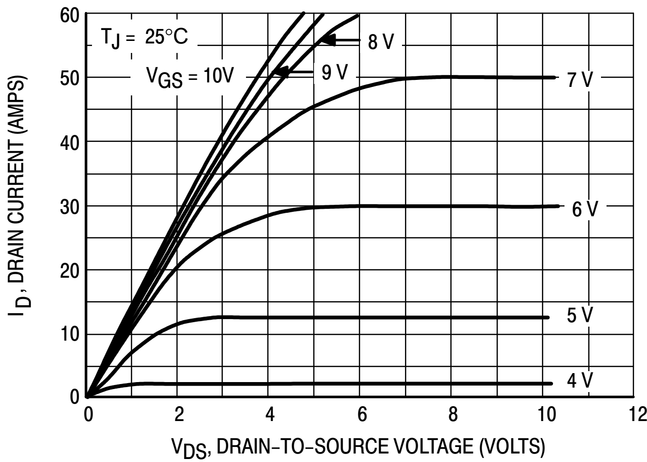
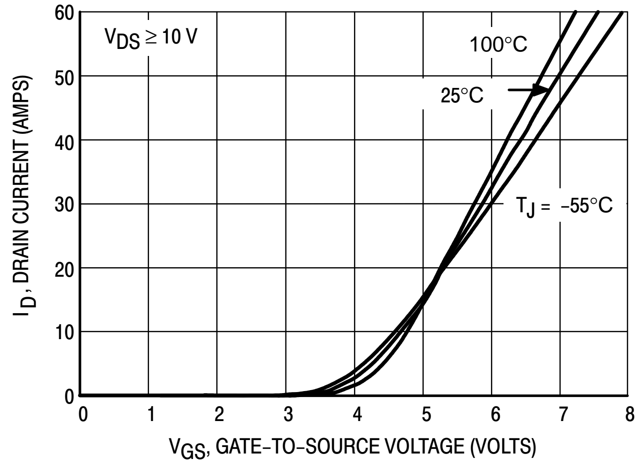



**Figure 1. On–Region Characteristics**

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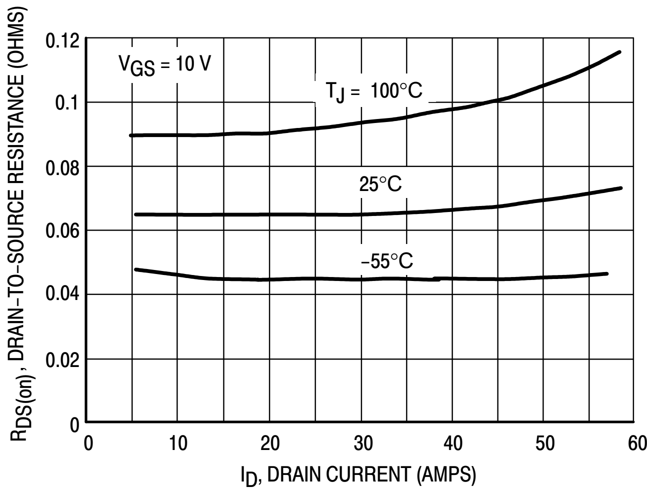



**Figure 3. On–Resistance versus Drain Current and Temperature**

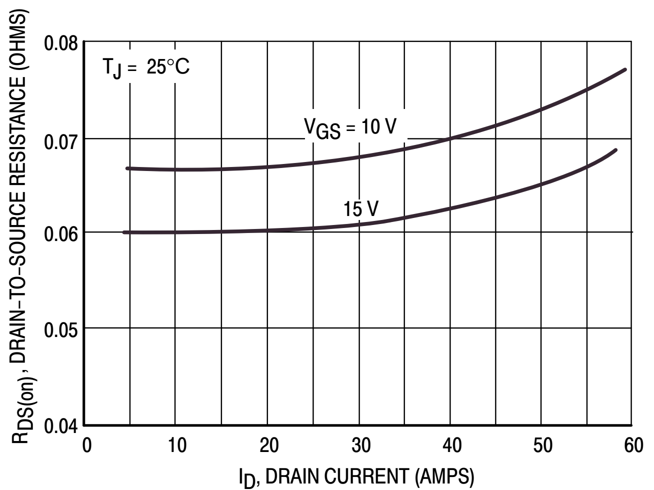



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

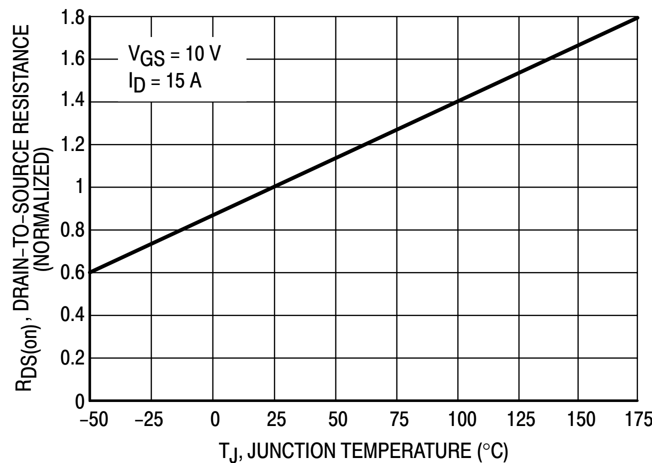
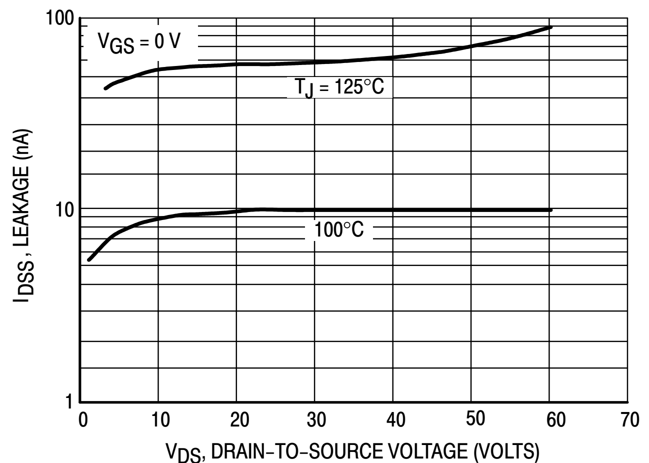



**Figure 5. On–Resistance Variation with Temperature**

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## POWER MOSFET SWITCHING

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The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

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$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

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The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

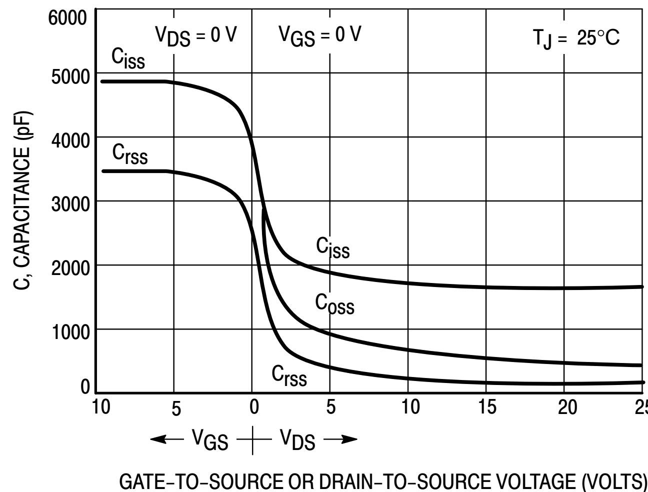



**Figure 7. Capacitance Variation**

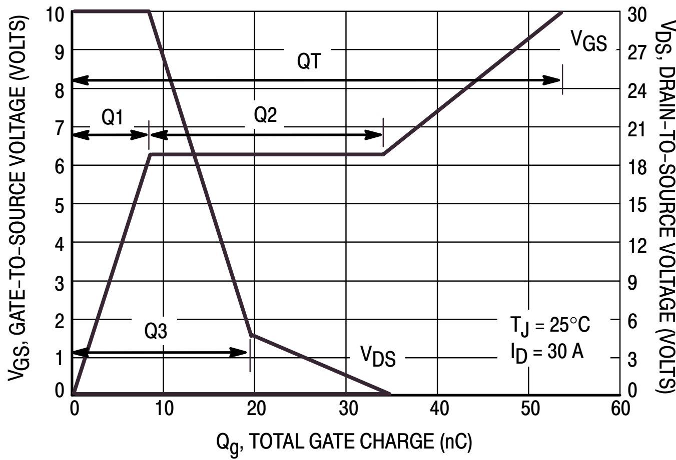



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

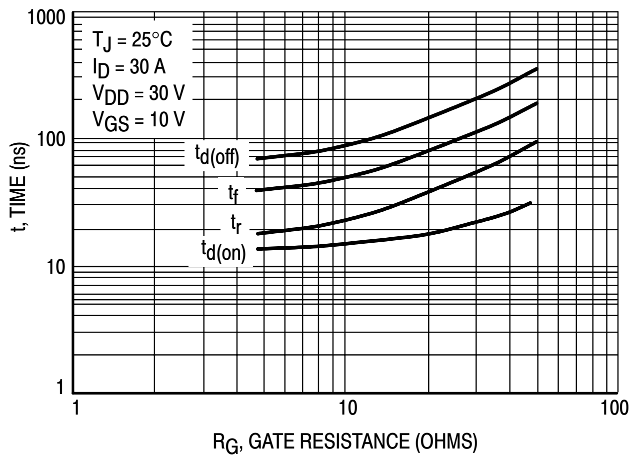



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

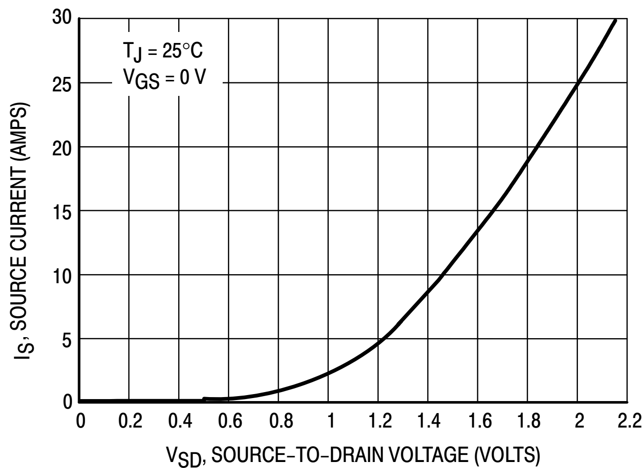



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

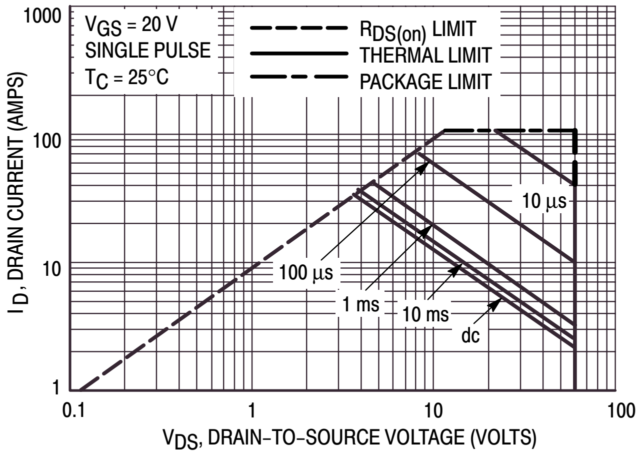



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

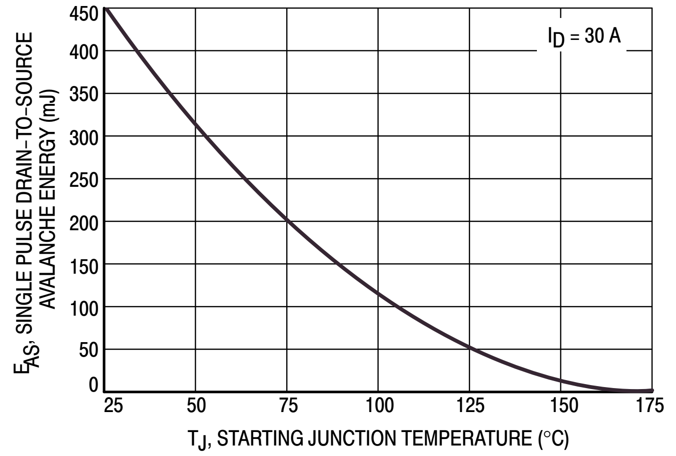



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

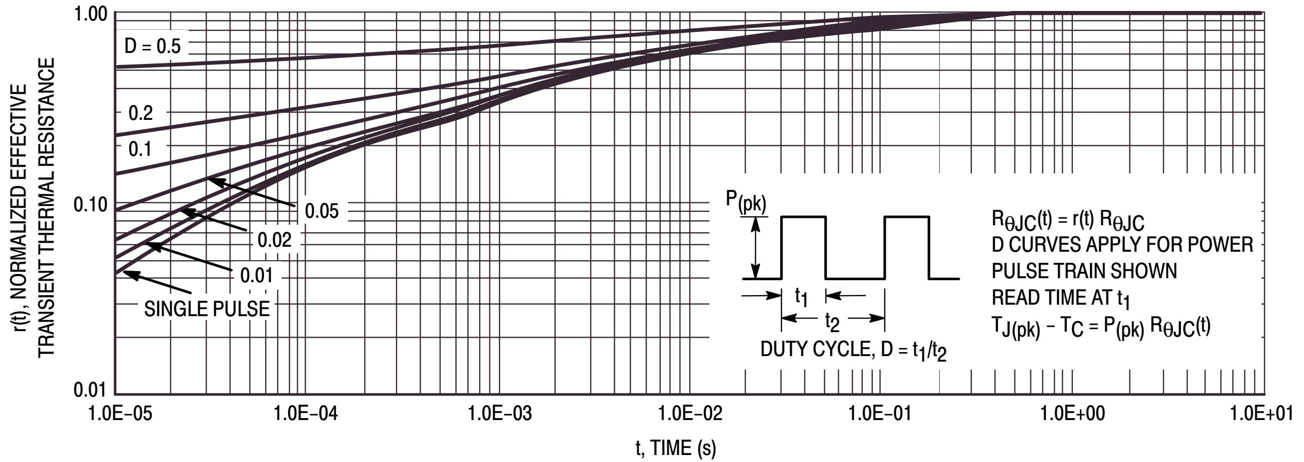



**Figure 13. Thermal Response**

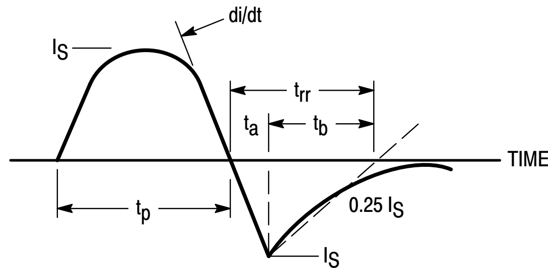



**Figure 14. Diode Reverse Recovery Waveform**

# MTP36N06V

**Preferred Device**

# Power MOSFET 32 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

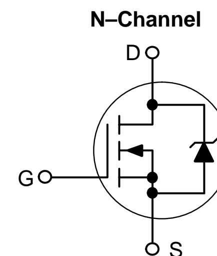
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25 °C<br>– Continuous @ 100 °C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 32<br>22.6<br>112 | Adc<br><br>Apk |
| Total Power Dissipation @ 25 °C<br>Derate above 25 °C | $P_D$ | 90<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 32 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 205 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

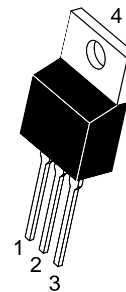
**http://onsemi.com**

**32 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

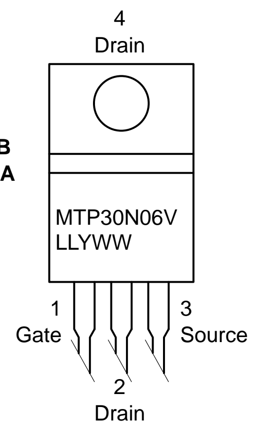
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




MTP30N06V = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP36N06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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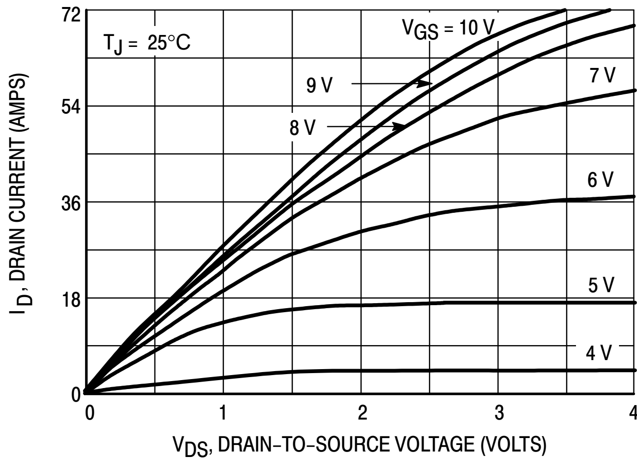
**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25 °C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>61 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.6<br>6.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 0.034 | 0.04 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 32 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc, $T_J$ = 150 °C) | | $V_{DS(on)}$ | –<br>– | 1.25<br>– | 1.54<br>1.47 | Vdc |
| Forward Transconductance ($V_{DS}$ = 7.6 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | 5.0 | 7.83 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1220 | 1700 | pF |
| Output Capacitance | | $C_{oss}$ | – | 337 | 470 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 74.8 | 150 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 30 | ns |
| Rise Time | | $t_r$ | – | 138 | 270 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 54 | 100 | |
| Fall Time | | $t_f$ | – | 91 | 180 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 39 | 50 | nC |
| | | $Q_1$ | – | 7.0 | – | |
| | | $Q_2$ | – | 17 | – | |
| | | $Q_3$ | – | 13 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | $V_{SD}$ | –<br>– | 1.03<br>0.94 | 2.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 92 | – | ns |
| | | $t_a$ | – | 64 | – | |
| | | $t_b$ | – | 28 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.332 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

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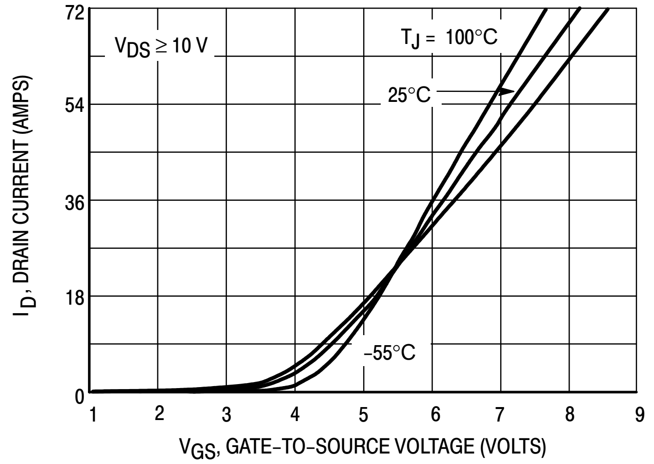


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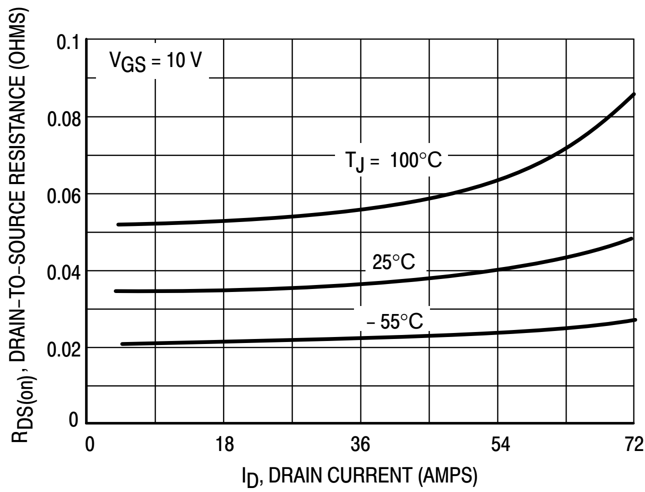


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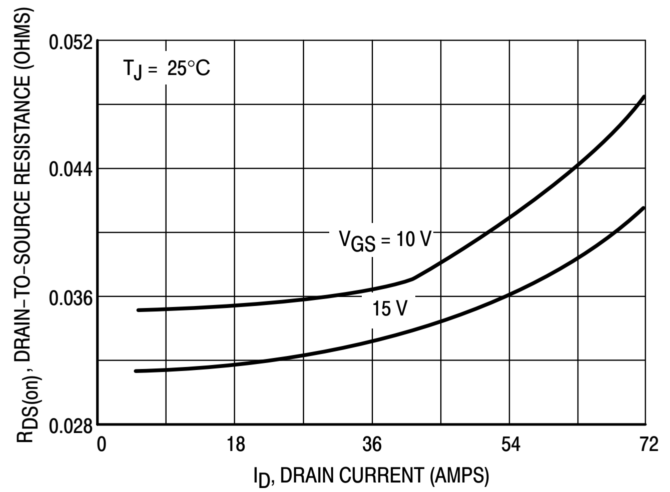


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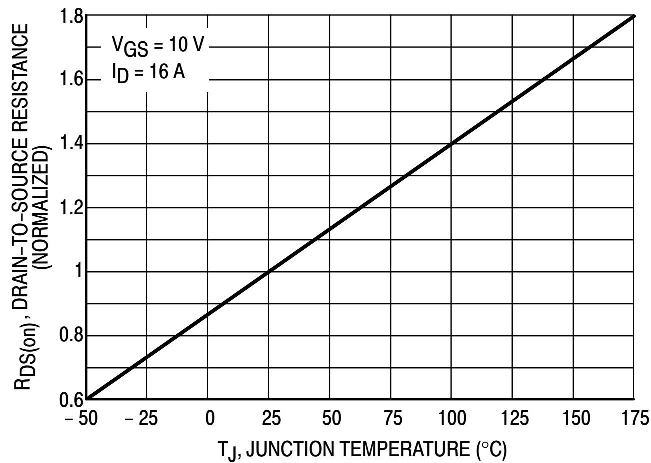


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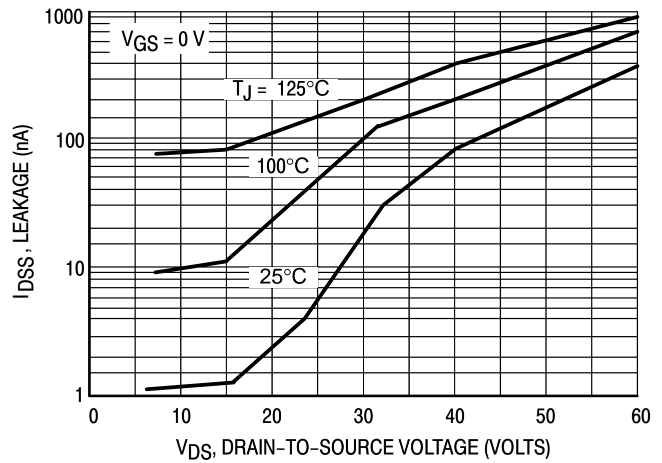


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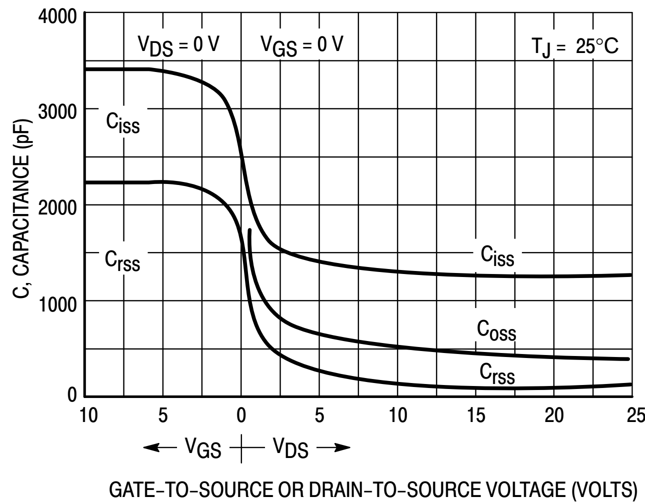


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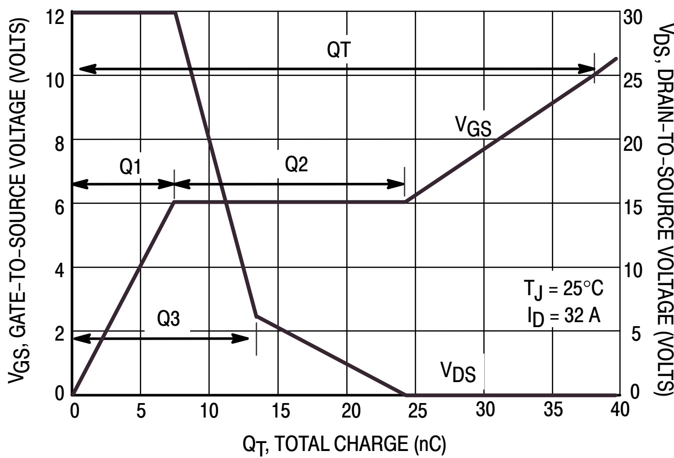


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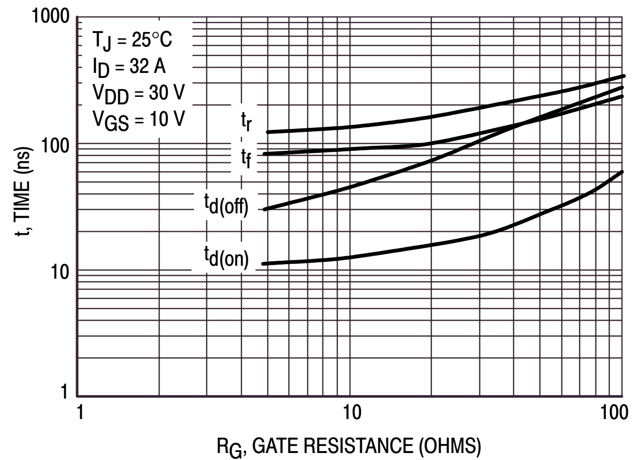


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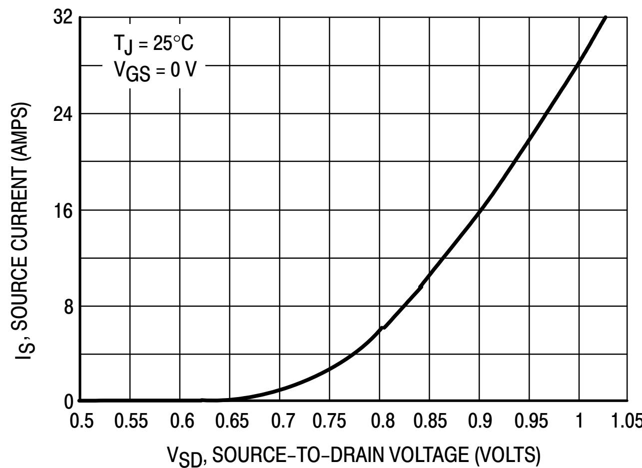
### DRAIN–TO–SOURCE DIODE CHARACTERISTICS

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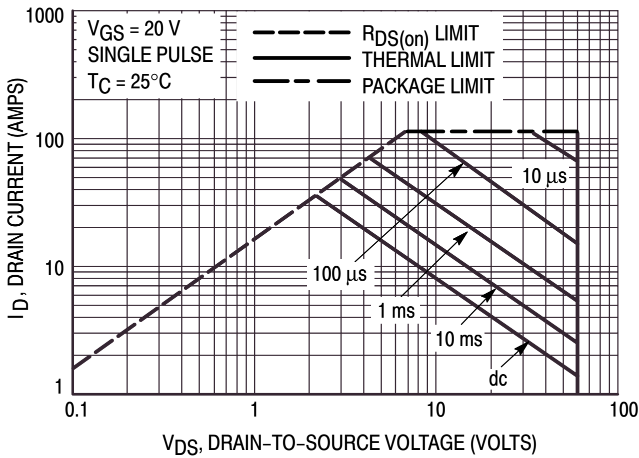
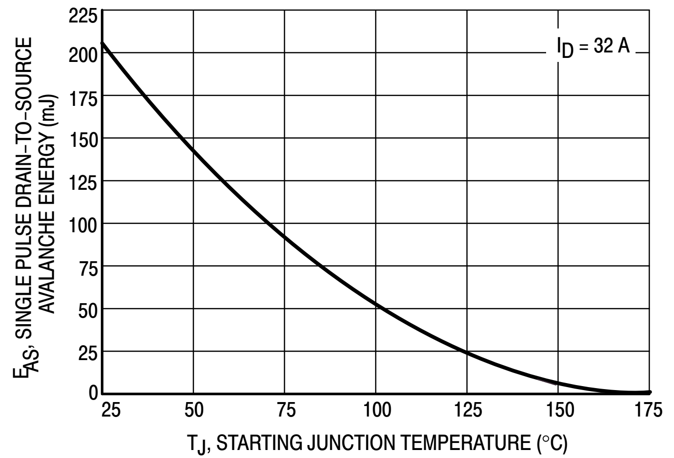



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

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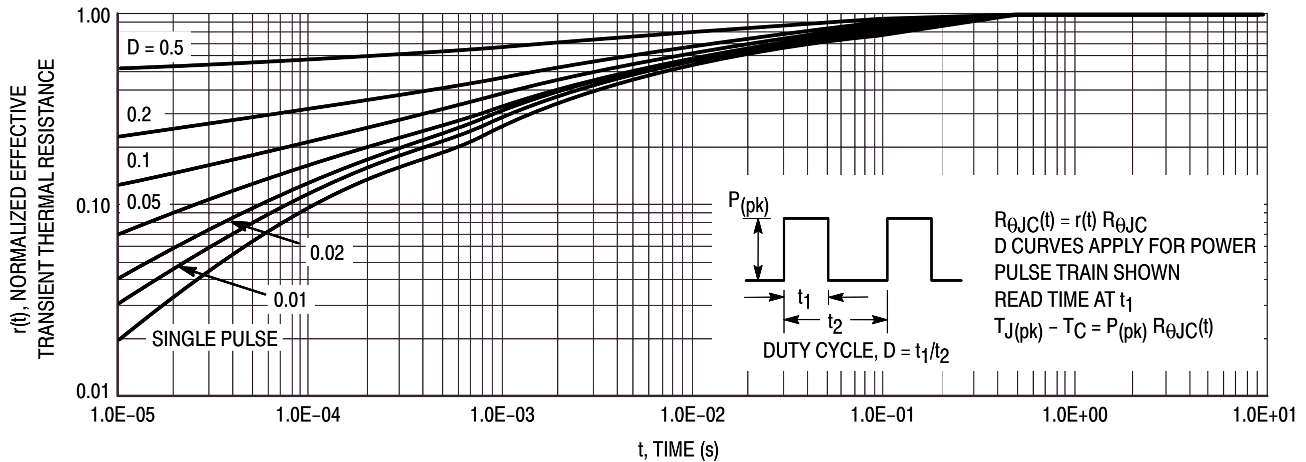



**Figure 13. Thermal Response**

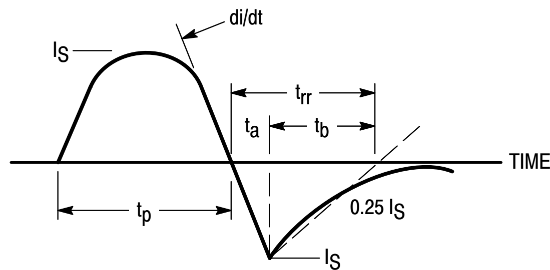



**Figure 14. Diode Reverse Recovery Waveform**

# MTP40N10E

**Preferred Device**

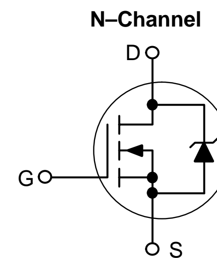
# Power MOSFET
# 40 Amps, 100 Volts
## N–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

**40 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

**N–Channel**



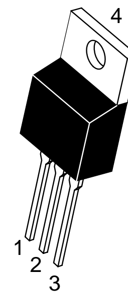

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

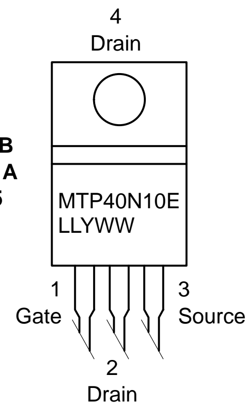
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 40<br>29<br>140 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 169<br>1.35 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 75 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 40 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 800 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{θJC}$<br>$R_{θJA}$ | <br>0.74<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP40N10E | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP40N10E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc) | | $V_{(BR)DSS}$ | 100 | – | – | Vdc |
| Temperature Coefficient (Positive) (Cpk ≥ 2.0) (Note 3.) | | | – | 112 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ =125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 2.9 | 4.0 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 6.7 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.) ($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc) | | $R_{DS(on)}$ | – | 0.033 | 0.04 | Ohms |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 40 Adc) | | $V_{DS(on)}$ | – | – | 1.9 | Vdc |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 20 Adc, $T_J$ = 125°C) | | | – | – | 1.7 | |
| Forward Transconductance ($V_{DS}$ = 8.4 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 21 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2305 | 3230 | pF |
| Output Capacitance | | $C_{oss}$ | – | 620 | 1240 | |
| Transfer Capacitance | | $C_{rss}$ | – | 205 | 290 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 50 Vdc, $I_D$ = 40 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 19 | 40 | ns |
| Rise Time | | $t_r$ | – | 165 | 330 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 75 | 150 | |
| Fall Time | | $t_f$ | – | 97 | 190 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 40 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 80 | 110 | nC |
| | | $Q_1$ | – | 15 | – | |
| | | $Q_2$ | – | 40 | – | |
| | | $Q_3$ | – | 29 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.96 | 1.0 | Vdc |
| | ($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.88 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 40 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 152 | – | ns |
| | | $t_a$ | – | 117 | – | |
| | | $t_b$ | – | 35 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.0 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) | | $L_D$ | – | 3.5 | – | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | – | 4.5 | – | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $Cpk = \left|\frac{\text{Max limit} - \text{Typ}}{3 \times \text{sigma}}\right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

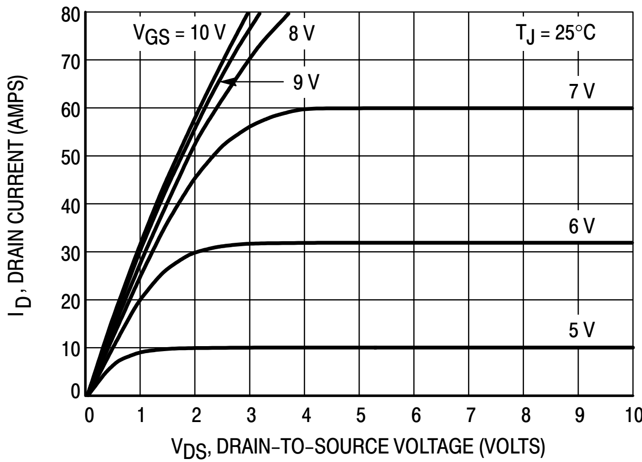



**Figure 1. On–Region Characteristics**

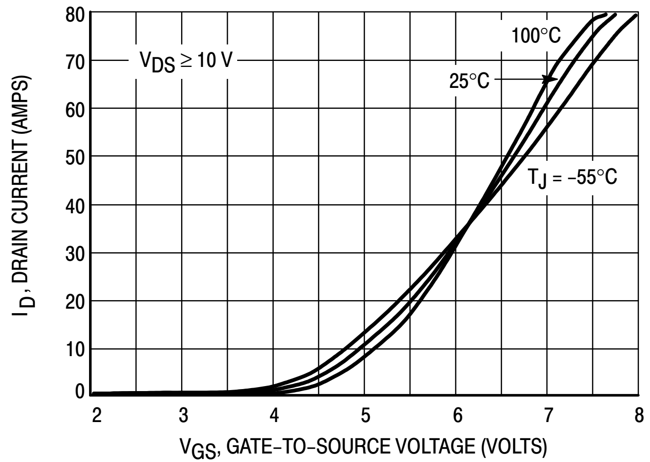



**Figure 2. Transfer Characteristics**

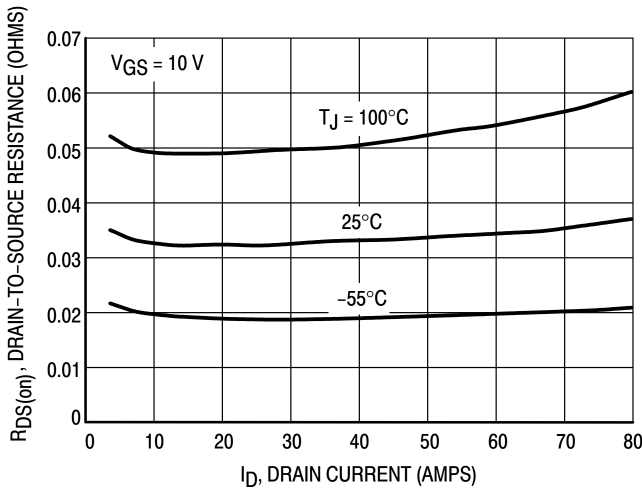



**Figure 3. On–Resistance versus Drain Current and Temperature**

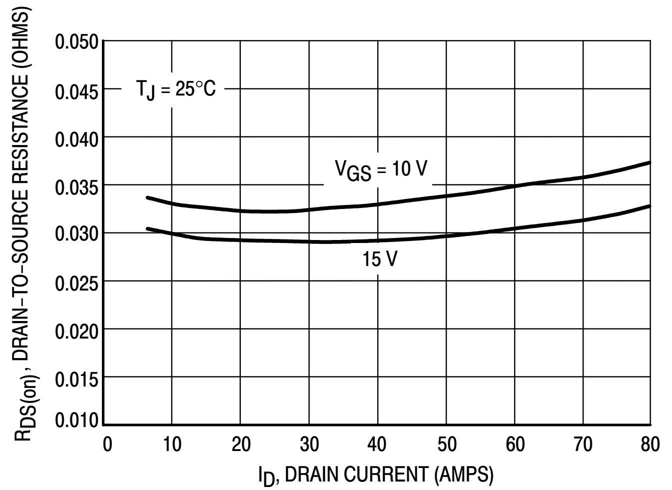



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

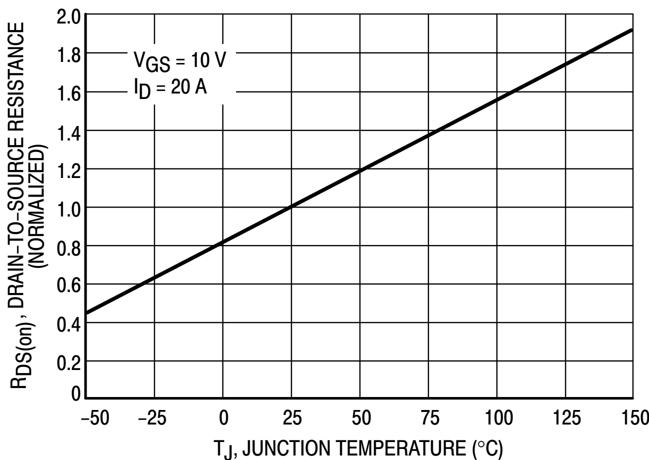



**Figure 5. On–Resistance Variation with Temperature**

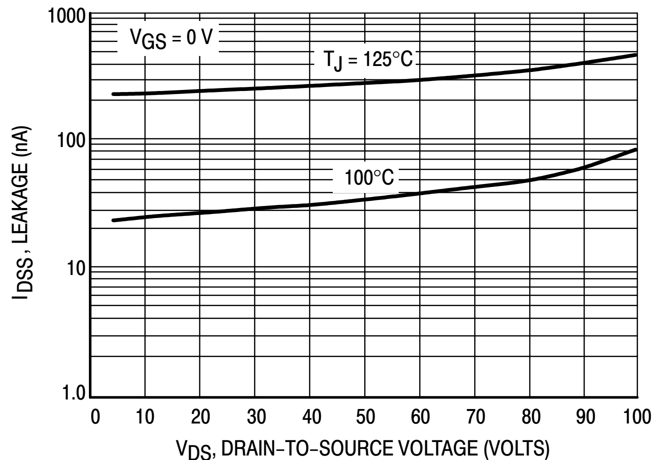



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

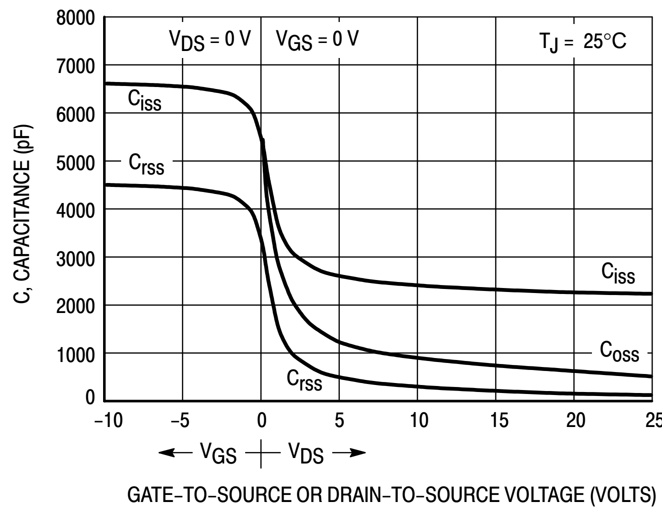



**Figure 7. Capacitance Variation**

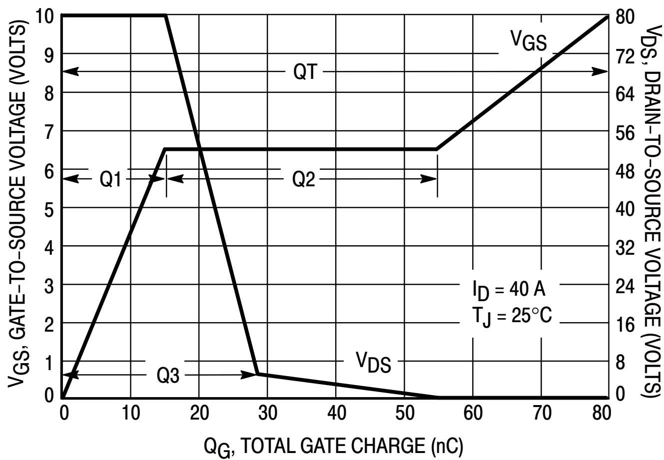



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

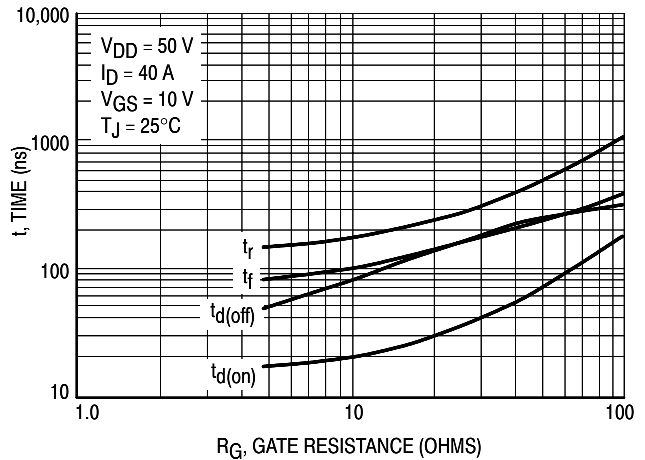



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

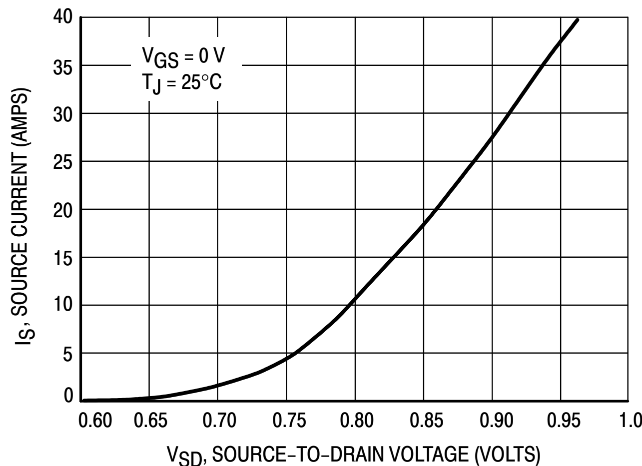



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

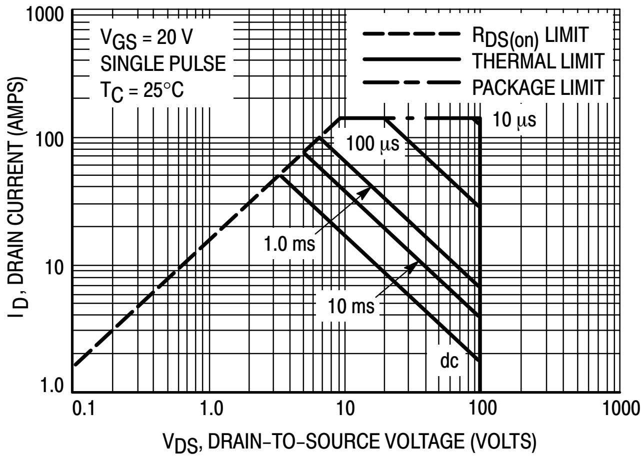



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

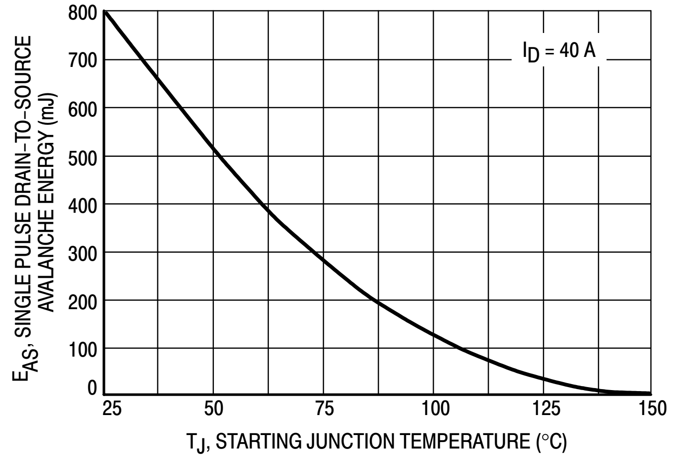



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

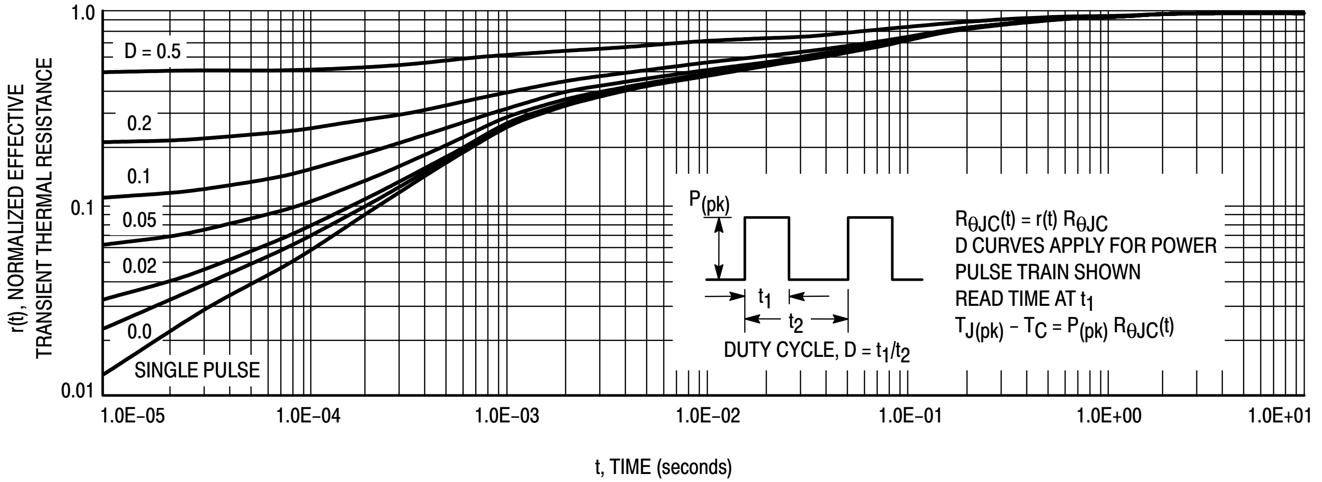



**Figure 13. Thermal Response**

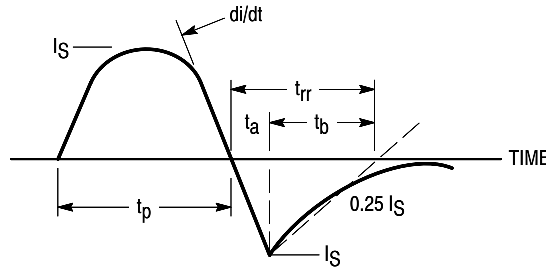



**Figure 14. Diode Reverse Recovery Waveform**

# MTP50N06V

**Preferred Device**

# Power MOSFET 42 Amps, 60 Volts

## N–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

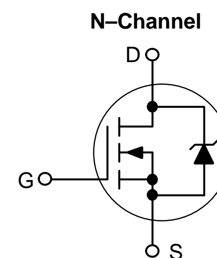
- On–resistance Area Product about One–half that of Standard MOSFETs with New Low Voltage, Low $R_{DS(on)}$ Technology
- Faster Switching than E–FET Predecessors
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Static Parameters are the Same for both TMOS V and TMOS E–FET

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

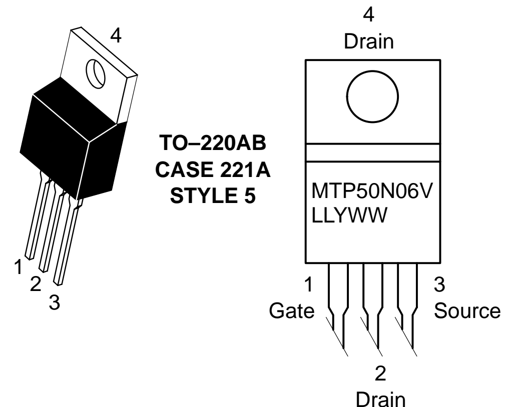
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage – Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ± 20<br>± 25 | Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 42<br>30<br>147 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 125<br>0.83 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc $I_L$ = 42 Apk, L = 0.454 µH, $R_G$ = 25 Ω) | $E_{AS}$ | 400 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.2<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**42 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




MTP50N06V = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP50N06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>69 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.7<br>3.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 21 Adc) | | $R_{DS(on)}$ | – | 0.025 | 0.028 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 42 Adc)<br>($I_D$ = 21 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | 1.4<br>– | 1.7<br>1.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.25 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 16 | 23 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1644 | 2320 | pF |
| Output Capacitance | | $C_{oss}$ | – | 465 | 660 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 112 | 230 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 25 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 20 | ns |
| Rise Time | | $t_r$ | – | 122 | 250 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 64 | 110 | |
| Fall Time | | $t_f$ | – | 54 | 90 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 47 | 70 | nC |
| | | $Q_1$ | – | 9 | – | |
| | | $Q_2$ | – | 21 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.06<br>0.99 | 2.5<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 84 | – | ns |
| | | $t_a$ | – | 73 | – | |
| | | $t_b$ | – | 11 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.28 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

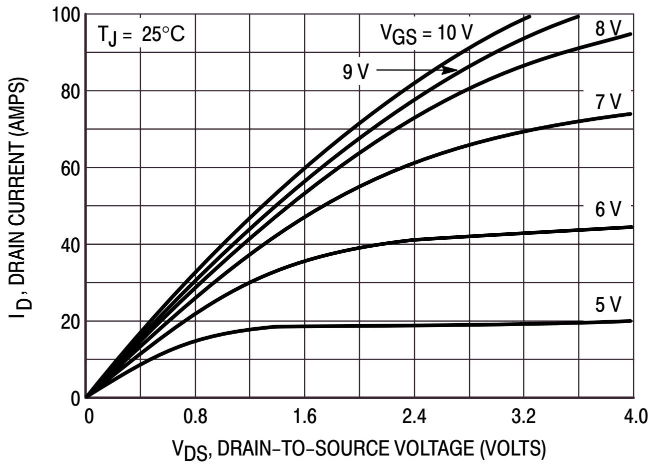


**Figure 1. On–Region Characteristics**

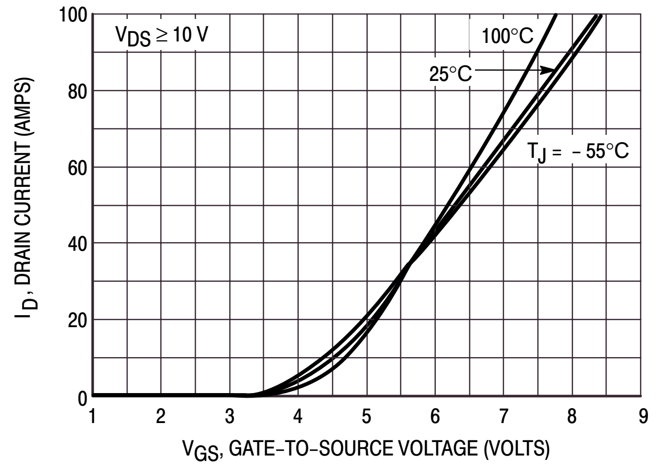


**Figure 2. Transfer Characteristics**

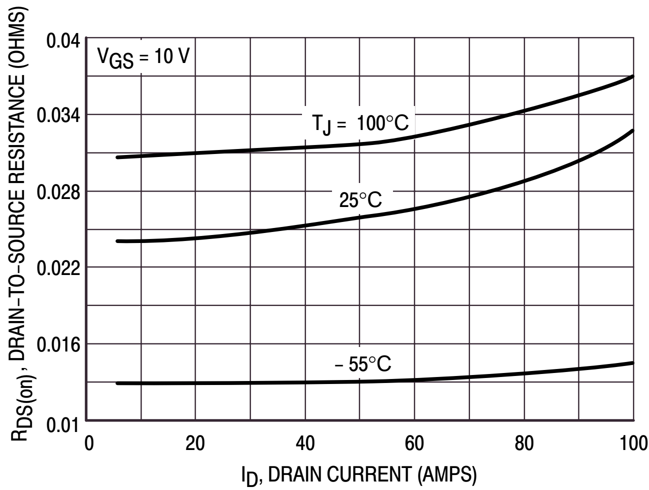


**Figure 3. On–Resistance versus Drain Current and Temperature**

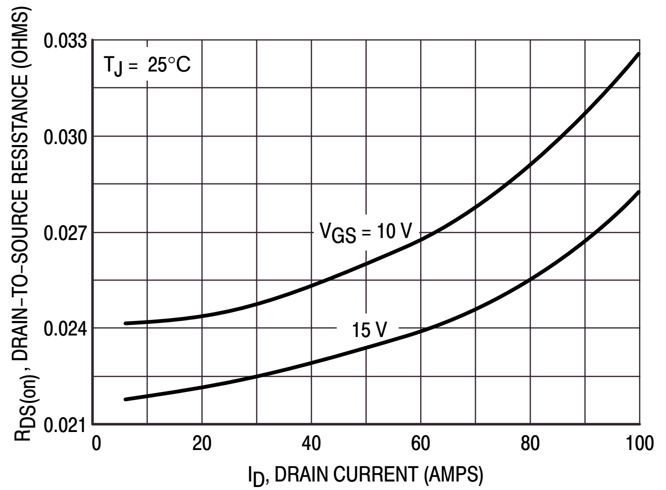


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

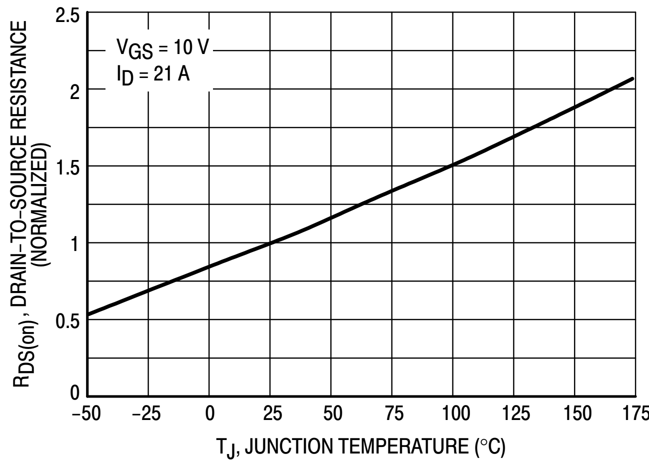


**Figure 5. On–Resistance Variation with Temperature**

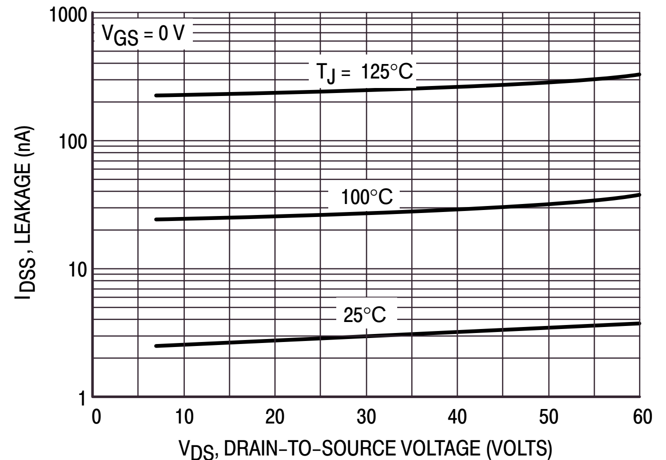


**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

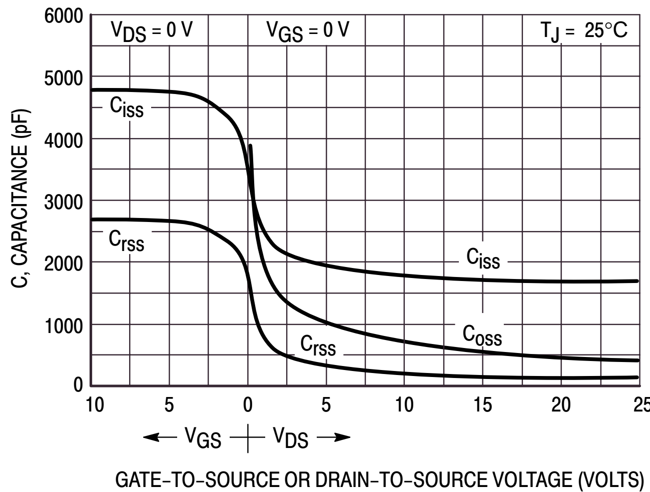



**Figure 7. Capacitance Variation**

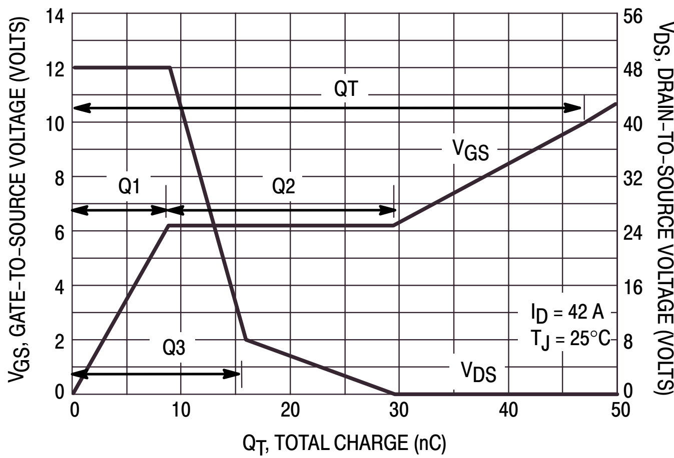



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

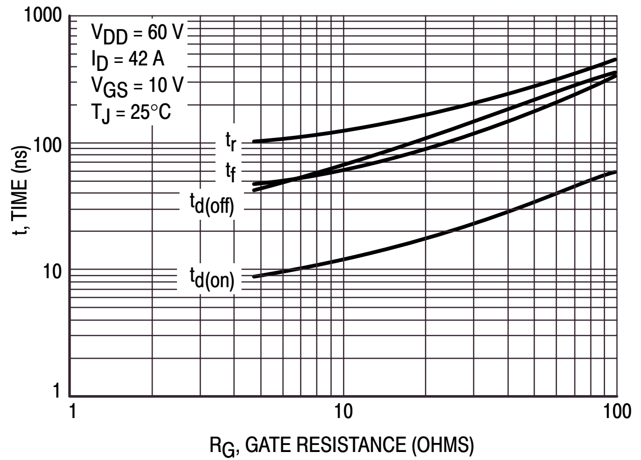



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

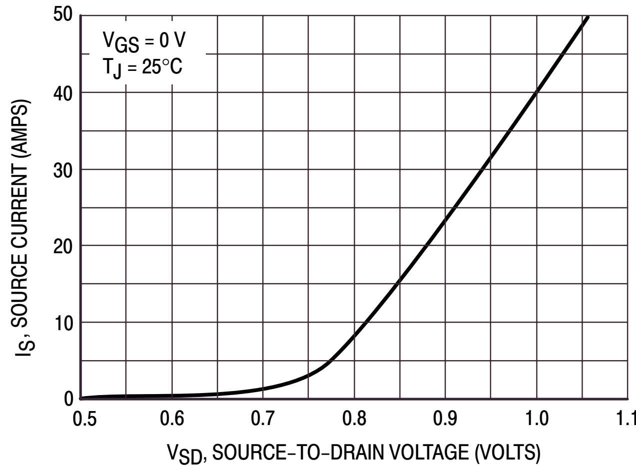



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

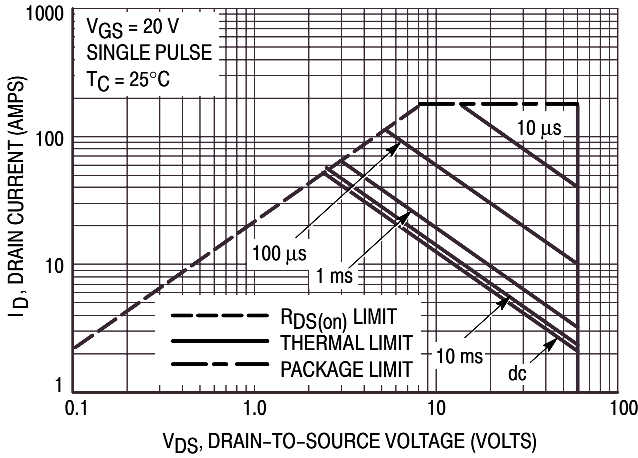



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

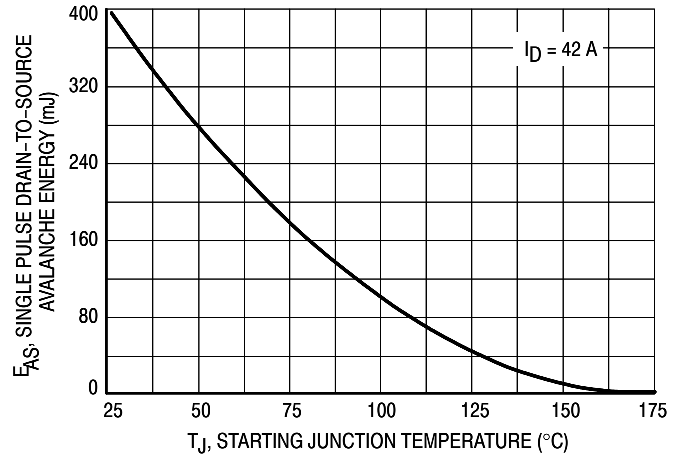



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

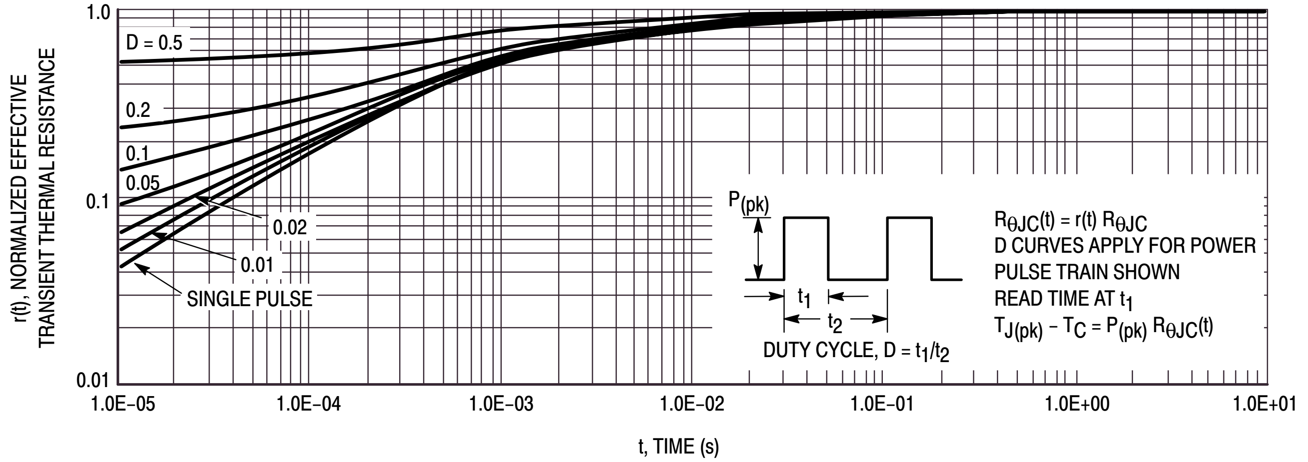



**Figure 13. Thermal Response**

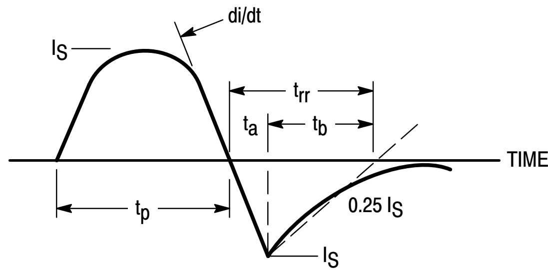



**Figure 14. Diode Reverse Recovery Waveform**

# MTP50N06VL

**Preferred Device**

# Power MOSFET 42 Amps, 60 Volts, Logic Level

## N–Channel TO–220

**ON Semiconductor™**

**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

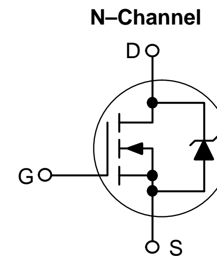
- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

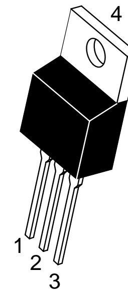
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 20 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 42<br>30<br>147 | Adc<br><br>Apk |
| Total Power Dissipation @ 25°C<br>Derate above 25°C | $P_D$ | 125<br>0.83 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 42 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 265 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 1.2<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**42 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 32 mΩ**

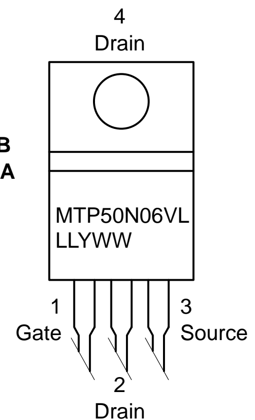
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP50N06VL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP50N06VL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = .25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>64 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 1.0<br>– | 1.4<br>4.3 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5 Vdc, $I_D$ = 21 Adc) | | $R_{DS(on)}$ | – | 0.025 | 0.032 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5 Vdc, $I_D$ = 42 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 21 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 1.6<br>1.5 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 28 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1570 | 2200 | pF |
| Output Capacitance | | $C_{oss}$ | – | 508 | 710 | |
| Transfer Capacitance | | $C_{rss}$ | – | 135 | 270 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 16 | 30 | ns |
| Rise Time | | $t_r$ | – | 355 | 701 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 80 | 160 | |
| Fall Time | | $t_f$ | – | 160 | 320 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 42 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 40 | 60 | nC |
| | | $Q_1$ | – | 11 | – | |
| | | $Q_2$ | – | 20 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | $V_{SD}$ | –<br>– | 1.03<br>0.94 | 2.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 42 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 91.1 | – | ns |
| | | $t_a$ | – | 63.8 | – | |
| | | $t_b$ | – | 27.3 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.299 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
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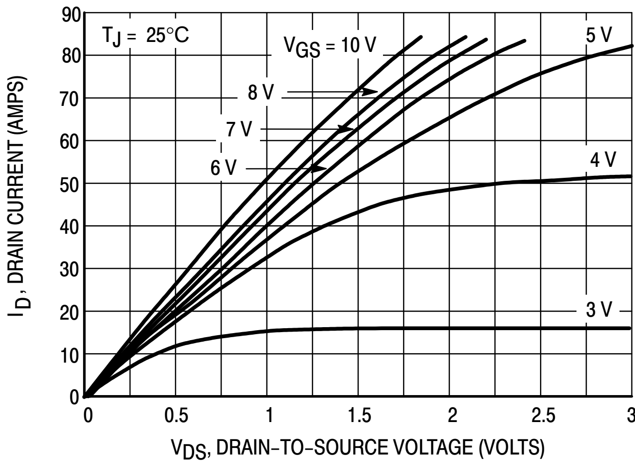


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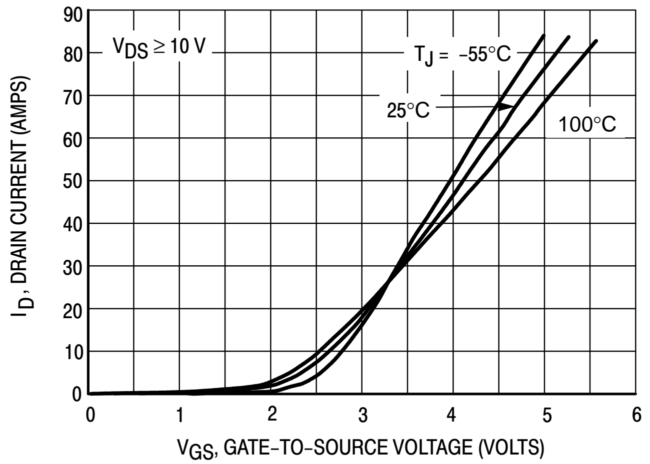


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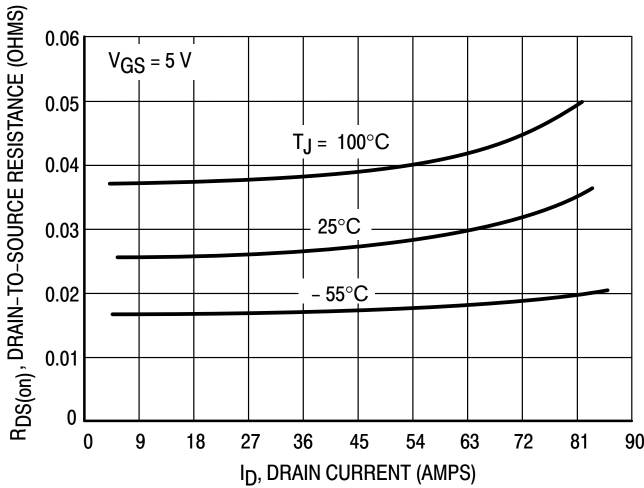
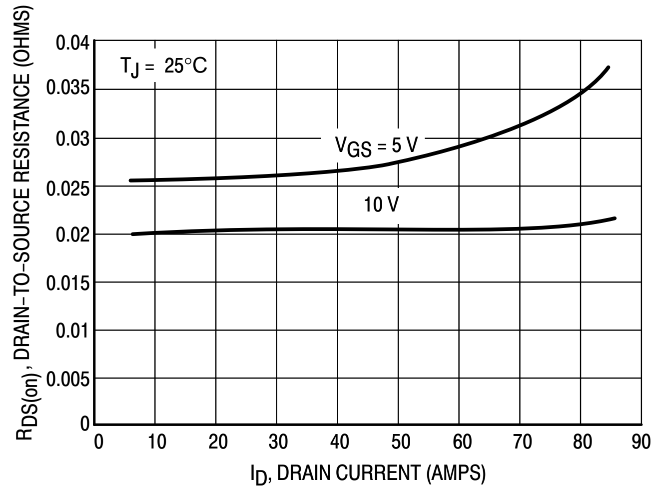



**Figure 3. On–Resistance versus Drain Current and Temperature**

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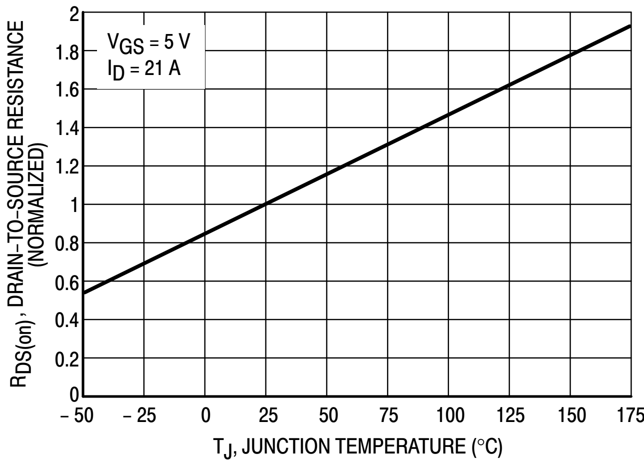


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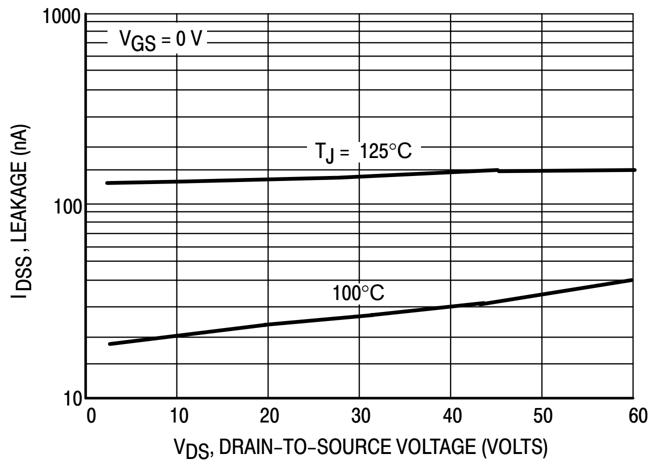


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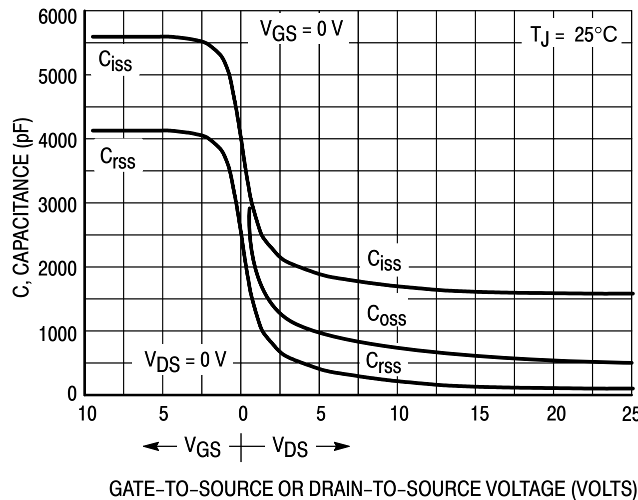


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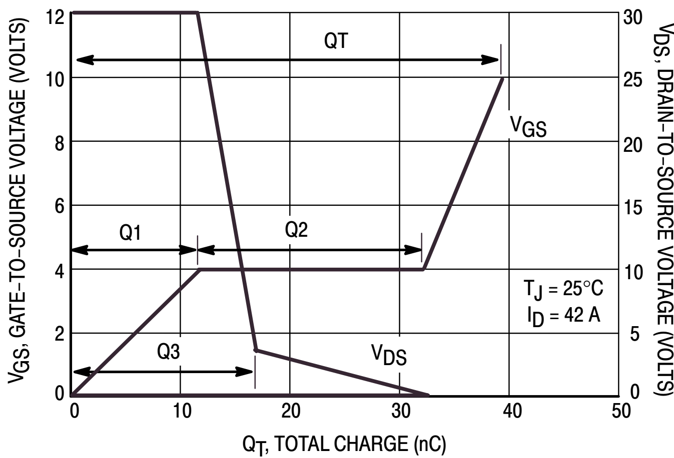


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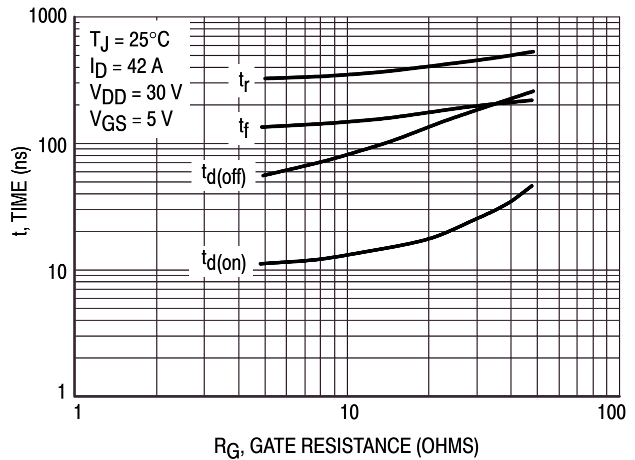


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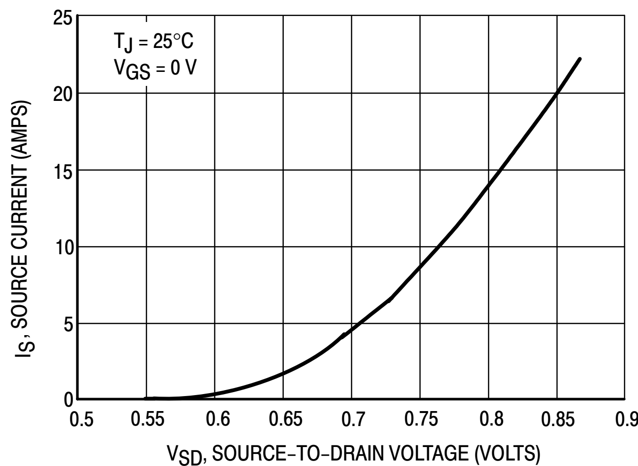


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Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

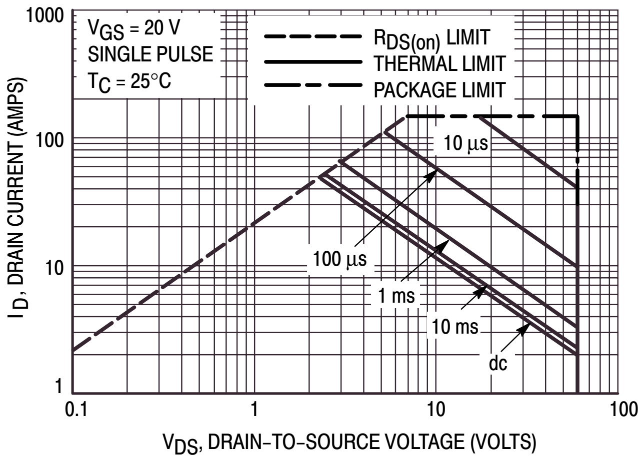



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

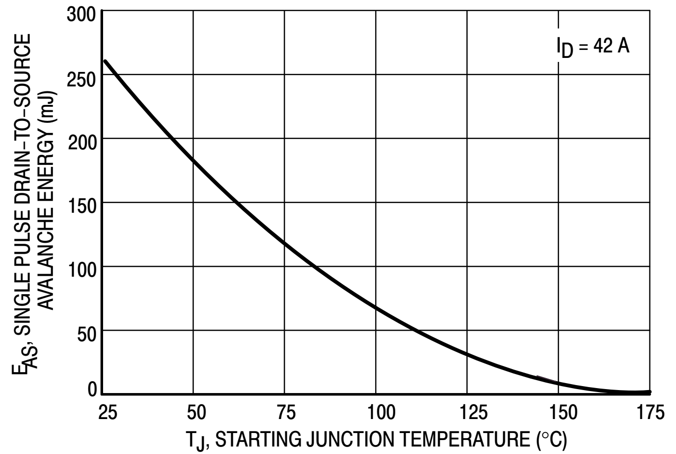



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

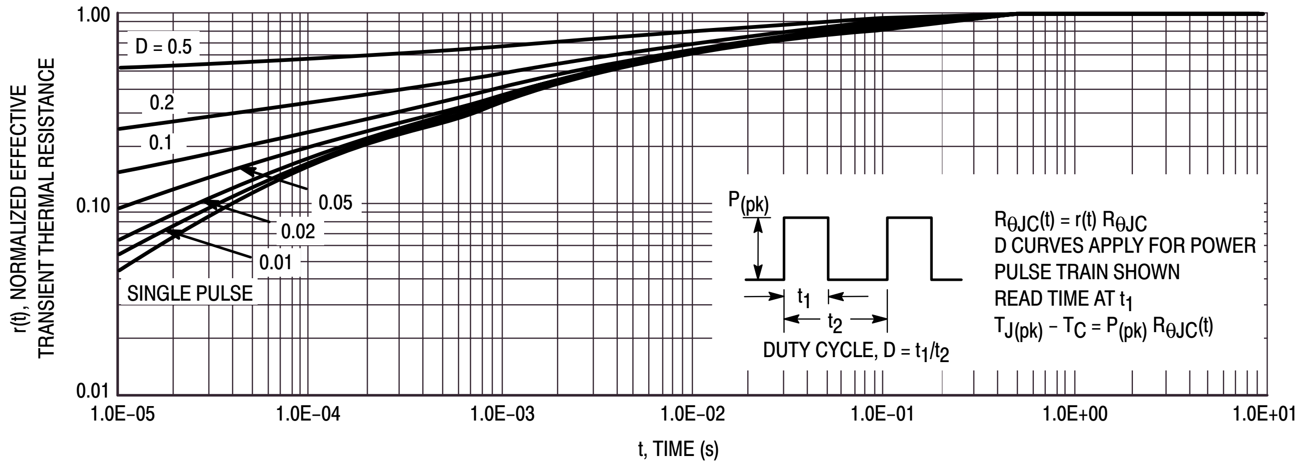



**Figure 13. Thermal Response**

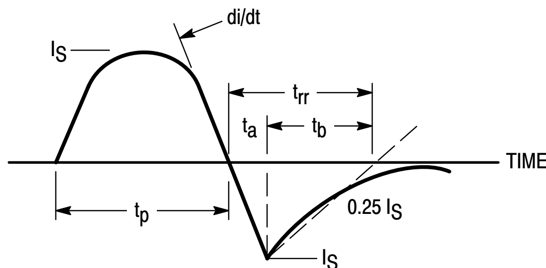



**Figure 14. Diode Reverse Recovery Waveform**

# MTP50P03HDL

**Preferred Device**

# Power MOSFET 50 Amps, 30 Volts, Logic Level

## P–Channel TO–220

**ON Semiconductor™**

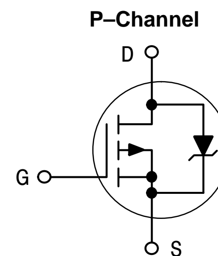
**http://onsemi.com**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**50 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 25 mΩ**

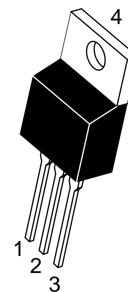
**P–Channel**



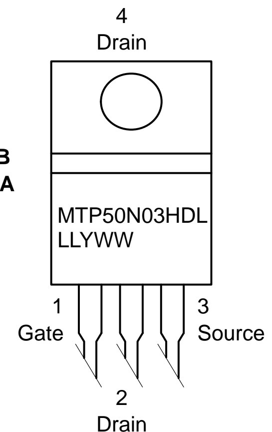

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 30 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 30 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ± 15<br>± 20 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 50<br>31<br>150 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 125<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 50 Apk, L = 1.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 1250 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient, when mounted with the minimum recommended pad size | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP50N03HDL | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP50N03HDL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) Temperature Coefficient (Positive) | ($C_{pk}$ ≥ 2.0) (Note 3.) | $V_{(BR)DSS}$ | 30<br>– | –<br>26 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc) ($V_{DS}$ = 30 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 1.0<br>10 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) Threshold Temperature Coefficient (Negative) | ($C_{pk}$ ≥ 3.0) (Note 3.) | $V_{GS(th)}$ | 1.0<br>– | 1.5<br>4.0 | 2.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 5.0 Vdc, $I_D$ = 25 Adc) | ($C_{pk}$ ≥ 3.0) (Note 3.) | $R_{DS(on)}$ | – | 0.020 | 0.025 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 50 Adc) ($I_D$ = 25 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 0.83<br>– | 1.5<br>1.3 | Vdc |
| Forward Transconductance ($V_{DS}$ = 5.0 Vdc, $I_D$ = 25 Adc) | | $g_{FS}$ | 15 | 20 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3500 | 4900 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1550 | 2170 | |
| Transfer Capacitance | | $C_{rss}$ | – | 550 | 770 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 5.0 Vdc, $R_G$ = 2.3 Ω) | $t_{d(on)}$ | – | 22 | 30 | ns |
| Rise Time | | $t_r$ | – | 340 | 466 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 90 | 117 | |
| Fall Time | | $t_f$ | – | 218 | 300 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 24 Vdc, $I_D$ = 50 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 74 | 100 | nC |
| | | $Q_1$ | – | 13.6 | – | |
| | | $Q_2$ | – | 44.8 | – | |
| | | $Q_3$ | – | 35 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ =50 Adc, $V_{GS}$ = 0 Vdc) ($I_S$ = 50 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 2.39<br>1.84 | 3.0<br>– | Vdc |
| Reverse Recovery Time (See Figure 15) | ($I_S$ = 50 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 106 | – | ns |
| | | $t_a$ | – | 58 | – | |
| | | $t_b$ | – | 48 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.246 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

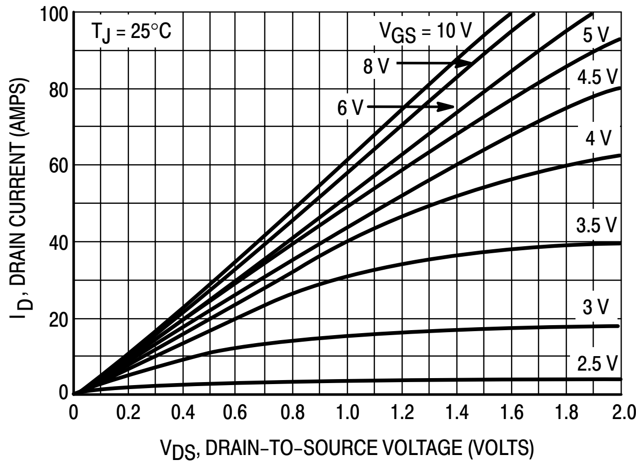



**Figure 1. On–Region Characteristics**

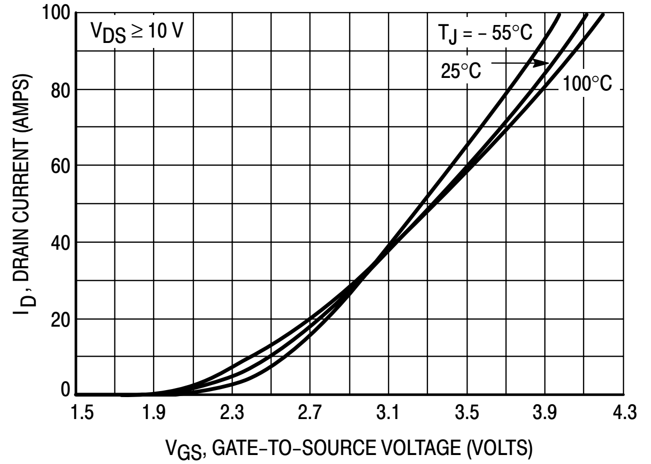



**Figure 2. Transfer Characteristics**

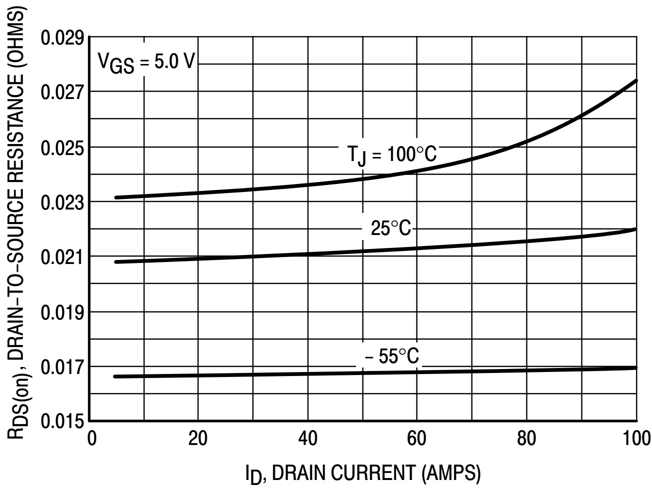



**Figure 3. On–Resistance versus Drain Current and Temperature**

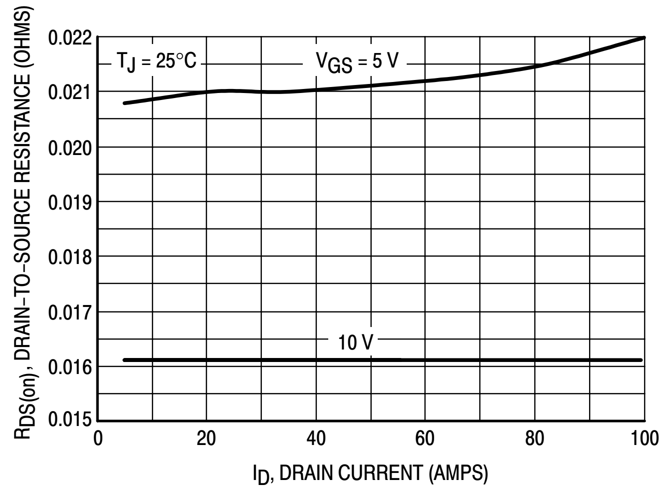



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

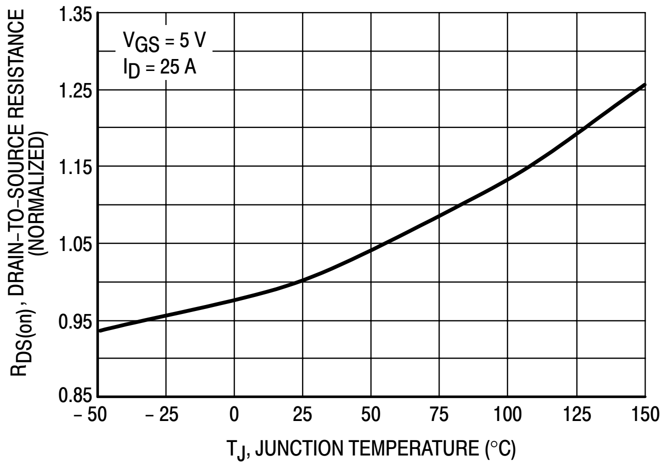



**Figure 5. On–Resistance Variation with Temperature**

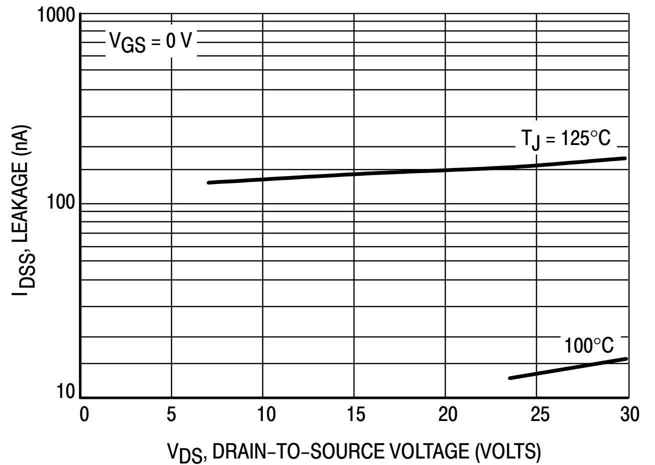



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

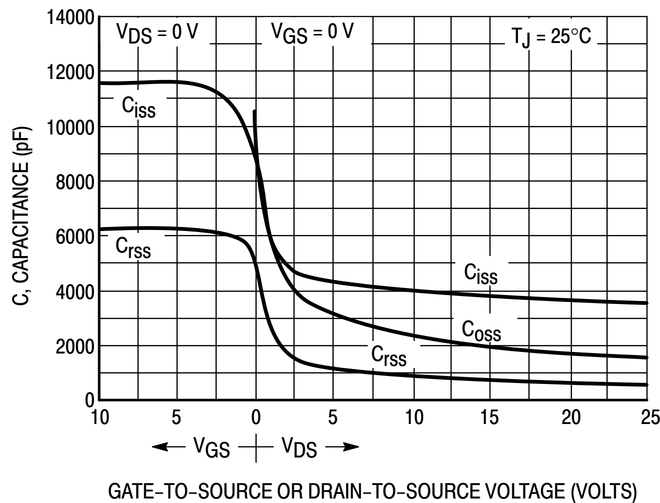



**Figure 7. Capacitance Variation**

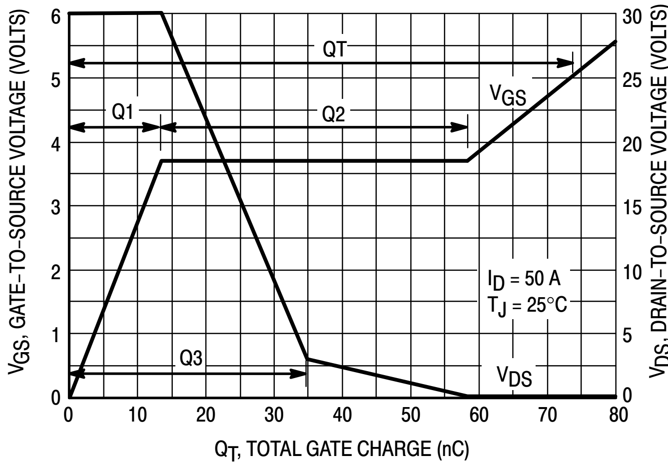



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

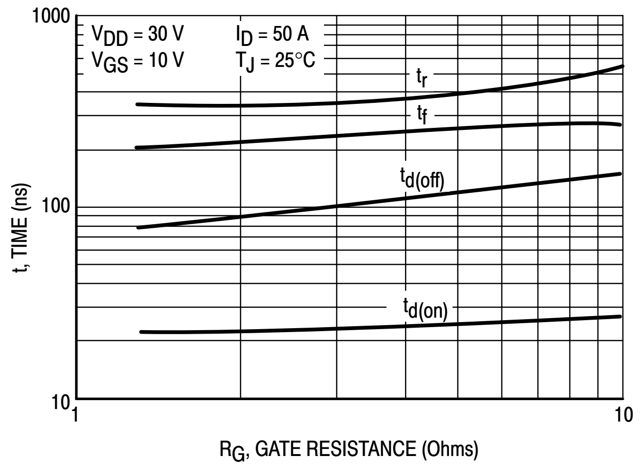



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

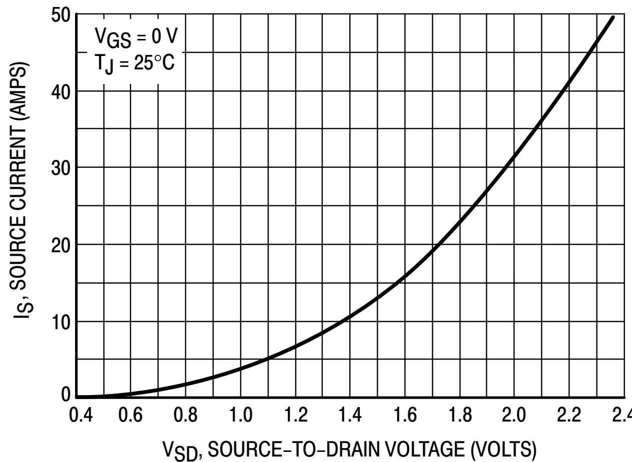



**Figure 10. Diode Forward Voltage versus Current**

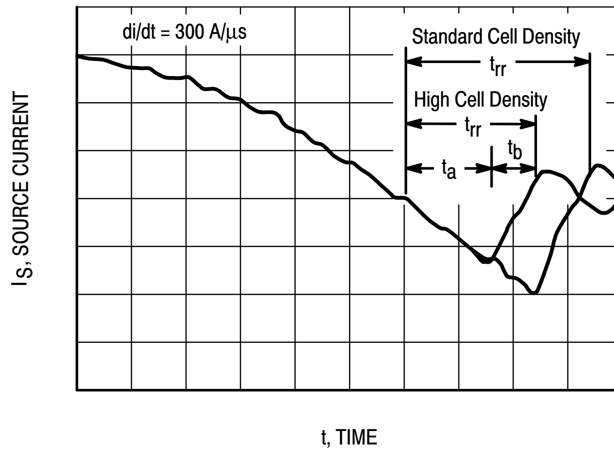



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

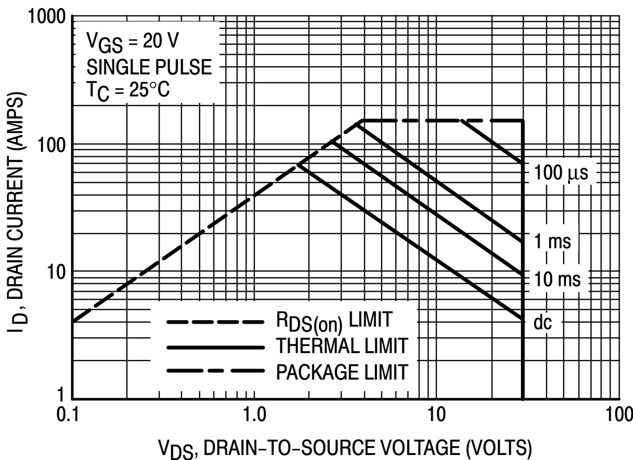



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

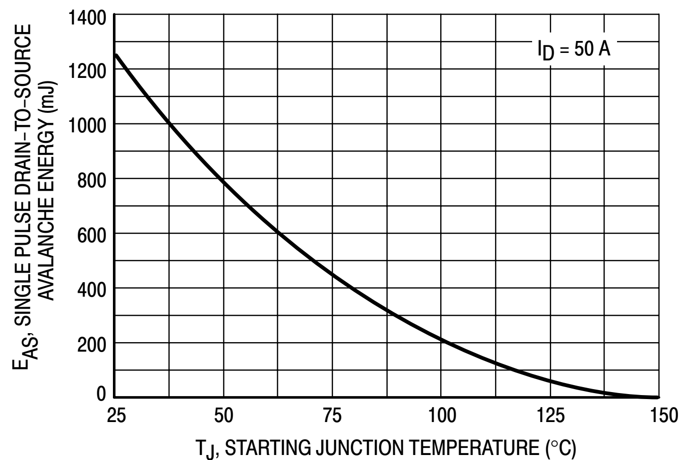



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

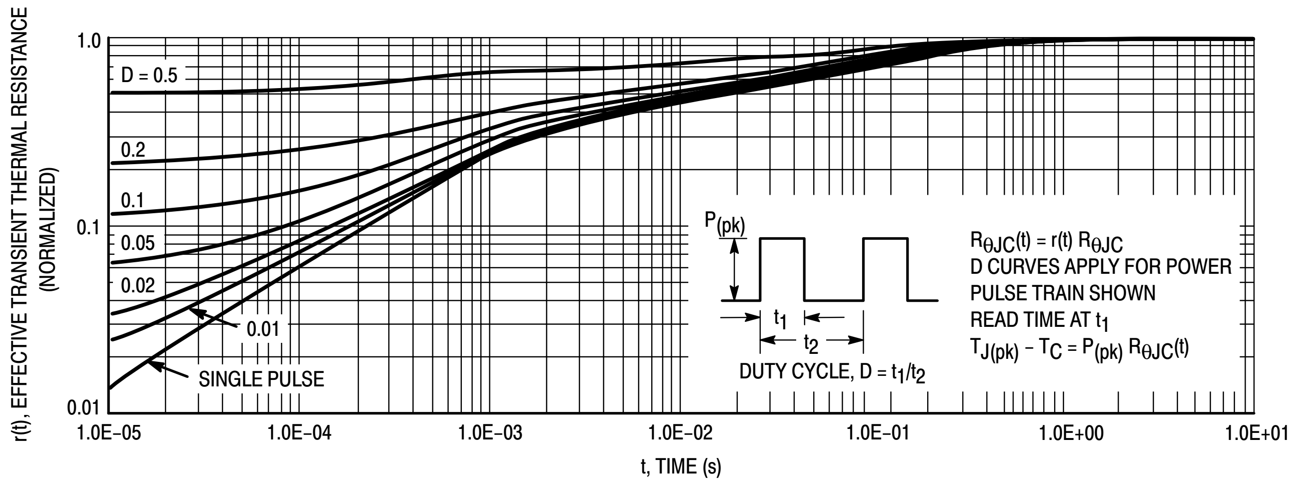



**Figure 14. Thermal Response**

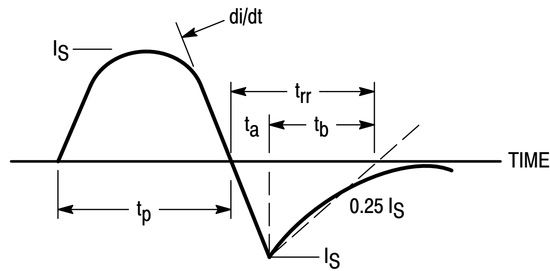



**Figure 15. Diode Reverse Recovery Waveform**

# MTP52N06V

Preferred Device

# Power MOSFET 52 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

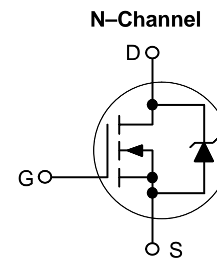
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 52<br>41<br>182 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 188<br>1.25 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 52 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 406 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>0.8<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

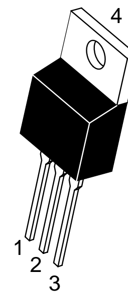
**http://onsemi.com**

**52 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 22 mΩ**

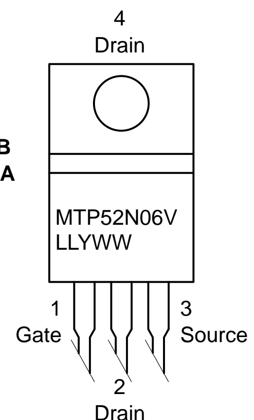
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP52N06V = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP52N06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>66 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>2.7<br>6.4 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 26 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.019 | <br>0.022 | Ohm |
| Drain–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 52 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 26 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.4<br>1.2 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.3 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 24 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1900 | 2660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 580 | 810 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 150 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 20 | ns |
| Rise Time | | $t_r$ | – | 298 | 600 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 70 | 140 | |
| Fall Time | | $t_f$ | – | 110 | 220 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 125 | 175 | nC |
| | | $Q_1$ | – | 10 | – | |
| | | $Q_2$ | – | 30 | – | |
| | | $Q_3$ | – | 40 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | <br>–<br>– | <br>1.0<br>0.98 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 100 | – | ns |
| | | $t_a$ | – | 80 | – | |
| | | $t_b$ | – | 20 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.341 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

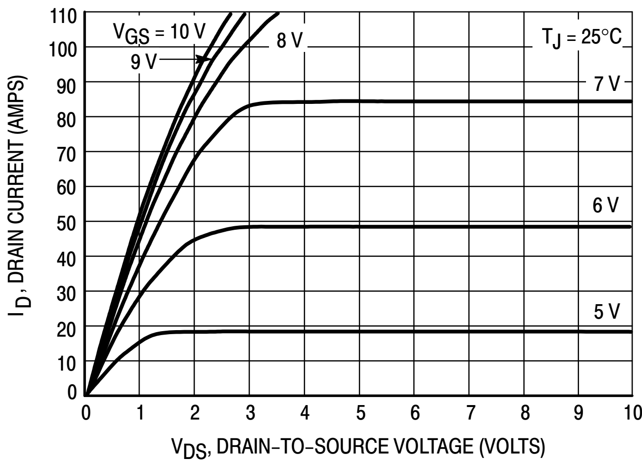



**Figure 1. On–Region Characteristics**

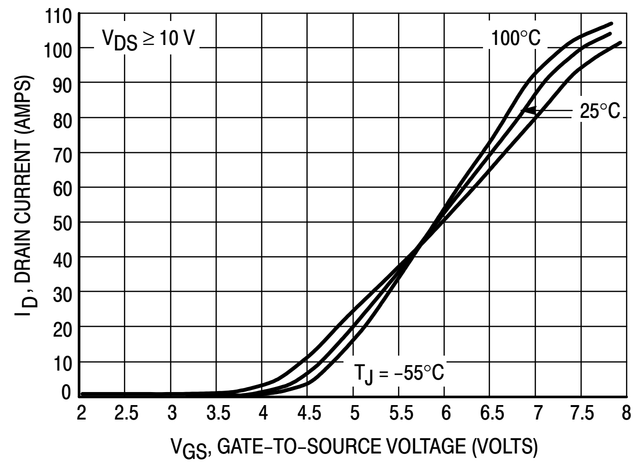



**Figure 2. Transfer Characteristics**

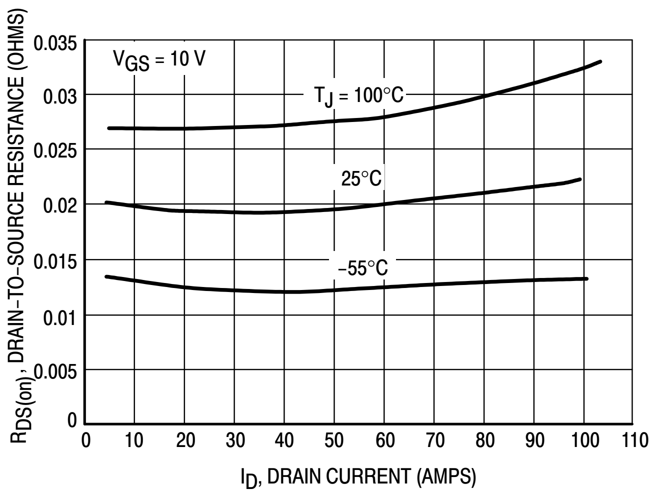



**Figure 3. On–Resistance versus Drain Current and Temperature**

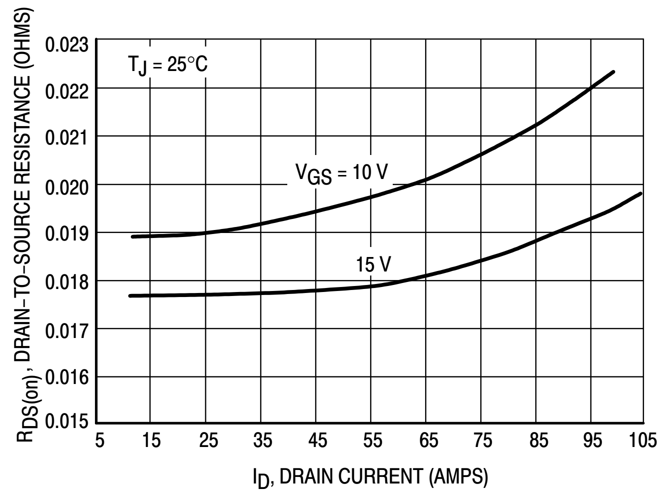



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

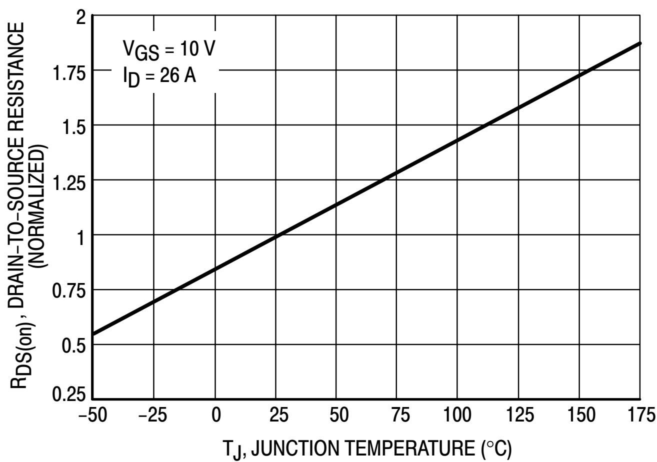



**Figure 5. On–Resistance Variation with Temperature**

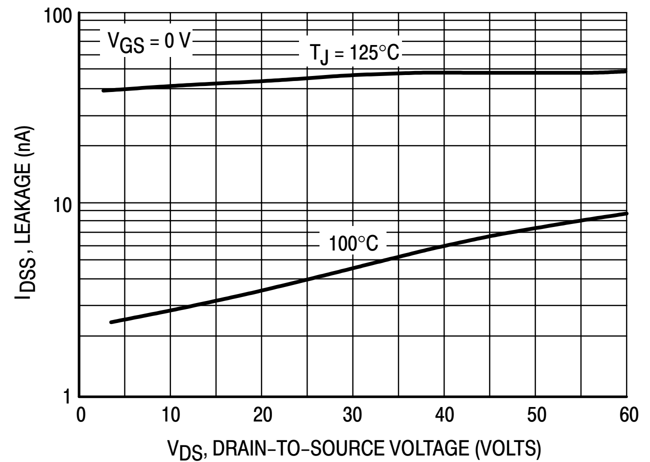



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

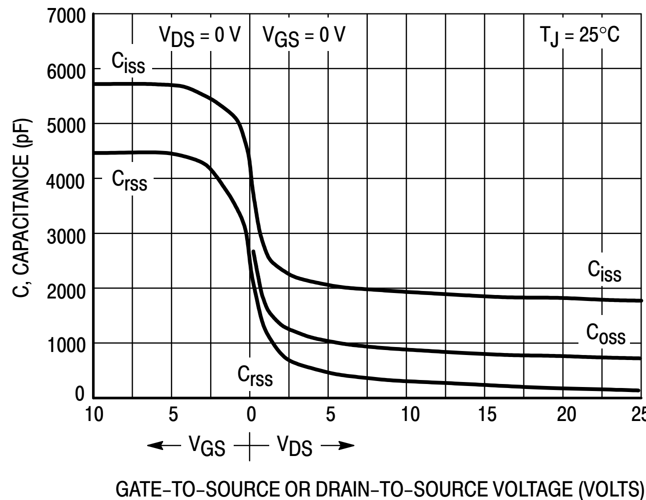



**Figure 7. Capacitance Variation**

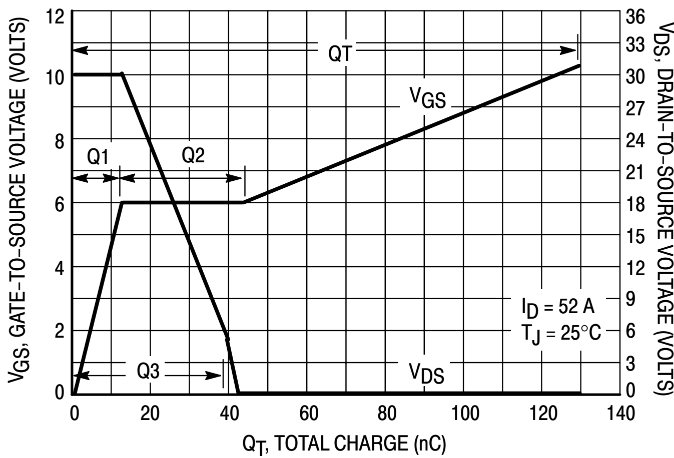



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

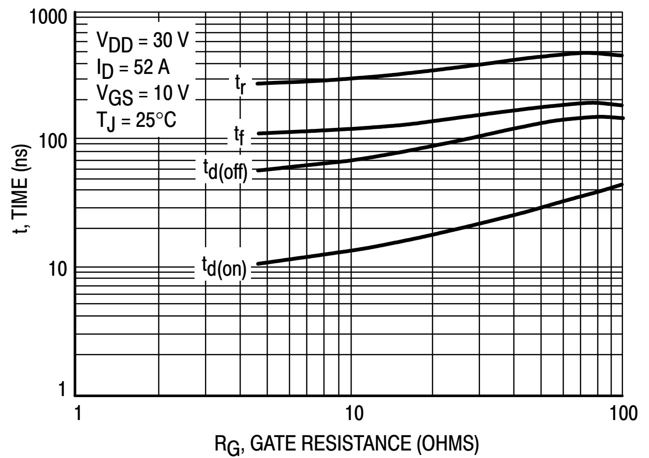



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

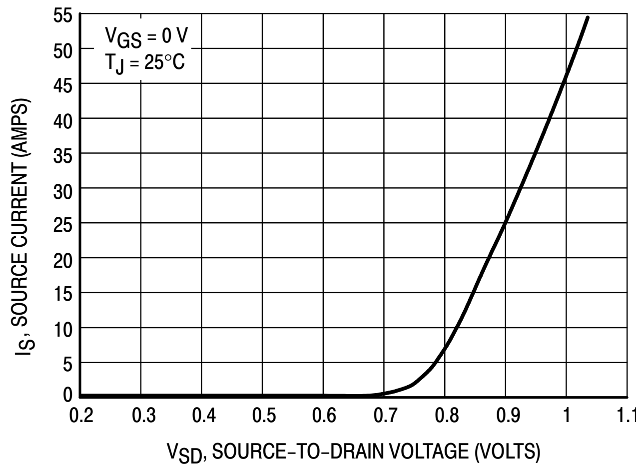



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

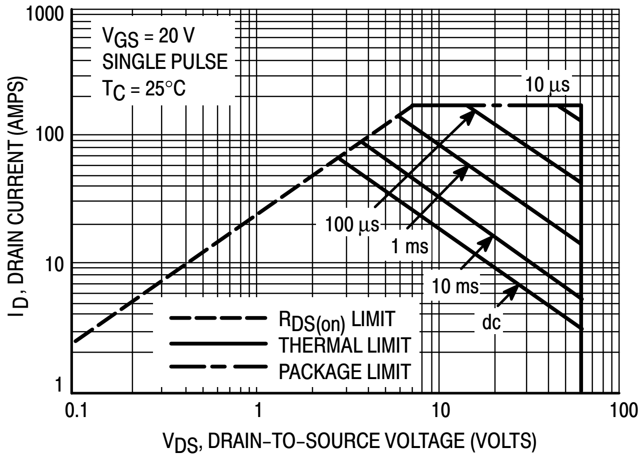



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

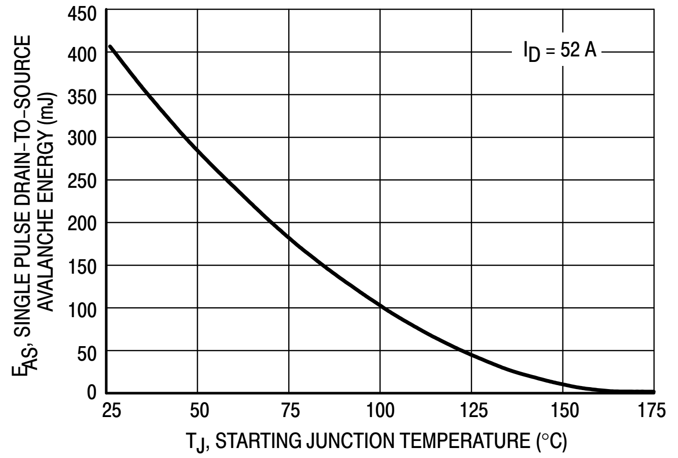



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

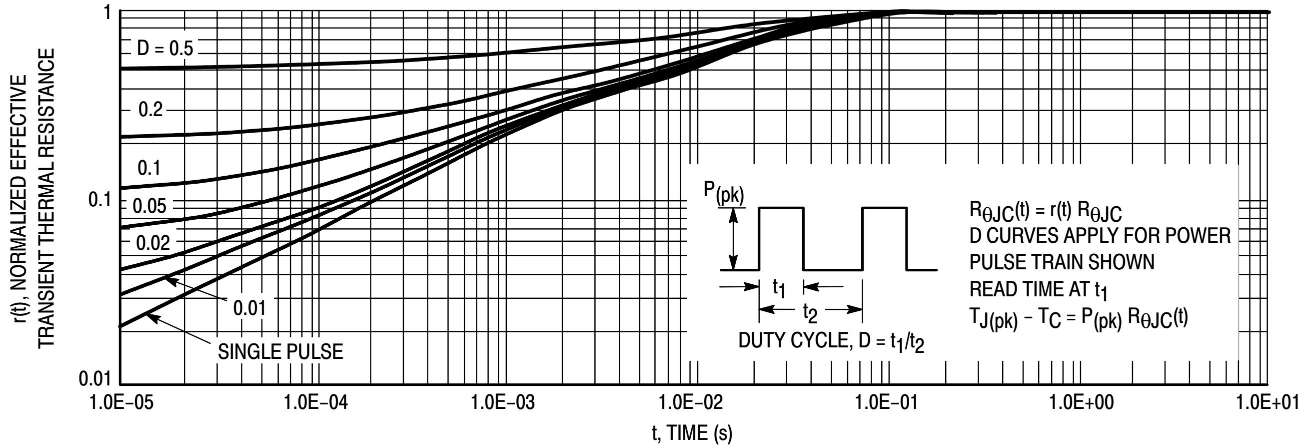



**Figure 13. Thermal Response**

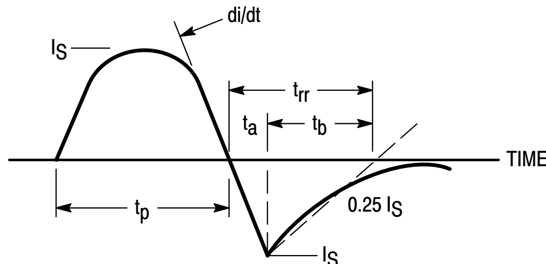



**Figure 14. Diode Reverse Recovery Waveform**

# MTP52N06VL

**Preferred Device**

# Power MOSFET 52 Amps, 60 Volts, Logic Level

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

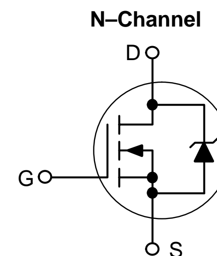
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 52<br>41<br>182 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 188<br>1.25 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5 Vdc, Peak $I_L$ = 52 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 406 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.8<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

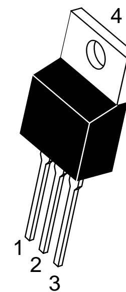
http://onsemi.com

**52 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 25 mΩ**

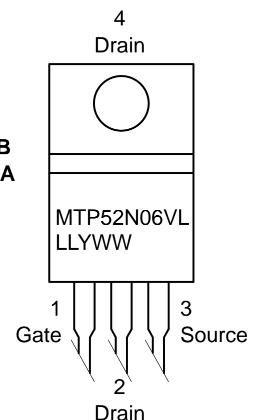
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP52N06VL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP52N06VL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = .25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>65 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.5 | <br>2.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 26 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.022 | <br>0.025 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 5 Vdc, $I_D$ = 52 Adc)<br>($V_{GS}$ = 5 Vdc, $I_D$ = 26 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.6<br>1.4 | Vdc |
| Forward Transconductance ($V_{DS}$ = 6.3 Vdc, $I_D$ = 20 Adc) | | $g_{FS}$ | 17 | 30 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1900 | 2660 | pF |
| Output Capacitance | | $C_{oss}$ | – | 550 | 770 | |
| Transfer Capacitance | | $C_{rss}$ | – | 170 | 340 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 5 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | | $t_r$ | – | 500 | 1000 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 100 | 200 | |
| Fall Time | | $t_f$ | – | 200 | 400 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 52 Adc, $V_{GS}$ = 5 Vdc) | $Q_T$ | – | 62 | 90 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 31 | – | |
| | | $Q_3$ | – | 16 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150 °C) | $V_{SD}$ | <br>–<br>– | <br>1.03<br>0.9 | <br>1.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 52 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 104 | – | ns |
| | | $t_a$ | – | 63 | – | |
| | | $t_b$ | – | 41 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.28 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
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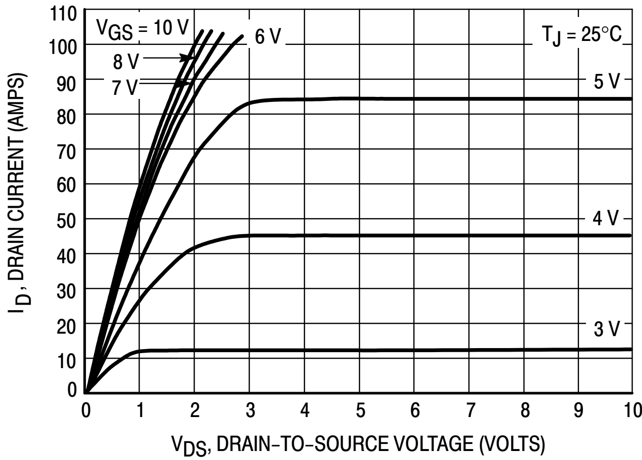


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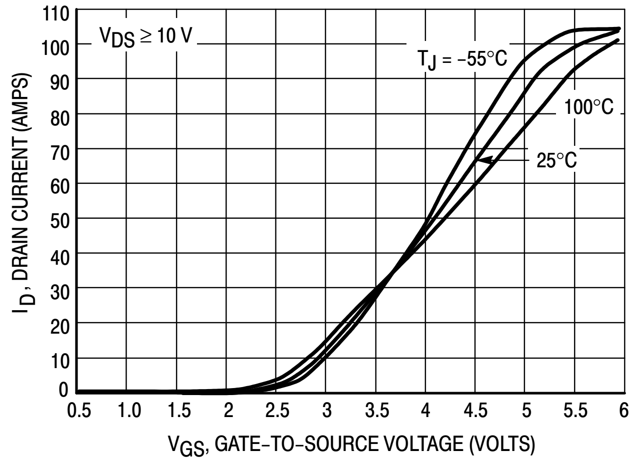


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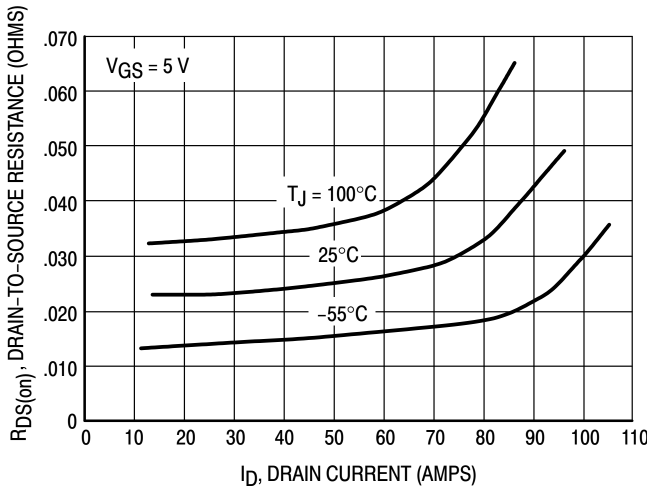


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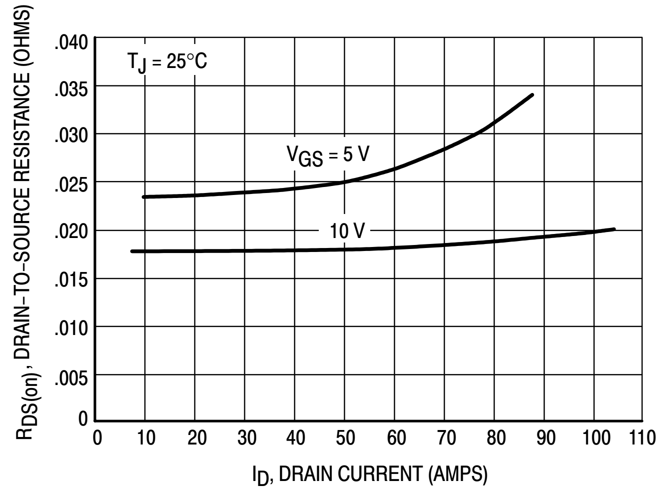


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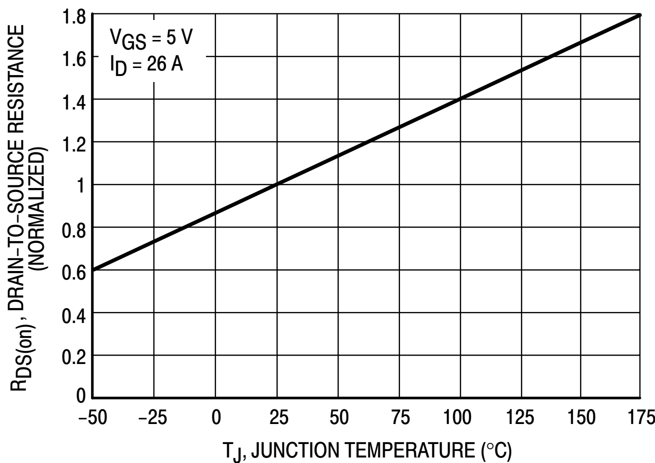


**Figure 5. On−Resistance Variation with Temperature**

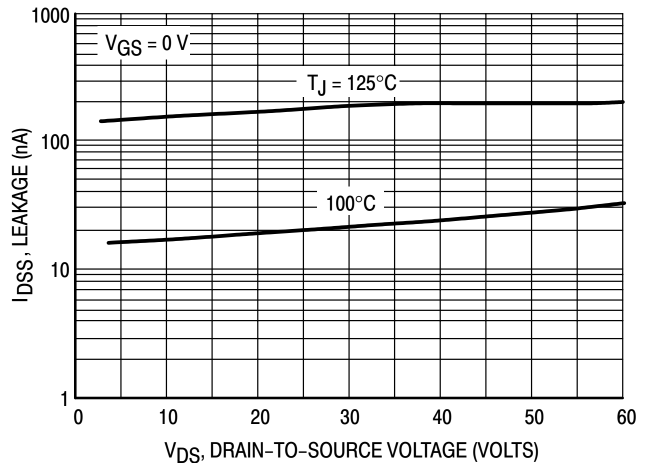


**Figure 6. Drain−To−Source Leakage Current versus Voltage**

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$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

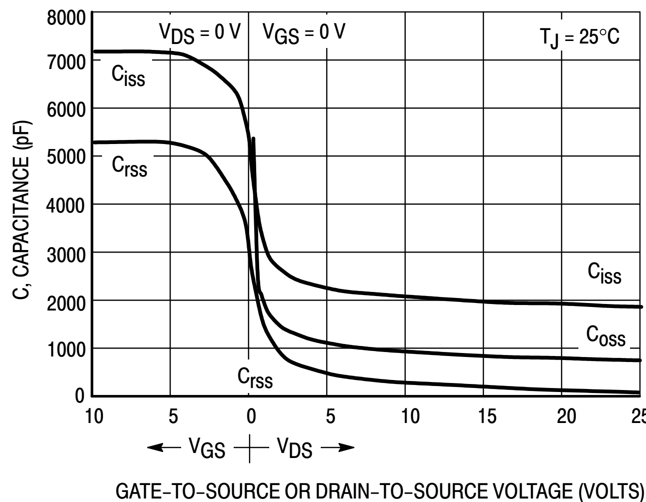



**Figure 7. Capacitance Variation**

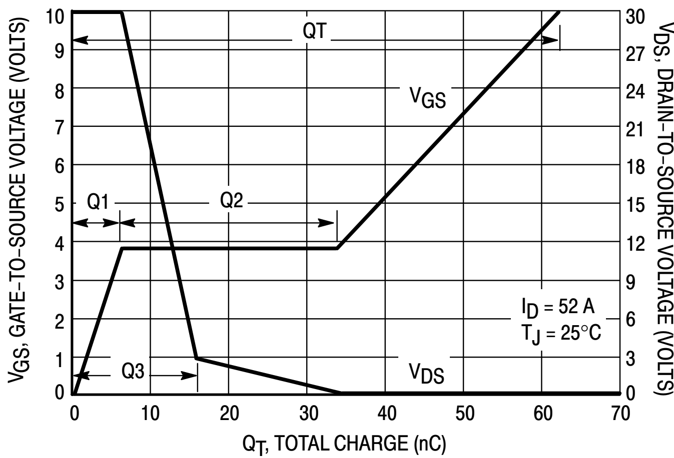



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

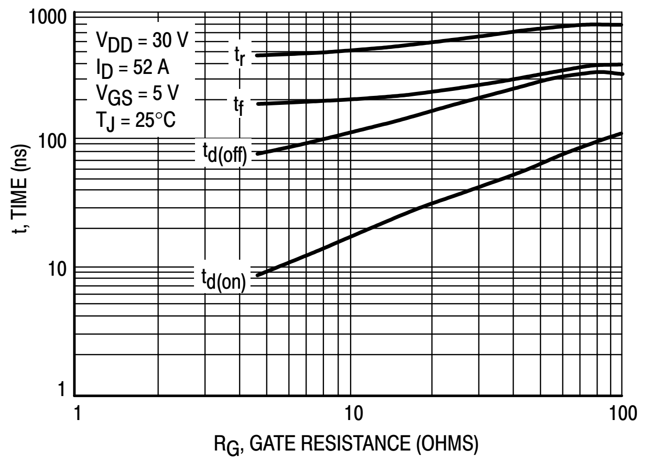



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

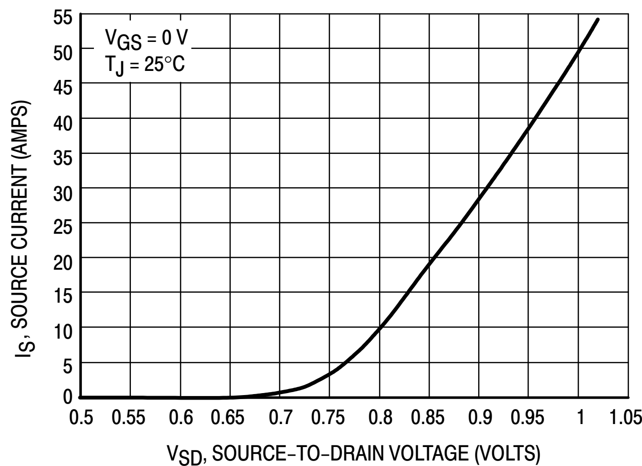



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

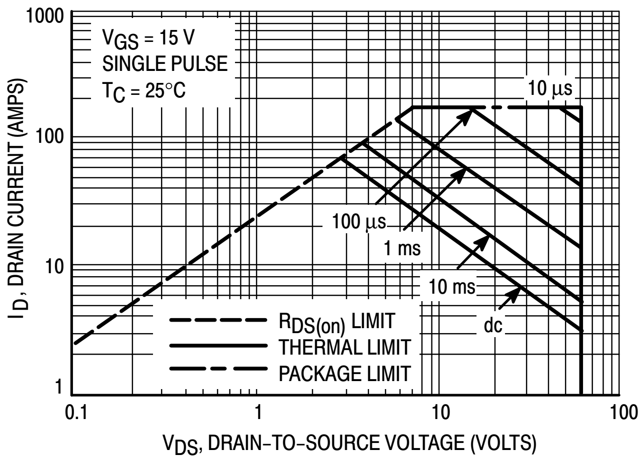



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

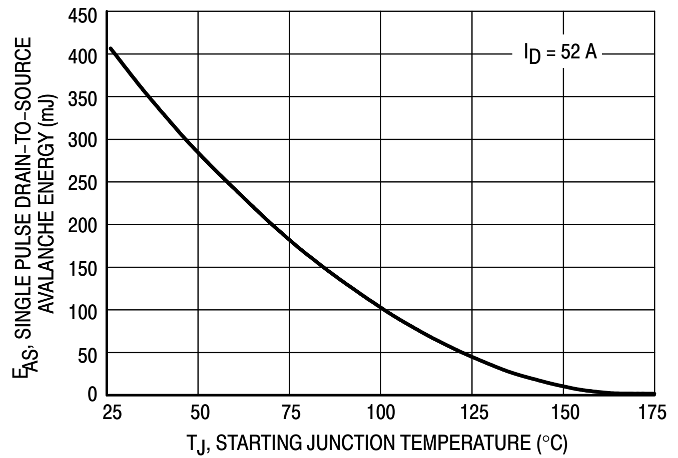



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

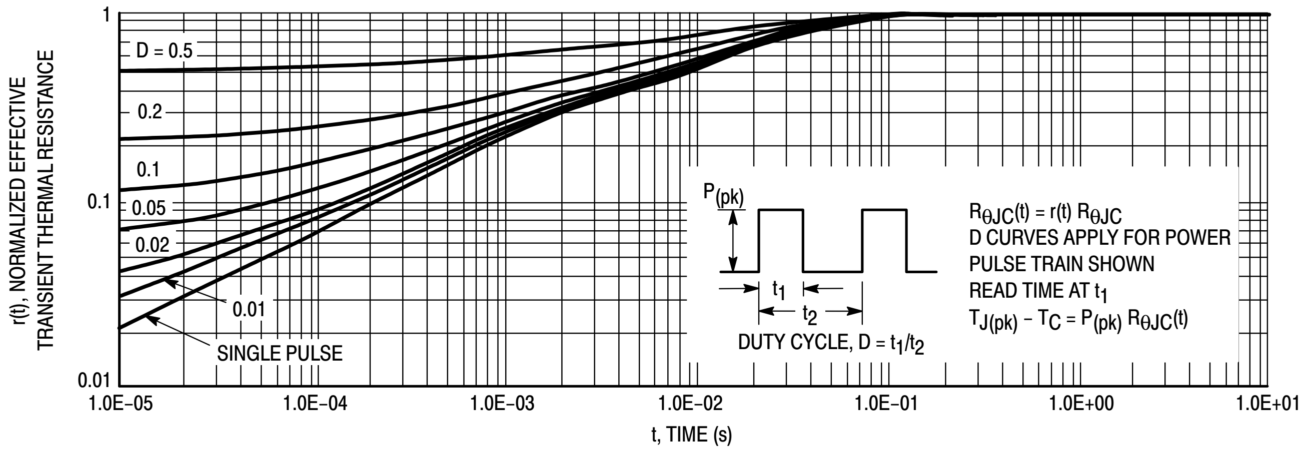



**Figure 13. Thermal Response**

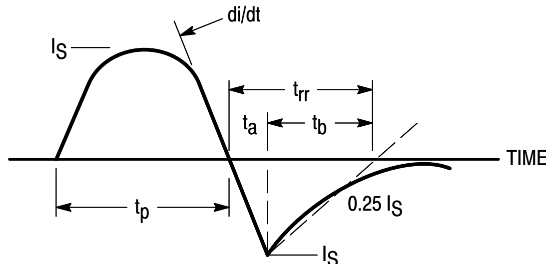



**Figure 14. Diode Reverse Recovery Waveform**

# MTP5P06V

**Preferred Device**

# Power MOSFET 5 Amps, 60 Volts
## P–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

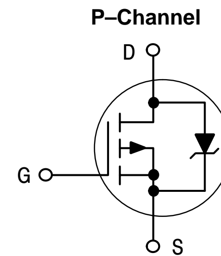
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 15<br>± 25 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ 25°C<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 5<br>4<br>18 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 40<br>0.27 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 5 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 125 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 3.75<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from Case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

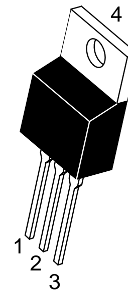
**http://onsemi.com**

**5 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 450 mΩ**

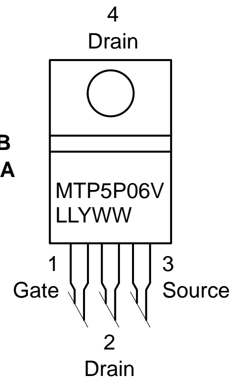
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP5P06V | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP5P06V | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 60<br>– | –<br>61.2 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 15 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | 2.8<br>4.7 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 2.5 Adc) | | $R_{DS(on)}$ | – | 0.34 | 0.45 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc, $I_D$ = 5 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 2.5 Adc, $T_J$ = 150°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 2.7<br>2.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 2.5 Adc) | | $g_{FS}$ | 1.5 | 3.6 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 367 | 510 | pF |
| Output Capacitance | | $C_{oss}$ | – | 140 | 200 | |
| Transfer Capacitance | | $C_{rss}$ | – | 29 | 60 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 5 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 11 | 20 | ns |
| Rise Time | | $t_r$ | – | 26 | 50 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 17 | 30 | |
| Fall Time | | $t_f$ | – | 19 | 40 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 5 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 12 | 20 | nC |
| | | $Q_1$ | – | 3.0 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 5.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 150°C) | $V_{SD}$ | –<br>– | 1.72<br>1.34 | 3.5<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 5 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 97 | – | ns |
| | | $t_a$ | – | 73 | – | |
| | | $t_b$ | – | 24 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.42 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5<br>4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

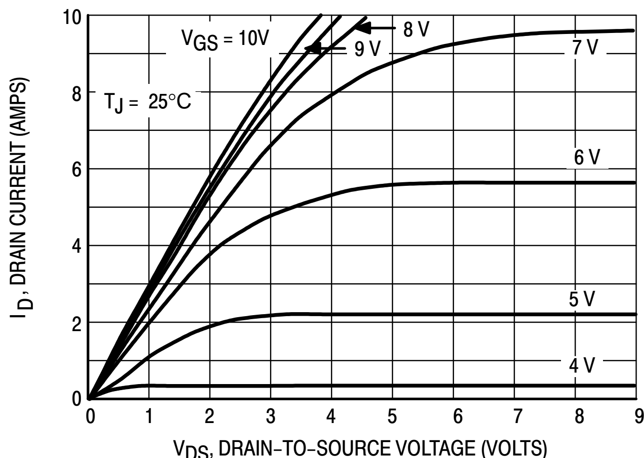



**Figure 1. On–Region Characteristics**

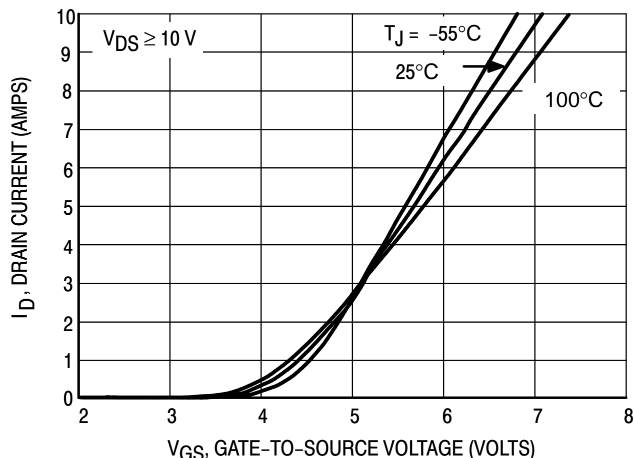



**Figure 2. Transfer Characteristics**

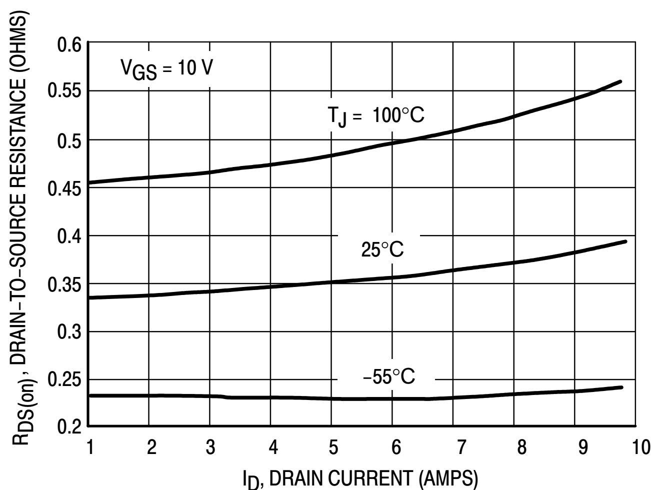



**Figure 3. On–Resistance versus Drain Current and Temperature**

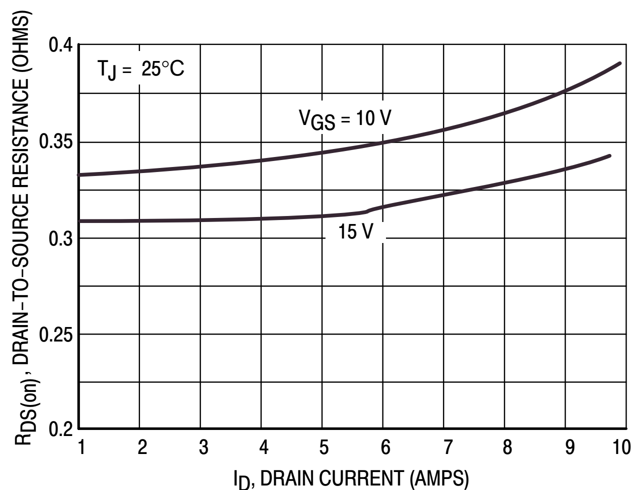



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

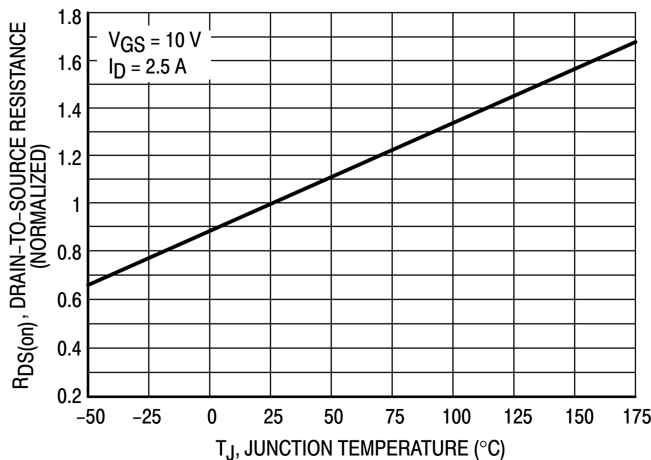



**Figure 5. On–Resistance Variation with Temperature**

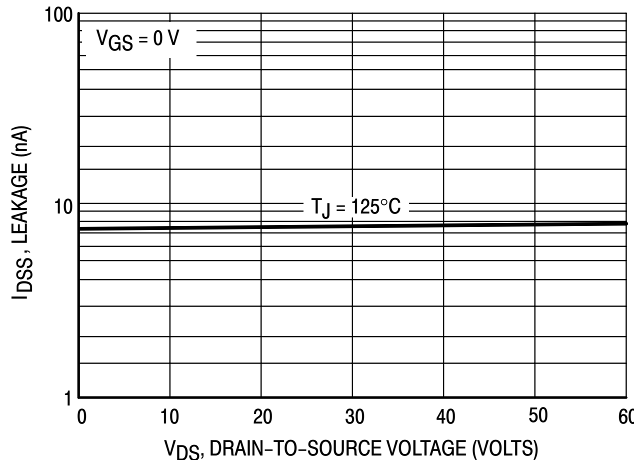



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

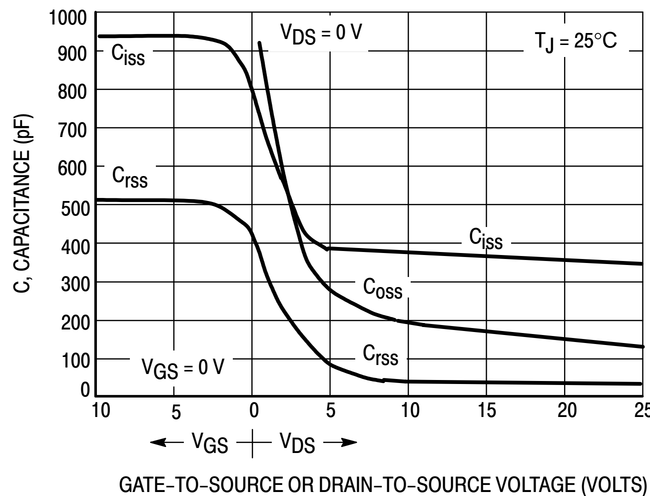



**Figure 7. Capacitance Variation**

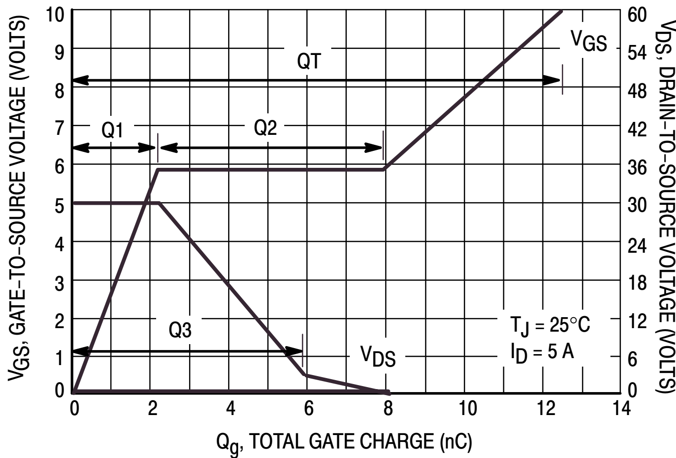



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

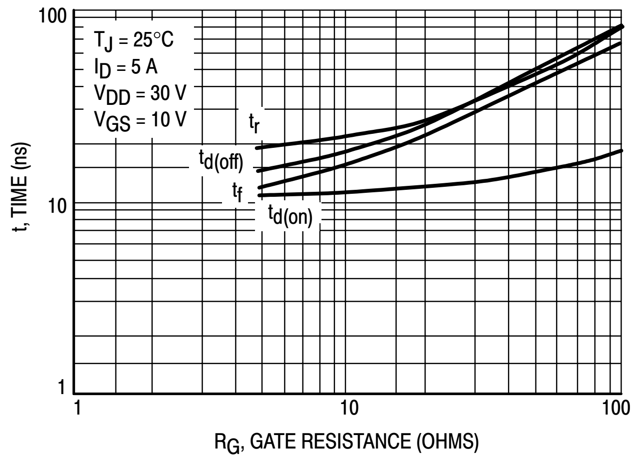



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

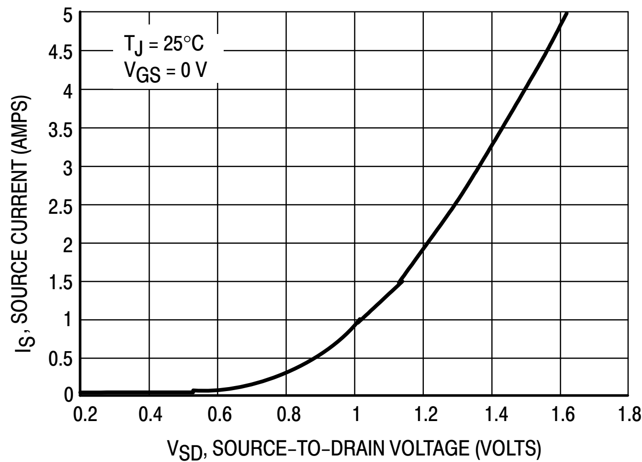



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

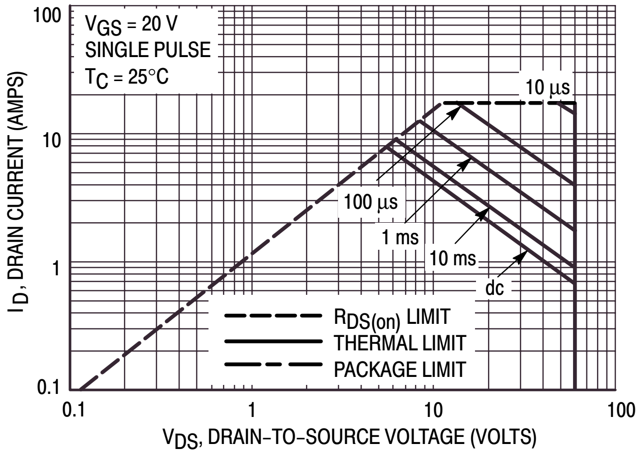



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

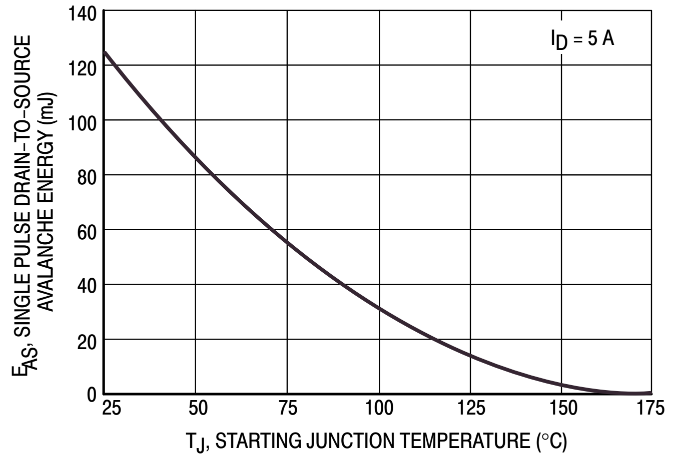



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

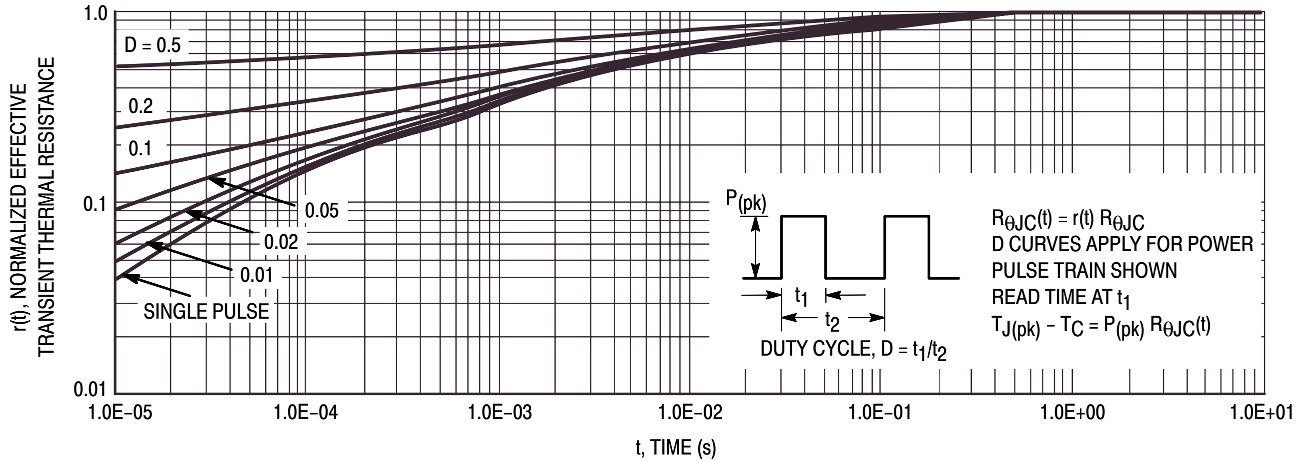



**Figure 13. Thermal Response**

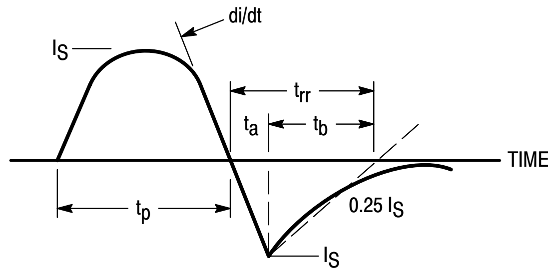



**Figure 14. Diode Reverse Recovery Waveform**

# MTP60N06HD

**Preferred Device**

# Power MOSFET
# 60 Amps, 60 Volts
## N–Channel TO–220

**ON Semiconductor™**

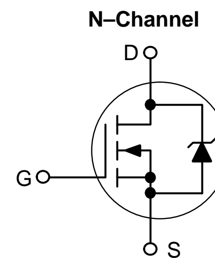
**http://onsemi.com**

**60 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 14 mΩ**

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

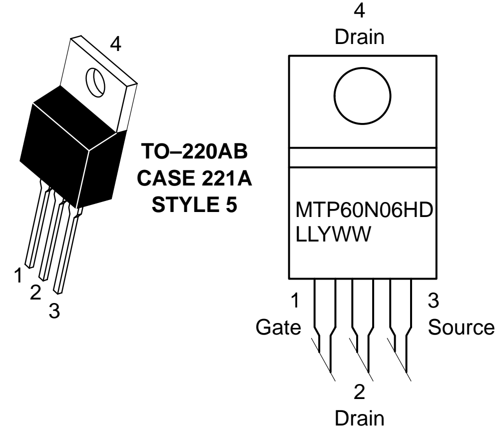
**N–Channel**




**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 30 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 60<br>42.3<br>180 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 60 Apk, L = 0.3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 540 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{θJC}$<br>$R_{θJA}$ | <br>1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTP60N06HD | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP60N06HD | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>60<br>– | <br>–<br>71 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current<br>($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | <br>– | <br>– | <br>100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>2.0<br>– | <br>3.0<br>7.0 | <br>4.0<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 30 Adc) | | $R_{DS(on)}$ | <br>– | <br>0.011 | <br>0.014 | Ohm |
| Drain–to–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 60 Adc)<br>($I_D$ = 30 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>0.9 | Vdc |
| Forward Transconductance<br>($V_{DS}$ = 5.0 Vdc, $I_D$ = 30 Adc) | | $g_{FS}$ | <br>15 | <br>20 | <br>– | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 1950 | 2800 | pF |
| Output Capacitance | | $C_{oss}$ | – | 660 | 924 | |
| Transfer Capacitance | | $C_{rss}$ | – | 147 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 30 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 14 | 26 | ns |
| Rise Time | | $t_r$ | – | 197 | 394 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | 102 | |
| Fall Time | | $t_f$ | – | 124 | 246 | |
| Gate Charge<br>(See Figure 8) | ($V_{DS}$ = 48 Vdc, $I_D$ = 60 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 51 | 71 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 24 | – | |
| | | $Q_3$ | – | 21 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.99<br>0.89 | <br>1.2<br>– | Vdc |
| Reverse Recovery Time<br>(See Figure 15) | ($I_S$ = 60 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 60 | – | ns |
| | | $t_a$ | – | 36 | – | |
| | | $t_b$ | – | 24 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.143 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

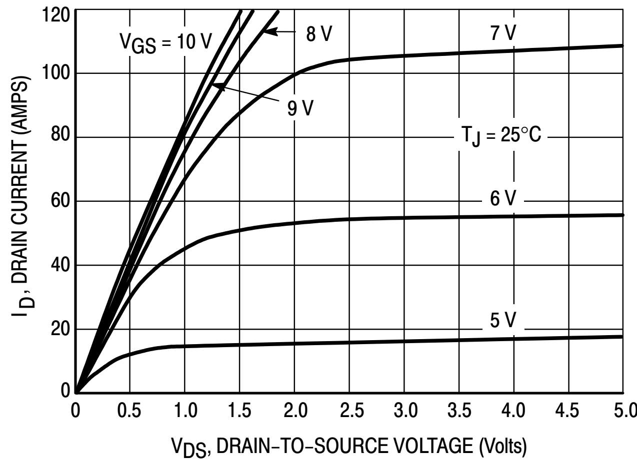



**Figure 1. On–Region Characteristics**

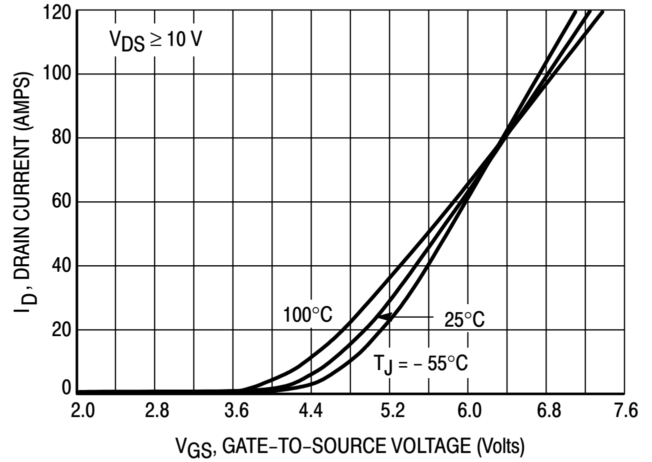



**Figure 2. Transfer Characteristics**

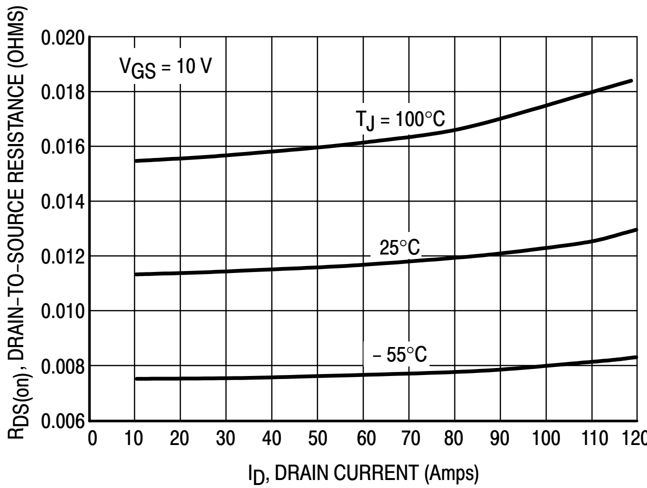



**Figure 3. On–Resistance versus Drain Current and Temperature**

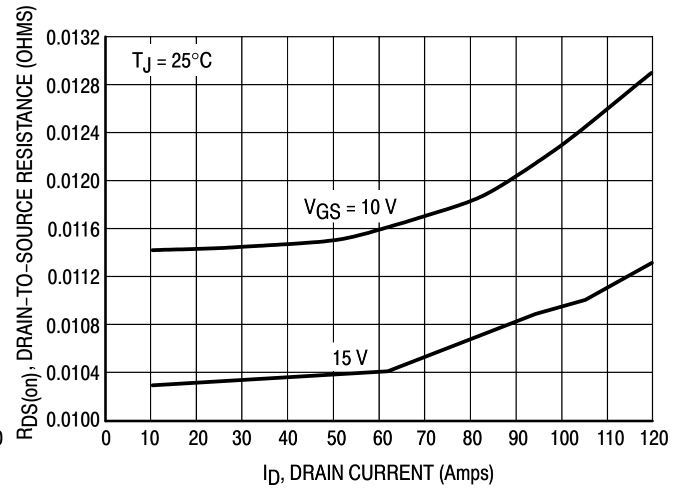



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

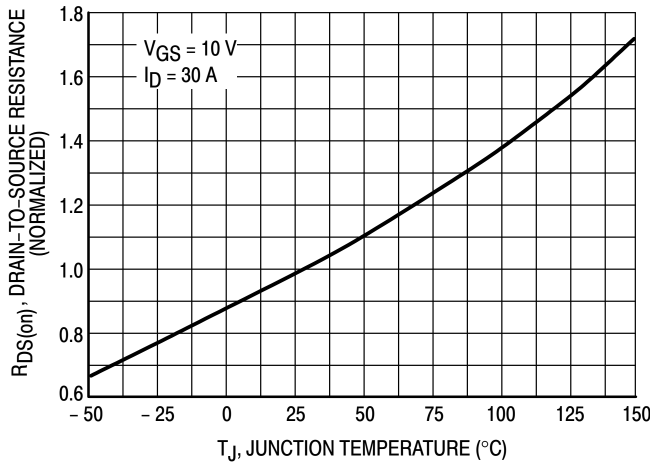



**Figure 5. On–Resistance Variation with Temperature**

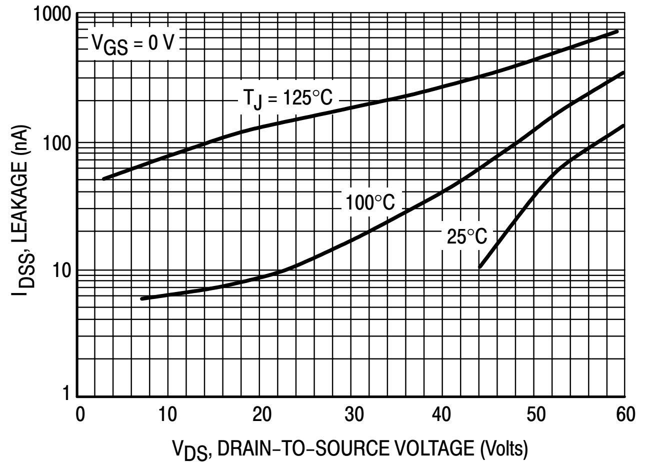



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

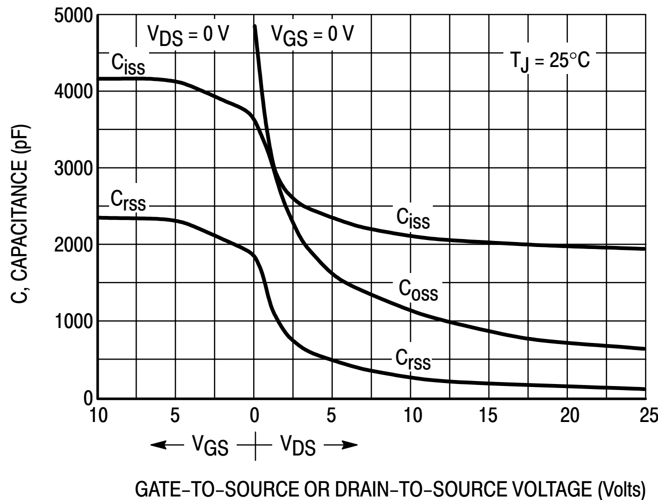



**Figure 7. Capacitance Variation**

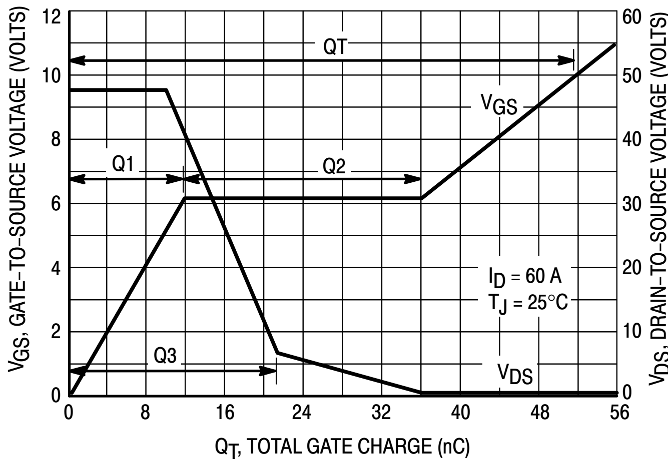



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

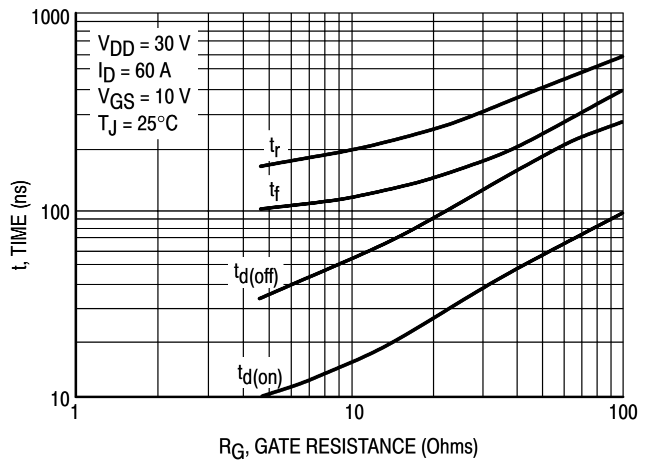



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

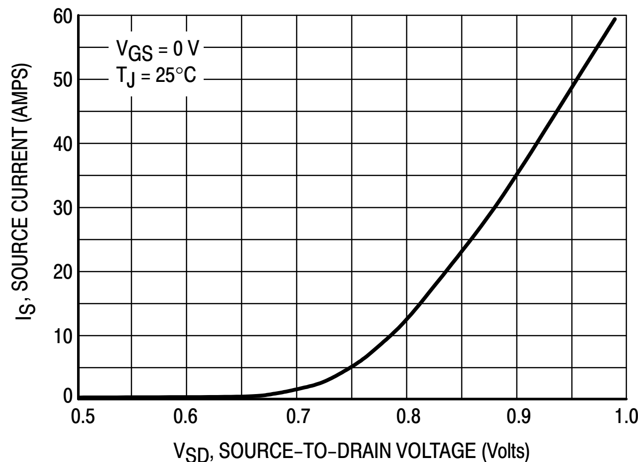



**Figure 10. Diode Forward Voltage versus Current**

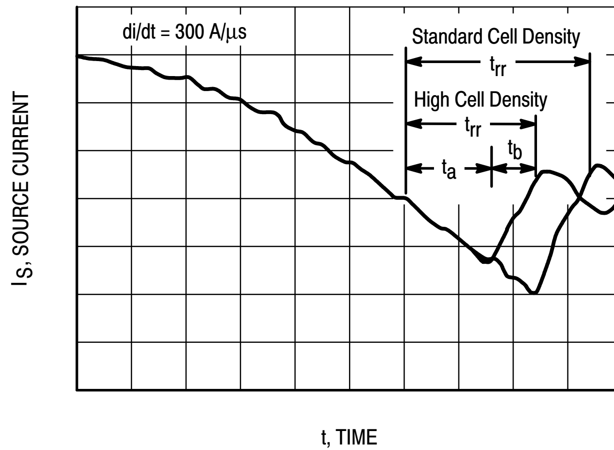



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

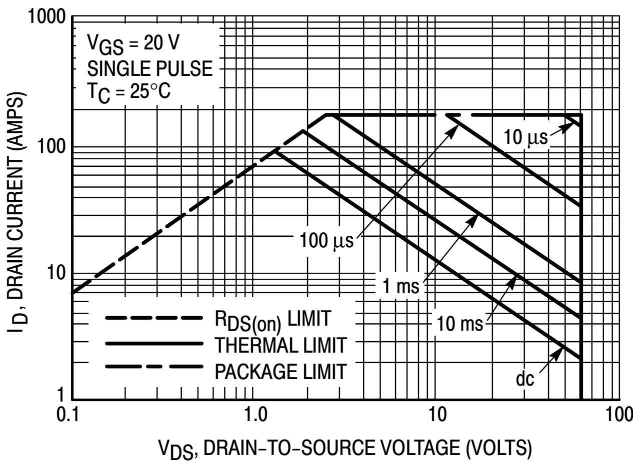



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

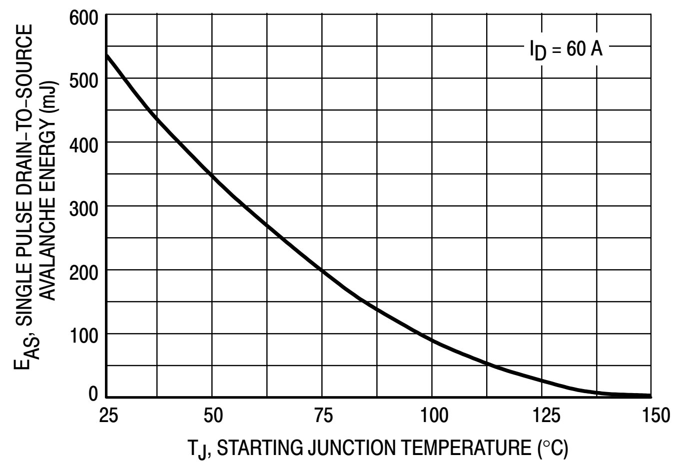



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

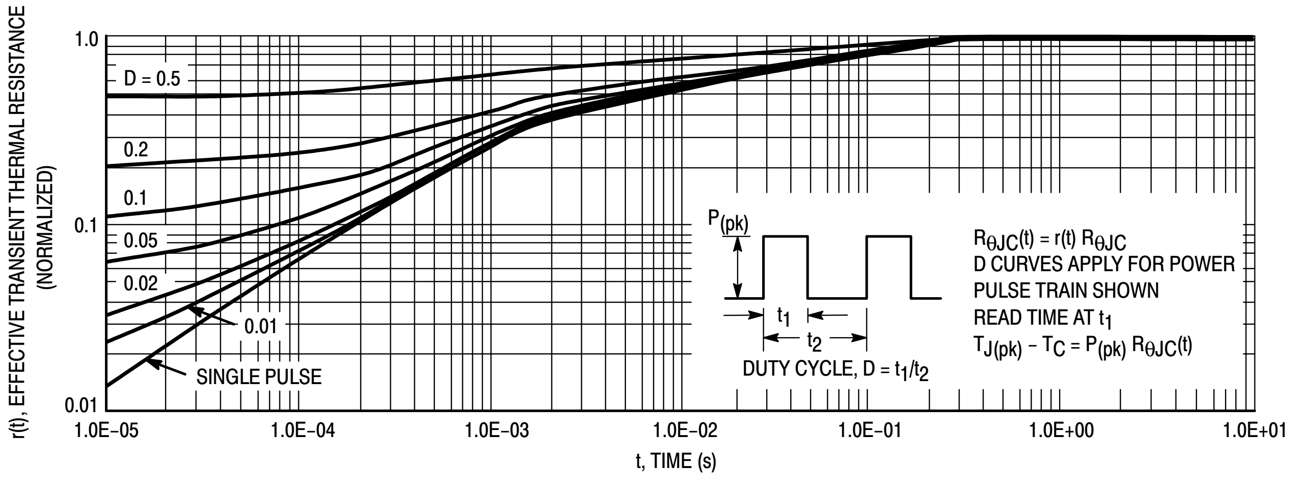



**Figure 14. Thermal Response**

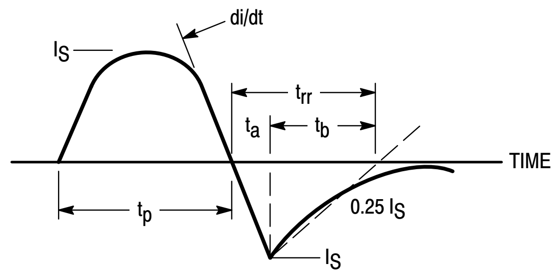



**Figure 15. Diode Reverse Recovery Waveform**

# MTP6P20E

**Preferred Device**

# Power MOSFET 6 Amps, 200 Volts

## P–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

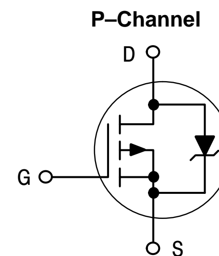
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le$ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 6.0<br>3.9<br>21 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 75<br>0.6 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 6.0 Apk, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 180 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.67<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

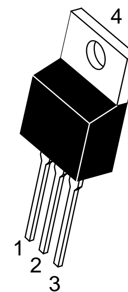
**http://onsemi.com**

**6 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 1 Ω**

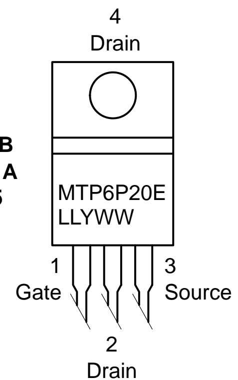
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




MTP6P20E = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP6P20E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 200 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 211 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 3.1 | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 4.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.0 Adc) | | $R_{DS(on)}$ | – | 0.81 | 1.0 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 6.0 Adc) | | $V_{DS(on)}$ | – | 6.0 | 7.2 | Vdc |
| ($I_D$ = 3.0 Adc, $T_J$ = 125°C) | | | – | – | 6.3 | |
| Forward Transconductance ($V_{DS}$ = 8.0 Vdc, $I_D$ = 3.0 Adc) | | $g_{FS}$ | 1.5 | 3.8 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 540 | 750 | pF |
| Output Capacitance | | $C_{oss}$ | – | 128 | 180 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 40 | 90 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 12 | 25 | ns |
| Rise Time | | $t_r$ | – | 32 | 65 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 24 | 50 | |
| Fall Time | | $t_f$ | – | 16 | 30 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 6.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 22 | 30 | nC |
| | | $Q_1$ | – | 4.0 | – | |
| | | $Q_2$ | – | 11 | – | |
| | | $Q_3$ | – | 9.0 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 2.8 | 4.0 | Vdc |
| | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 2.6 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 6.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 188 | – | ns |
| | | $t_a$ | – | 152 | – | |
| | | $t_b$ | – | 36 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.595 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) | | $L_D$ | – | 3.5 | – | nH |
| (Measured from the drain lead 0.25″ from package to center of die) | | | – | 4.5 | – | |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

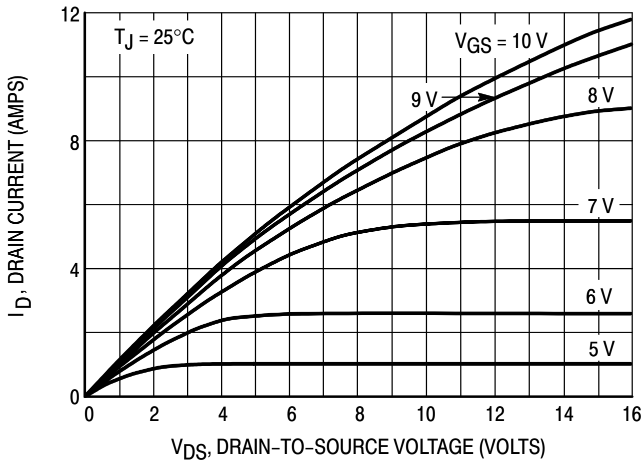



**Figure 1. On–Region Characteristics**

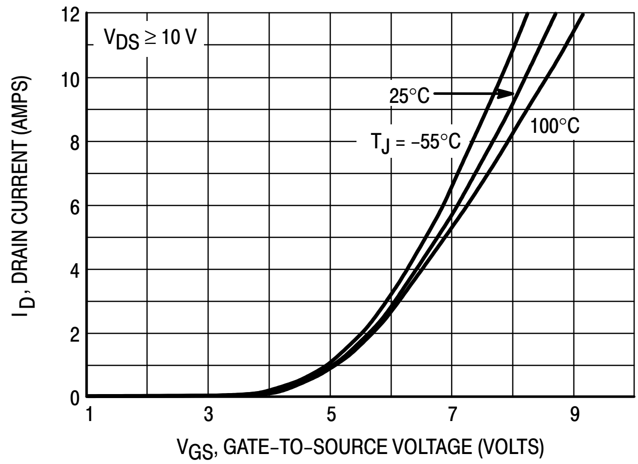



**Figure 2. Transfer Characteristics**

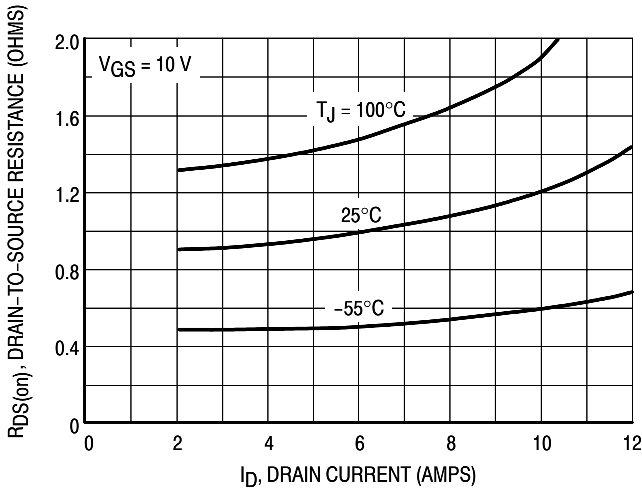



**Figure 3. On–Resistance versus Drain Current and Temperature**

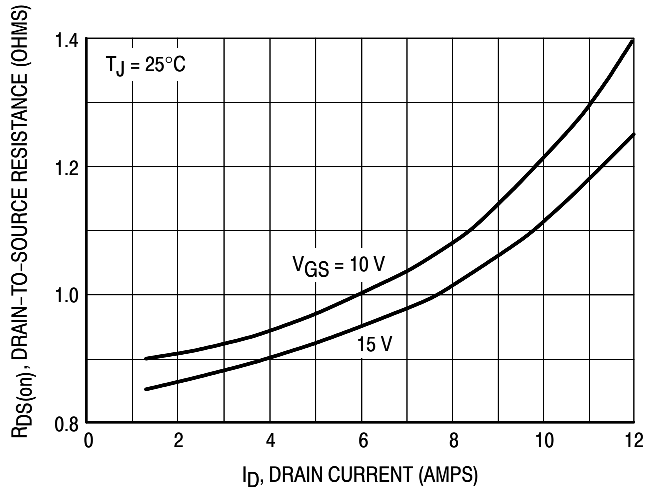



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

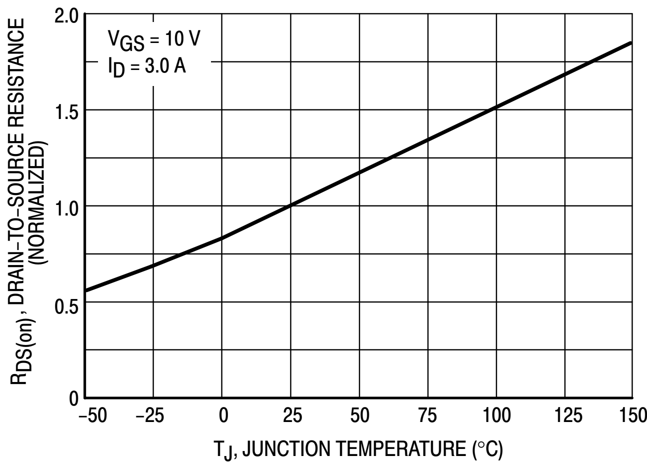



**Figure 5. On–Resistance Variation with Temperature**

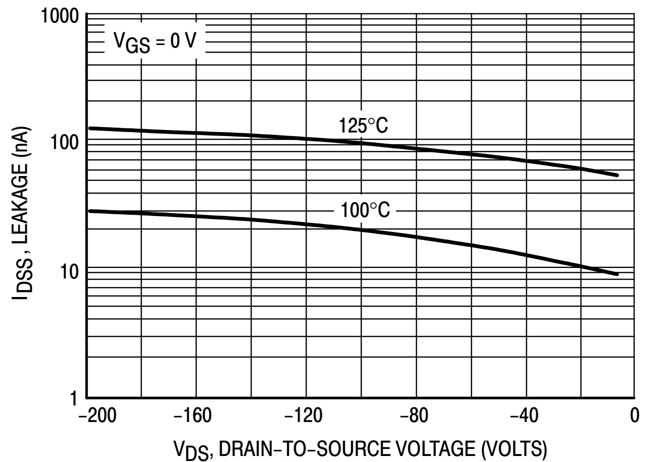



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

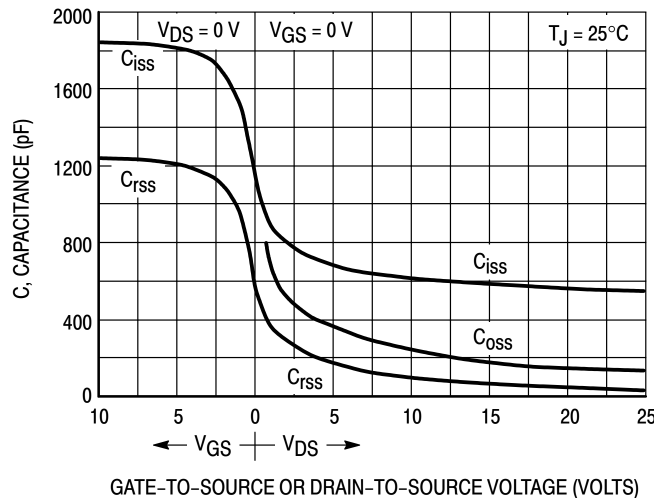



**Figure 7. Capacitance Variation**

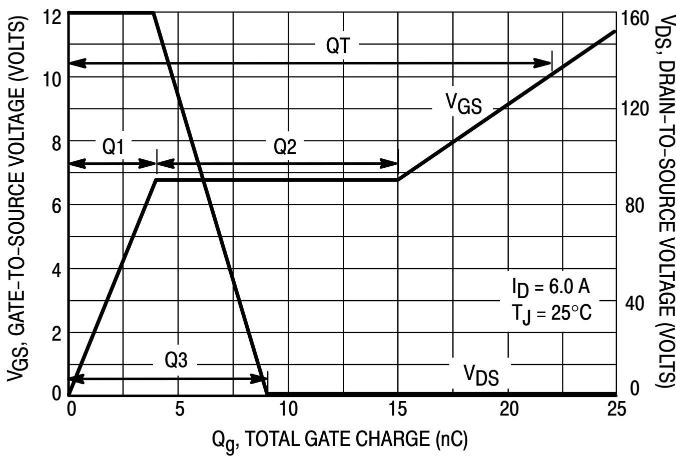



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

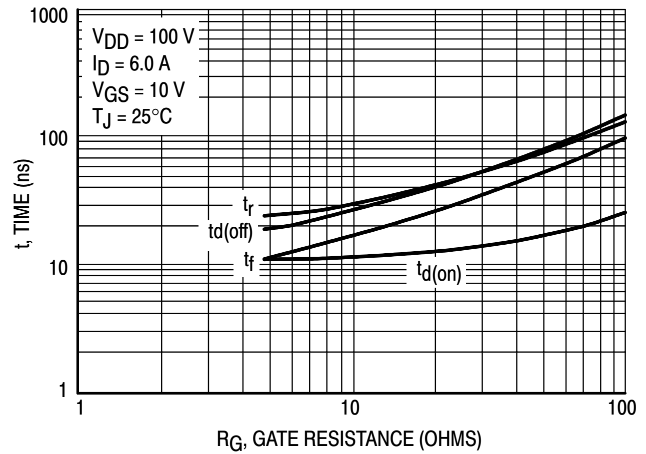



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

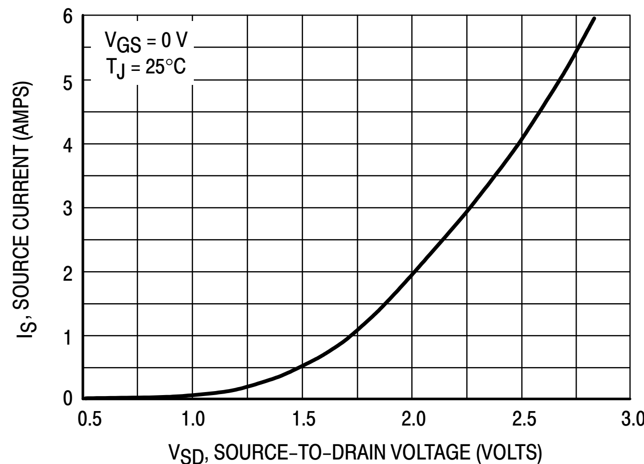



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

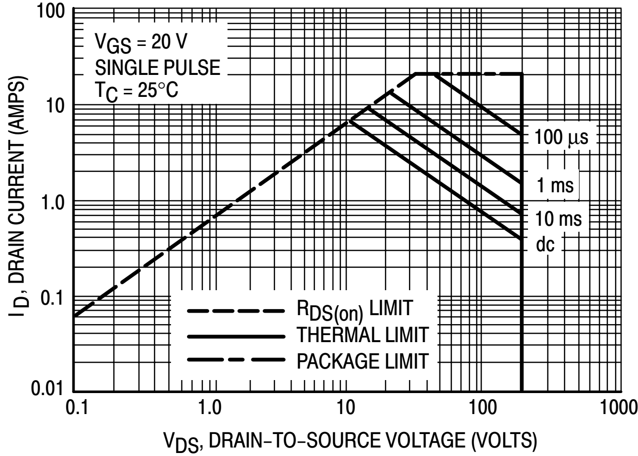



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

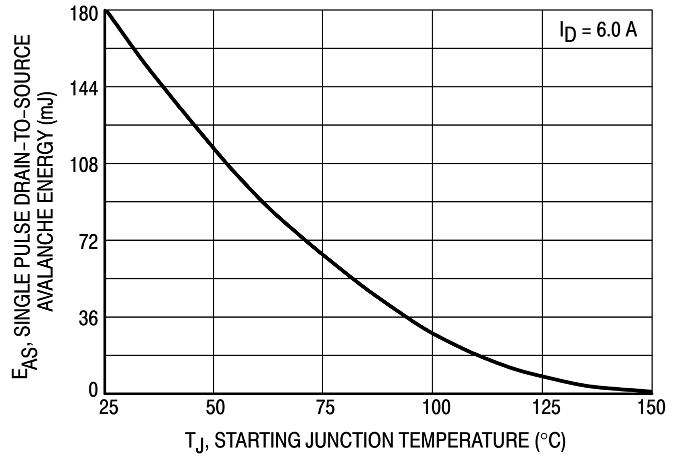



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

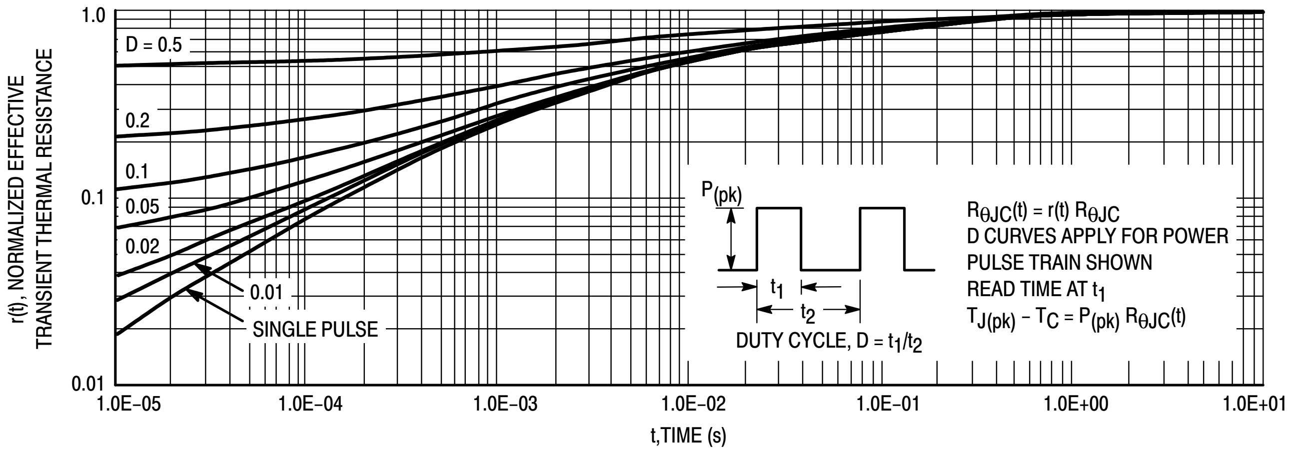



**Figure 13. Thermal Response**

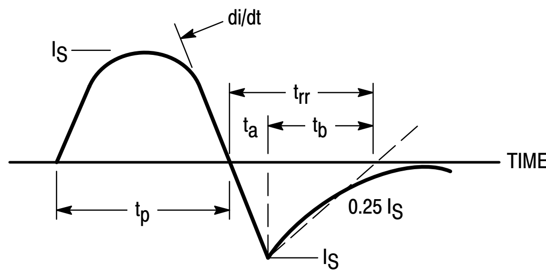



**Figure 14. Diode Reverse Recovery Waveform**

# MTP75N03HDL

**Preferred Device**

# Power MOSFET
# 75 Amps, 25 Volts, Logic Level
## N–Channel TO–220

**ON Semiconductor™**

http://onsemi.com

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

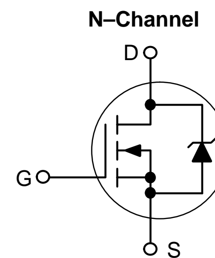
- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

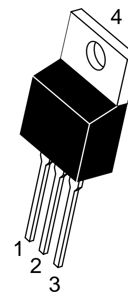
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 25 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 25 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Single Pulse ($t_p \leq$ 10 ms) | $V_{GS}$ | ± 15<br>± 20 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>59<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 25 Vdc, $V_{GS}$ = 5.0 Vdc,<br>$I_L$ = 75 Apk, L = 0.1 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 280 | mJ |
| Thermal Resistance<br>–Junction to Case<br>–Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**75 AMPERES**
**25 VOLTS**
**$R_{DS(on)}$ = 9 mΩ**

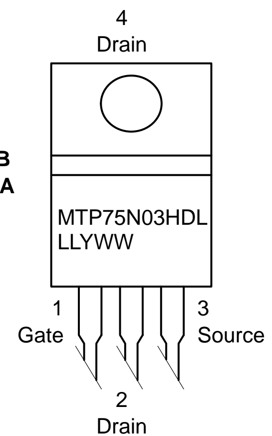
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




MTP75N03HDL = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP75N03HDL | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mA)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>25<br> | <br>–<br> | <br>–<br> | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>100<br>500 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 V) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 0.25 mA)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>1.0<br> | <br>1.5<br> | <br>2.0<br> | Vdc<br><br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 5.0 Vdc, $I_D$ = 37.5 Adc) | $R_{DS(on)}$ | <br>– | <br>6.0 | <br>9.0 | mΩ |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 75 Adc)<br>($I_D$ = 37.5 Adc, $T_J$ = 125°C) | $V_{DS(on)}$ | <br>–<br>– | <br><br>– | <br>0.68<br>0.6 | Vdc |
| Forward Transconductance ($V_{DS}$ = 3.0 Vdc, $I_D$ = 20 Adc) | $g_{FS}$ | 15 | 55 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 4025 | 5635 | pF |
| Output Capacitance | $C_{oss}$ | – | 1353 | 1894 | |
| Reverse Transfer Capacitance | $C_{rss}$ | – | 307 | 430 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | |
| Turn–On Delay Time ($V_{DS}$ = 15 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc, $R_g$ = 4.7 Ω) | $t_{d(on)}$ | – | 24 | 48 | ns |
| Rise Time | $t_r$ | – | 493 | 986 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 60 | 120 | |
| Fall Time | $t_f$ | – | 149 | 300 | |
| Gate Charge ($V_{DS}$ = 24 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 5.0 Vdc) | $Q_T$ | – | 61 | 122 | nC |
| | $Q_1$ | – | 14 | 28 | |
| | $Q_2$ | – | 33 | 66 | |
| | $Q_3$ | – | 27 | 54 | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.97<br>0.87 | <br>1.1<br>– | Vdc |
| Reverse Recovery Time ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 58 | – | ns |
| | $t_a$ | – | 27 | – | |
| | $t_b$ | – | 30 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.088 | – | μC |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

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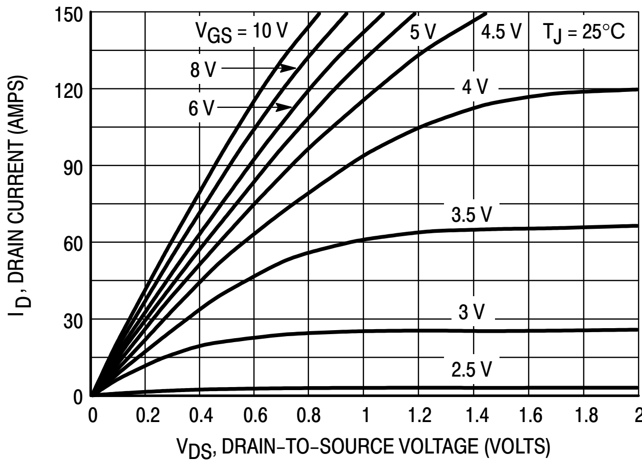


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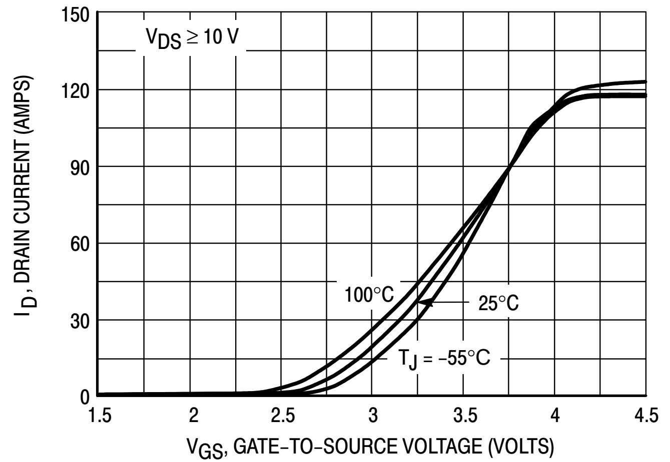


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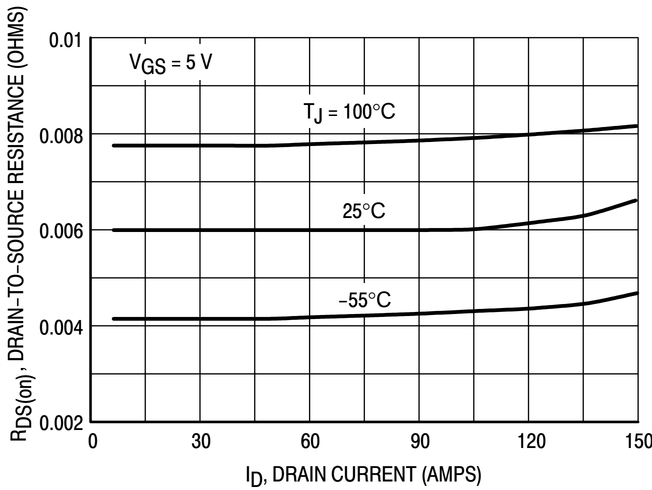
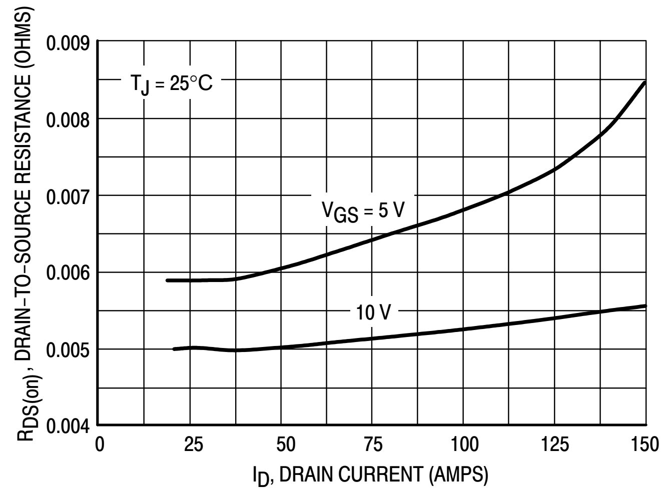



**Figure 3. On–Resistance versus Drain Current and Temperature**

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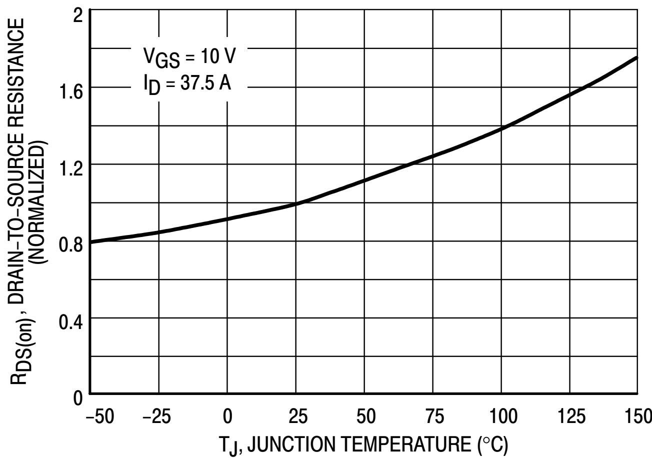


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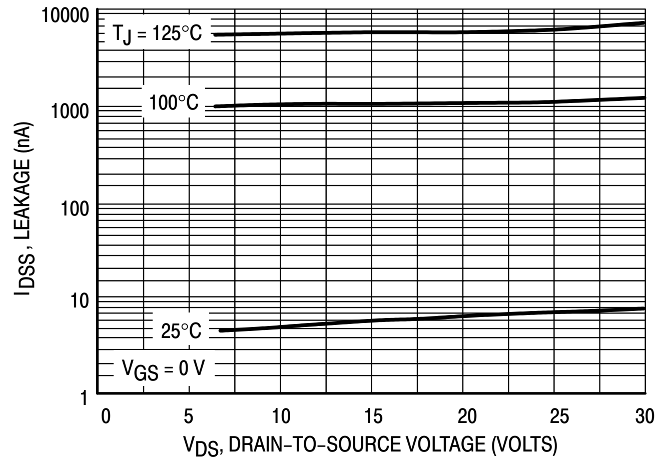


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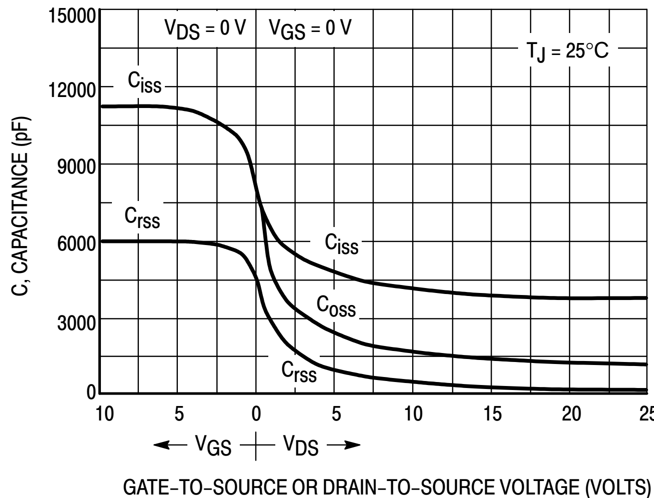


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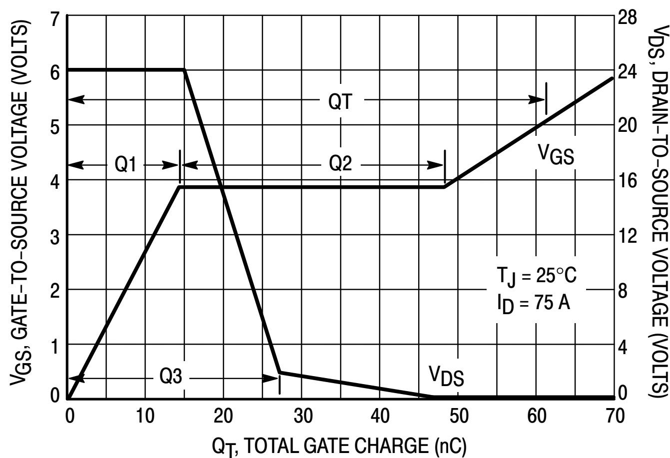


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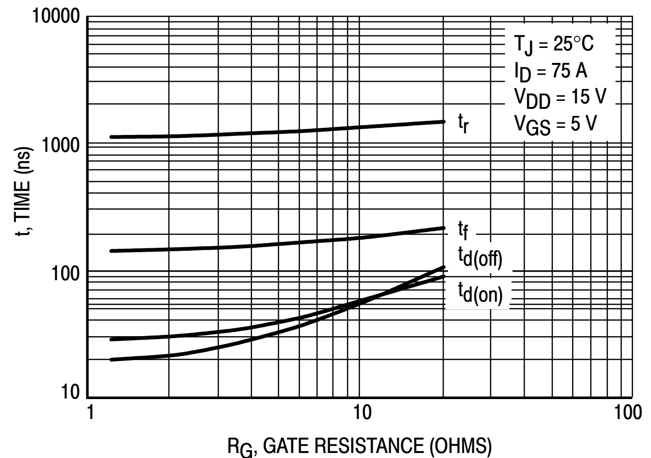



Figure 9. Resistive Switching Time Variation versus Gate Resistance

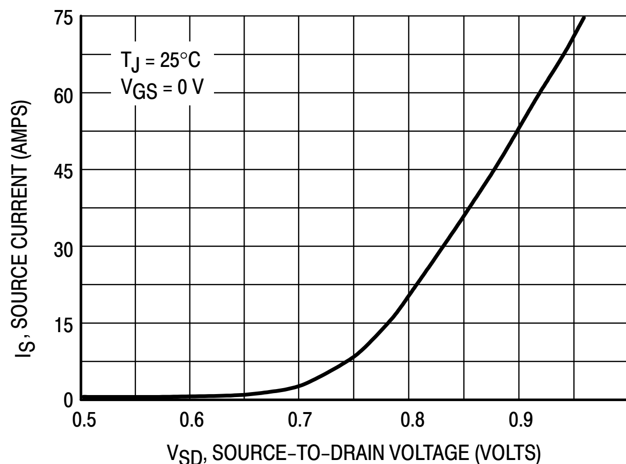
## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

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The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage (VDSS) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

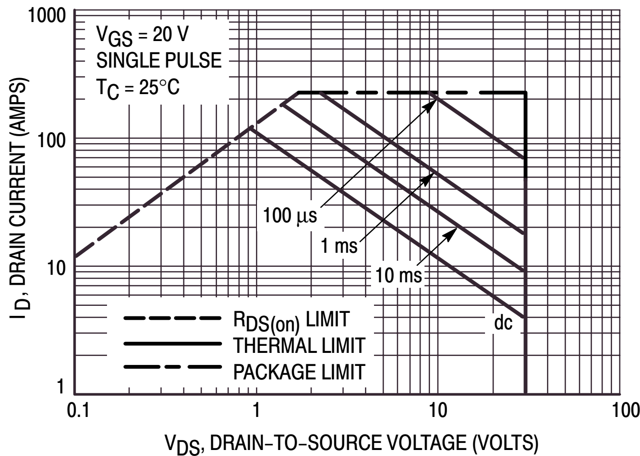


**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

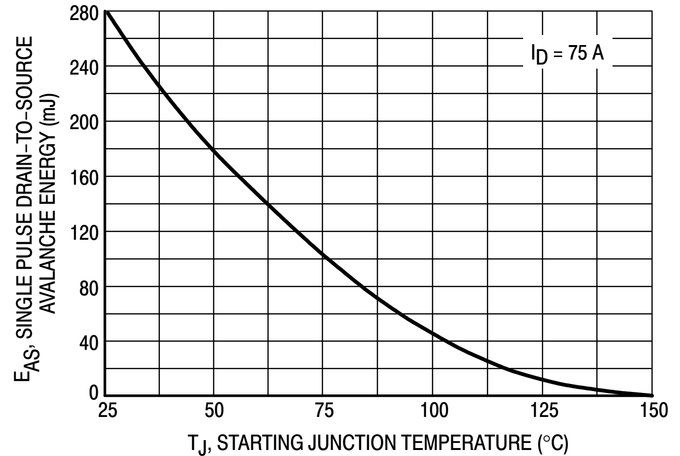


**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

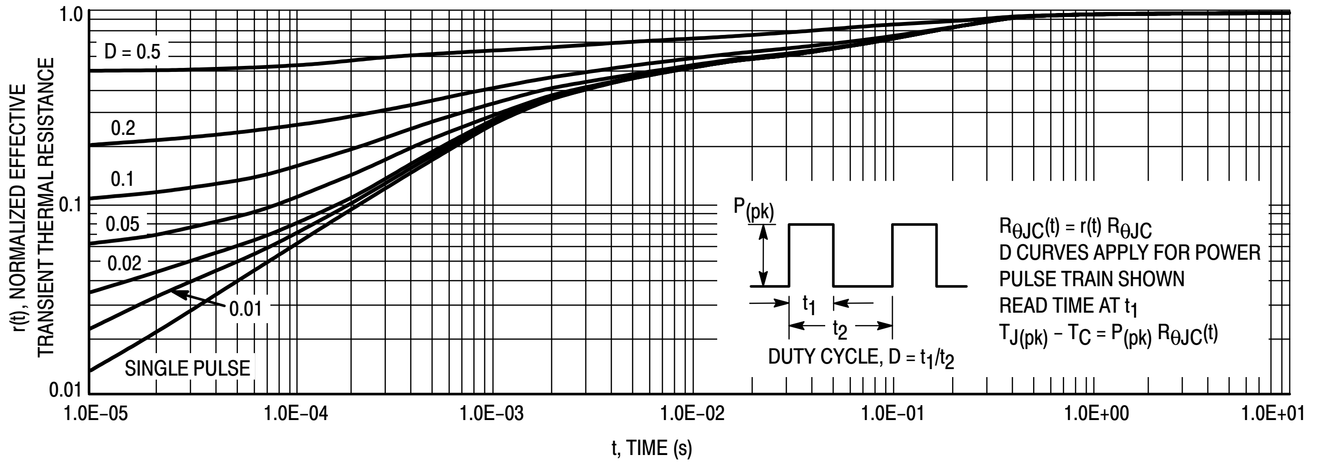


**Figure 13. Thermal Response**

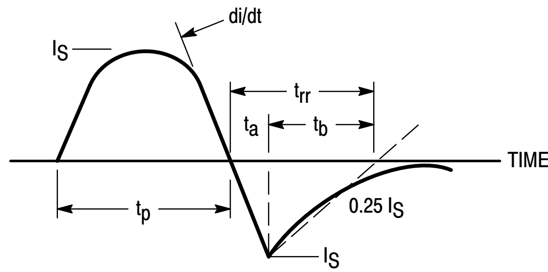


**Figure 14. Diode Reverse Recovery Waveform**

# MTP75N05HD

Preferred Device

# Power MOSFET 75 Amps, 50 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy–efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- SPICE Parameters Available
- Diode is Characterized for Use in Bridge Circuits
- Diode Exhibits High Speed, Yet Soft Recovery
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 50 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 50 | Vdc |
| Gate–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \le 10$ µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>65<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vpk, $I_L$ = 75 Apk, L = 0.177 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.00<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

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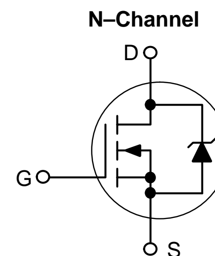
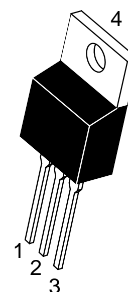
**75 AMPERES**
**50 VOLTS**
**$R_{DS(on)}$ = 9.5 mΩ**

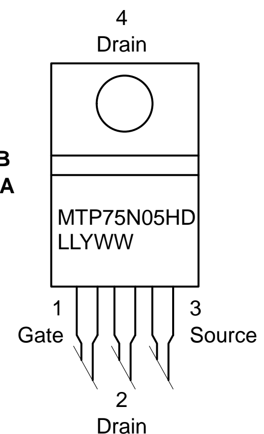
N–Channel




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB CASE 221A STYLE 5**




MTP75N05HD = Device Code
LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP75N05HD | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.)<br>($V_{GS}$ = 0 V, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | $V_{(BR)DSS}$ | <br>50<br>– | <br>–<br>54.9 | <br>–<br>– | <br>Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0)<br>($V_{DS}$ = 50 Vdc, $V_{GS}$ = 0, $T_J$ = 150°C) | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 1.5) (Note 3.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | $V_{GS(th)}$ | <br>2.0<br>– | <br>–<br>6.3 | <br>4.0<br>– | <br>Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 3.0) (Note 3.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc) | $R_{DS(on)}$ | <br>– | <br>7.0 | <br>9.5 | mW |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 75 Adc)<br>($I_D$ = 37.5 Adc, $T_J$ = 150°C) | $V_{DS(on)}$ | <br>–<br>– | <br>–<br>– | <br>0.86<br>0.64 | Vdc |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 20 Adc) | $g_{FS}$ | 15 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) ($C_{pk}$ ≥ 2.0)(2) | $C_{iss}$ | – | 2600 | 3900 | pF |
| Output Capacitance | $C_{oss}$ | – | 1000 | 1300 | |
| Transfer Capacitance | $C_{rss}$ | – | 230 | 300 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | |
| Turn–On Delay Time ($V_{DD}$ = 25 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 15 | 30 | ns |
| Rise Time | $t_r$ | – | 170 | 340 | |
| Turn–Off Delay Time | $t_{d(off)}$ | – | 70 | 140 | |
| Fall Time | $t_f$ | – | 100 | 200 | |
| Gate Charge ($V_{DS}$ = 40 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 71 | 100 | nC |
| | $Q_1$ | – | 13 | – | |
| | $Q_2$ | – | 33 | – | |
| | $Q_3$ | – | 26 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | |
| Forward On–Voltage<br>($I_S$ = 75 Adc, $V_{GS}$ = 0)<br>($I_S$ = 75 Adc, $V_{GS}$ = 0, $T_J$ = 150°C)<br>($C_{pk}$ ≥ 10)(2) | $V_{SD}$ | <br>–<br>– | <br>0.97<br>0.88 | <br>1.1<br>– | Vdc |
| Reverse Recovery Time ($I_S$ = 37.5 Adc, $V_{GS}$ = 0, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 57 | – | ns |
| | $t_a$ | – | 40 | – | |
| | $t_b$ | – | 17 | – | |
| Reverse Recovery Stored Charge | $Q_{RR}$ | – | 0.17 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | $L_D$ | <br>–<br>– | <br>3.5<br>4.5 | <br>–<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | $L_S$ | <br>– | <br>7.5 | <br>– | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS (Note 4.)

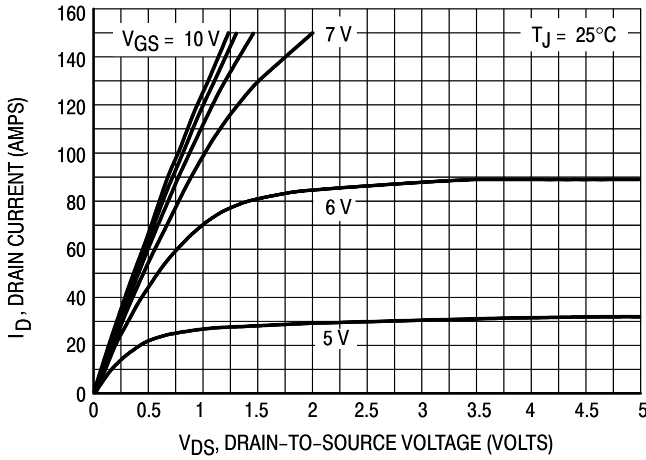



**Figure 1. On–Region Characteristics**

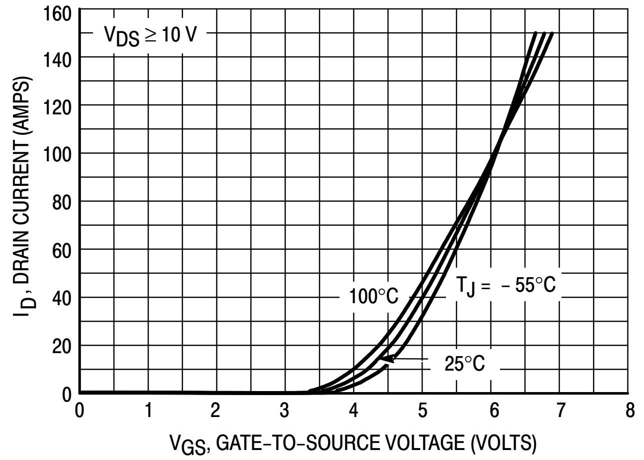



**Figure 2. Transfer Characteristics**

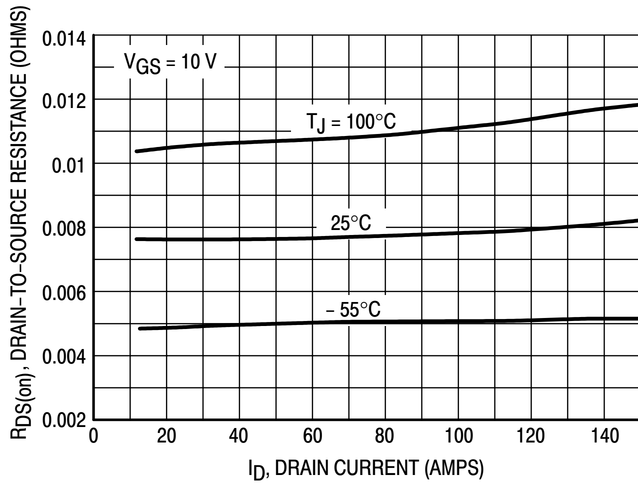



**Figure 3. On–Resistance versus Drain Current and Temperature**

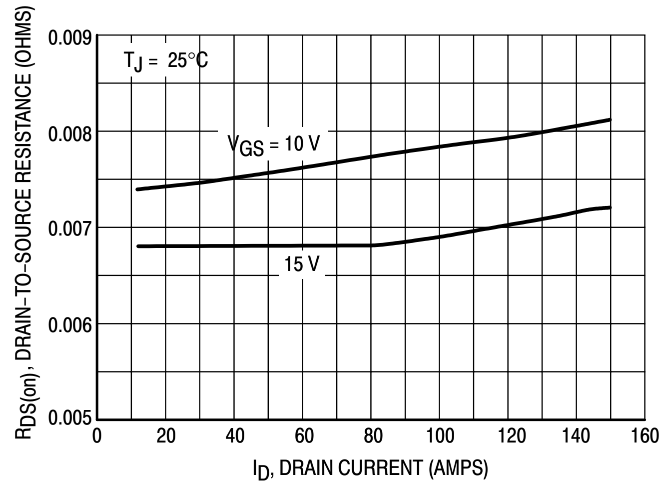



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

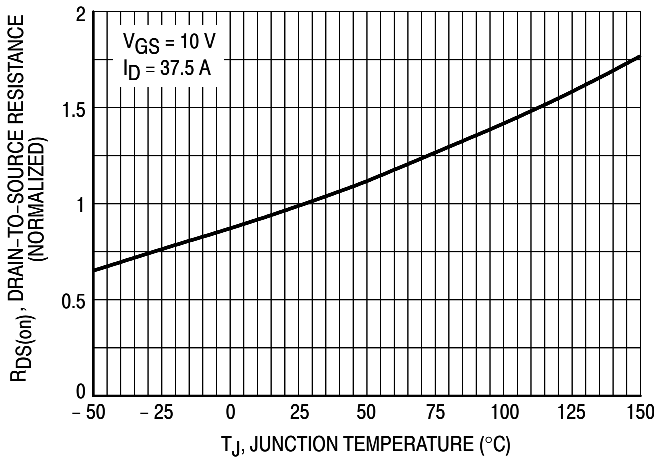



**Figure 5. On–Resistance Variation with Temperature**

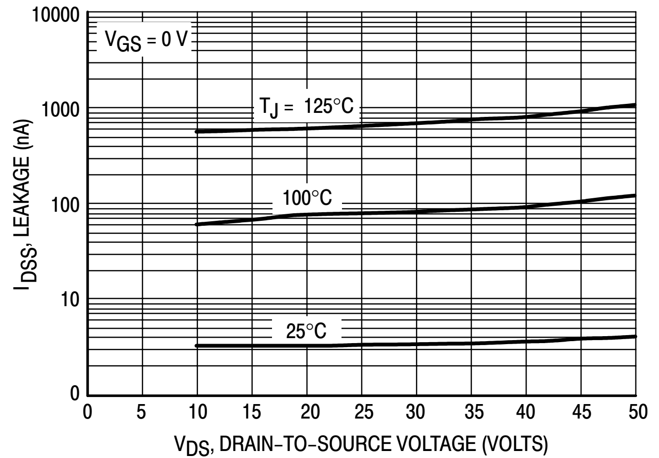



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

4. Pulse Tests: Pulse Width ≤ 250 μs, Duty Cycle ≤ 2%.

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals (Δt) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \, C_{iss} \, \text{In} \, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \, C_{iss} \, \text{In} \, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board–mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

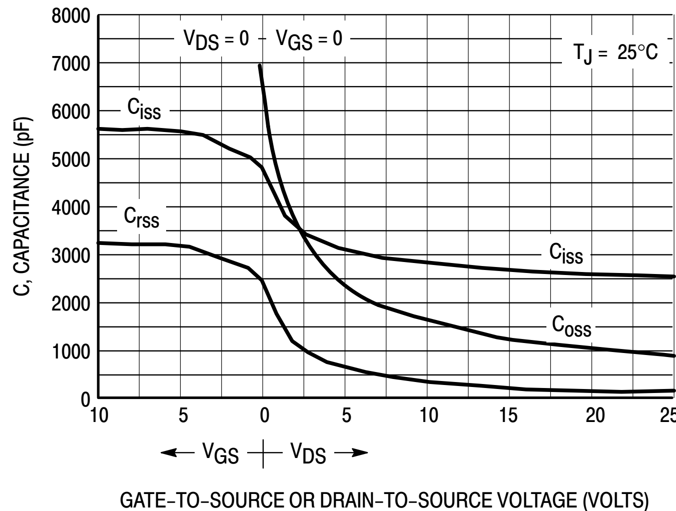



**Figure 7. Capacitance Variation**

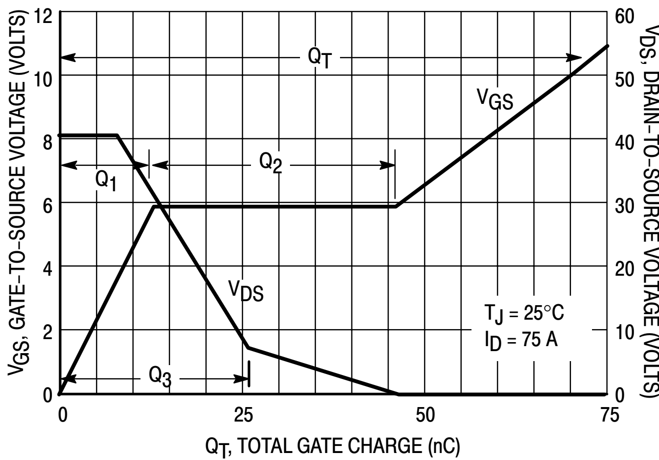



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

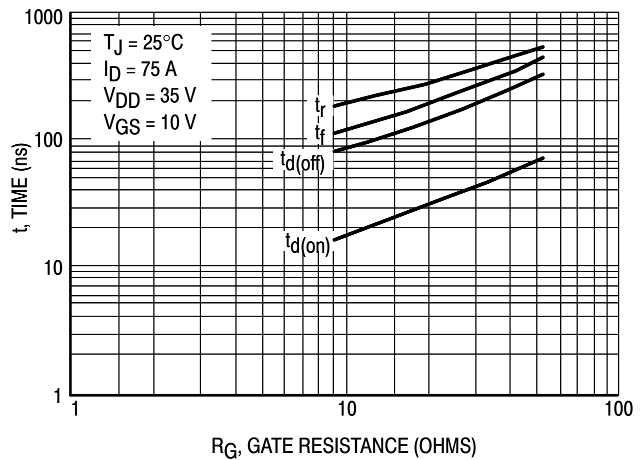



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

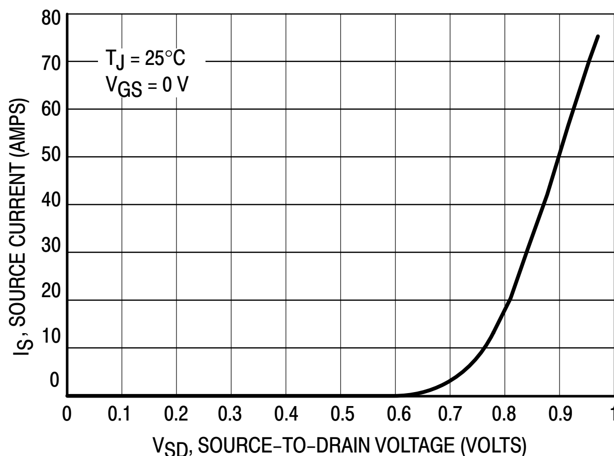



**Figure 10. Diode Forward Voltage versus Current**

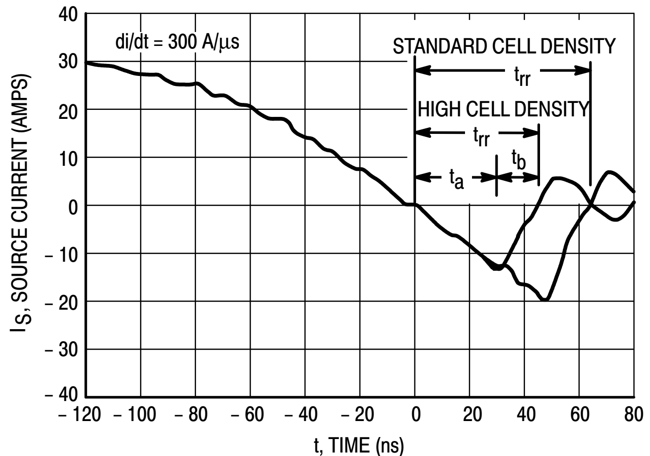



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$,$t_f$) does not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

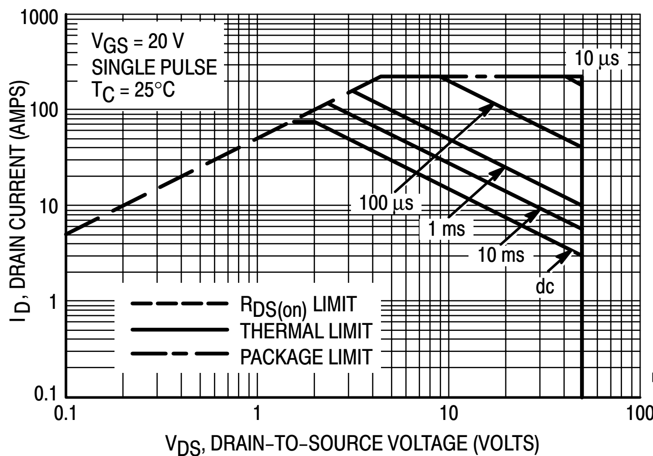



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

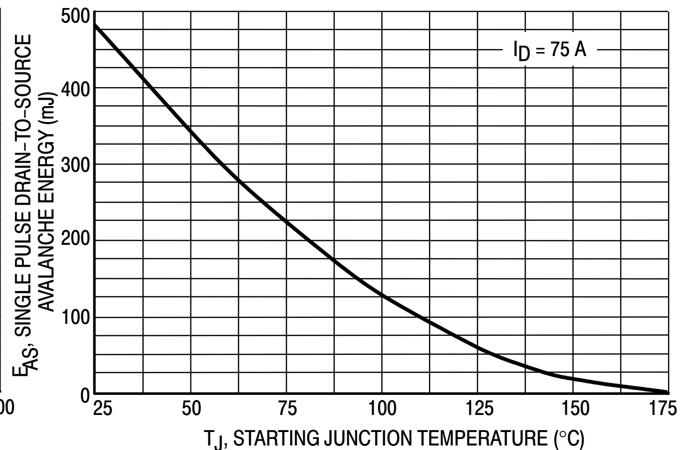



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

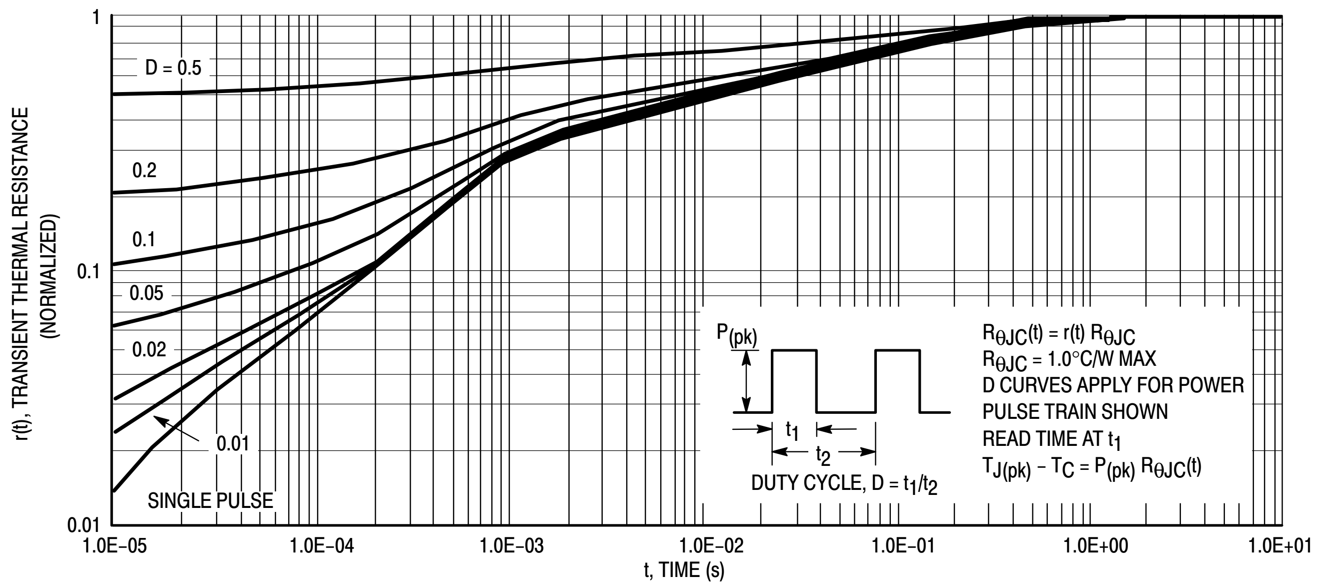



**Figure 14. Thermal Response**

# MTP75N06HD

**Preferred Device**

# Power MOSFET 75 Amps, 60 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low–voltage, high–speed switching applications in power supplies, converters and PWM motor controls, and inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched, and to offer additional safety margin against unexpected voltage transients.

- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Avalanche Energy Specified

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

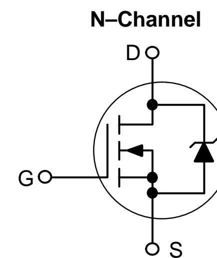
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage – Continuous<br>– Single Pulse | $V_{GS}$ | ± 20<br>± 30 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 75<br>50<br>225 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 150<br>1.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 75 Apk, L = 0.177 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 500 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>1.0<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**ON Semiconductor™**

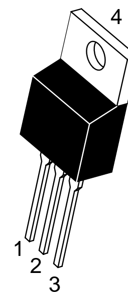
http://onsemi.com

**75 AMPERES**
**60 VOLTS**
**$R_{DS(on)}$ = 10 mΩ**

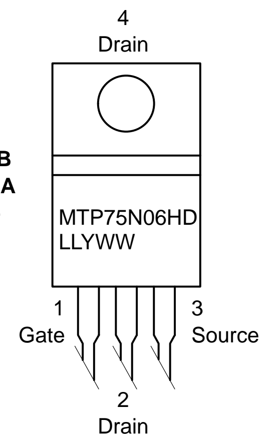
**N–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**TO–220AB**
**CASE 221A**
**STYLE 5**




| | |
|---|---|
| MTP75N06HD | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP75N06HD | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($C_{pk}$ ≥ 2.0) (Note 3.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 60 | 68 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 60.4 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 60 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0 V) | | $I_{GSS}$ | – | 5.0 | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($C_{pk}$ ≥ 5.0) (Note 3.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 8.38 | – | mV/°C |
| Static Drain–Source On–Resistance ($C_{pk}$ ≥ 2.0) (Note 3.) ($V_{GS}$ = 10 Vdc, $I_D$ = 37.5 Adc) | | $R_{DS(on)}$ | – | 8.3 | 10 | mΩ |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 75 Adc) | | $V_{DS(on)}$ | – | 0.7 | 0.9 | Vdc |
| ($I_D$ = 37.5 Adc, $T_J$ = 125°C) | | | – | 0.53 | 0.8 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 37.5 Adc) | | $g_{FS}$ | 15 | 32 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 2800 | 3920 | pF |
| Output Capacitance | | $C_{oss}$ | – | 928 | 1300 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 180 | 252 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 30 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 18 | 26 | ns |
| Rise Time | | $t_r$ | – | 218 | 306 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 67 | 94 | |
| Fall Time | | $t_f$ | – | 125 | 175 | |
| Gate Charge | ($V_{DS}$ = 48 Vdc, $I_D$ = 75 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 71 | 100 | nC |
| | | $Q_1$ | – | 16.3 | – | |
| | | $Q_2$ | – | 31 | – | |
| | | $Q_3$ | – | 29.4 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.97 | 1.1 | Vdc |
| | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.88 | – | |
| Reverse Recovery Time | ($I_S$ = 75 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 56 | – | ns |
| | | $t_a$ | – | 44 | – | |
| | | $t_b$ | – | 12 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.103 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from contact screw on tab to center of die) (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 3.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 7.5 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.
3. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

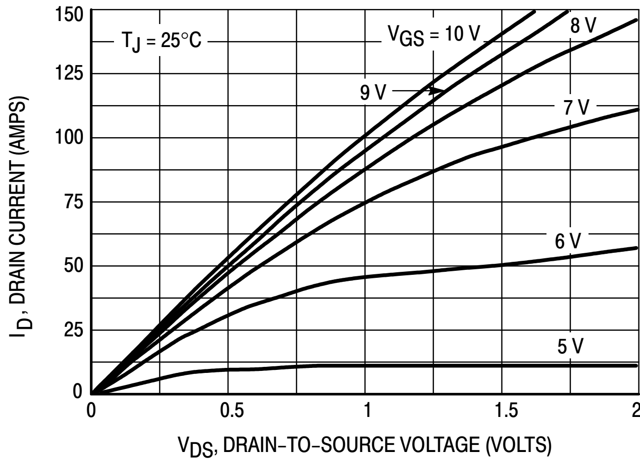



**Figure 1. On–Region Characteristics**

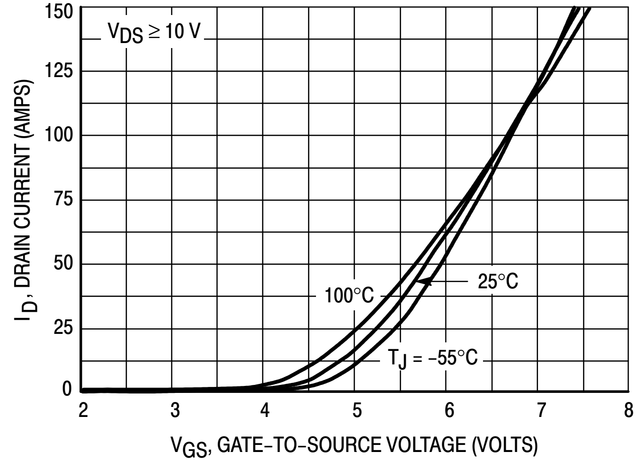



**Figure 2. Transfer Characteristics**

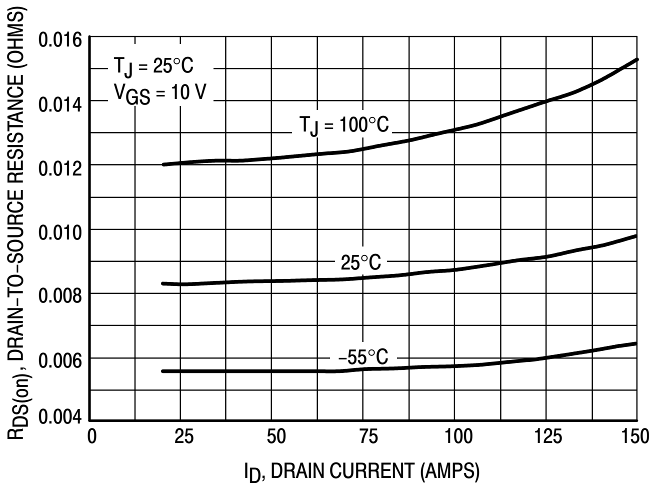



**Figure 3. On–Resistance versus Drain Current and Temperature**

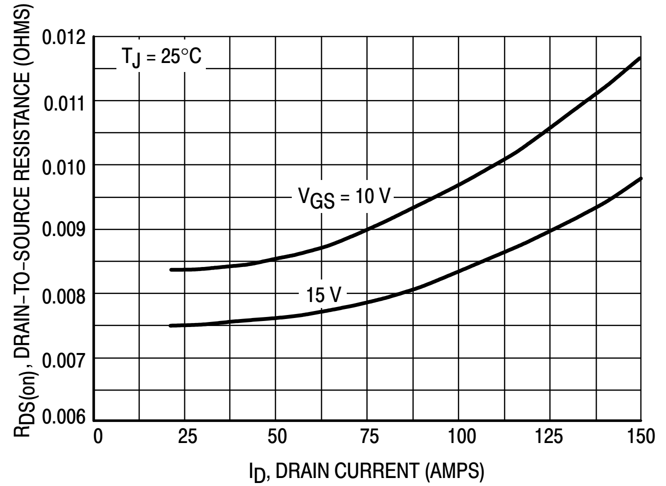



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

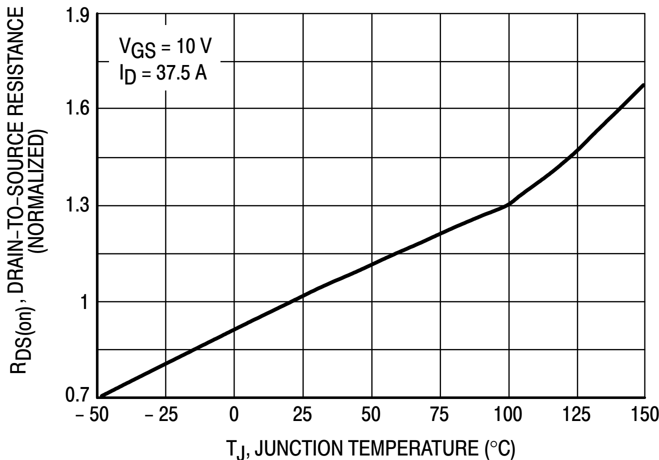



**Figure 5. On–Resistance Variation with Temperature**

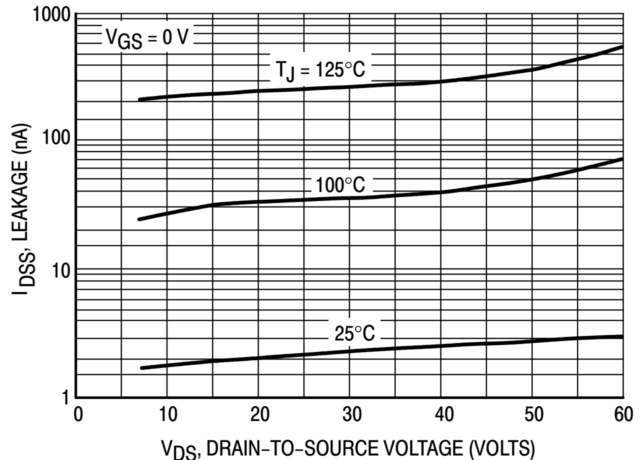



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$

$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$

$R_G$ = the gate drive resistance

and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$

$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

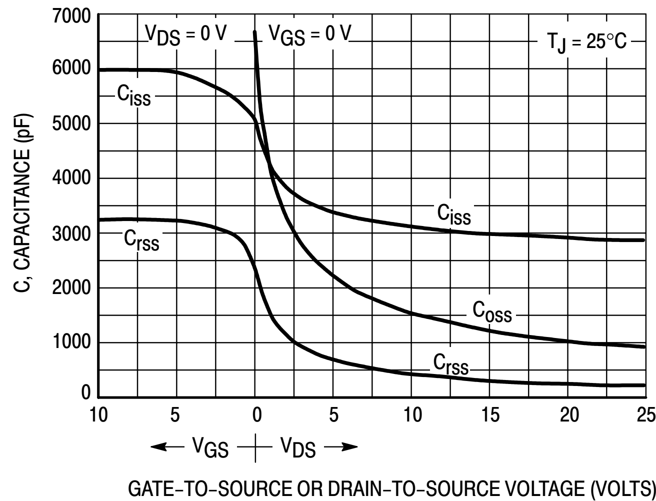



**Figure 7. Capacitance Variation**

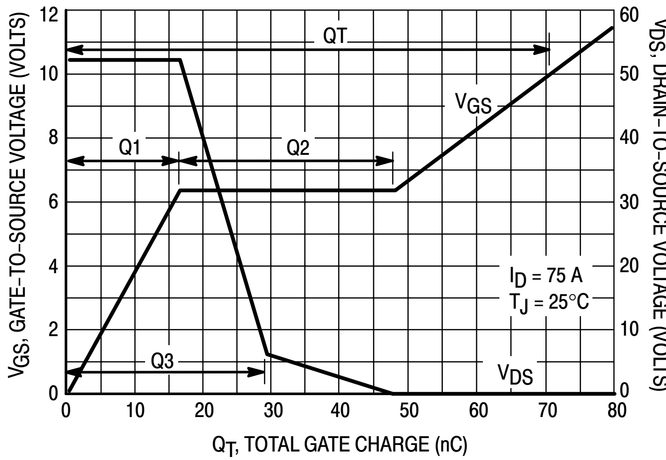



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

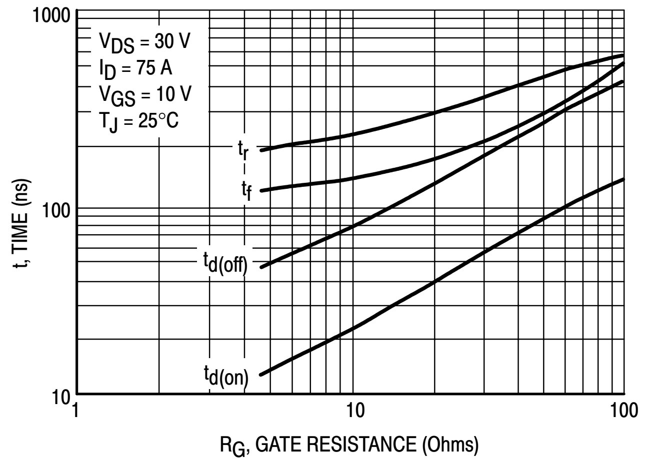



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 12. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

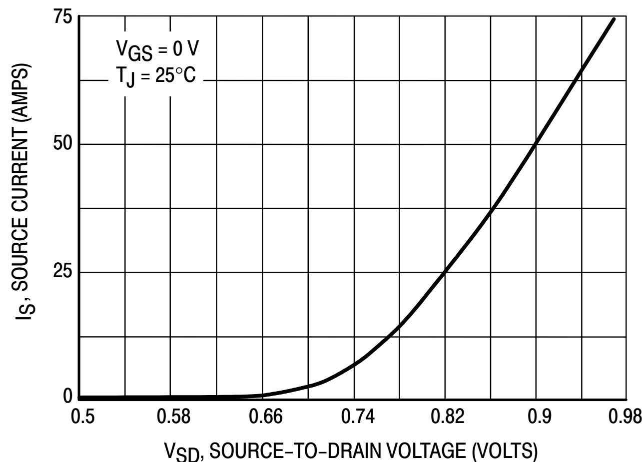



**Figure 10. Diode Forward Voltage versus Current**

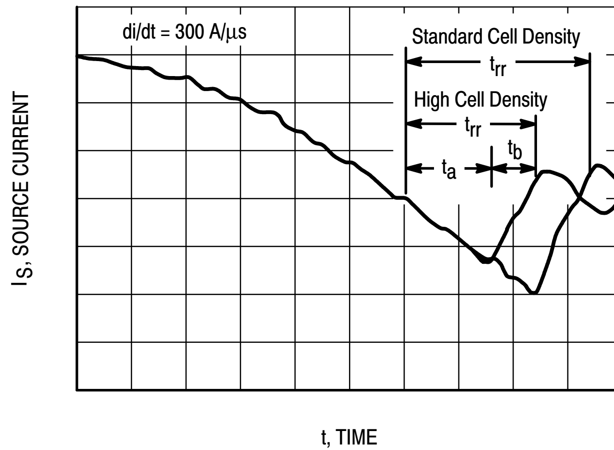



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance – General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} – T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

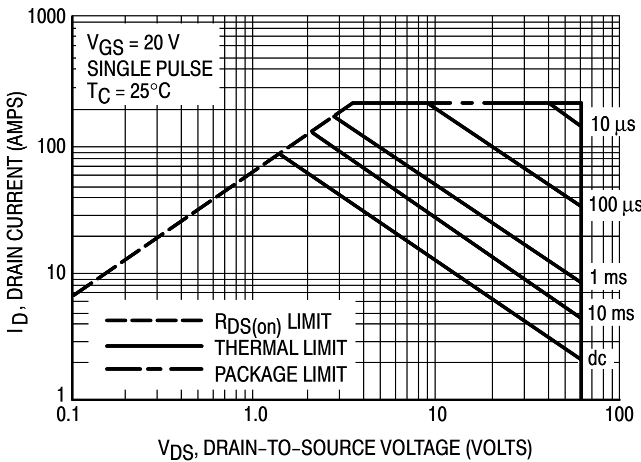



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

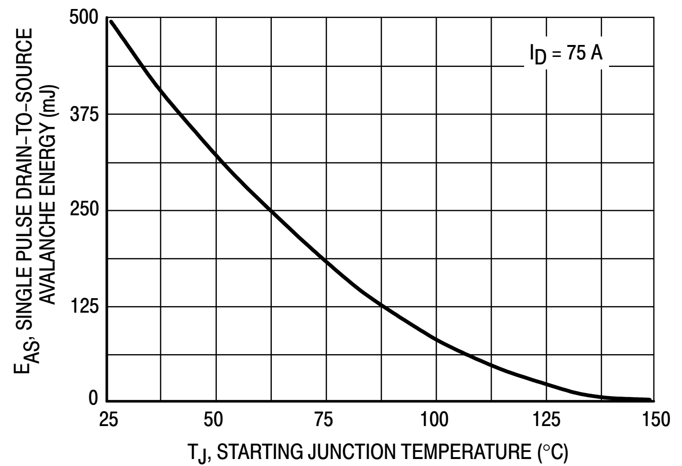



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

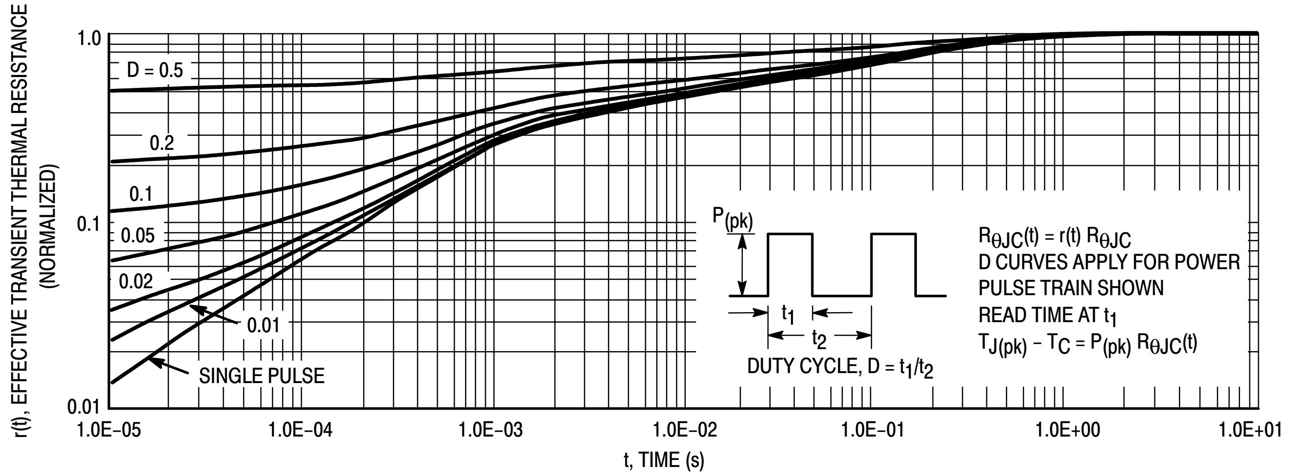



**Figure 14. Thermal Response**

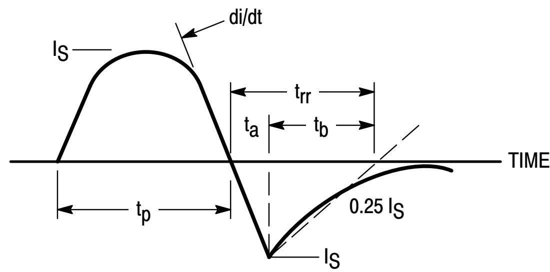



**Figure 15. Diode Reverse Recovery Waveform**

# MTP7N20E

**Preferred Device**

# Power MOSFET 7 Amps, 200 Volts

## N–Channel TO–220

This Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

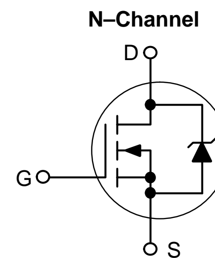
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | <br>$I_D$<br>$I_D$<br>$I_{DM}$ | <br>7.0<br>3.8<br>21 | <br>Adc<br><br>Apk |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 50<br>0.4 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 80 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 7.0 Adc, L = 10 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 74 | mJ |
| Thermal Resistance<br>– Junction to Case<br>– Junction to Ambient | <br>$R_{\theta JC}$<br>$R_{\theta JA}$ | <br>2.5<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

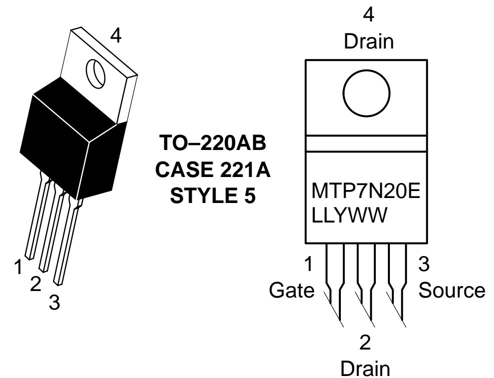
**ON Semiconductor™**

**http://onsemi.com**

**7 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 700 mΩ**




**MARKING DIAGRAM & PIN ASSIGNMENT**




| | |
|---|---|
| MTP7N20E | = Device Code |
| LL | = Location Code |
| Y | = Year |
| WW | = Work Week |

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTP7N20E | TO–220AB | 50 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 0.25 mAdc)<br>Temperature Coefficient (positive) | | $V_{(BR)DSS}$ | 200<br>– | –<br>689 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 10<br>100 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (negative) | | $V_{GS(th)}$ | 2.0<br>– | 3.1<br>7.1 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–to–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 3.5 Adc) | | $R_{DS(on)}$ | – | 0.46 | 0.7 | Ohm |
| Drain–to–Source On–Voltage<br>($V_{GS}$ = 10 Vdc, $I_D$ = 7.0 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.5 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | 3.4<br>– | 5.9<br>5.1 | Vdc |
| Forward Transconductance ($V_{DS}$ = 14 Vdc, $I_D$ = 3.5 Adc) | | $g_{FS}$ | 1.5 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 342 | 480 | pF |
| Output Capacitance | | $C_{oss}$ | – | 92 | 130 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 27 | 55 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 7.0 Adc, $V_{GS}$ = 10 Vdc, $R_g$ = 9.1 Ω) | $t_{d(on)}$ | – | 8.8 | 17.6 | ns |
| Rise Time | | $t_r$ | – | 29 | 58 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 22 | 44 | |
| Fall Time | | $t_f$ | – | 20 | 40.8 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 7.0 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 13.7 | 21 | nC |
| | | $Q_1$ | – | 3.3 | | |
| | | $Q_2$ | – | 6.6 | – | |
| | | $Q_3$ | – | 5.9 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc)<br>($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.02<br>0.9 | 1.2<br>– | Vdc |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 7.0 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 138 | – | ns |
| | | $t_a$ | – | 93 | – | |
| | | $t_b$ | – | 45 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.74 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from contact screw on tab to center of die)<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_d$ | –<br>– | 3.5<br>4.5 | –<br>– | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad.) | | $L_s$ | – | 7.5 | – | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

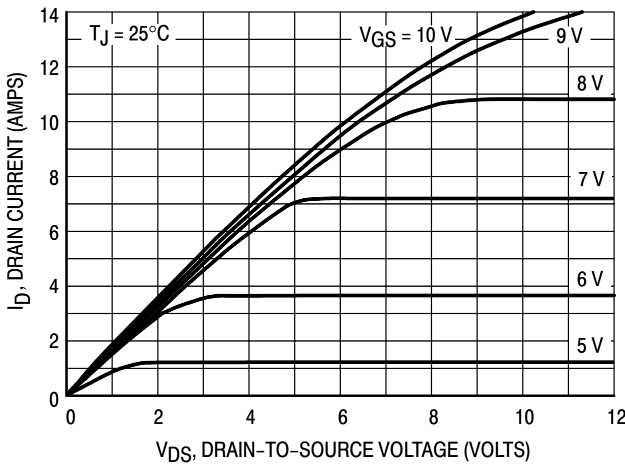


**Figure 1. On–Region Characteristics**

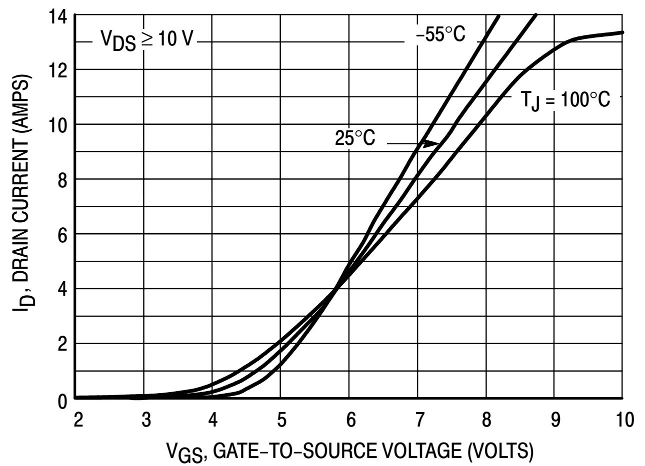


**Figure 2. Transfer Characteristics**

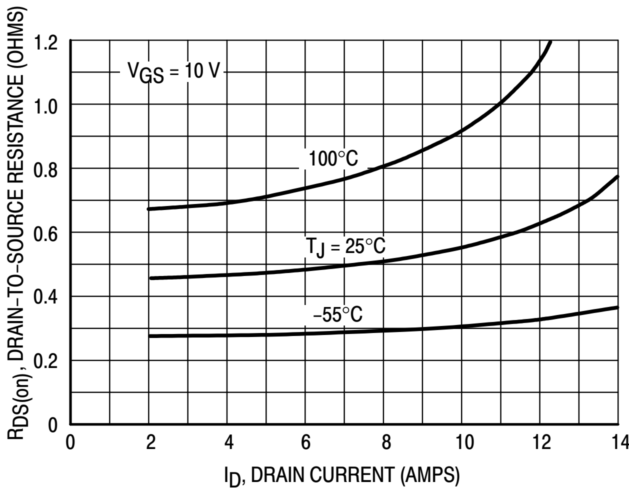


**Figure 3. On–Resistance versus Drain Current and Temperature**

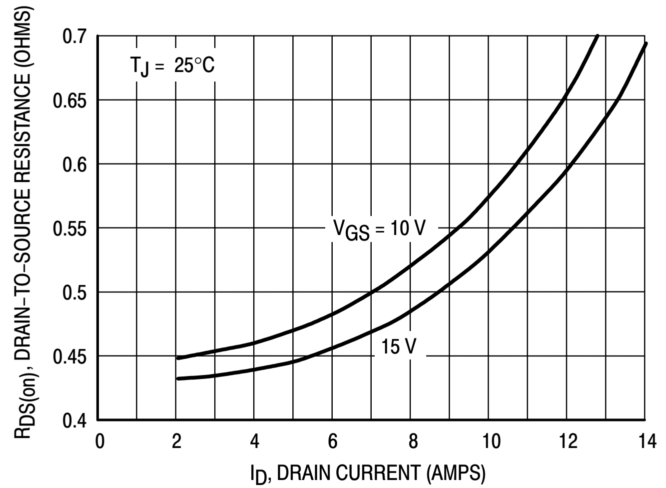


**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

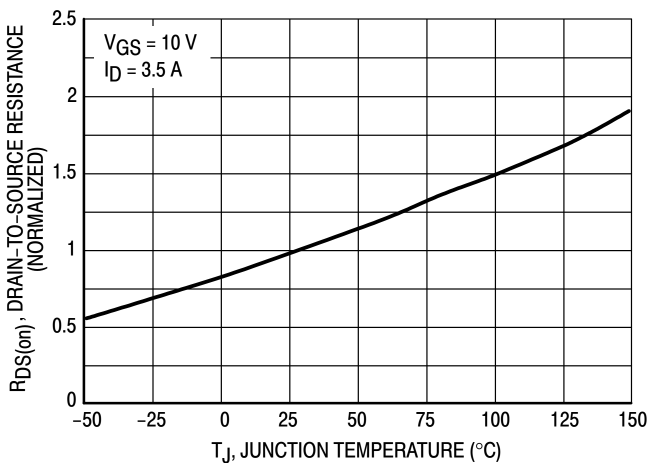


**Figure 5. On–Resistance Variation with Temperature**

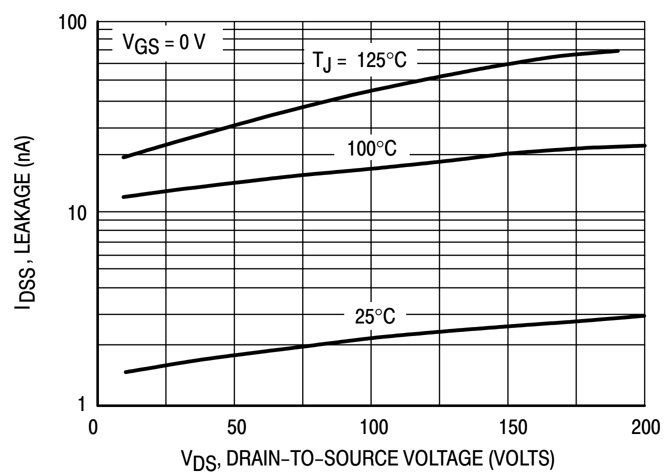


**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

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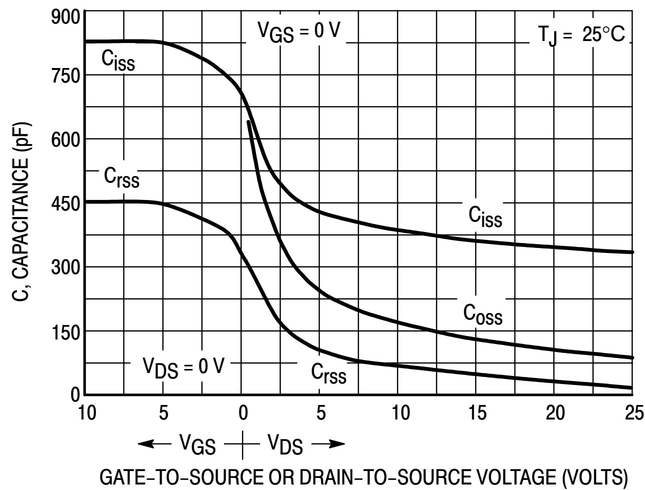



**Figure 7. Capacitance Variation**

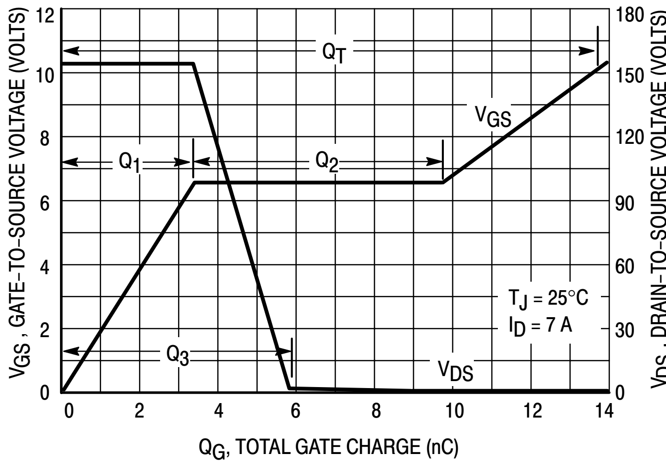



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

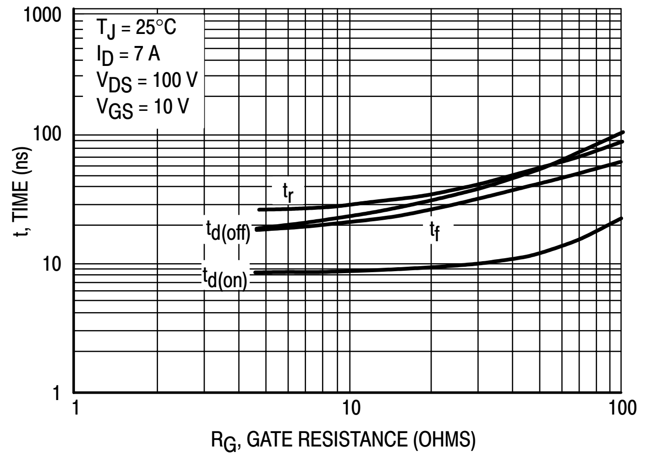



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

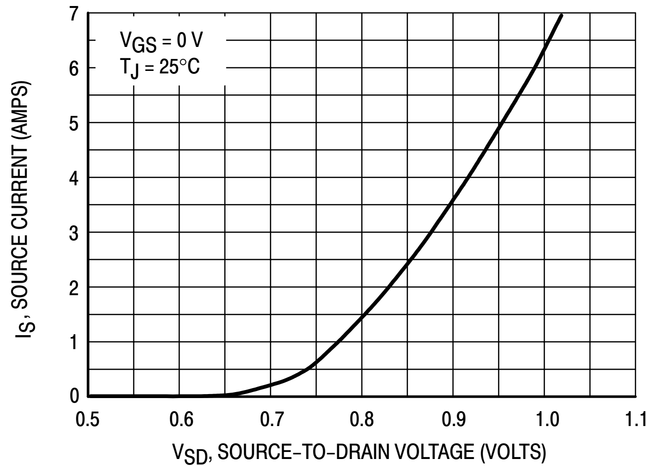



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

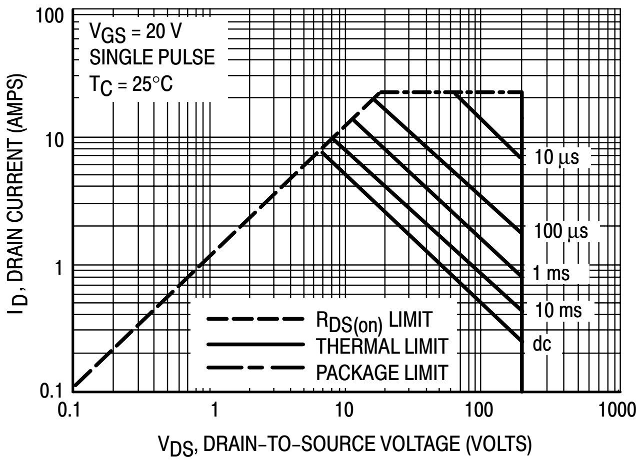



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

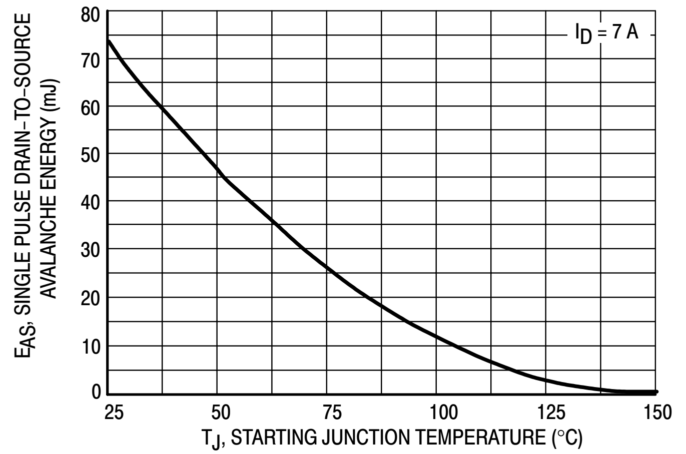



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

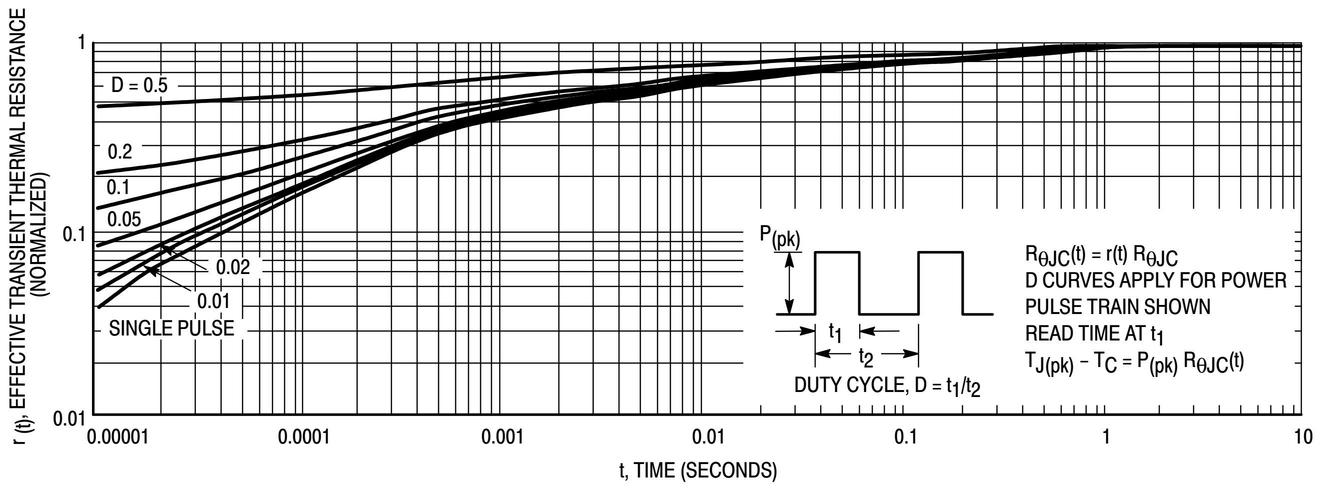



**Figure 13. Thermal Response**

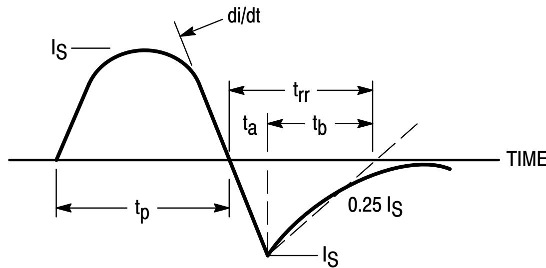



**Figure 14. Diode Reverse Recovery Waveform**

# MTSF1P02HD

Preferred Device

*Advance Information*

# Power MOSFET 1 Amp, 20 Volts

## P–Channel Micro8™

These Power MOSFET devices are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8 devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

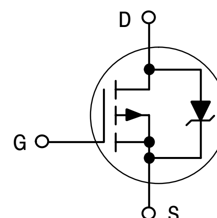
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

**ON Semiconductor™**

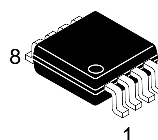
**http://onsemi.com**

**1 AMPERE**
**20 VOLTS**
**$R_{DS(on)}$ = 160 mΩ**

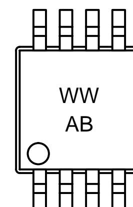
**P–Channel**




**MARKING DIAGRAM**

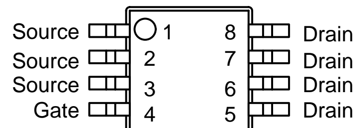



**Micro8**
**CASE 846A**
**STYLE 1**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTSF1P02HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

This document contains information on a new product. Specifications and information herein are subject to change without notice.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted) *

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | 20 | Vdc |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 20 | Vdc |
| Gate–to–Source Voltage – Continuous | $V_{GS}$ | ± 8.0 | Vdc |
| Drain Current – Continuous @ $T_A$ = 25°C (Note 2.)<br>– Continuous @ $T_A$ = 70°C (Note 2.)<br>– Pulsed Drain Current (Note 3.) | $I_D$<br>$I_D$<br>$I_{DM}$ | 1.8<br>1.6<br>14.4 | Adc<br><br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C (Note 1.)<br>Linear Derating Factor (Note 1.) | $P_D$ | 1.8<br>14.3 | Watts<br>mW/°C |
| Total Power Dissipation @ $T_A$ = 25°C (Note 2.)<br>Linear Derating Factor (Note 2.) | $P_D$ | 0.78<br>6.25 | Watts<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | – 55 to 150 | °C |

**THERMAL RESISTANCE**

| Rating | Symbol | Typ. | Max. | Unit |
|---|---|---|---|---|
| Thermal Resistance – Junction to Ambient, PCB Mount (Note 1.)<br>– Junction to Ambient, PCB Mount (Note 2.) | $R_{\theta JA}$<br>$R_{\theta JA}$ | 55<br>125 | 70<br>160 | °C/W |

*Negative signs for P–Channel device omitted for clarity.

1. When mounted on 1″ square FR–4 or G–10 board ($V_{GS}$ = 4.5 V, @ Steady State)
2. When mounted on minimum recommended FR–4 or G–10 board ($V_{GS}$ = 4.5 V, @ Steady State)
3. Repetitive rating; pulse width limited by maximum junction temperature.

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted) (Note 4.)

| Characteristic | Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 4. & 6.) ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 12.8 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 1.0 | μAdc |
| ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 10 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0 Vdc) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 5.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 6.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 0.6 | 0.8 | – | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 2.5 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Note 6.) ($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.8 Adc) | | $R_{DS(on)}$ | – | 120 | 160 | mΩ |
| ($V_{GS}$ = 2.7 Vdc, $I_D$ = 0.9 Adc) | | | – | 160 | 190 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 0.9 Adc) (Note 4.) | | $g_{FS}$ | 2.0 | 4.0 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 10 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 440 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 300 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 150 | – | |
| **SWITCHING CHARACTERISTICS** (Note 6.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 1.8 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6.0 Ω) (Note 4.) | $t_{d(on)}$ | – | 15 | – | ns |
| Rise Time | | $t_r$ | – | 35 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 55 | – | |
| Fall Time | | $t_f$ | – | 75 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 0.9 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6.0 Ω) (Note 4.) | $t_{d(on)}$ | – | 20 | – | |
| Rise Time | | $t_r$ | – | 93 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | – | |
| Fall Time | | $t_f$ | – | 75 | – | |
| Gate Charge | ($V_{DS}$ = 10 Vdc, $I_D$ = 1.8 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 11 | 22 | nC |
| | | $Q_1$ | – | 0.7 | – | |
| | | $Q_2$ | – | 5.5 | – | |
| | | $Q_3$ | – | 3.8 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 1.8 Adc, $V_{GS}$ = 0 Vdc) (Note 4.) | $V_{SD}$ | – | 1.24 | 2.0 | Vdc |
| | ($I_S$ = 1.8 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.9 | – | |
| Reverse Recovery Time | ($I_S$ = 1.8 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 4.) | $t_{rr}$ | – | 120 | – | ns |
| | | $t_a$ | – | 33 | – | |
| | | $t_b$ | – | 87 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 0.223 | – | μC |

4. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
5. Switching characteristics are independent of operating junction temperature.
6. Reflects typical values. $C_{pk} = \left| \dfrac{\text{Max limit – Typ}}{3 \text{ x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

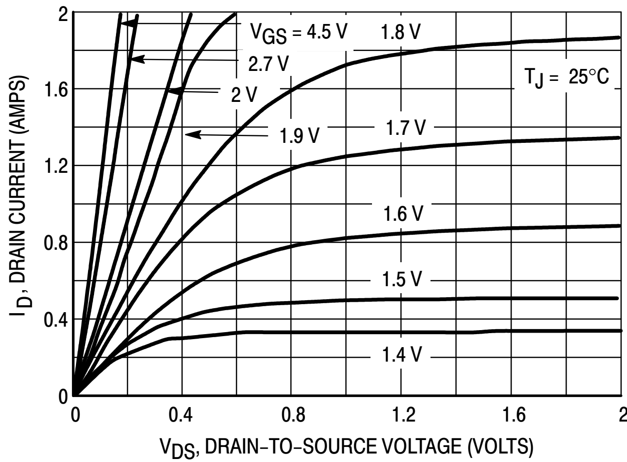



**Figure 1. On–Region Characteristics**

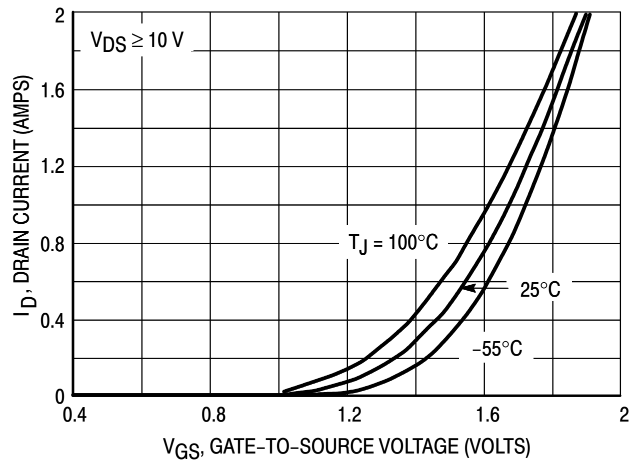



**Figure 2. Transfer Characteristics**

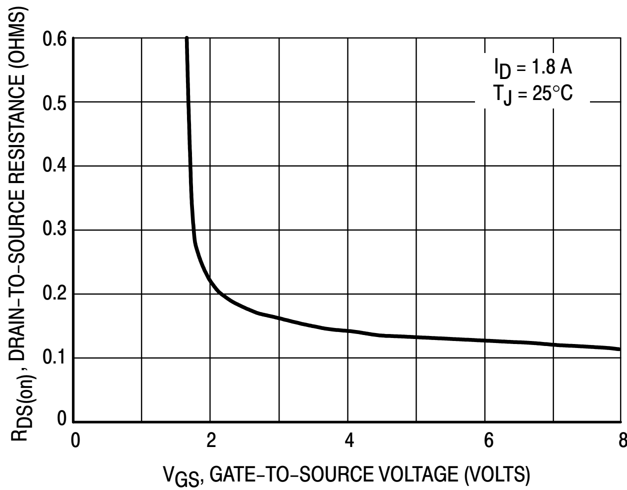



**Figure 3. On–Resistance versus Gate–To–Source Voltage**

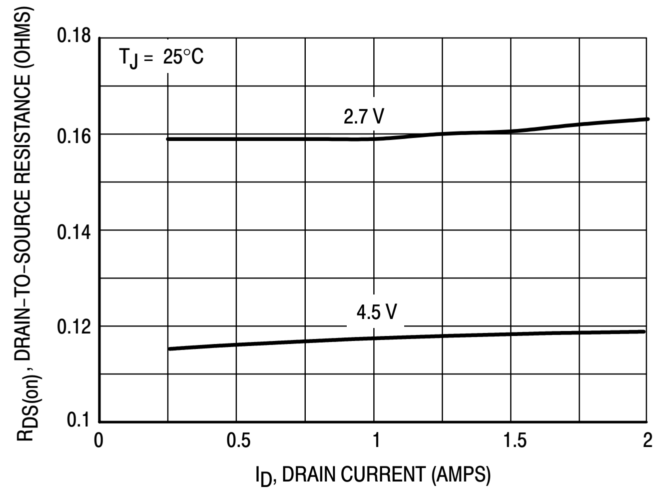
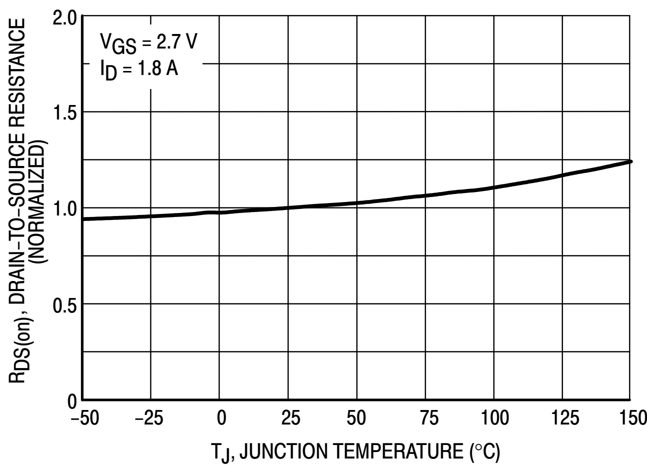



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

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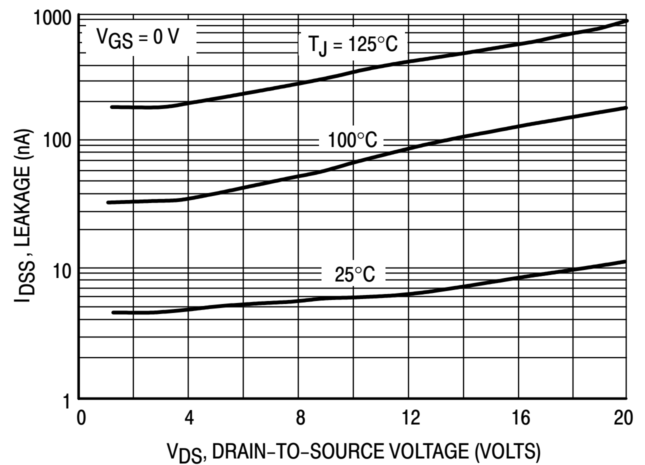


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$t_f = Q_2 \times R_G/V_{GSP}$

where

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$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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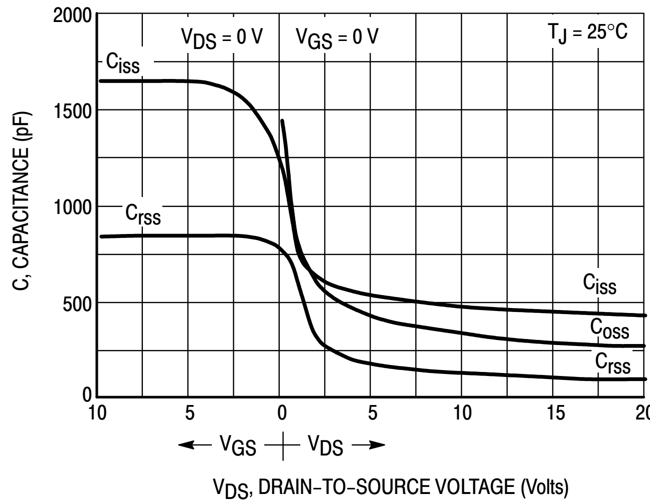



**Figure 7. Capacitance Variation**

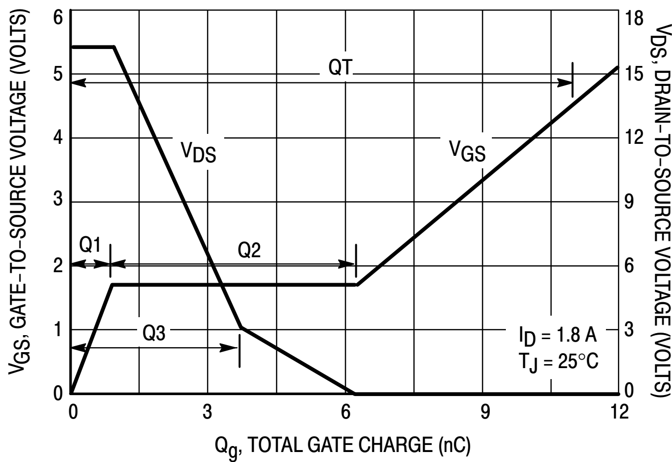



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

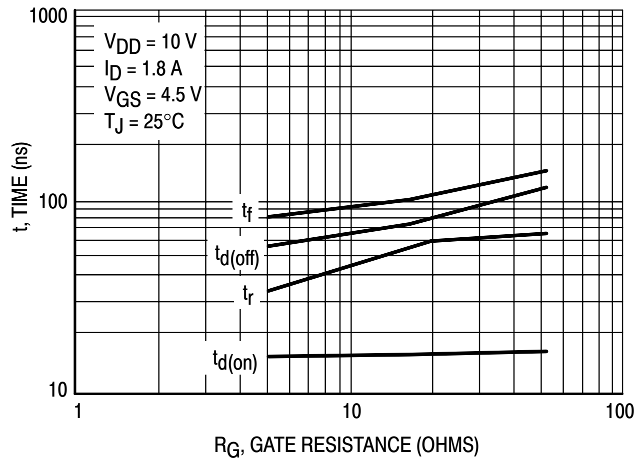



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 11. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

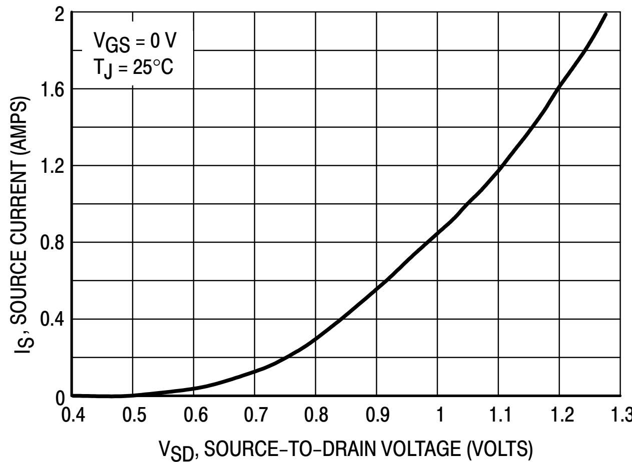



**Figure 10. Diode Forward Voltage versus Current**

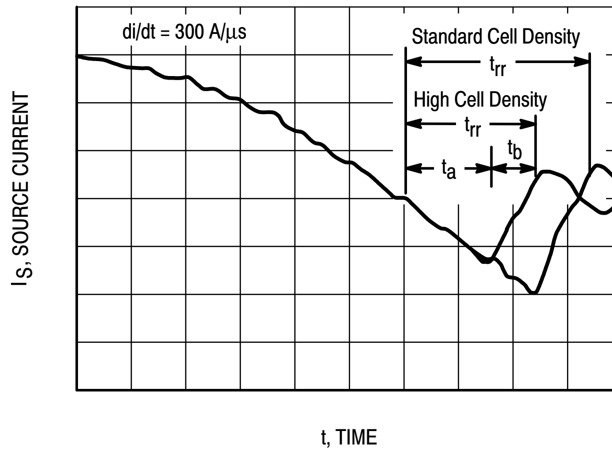



**Figure 11. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 12) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 13). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

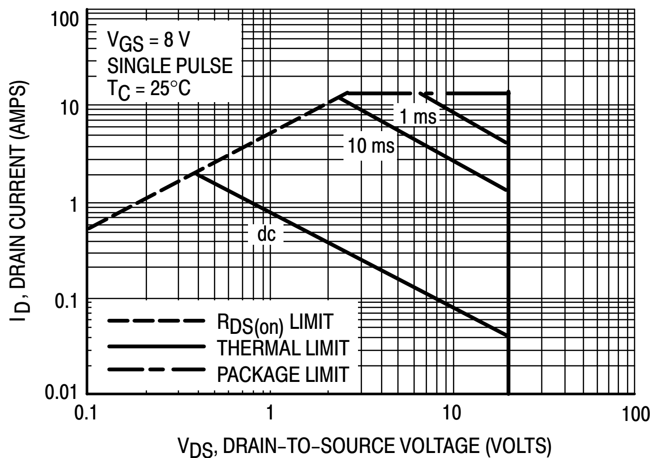



**Figure 12. Maximum Rated Forward Biased Safe Operating Area**

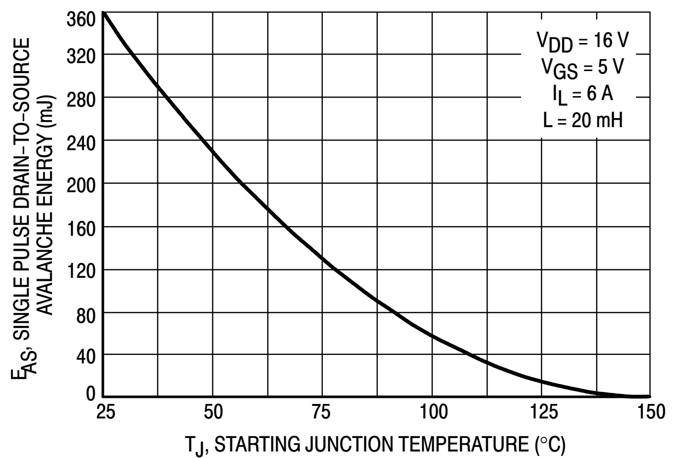



**Figure 13. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

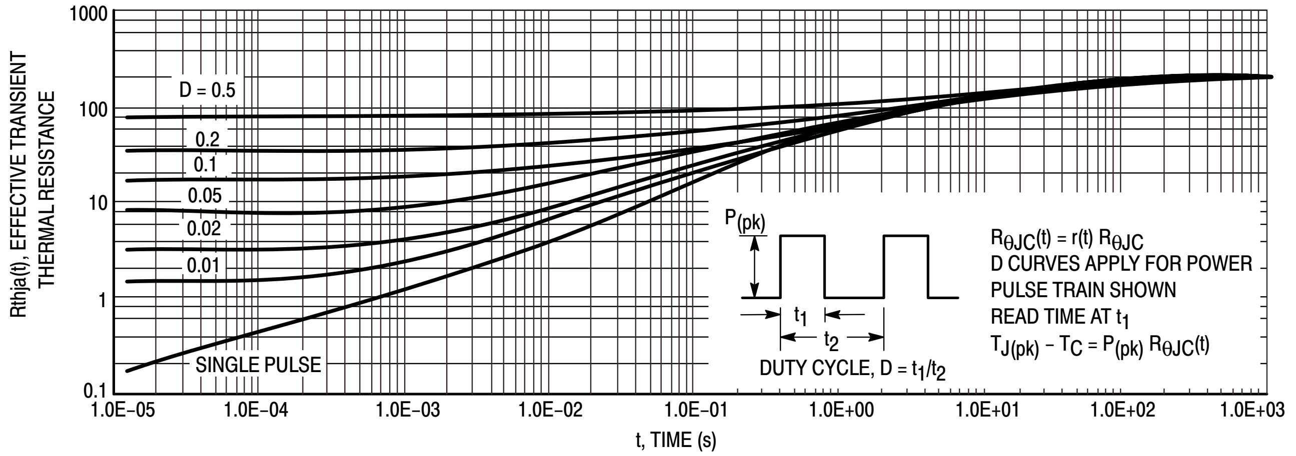



**Figure 14. Thermal Response**

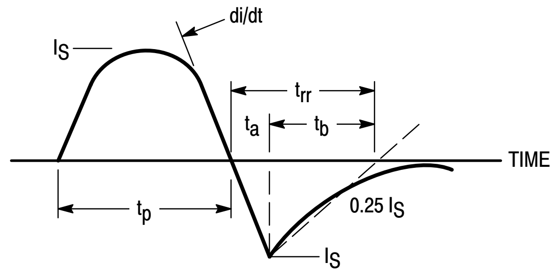
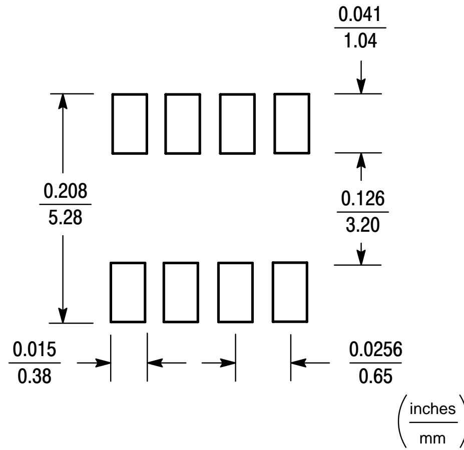



**Figure 15. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 1.8 Watts.

$$P_D = \frac{150°C - 25°C}{70°C/W} = 1.8 \text{ Watts}$$

The 70°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 1.8 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating "profile" for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 16 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

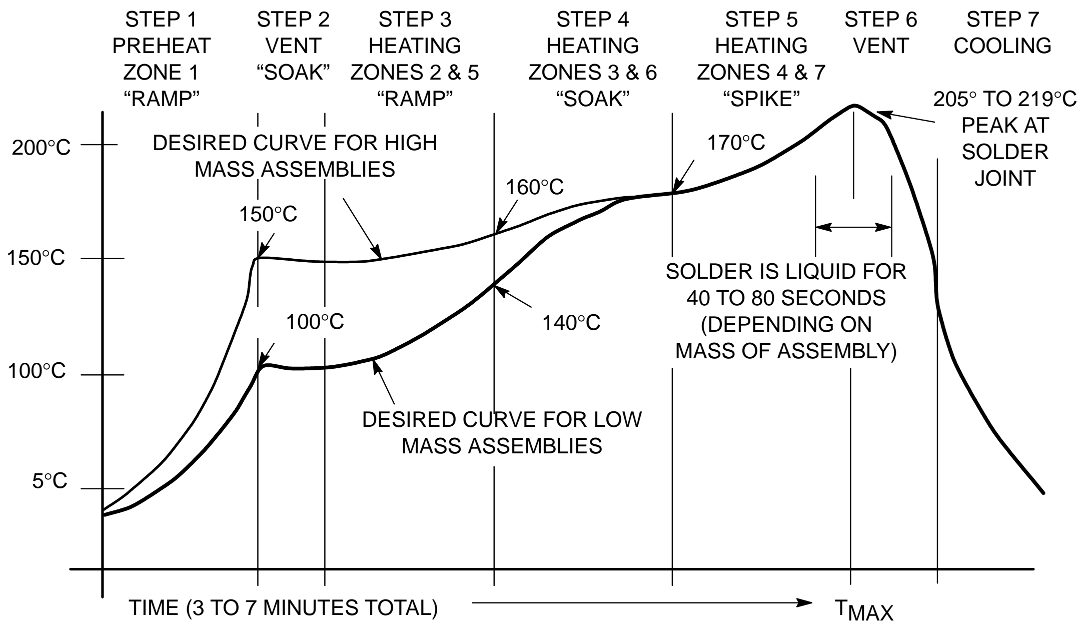
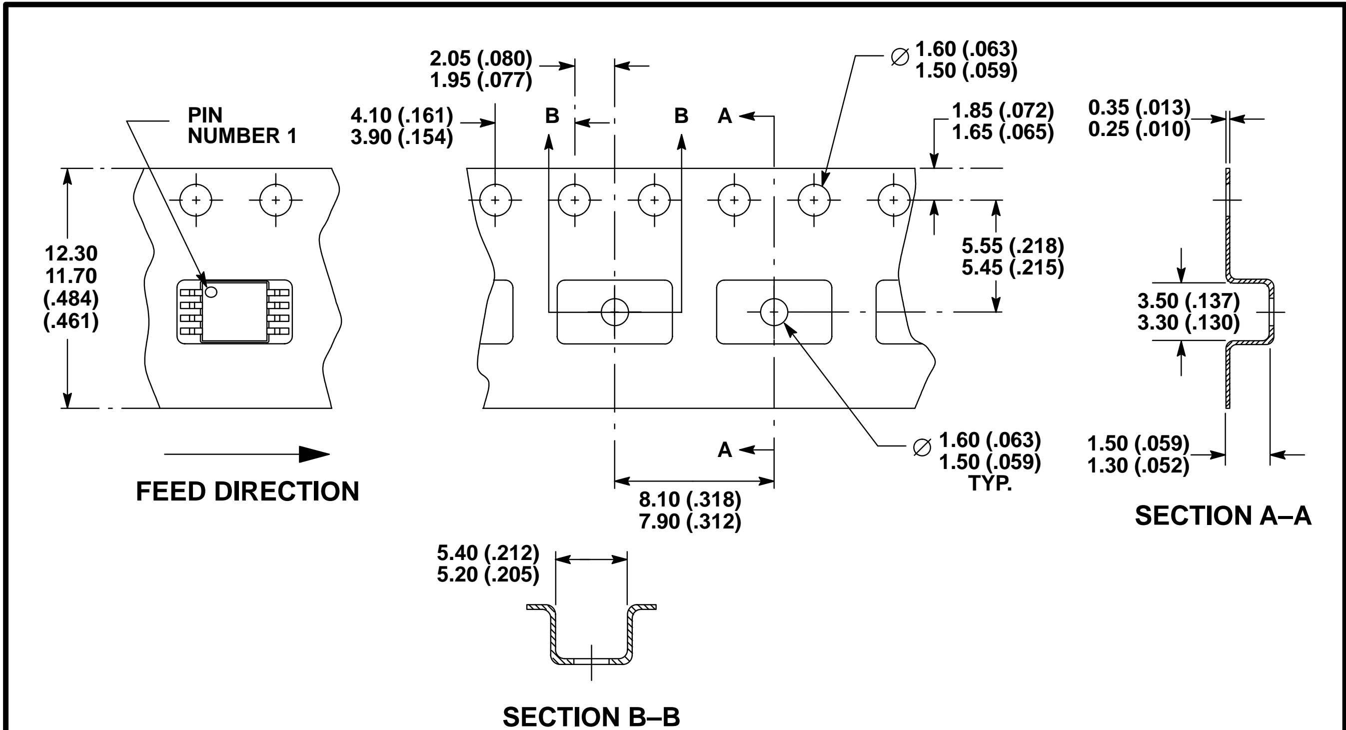


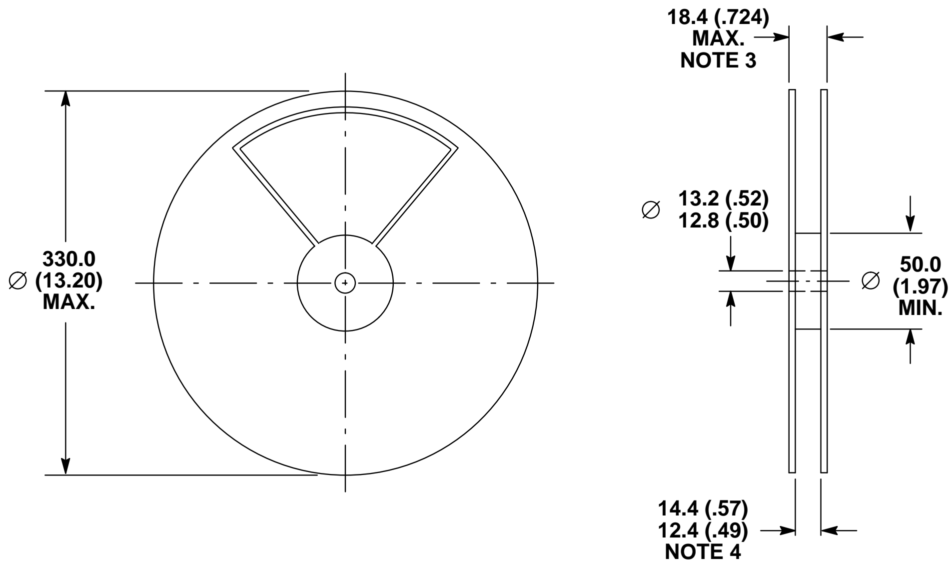

**Figure 16. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro8**
Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# MTSF3N02HD

**Preferred Device**

# Power MOSFET 3 Amps, 20 Volts

## N–Channel Micro8™

These Power MOSFET devices are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8 devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

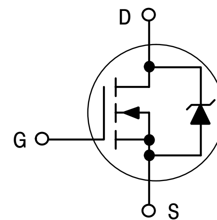
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Extremely Low Profile (<1.1mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

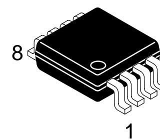
**ON Semiconductor™**

**http://onsemi.com**

**3 AMPERES**
**20 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

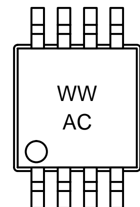
**N–Channel**



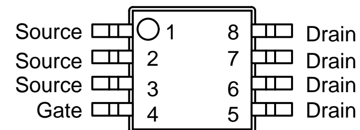

**Micro8**
**CASE 846A**
**STYLE 1**

**MARKING DIAGRAM**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTSF3N02HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.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November, 2000 – Rev. 5

Publication Order Number:
MTSF3N02HD/D

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Max | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | | $V_{DSS}$ | 20 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | | $V_{DGR}$ | 20 | V |
| Gate–to–Source Voltage – Continuous | | $V_{GS}$ | ± 8.0 | V |
| 1″ SQ.<br>FR–4 or G–10 PCB<br>Figure 1 below<br><br><br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 70<br>1.79<br>14.29<br>6.1<br>4.9<br>49 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Minimum<br>FR–4 or G–10 PCB<br>Figure 2 below<br><br><br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 160<br>0.78<br>6.25<br>4.0<br>3.2<br>32 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Operating and Storage Temperature Range | | $T_J$, $T_{stg}$ | – 55 to 150 | °C |

1. Repetitive rating; pulse width limited by maximum junction temperature.

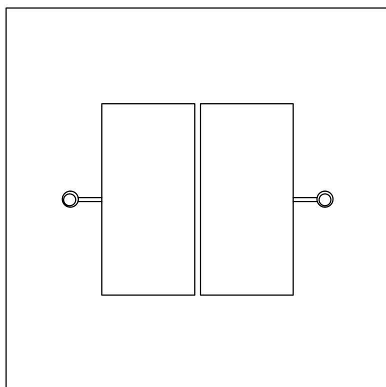


**Figure 1. 1″ Square FR–4 or G–10 PCB**

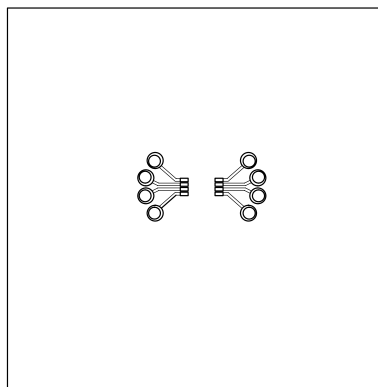


**Figure 2. Minimum FR–4 or G–10 PCB**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Test Conditions | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2. & 4.) | ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | $V_{(BR)DSS}$ | 20 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 16 | – | mV/°C |
| Zero Gate Voltage Drain Current | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc) | $I_{DSS}$ | – | – | 1.0 | μAdc |
| | ($V_{DS}$ = 16 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | – | 25 | |
| Gate–Body Leakage Current | ($V_{GS}$ = ± 8.0 Vdc, $V_{DS}$ = 0 Vdc) | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.) | ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | $V_{GS(th)}$ | 0.7 | 0.98 | 1.1 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 2.65 | – | mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.) | ($V_{GS}$ = 4.5 Vdc, $I_D$ = 3.8 Adc) | $R_{DS(on)}$ | – | 30 | 40 | mΩ |
| | ($V_{GS}$ = 2.7 Vdc, $I_D$ = 1.9 Adc) | | – | 40 | 50 | |
| Forward Transconductance (Note 2.) | ($V_{DS}$ = 10 Vdc, $I_D$ = 1.9 Adc) | $g_{FS}$ | 4.0 | 7.5 | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 475 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 255 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 110 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 10 Vdc, $I_D$ = 3.8 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 9.5 | – | ns |
| Rise Time | | $t_r$ | – | 45 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 50 | – | |
| Fall Time | | $t_f$ | – | 62 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 10 Vdc, $I_D$ = 1.9 Adc, $V_{GS}$ = 2.7 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 19 | – | ns |
| Rise Time | | $t_r$ | – | 130 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 38 | – | |
| Fall Time | | $t_f$ | – | 47 | – | |
| Gate Charge | ($V_{DS}$ = 16 Vdc, $I_D$ = 3.8 Adc, $V_{GS}$ = 4.5 Vdc) | $Q_T$ | – | 12 | 17 | nC |
| | | $Q_1$ | – | 1.0 | – | |
| | | $Q_2$ | – | 5.0 | – | |
| | | $Q_3$ | – | 3.5 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 3.8 Adc, $V_{GS}$ = 0 Vdc) (Note 2.) | $V_{SD}$ | – | 0.83 | 1.0 | Vdc |
| | ($I_S$ = 3.8 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.68 | – | |
| Reverse Recovery Time | ($I_S$ = 3.8 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 46 | – | ns |
| | | $t_a$ | – | 23 | – | |
| | | $t_b$ | – | 23 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.05 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit – Typ}}{\text{3 x SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

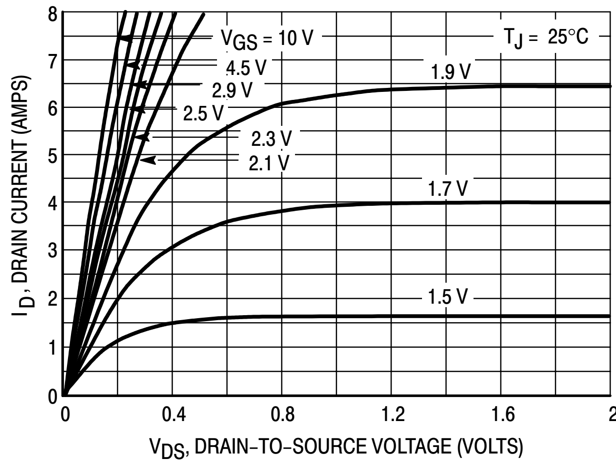



**Figure 3. On–Region Characteristics**

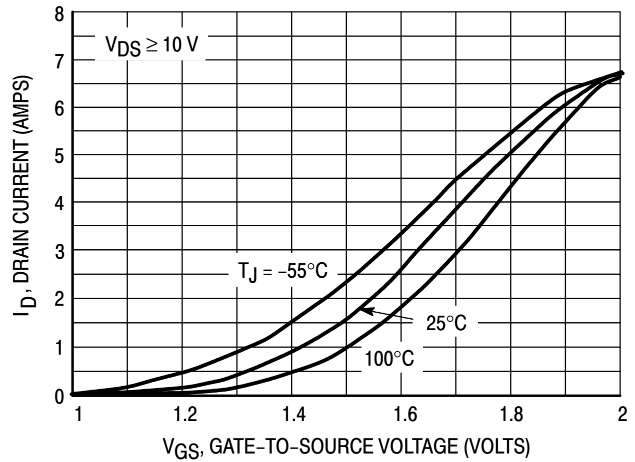



**Figure 4. Transfer Characteristics**

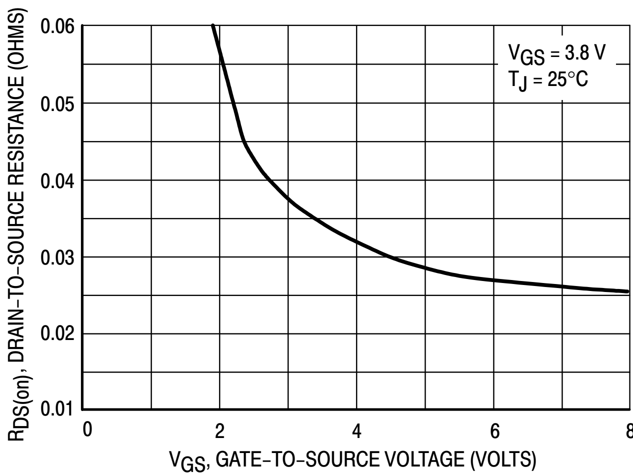



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

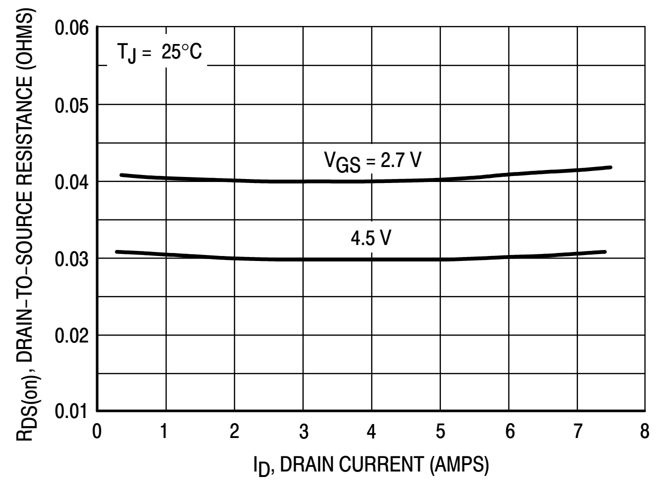



**Figure 6. On–Resistance versus Drain Current and Gate Voltage**

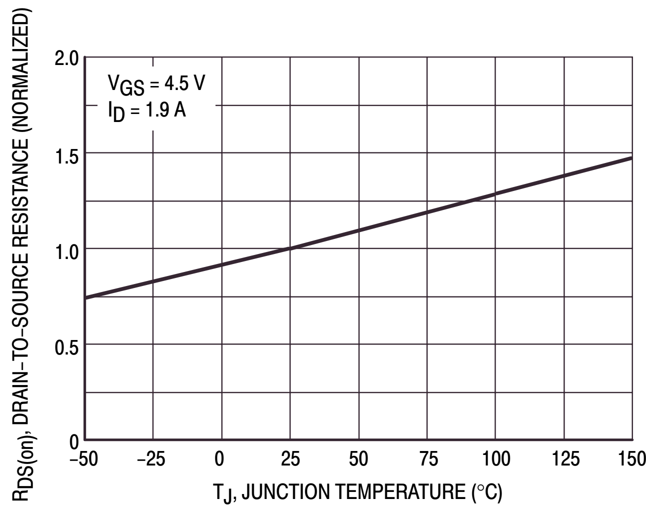



**Figure 7. On–Resistance Variation with Temperature**

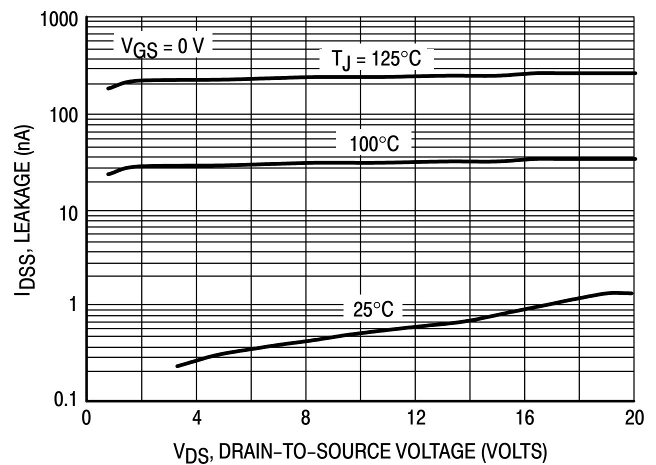



**Figure 8. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\, C_{iss}\, \text{In}\, [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\, C_{iss}\, \text{In}\, (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 11) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

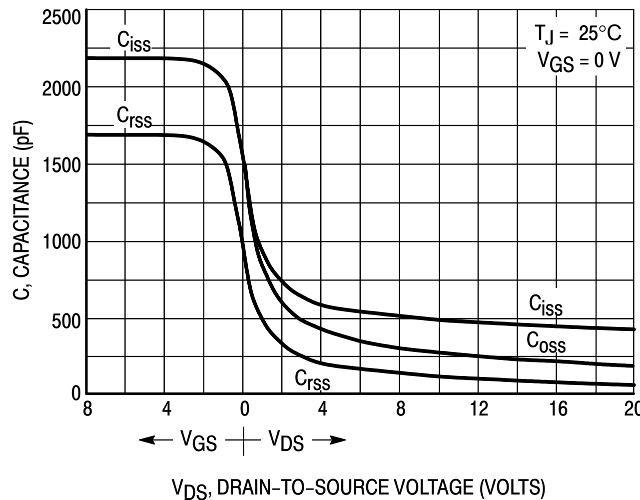



**Figure 9. Capacitance Variation**

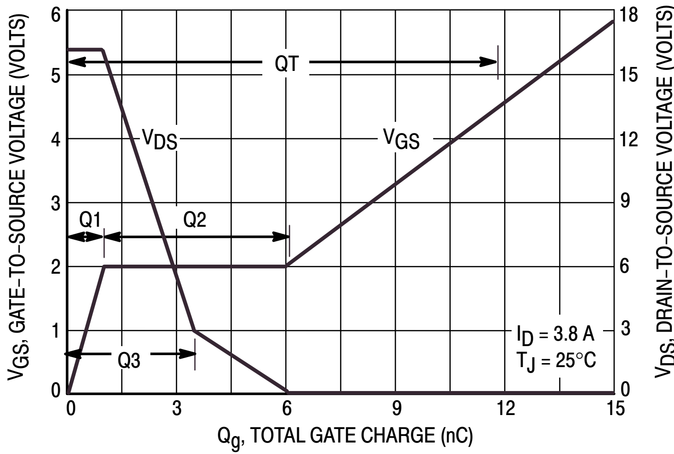



**Figure 10. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

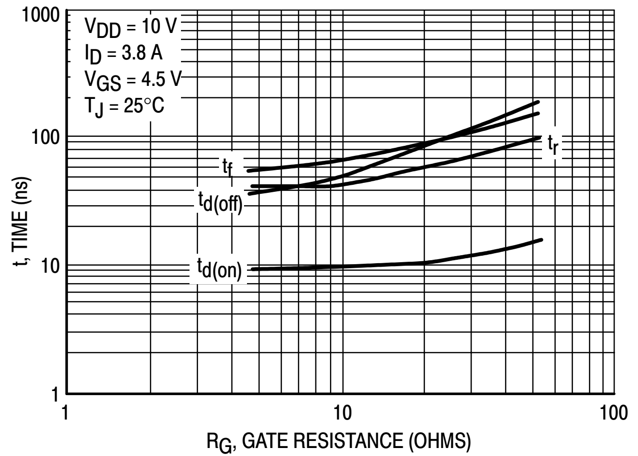



**Figure 11. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 14. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

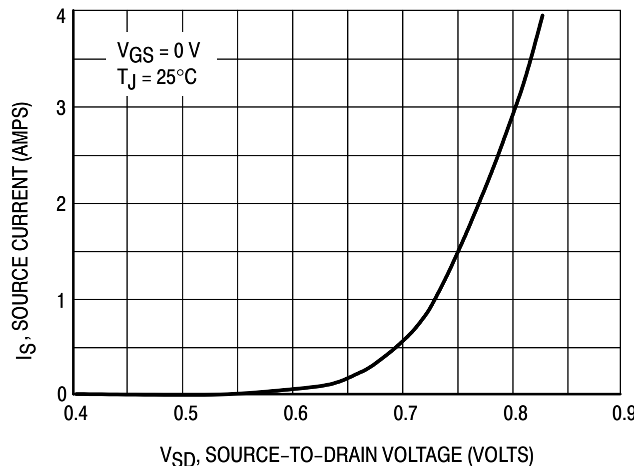



**Figure 12. Diode Forward Voltage versus Current**

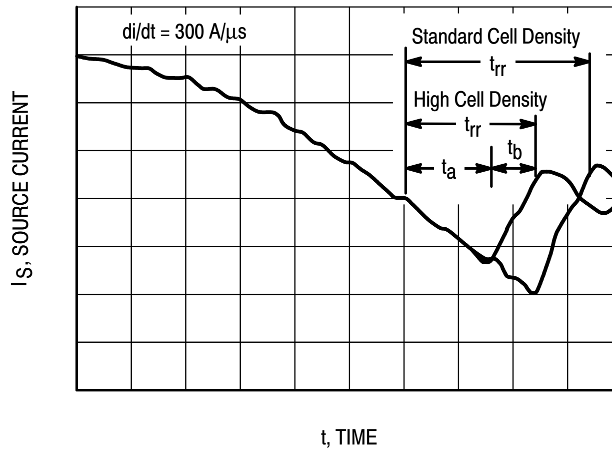



**Figure 13. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

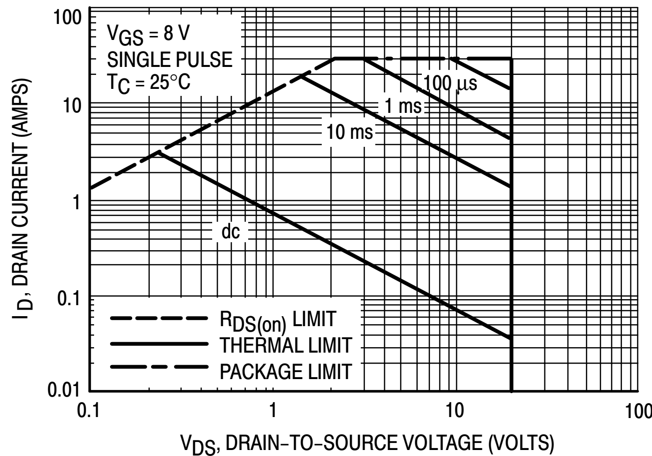



**Figure 14. Maximum Rated Forward Biased Safe Operating Area**

## TYPICAL ELECTRICAL CHARACTERISTICS

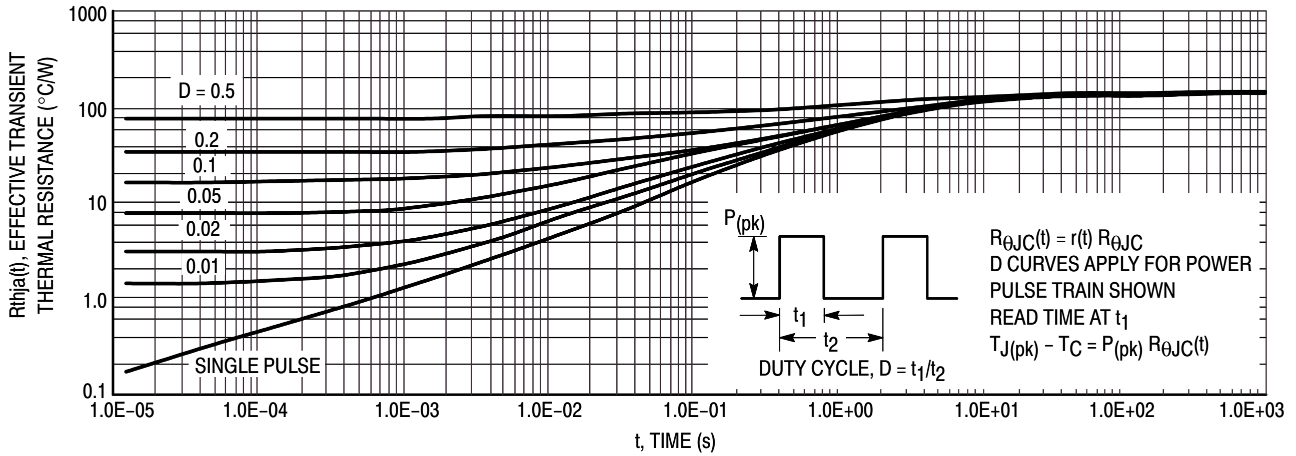



**Figure 15. Thermal Response**

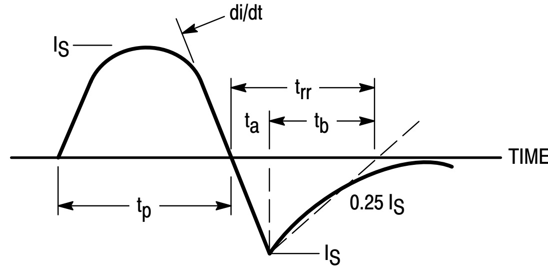
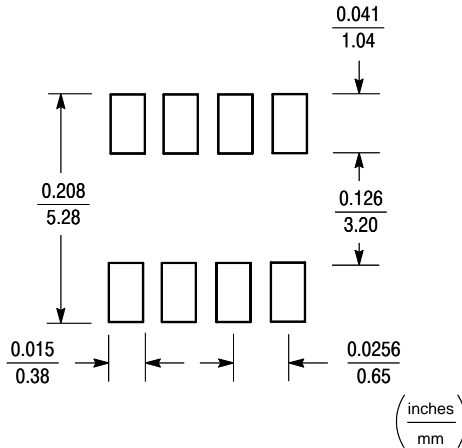



**Figure 16. Diode Reverse Recovery Waveform**

# INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

## MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




## Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.78 Watts.

$$P_D = \frac{150°C - 25°C}{160°C/W} = 0.78 \text{ Watts}$$

The 160°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.78 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

## SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 14 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

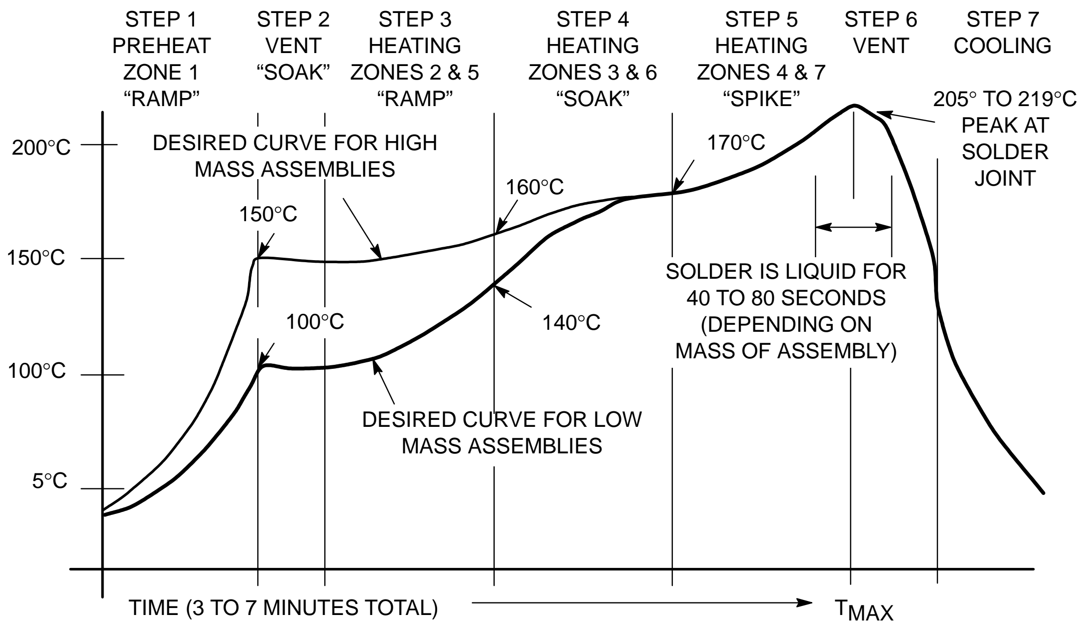
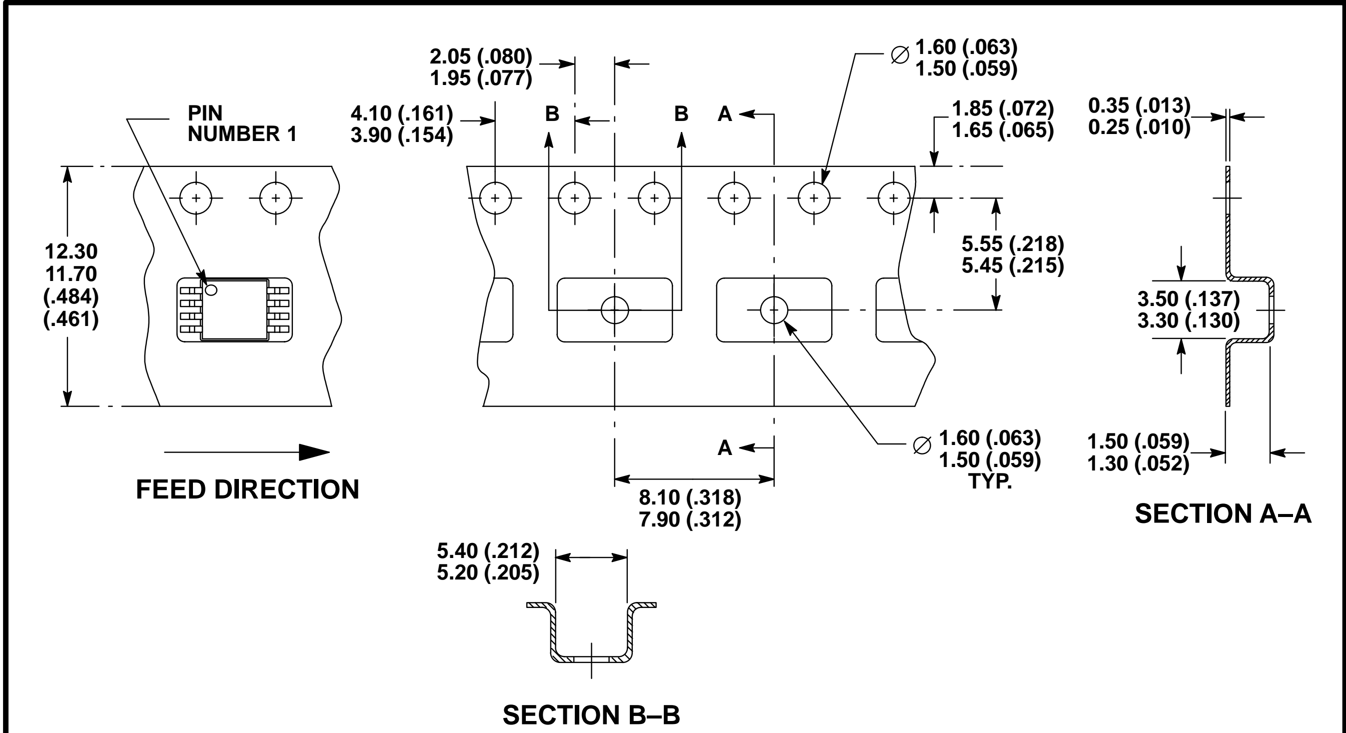
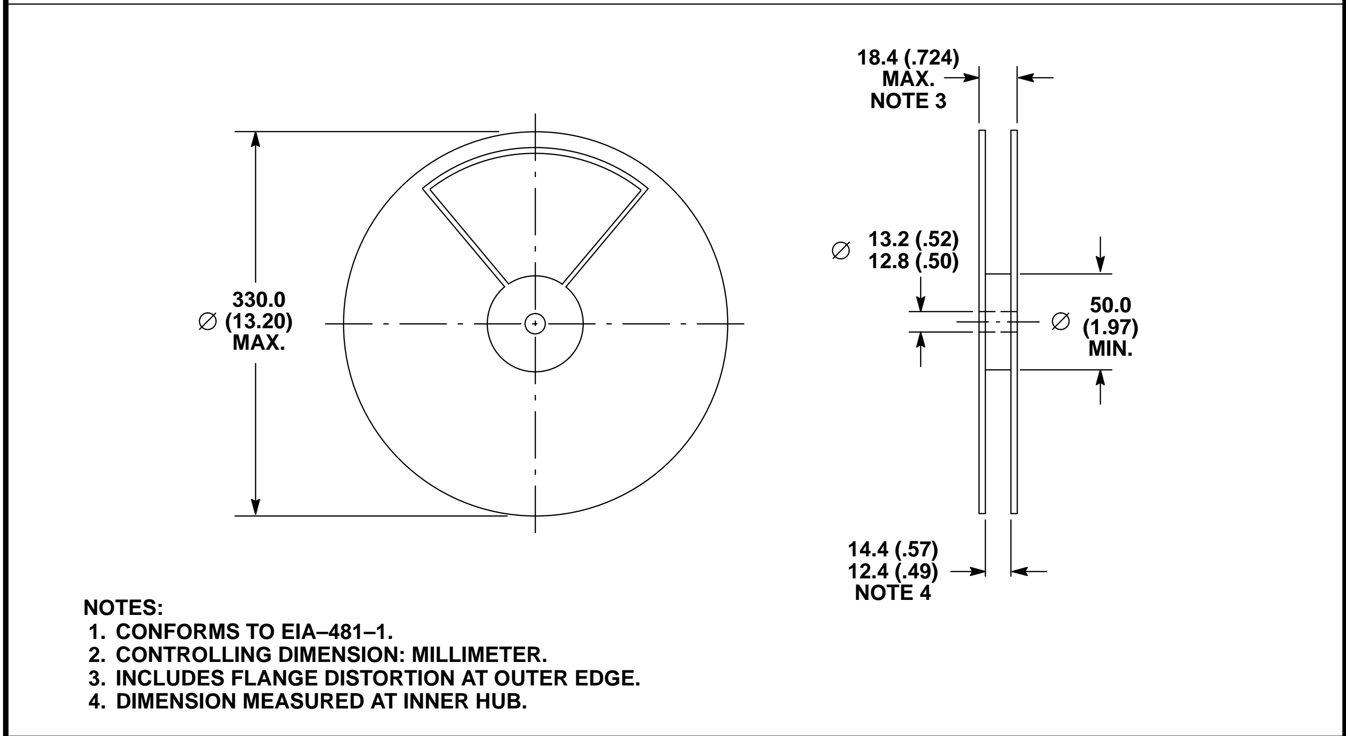



**Figure 17. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro8**
Dimensions are shown in millimeters (inches)



# MTSF3N03HD

**Preferred Device**

# Power MOSFET 3 Amps, 30 Volts

## N–Channel Micro8™

These Power MOSFET devices are capable of withstanding high energy in the avalanche and commutation modes and the drain–to–source diode has a very low reverse recovery time. Micro8 devices are designed for use in low voltage, high speed switching applications where power efficiency is important. Typical applications are dc–dc converters, and power management in portable and battery powered products such as computers, printers, cellular and cordless phones. They can also be used for low voltage motor controls in mass storage products such as disk drives and tape drives. The avalanche energy is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

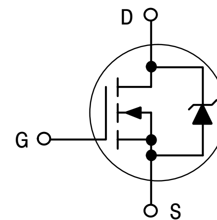
- Miniature Micro8 Surface Mount Package – Saves Board Space
- Extremely Low Profile (<1.1 mm) for thin applications such as PCMCIA cards
- Ultra Low $R_{DS(on)}$ Provides Higher Efficiency and Extends Battery Life
- Logic Level Gate Drive – Can Be Driven by Logic ICs
- Diode Is Characterized for Use In Bridge Circuits
- Diode Exhibits High Speed, With Soft Recovery
- $I_{DSS}$ Specified at Elevated Temperature
- Avalanche Energy Specified
- Mounting Information for Micro8 Package Provided

**ON Semiconductor™**

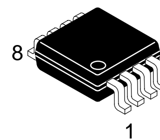
**http://onsemi.com**

**3 AMPERES**
**30 VOLTS**
**$R_{DS(on)}$ = 40 mΩ**

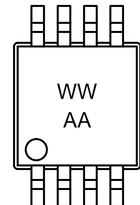
**N–Channel**




**MARKING DIAGRAM**

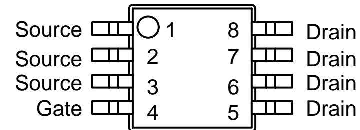



**Micro8**
**CASE 846A**
**STYLE 1**




WW = Date Code

**PIN ASSIGNMENT**




Top View

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTSF3N03HDR2 | Micro8 | 4000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | | Symbol | Max | Unit |
|---|---|---|---|---|
| Drain–to–Source Voltage | | $V_{DSS}$ | 30 | V |
| Drain–to–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | | $V_{DGR}$ | 30 | V |
| Gate–to–Source Voltage – Continuous | | $V_{GS}$ | ± 20 | V |
| 1″ SQ.<br>FR–4 or G–10 PCB<br>Figure 1 below<br><br><br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 70<br>1.79<br>14.29<br>5.7<br>4.5<br>45 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Minimum<br>FR–4 or G–10 PCB<br>Figure 2 below<br><br><br>Steady State | Thermal Resistance – Junction to Ambient<br>Total Power Dissipation @ $T_A$ = 25°C<br>Linear Derating Factor<br>Drain Current – Continuous @ $T_A$ = 25°C<br>Continuous @ $T_A$ = 70°C<br>Pulsed Drain Current (Note 1.) | $R_{THJA}$<br>$P_D$<br><br>$I_D$<br>$I_D$<br>$I_{DM}$ | 160<br>0.78<br>6.25<br>3.8<br>3.0<br>30 | °C/W<br>Watts<br>mW/°C<br>A<br>A<br>A |
| Operating and Storage Temperature Range | | $T_J$, $T_{stg}$ | – 55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C<br>($V_{DD}$ = 30 Vdc, $V_{GS}$ = 5.0 Vdc, Peak $I_L$ = 9.0 Apk, L = 5.0 mH, $R_G$ = 25 Ω) | | $E_{AS}$ | 200 | mJ |

1. Repetitive rating; pulse width limited by maximum junction temperature.

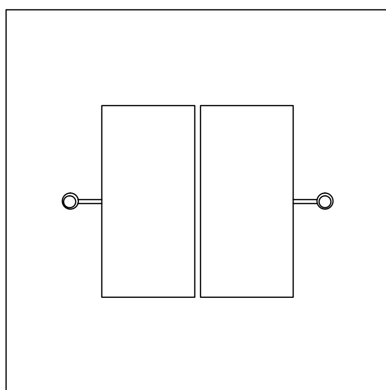


**Figure 1. 1″ Square FR–4 or G–10 PCB**

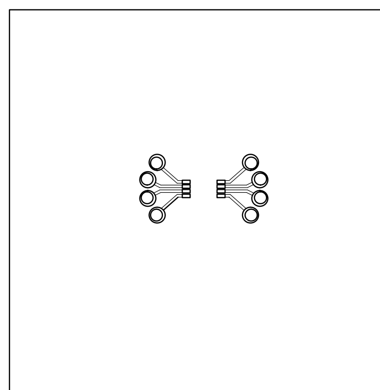


**Figure 2. Minimum FR–4 or G–10 PCB**

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–to–Source Breakdown Voltage (Cpk ≥ 2.0) (Notes 2. & 4.)<br>($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | <br>30<br>– | <br>–<br>27 | <br>–<br>– | Vdc<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc)<br>($V_{DS}$ = 24 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | $I_{DSS}$ | <br>–<br>– | <br>–<br>– | <br>1.0<br>25 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 2.) | | | | | | |
| Gate Threshold Voltage (Cpk ≥ 2.0) (Note 4.)<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Threshold Temperature Coefficient (Negative) | | $V_{GS(th)}$ | <br>1.0<br>– | <br>1.5<br>4.5 | <br>–<br>– | Vdc<br><br>mV/°C |
| Static Drain–to–Source On–Resistance (Cpk ≥ 2.0) (Note 4.)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 3.8 Adc)<br>($V_{GS}$ = 4.5 Vdc, $I_D$ = 1.9 Adc) | | $R_{DS(on)}$ | <br>–<br>– | <br>35<br>45 | <br>40<br>60 | mΩ |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 1.9 Adc) | | $g_{FS}$ | 2.0 | – | – | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 420 | – | pF |
| Output Capacitance | | $C_{oss}$ | – | 190 | – | |
| Transfer Capacitance | | $C_{rss}$ | – | 65 | – | |
| **SWITCHING CHARACTERISTICS** (Note 3.) | | | | | | |
| Turn–On Delay Time | ($V_{DS}$ = 15 Vdc, $I_D$ = 3.7 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 7.0 | – | ns |
| Rise Time | | $t_r$ | – | 19 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 32 | – | |
| Fall Time | | $t_f$ | – | 36 | – | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 1.9 Adc, $V_{GS}$ = 4.5 Vdc, $R_G$ = 6 Ω) (Note 2.) | $t_{d(on)}$ | – | 7.0 | – | ns |
| Rise Time | | $t_r$ | – | 11 | – | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 29 | – | |
| Fall Time | | $t_f$ | – | 23 | – | |
| Gate Charge | ($V_{DS}$ = 24 Vdc, $I_D$ = 3.7 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 18.5 | 26 | nC |
| | | $Q_1$ | – | 1.4 | – | |
| | | $Q_2$ | – | 5.5 | – | |
| | | $Q_3$ | – | 7.1 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 3.7 Adc, $V_{GS}$ = 0 Vdc) (Note 2.)<br>($I_S$ = 3.7 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | $V_{SD}$ | <br>–<br>– | <br>0.82<br>0.7 | <br>1.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 3.7 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) (Note 2.) | $t_{rr}$ | – | 28 | – | ns |
| | | $t_a$ | – | 14 | – | |
| | | $t_b$ | – | 14 | – | |
| Reverse Recovery Storage Charge | | $Q_{RR}$ | – | 0.028 | – | μC |

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperature.
4. Reflects typical values. $C_{pk} = \left| \frac{\text{Max limit} - \text{Typ}}{3 \times \text{SIGMA}} \right|$

## TYPICAL ELECTRICAL CHARACTERISTICS

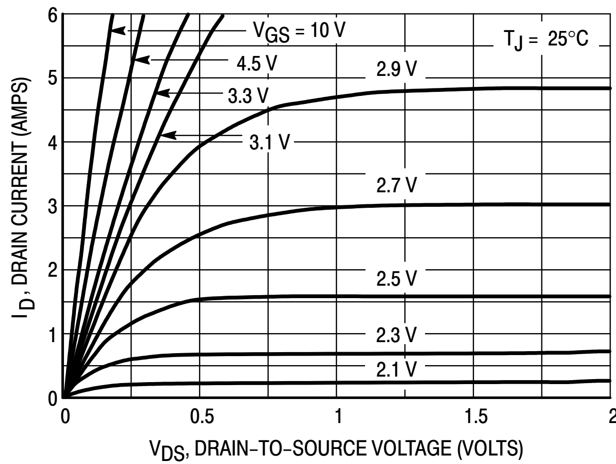



**Figure 3. On–Region Characteristics**

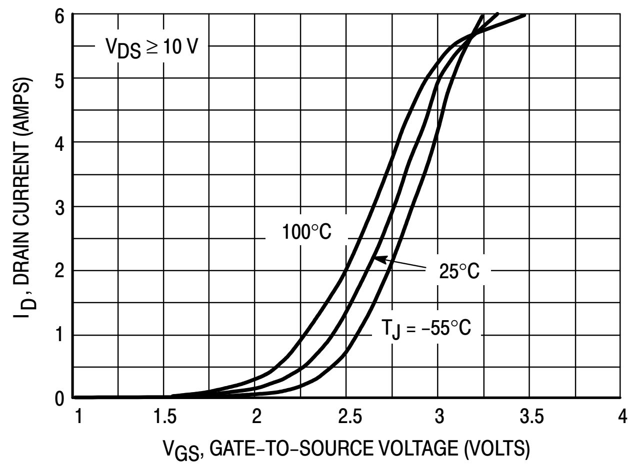



**Figure 4. Transfer Characteristics**

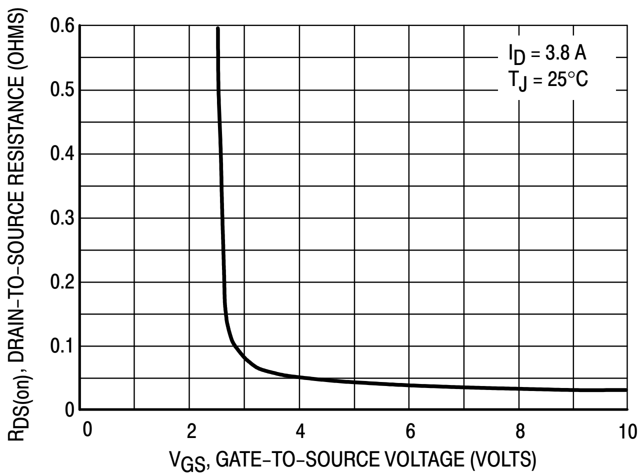



**Figure 5. On–Resistance versus Gate–to–Source Voltage**

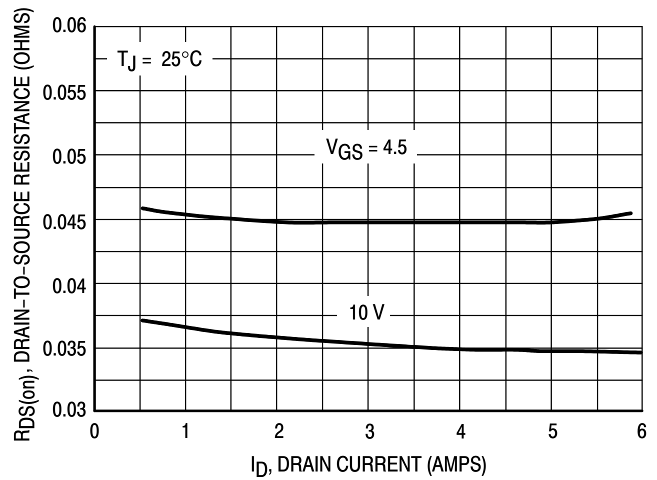



**Figure 6. On–Resistance versus Drain Current and Gate Voltage**

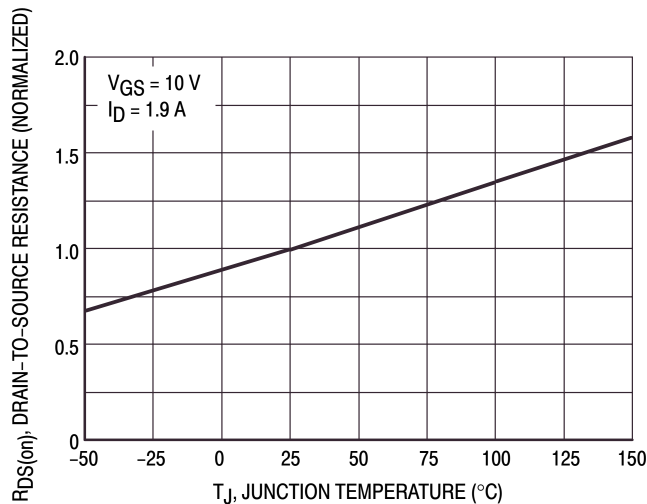



**Figure 7. On–Resistance Variation with Temperature**

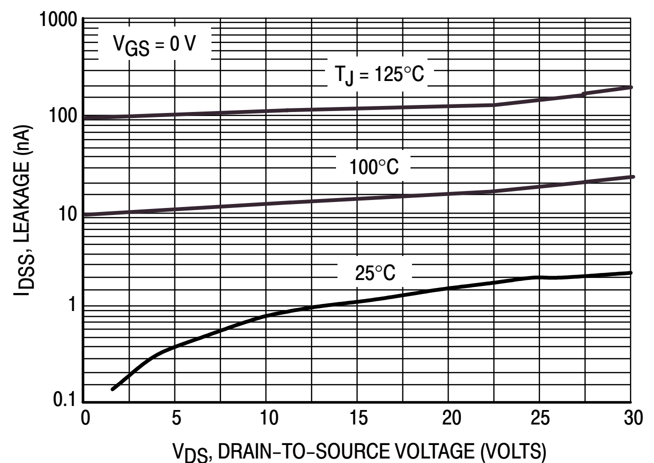



**Figure 8. Drain–to–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 11) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

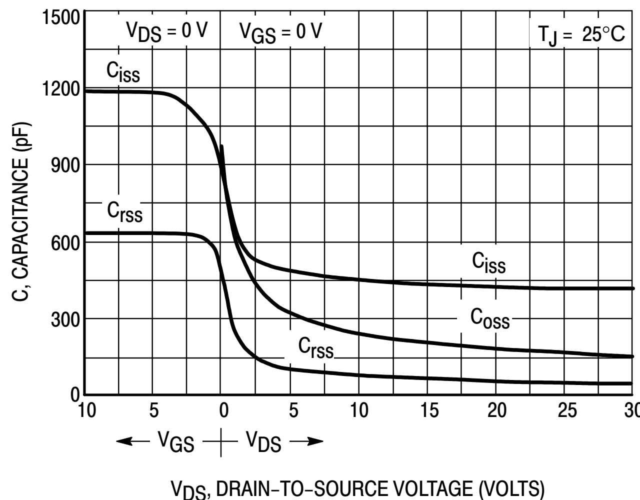



**Figure 9. Capacitance Variation**

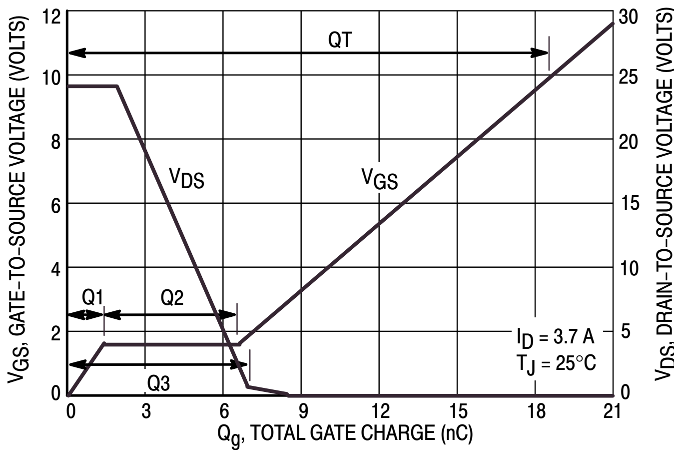



**Figure 10. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

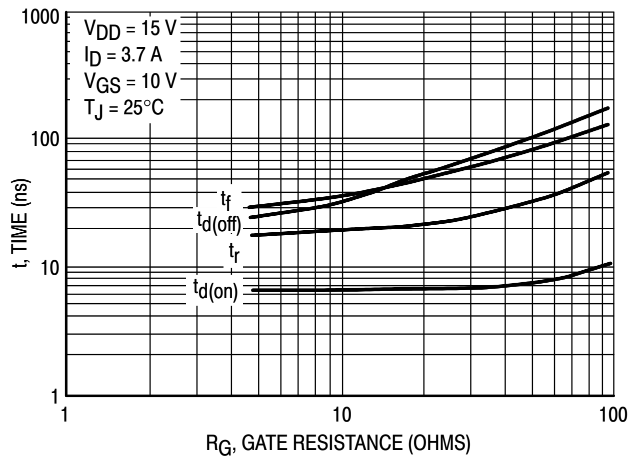



**Figure 11. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

The switching characteristics of a MOSFET body diode are very important in systems using it as a freewheeling or commutating diode. Of particular interest are the reverse recovery characteristics which play a major role in determining switching losses, radiated noise, EMI and RFI.

System switching losses are largely due to the nature of the body diode itself. The body diode is a minority carrier device, therefore it has a finite reverse recovery time, $t_{rr}$, due to the storage of minority carrier charge, $Q_{RR}$, as shown in the typical reverse recovery wave form of Figure 13. It is this stored charge that, when cleared from the diode, passes through a potential and defines an energy loss. Obviously, repeatedly forcing the diode through reverse recovery further increases switching losses. Therefore, one would like a diode with short $t_{rr}$ and low $Q_{RR}$ specifications to minimize these losses.

The abruptness of diode reverse recovery effects the amount of radiated noise, voltage spikes, and current ringing. The mechanisms at work are finite irremovable circuit parasitic inductances and capacitances acted upon by high di/dts. The diode's negative di/dt during $t_a$ is directly controlled by the device clearing the stored charge. However, the positive di/dt during $t_b$ is an uncontrollable diode characteristic and is usually the culprit that induces current ringing. Therefore, when comparing diodes, the ratio of $t_b/t_a$ serves as a good indicator of recovery abruptness and thus gives a comparative estimate of probable noise generated. A ratio of 1 is considered ideal and values less than 0.5 are considered snappy.

Compared to ON Semiconductor standard cell density low voltage MOSFETs, high cell density MOSFET diodes are faster (shorter $t_{rr}$), have less stored charge and a softer reverse recovery characteristic. The softness advantage of the high cell density diode means they can be forced through reverse recovery at a higher di/dt than a standard cell MOSFET diode without increasing the current ringing or the noise generated. In addition, power dissipation incurred from switching the diode will be less due to the shorter recovery time and lower switching losses.

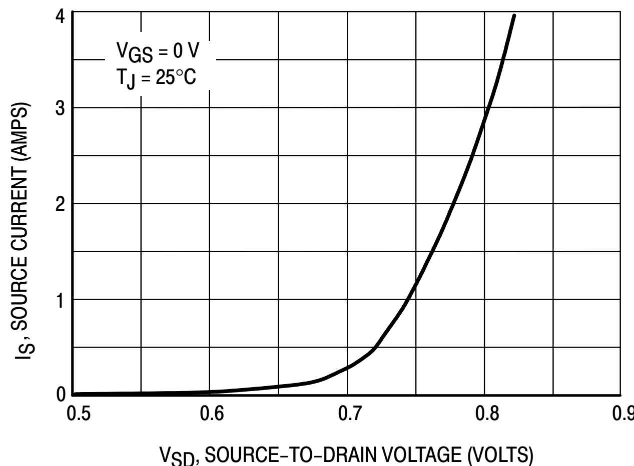



**Figure 12. Diode Forward Voltage versus Current**

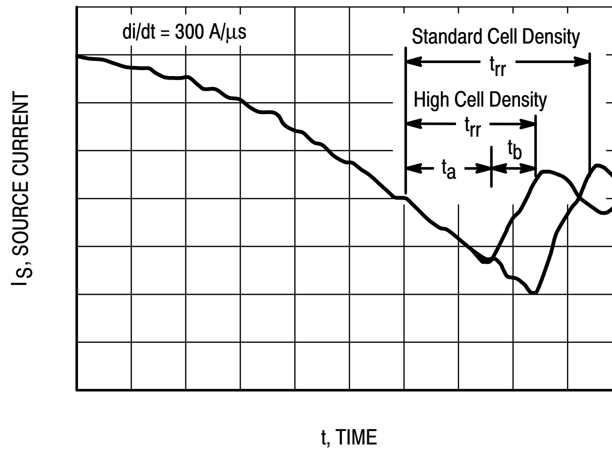



**Figure 13. Reverse Recovery Time ($t_{rr}$)**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curve (Figure 14) defines the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance – General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded, and that the transition time ($t_r$, $t_f$) does not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and must be adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 15). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

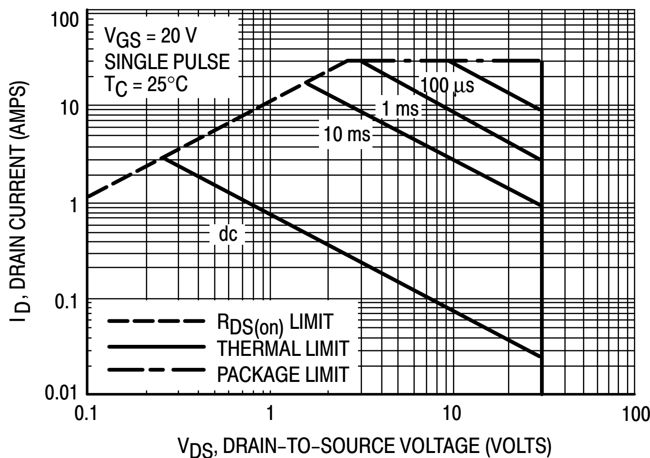



**Figure 14. Maximum Rated Forward Biased Safe Operating Area**

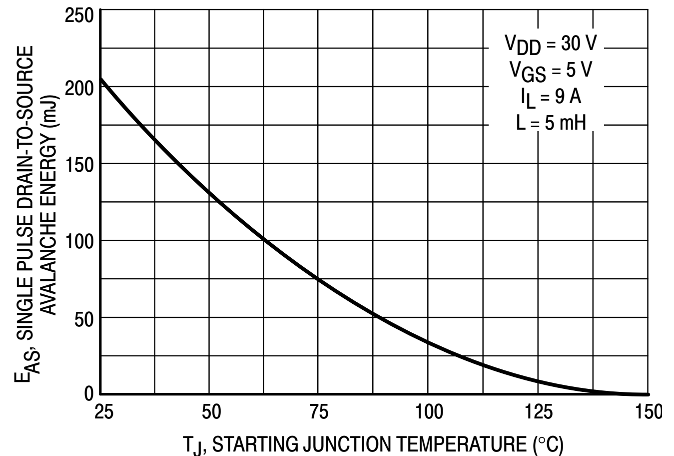



**Figure 15. Maximum Avalanche Energy versus Starting Junction Temperature**

## TYPICAL ELECTRICAL CHARACTERISTICS

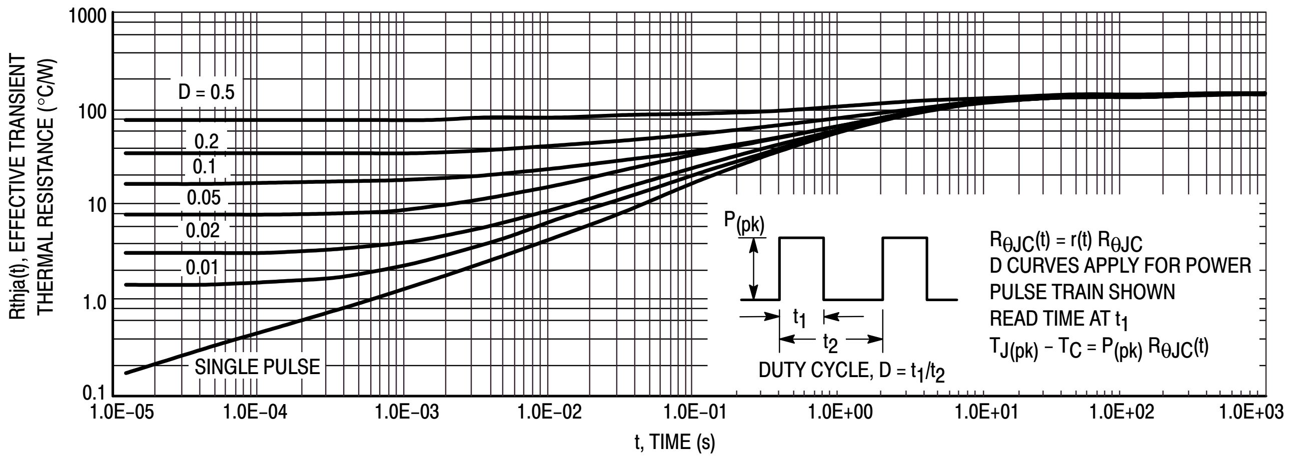



**Figure 16. Thermal Response**

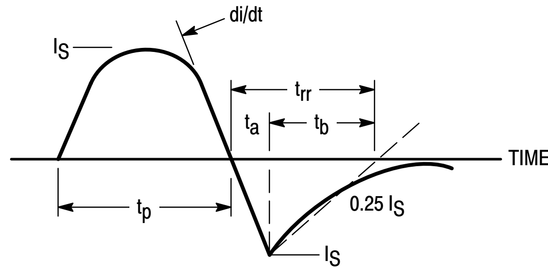
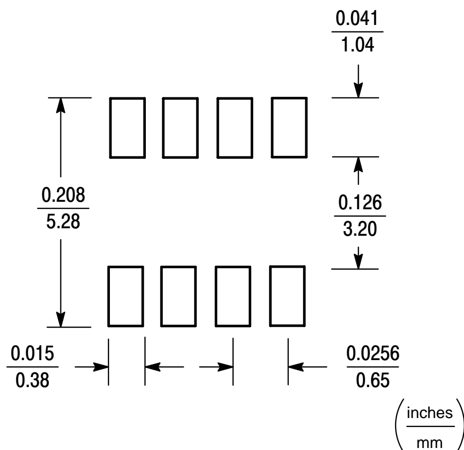



**Figure 17. Diode Reverse Recovery Waveform**

## INFORMATION FOR USING THE Micro8 SURFACE MOUNT PACKAGE

### MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to ensure proper solder connection interface between the board and the package. With the correct pad geometry, the packages will self–align when subjected to a solder reflow process.




### Micro8 POWER DISSIPATION

The power dissipation of the Micro8 is a function of the input pad size. This can vary from the minimum pad size for soldering to the pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by $T_{J(max)}$, the maximum rated junction temperature of the die, $R_{\theta JA}$, the thermal resistance from the device junction to ambient; and the operating temperature, $T_A$. Using the values provided on the data sheet for the Micro8 package, $P_D$ can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature $T_A$ of 25°C, one can calculate the power dissipation of the device which in this case is 0.78 Watts.

$$P_D = \frac{150°C - 25°C}{160°C/W} = 0.78 \text{ Watts}$$

The 160°C/W for the Micro8 package assumes the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 0.78 Watts using the footprint shown. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad™. Using board material such as Thermal Clad, the power dissipation can be doubled using the same footprint.

### SOLDERING PRECAUTIONS

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

## TYPICAL SOLDER HEATING PROFILE

For any given circuit board, there will be a group of control settings that will give the desired heat pattern. The operator must set temperatures for several heating zones and a figure for belt speed. Taken together, these control settings make up a heating “profile” for that particular circuit board. On machines controlled by a computer, the computer remembers these profiles from one operating session to the next. Figure 18 shows a typical heating profile for use when soldering a surface mount device to a printed circuit board. This profile will vary among soldering systems, but it is a good starting point. Factors that can affect the profile include the type of soldering system in use, density and types of components on the board, type of solder used, and the type of board or substrate material being used. This profile shows temperature versus time. The line on the graph shows the actual temperature that might be experienced on the surface of a test board at or near a central solder joint. The two profiles are based on a high density and a low density board. The Vitronics SMD310 convection/infrared reflow soldering system was used to generate this profile. The type of solder used was 62/36/2 Tin Lead Silver with a melting point between 177–189°C. When this type of furnace is used for solder reflow work, the circuit boards and solder joints tend to heat first. The components on the board are then heated by conduction. The circuit board, because it has a large surface area, absorbs the thermal energy more efficiently, then distributes this energy to the components. Because of this effect, the main body of a component may be up to 30 degrees cooler than the adjacent solder joints.

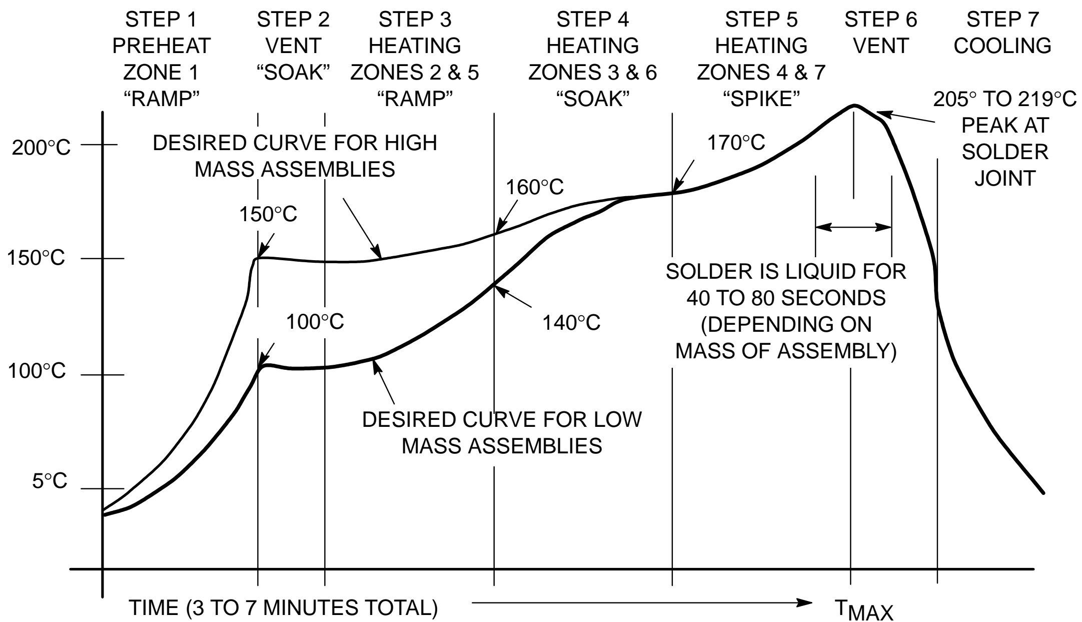
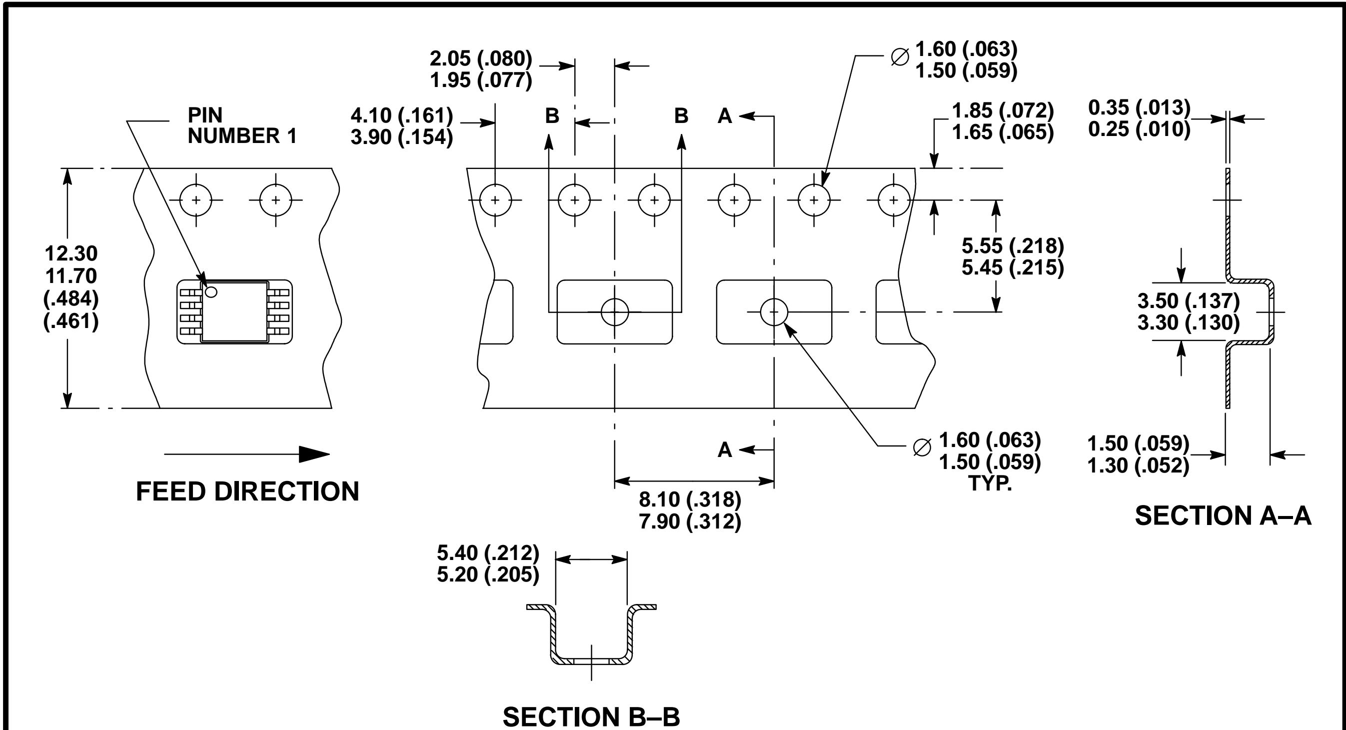


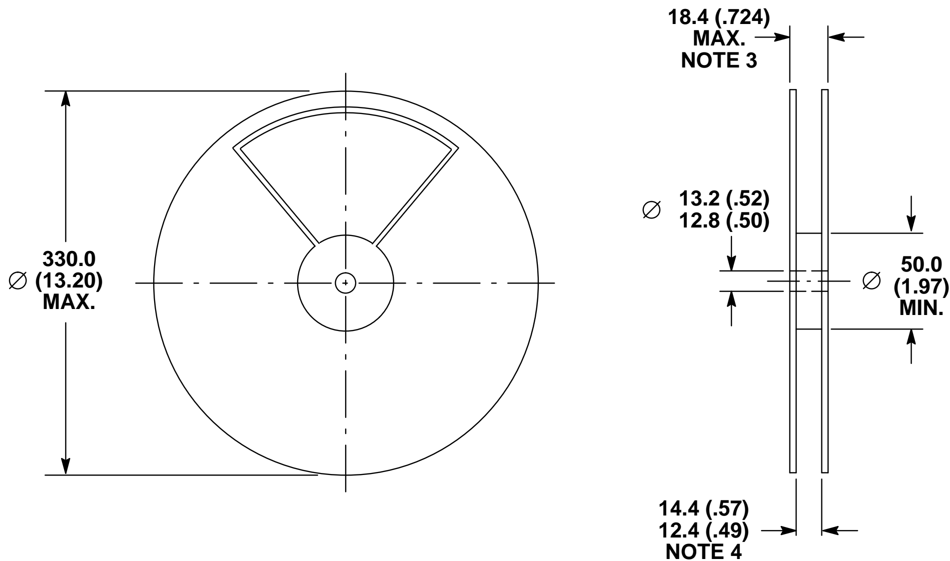

**Figure 18. Typical Solder Heating Profile**

## TAPE & REEL INFORMATION

**Micro8**
Dimensions are shown in millimeters (inches)




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.




NOTES:
1. CONFORMS TO EIA–481–1.
2. CONTROLLING DIMENSION: MILLIMETER.
3. INCLUDES FLANGE DISTORTION AT OUTER EDGE.
4. DIMENSION MEASURED AT INNER HUB.

# MTW32N20E

Preferred Device

# Power MOSFET 32 Amps, 200 Volts

## N–Channel TO–247

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

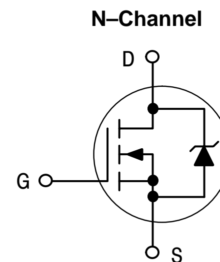
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage – Continuous | $V_{GS}$ | ±20 | Vdc |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq 10\ \mu s$) | $I_D$<br>$I_D$<br>$I_{DM}$ | 32<br>19<br>128 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 180<br>1.44 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 50 Vdc, $V_{GS}$ = 10 Vpk, $I_L$ = 32 Apk, L = 1.58 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 810 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.7<br>40 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

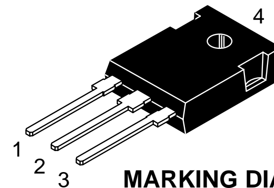
**ON Semiconductor™**

http://onsemi.com

**32 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 75 mΩ**

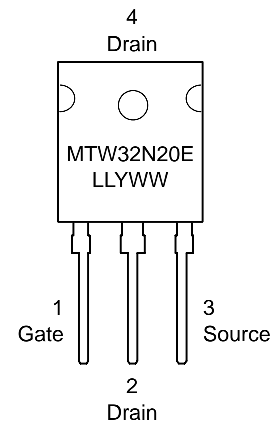
**N–Channel**




**TO–247AE**
**CASE 340K**
**Style 1**

**MARKING DIAGRAM & PIN ASSIGNMENT**




LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTW32N20E | TO–247 | 30 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 V, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Positive) | | $V_{(BR)DSS}$ | 200<br>– | –<br>247 | –<br>– | Vdc<br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0)<br>($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | –<br>– | 250<br>1000 | μAdc |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc)<br>Temperature Coefficient (Negative) | | $V_{GS(th)}$ | 2.0<br>– | –<br>8.0 | 4.0<br>– | Vdc<br>mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 0.064 | 0.075 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc)<br>($I_D$ = 32 Adc)<br>($I_D$ = 16 Adc, $T_J$ = 125°C) | | $V_{DS(on)}$ | –<br>– | –<br>– | 3.0<br>2.7 | Vdc |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | 12 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 3600 | 5000 | pF |
| Output Capacitance | | $C_{oss}$ | – | 130 | 250 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 690 | 1000 | |
| **SWITCHING CHARACTERISTICS** (Notes 1. & 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 6.2 Ω) | $t_{d(on)}$ | – | 25 | 50 | ns |
| Rise Time | | $t_r$ | – | 120 | 240 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 75 | 150 | |
| Fall Time | | $t_f$ | – | 91 | 182 | |
| Gate Charge | ($V_{DS}$ = 160 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 85 | 120 | nC |
| | | $Q_1$ | – | 12 | – | |
| | | $Q_2$ | – | 40 | – | |
| | | $Q_3$ | – | 30 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** (Note 1.) | | | | | | |
| Forward On–Voltage | ($I_S$ = 32 Adc, $V_{GS}$ = 0)<br>($I_S$ = 16 Adc, $V_{GS}$ = 0, $T_J$ = 125°C) | $V_{SD}$ | –<br>– | 1.1<br>0.9 | 2.0<br>– | Vdc |
| Reverse Recovery Time | ($I_S$ = 32 Adc, $V_{GS}$ = 0, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 280 | – | ns |
| | | $t_a$ | – | 195 | – | |
| | | $t_b$ | – | 85 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 2.94 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance<br>(Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 5.0 | – | nH |
| Internal Source Inductance<br>(Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 13 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

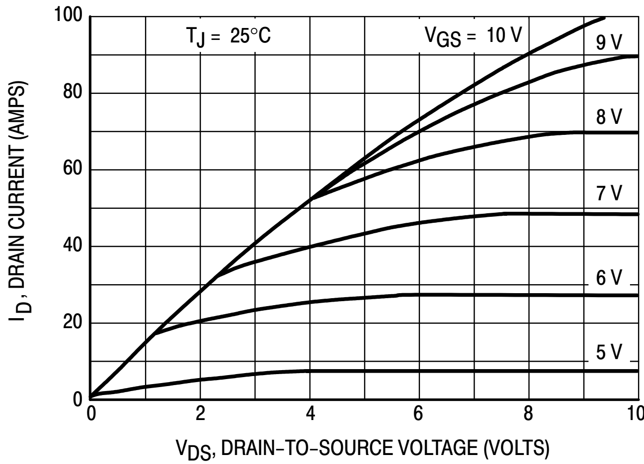



**Figure 1. On–Region Characteristics**

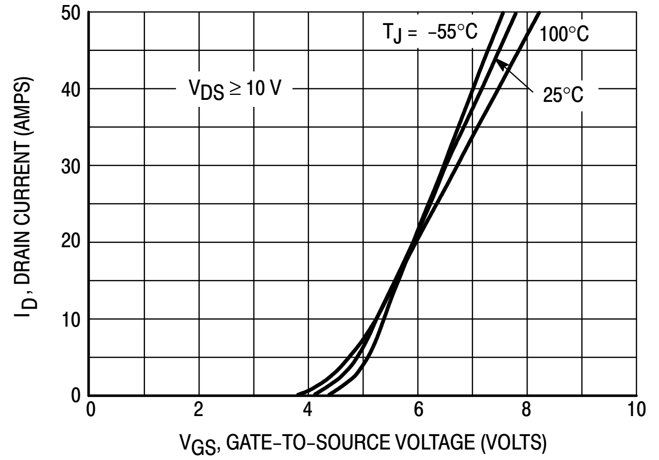



**Figure 2. Transfer Characteristics**

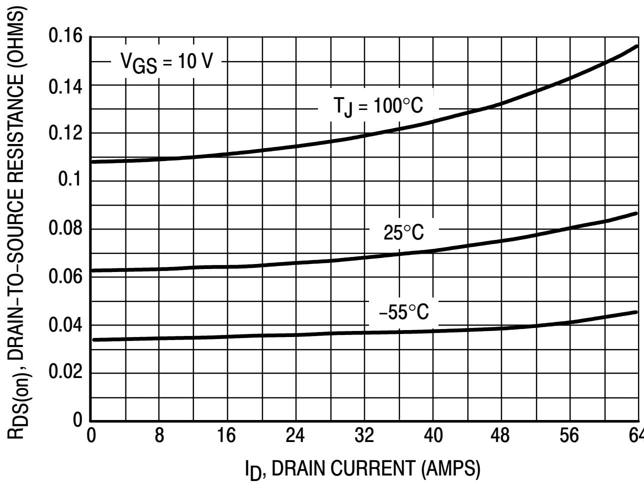



**Figure 3. On–Resistance versus Drain Current and Temperature**

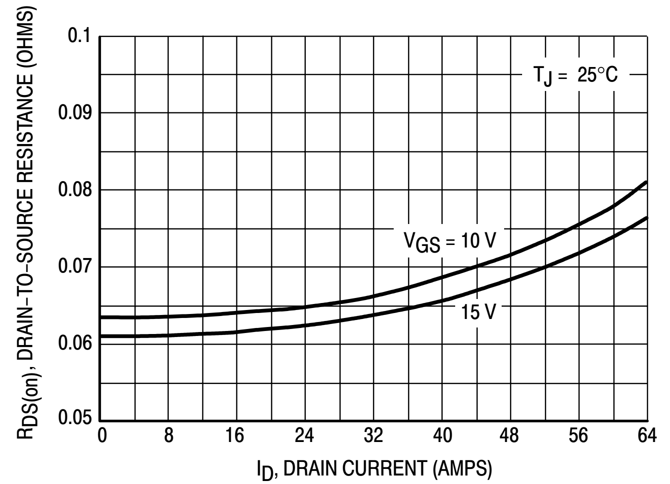



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

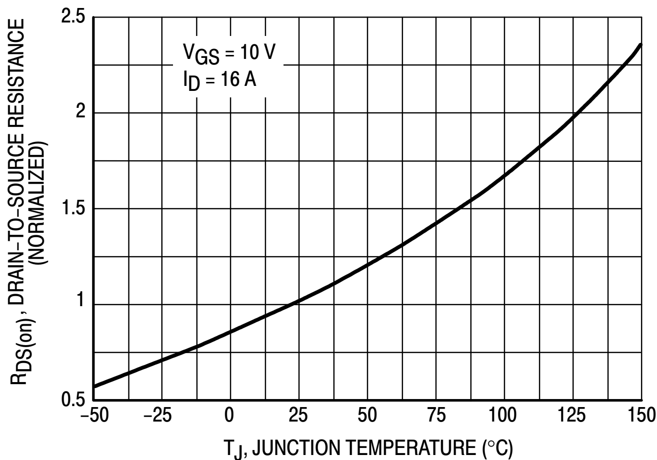



**Figure 5. On–Resistance Variation with Temperature**

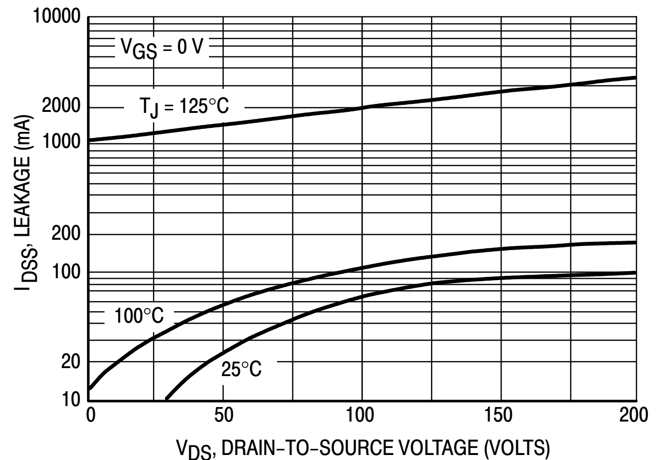



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ \text{In}\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by L di/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

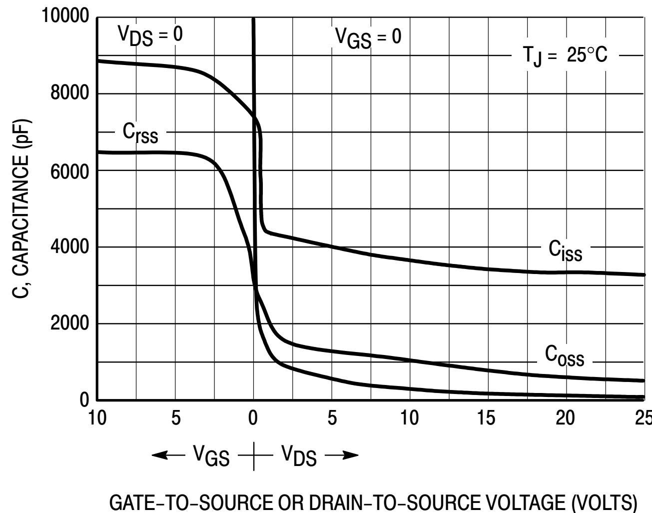



**Figure 7. Capacitance Variation**

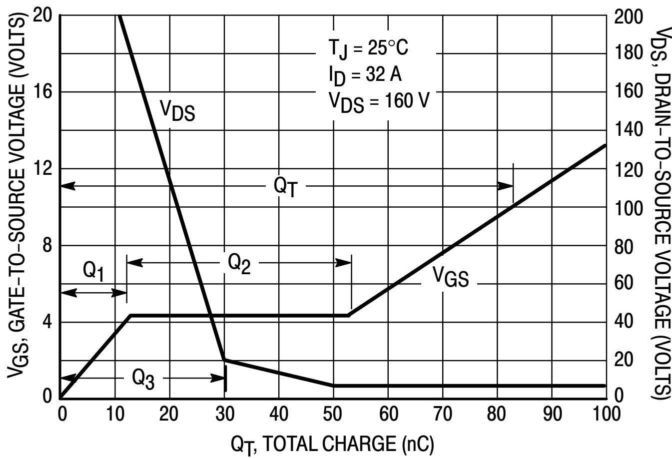



**Figure 9. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

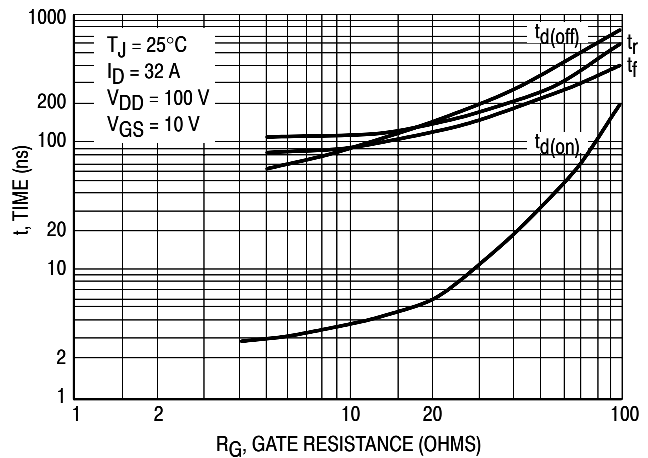



**Figure 8. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

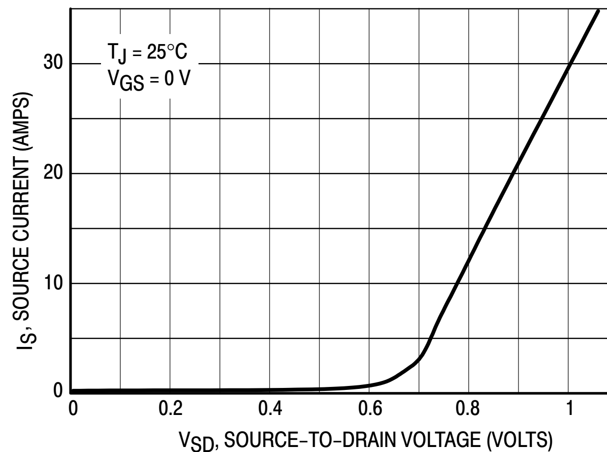



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10μs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

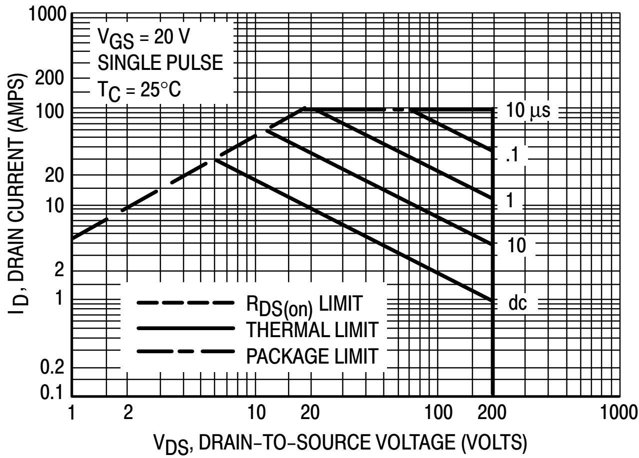



**Figure 13. Maximum Rated Forward Biased Safe Operating Area**

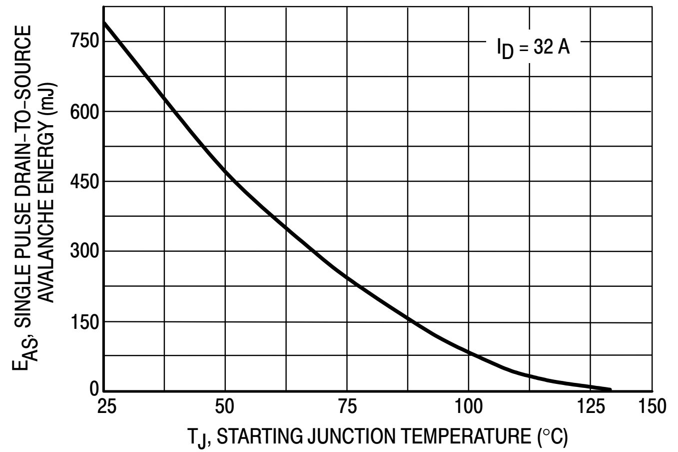



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

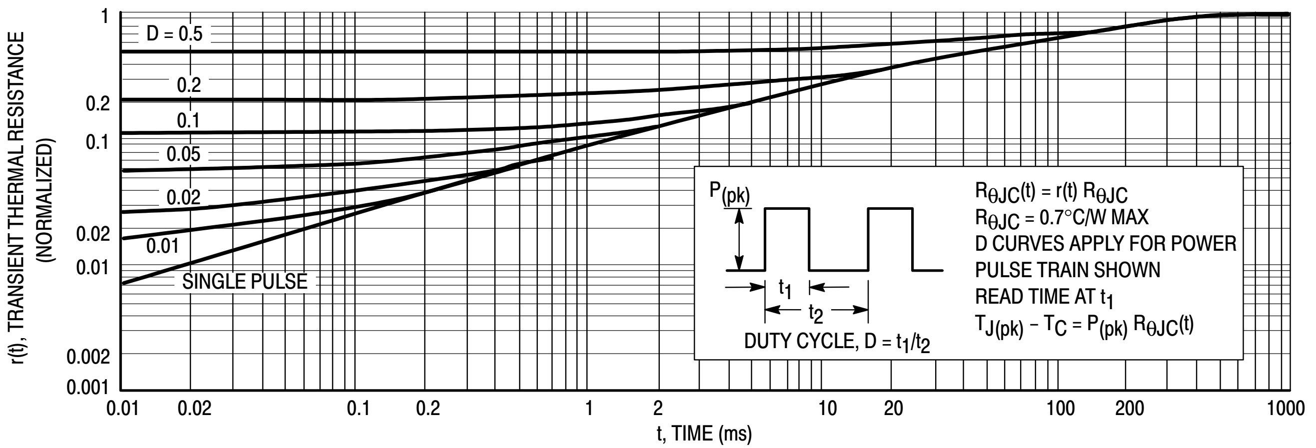



**Figure 11. Thermal Response**

# MTW32N25E

**Preferred Device**

# Power MOSFET 32 Amps, 250 Volts

## N–Channel TO–247

**ON Semiconductor**™

**http://onsemi.com**

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

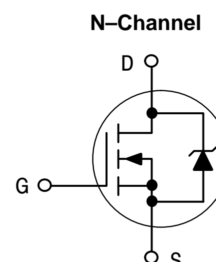
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware

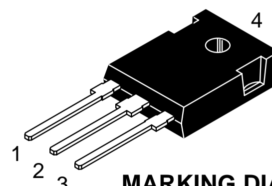
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 250 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 250 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \leq$ 10 ms) | $V_{GS}$<br>$V_{GSM}$ | ± 20<br>± 40 | Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p \leq$ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 32<br>25<br>96 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 250<br>2.0 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 100 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 20 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 600 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.50<br>40 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

**32 AMPERES**
**250 VOLTS**
**$R_{DS(on)}$ = 80 mΩ**

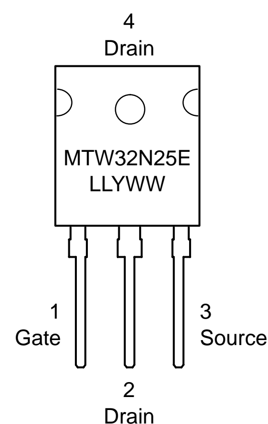
**N–Channel**




**TO–247AE**
**CASE 340K**
**Style 1**

**MARKING DIAGRAM & PIN ASSIGNMENT**




LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTW32N25E | TO–247 | 30 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 250 | 300 | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 380 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 250 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 250 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 7.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 16 Adc) | | $R_{DS(on)}$ | – | 0.07 | 0.08 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 32 Adc) | | $V_{DS(on)}$ | – | 2.2 | 2.6 | Vdc |
| ($I_D$ = 16 Adc, $T_J$ = 125°C) | | | – | – | 2.5 | |
| Forward Transconductance ($V_{DS}$ = 15 Vdc, $I_D$ = 16 Adc) | | $g_{FS}$ | 11 | 20 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3800 | 5350 | pF |
| Output Capacitance | | $C_{oss}$ | – | 726 | 1020 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 183 | 370 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$= 125 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 31 | 60 | ns |
| Rise Time | | $t_r$ | – | 133 | 266 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 93 | 186 | |
| Fall Time | | $t_f$ | – | 108 | 216 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 200 Vdc, $I_D$ = 32 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 97 | 136 | nC |
| | | $Q_1$ | – | 22 | – | |
| | | $Q_2$ | – | 43 | – | |
| | | $Q_3$ | – | 41 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.0 | 1.5 | Vdc |
| | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.92 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 32 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 312 | – | ns |
| | | $t_a$ | – | 220 | – | |
| | | $t_b$ | – | 93 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 3.6 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 13 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

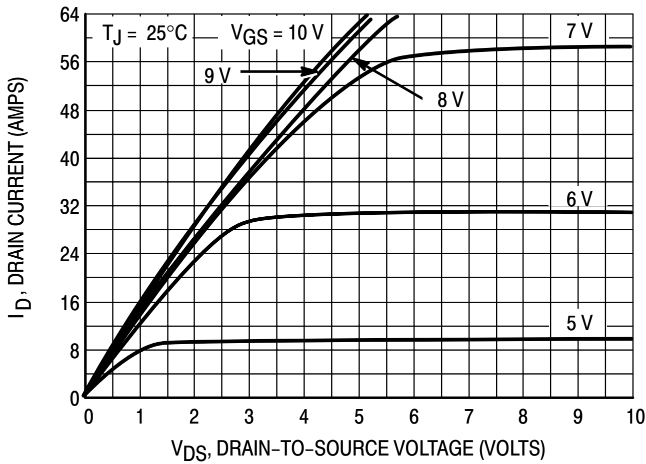



**Figure 1. On–Region Characteristics**

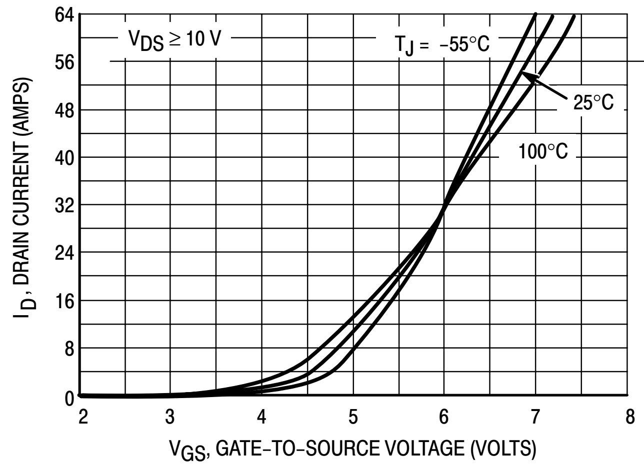



**Figure 2. Transfer Characteristics**

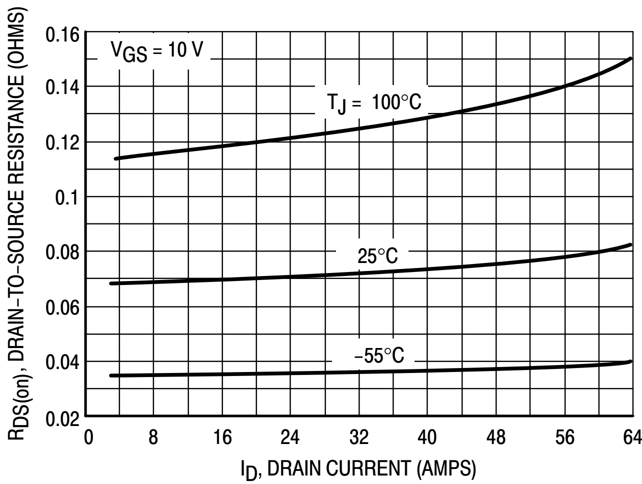



**Figure 3. On–Resistance versus Drain Current and Temperature**

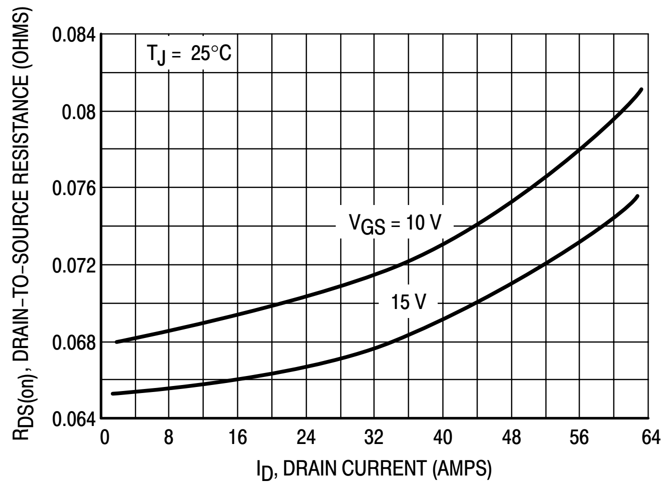



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

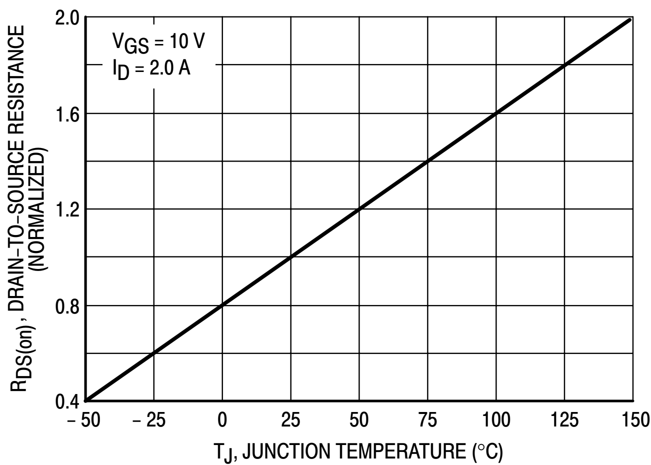



**Figure 5. On–Resistance Variation with Temperature**

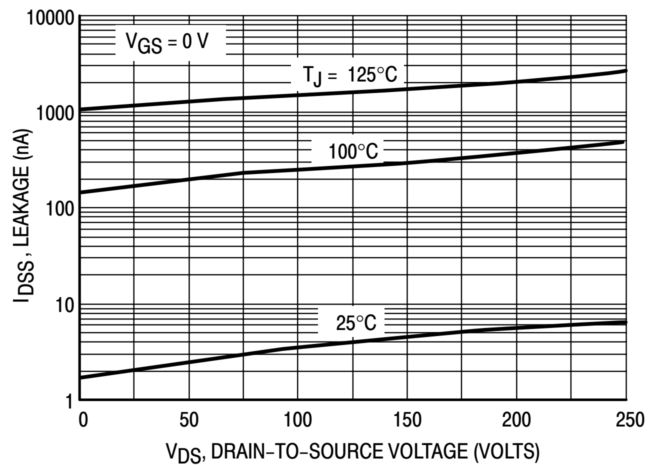



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G C_{iss} \text{ In } [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G C_{iss} \text{ In } (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

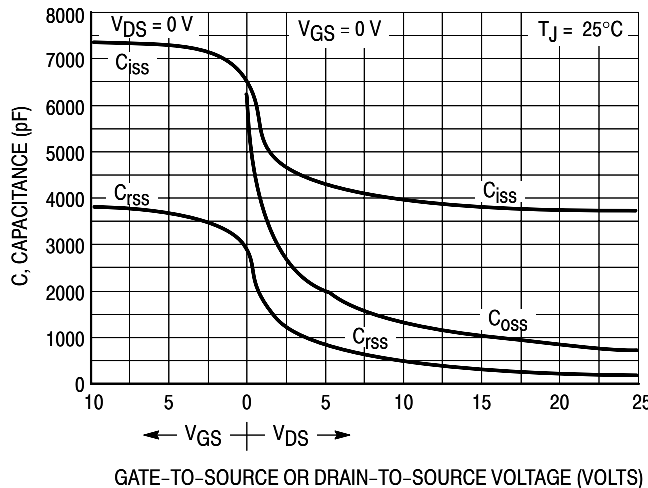



**Figure 7. Capacitance Variation**

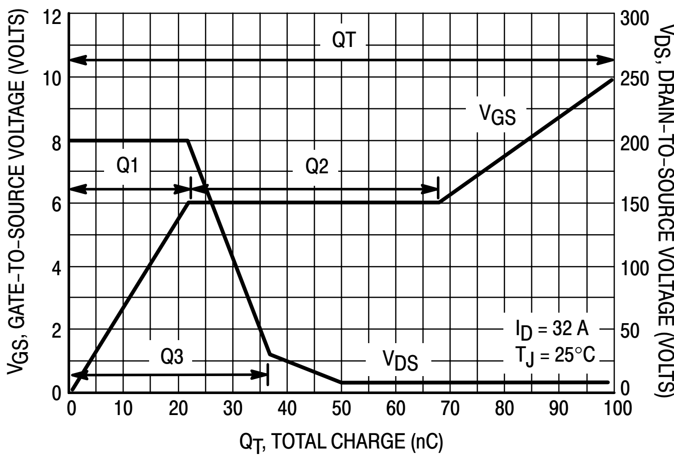



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

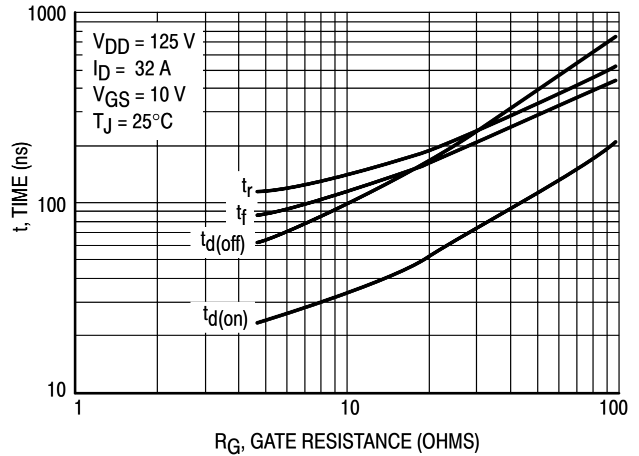



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

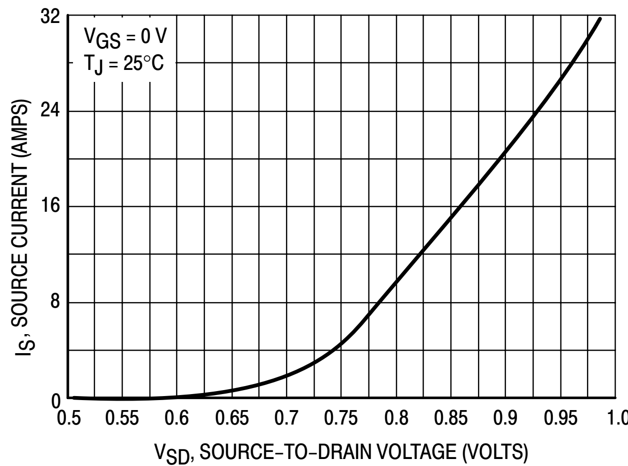



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

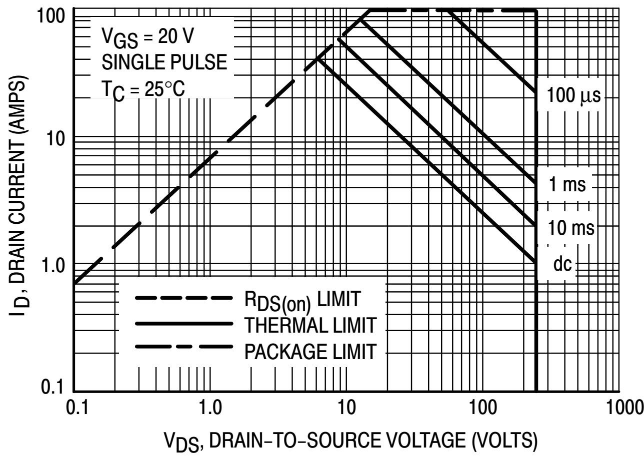



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

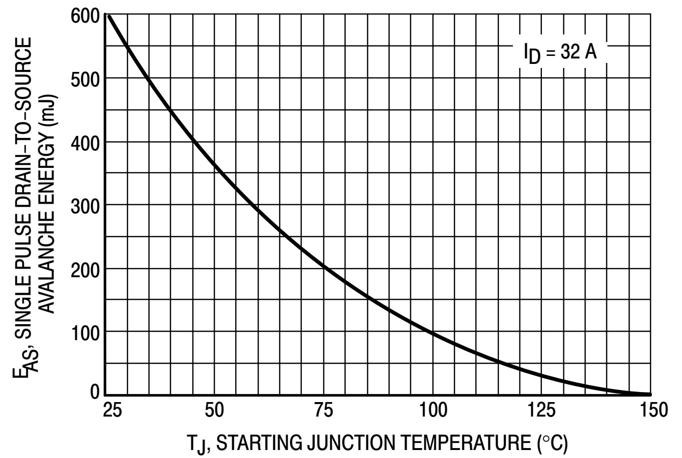



**Figure 14. Maximum Avalanche Energy versus Starting Junction Temperature**

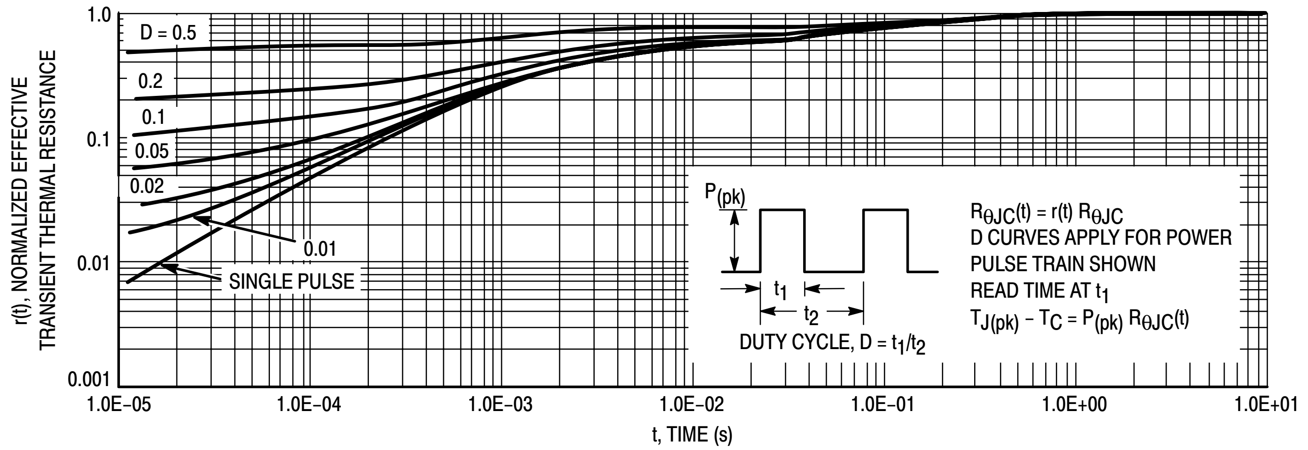



**Figure 12. Thermal Response**

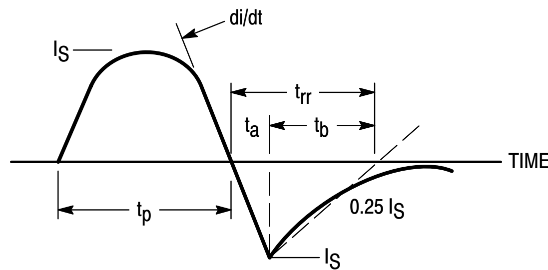



**Figure 13. Diode Reverse Recovery Waveform**

# MTW35N15E

**Preferred Device**

# Power MOSFET 35 Amps, 150 Volts

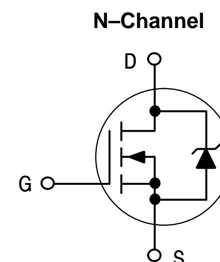
## N–Channel TO–247

**ON Semiconductor™**

**http://onsemi.com**

**35 AMPERES**
**150 VOLTS**
**$R_{DS(on)}$ = 50 mΩ**

**N–Channel**

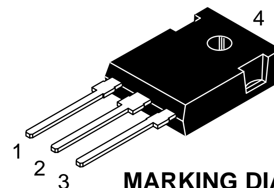



This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware

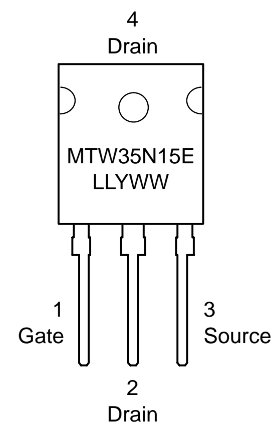
**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 150 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 150 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 µs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 35<br>26.9<br>105 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 180<br>1.45 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 80 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 20 Apk, L = 3.0 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 600 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.70<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |




**TO–247AE**
**CASE 340K**
**Style 1**

**MARKING DIAGRAM & PIN ASSIGNMENT**




LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTW35N15E | TO–247 | 30 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 150 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 210 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 150 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 7.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 17.5 Adc) | | $R_{DS(on)}$ | – | – | 0.05 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 35 Adc) | | $V_{DS(on)}$ | – | 1.45 | 1.8 | Vdc |
| ($I_D$ = 17.5 Adc, $T_J$ = 125°C) | | | – | – | 1.7 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 17.5 Adc) | | $g_{FS}$ | 11 | 18 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3600 | 5040 | pF |
| Output Capacitance | | $C_{oss}$ | – | 855 | 1170 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 165 | 330 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 75 Vdc, $I_D$ = 35 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 28 | 56 | ns |
| Rise Time | | $t_r$ | – | 170 | 346 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 90 | 180 | |
| Fall Time | | $t_f$ | – | 103 | 210 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 120 Vdc, $I_D$ = 35 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 98 | 137 | nC |
| | | $Q_1$ | – | 19 | – | |
| | | $Q_2$ | – | 49 | – | |
| | | $Q_3$ | – | 40 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 35 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.95 | 1.5 | Vdc |
| | ($I_S$ = 35 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 0.9 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 35 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 200 | – | ns |
| | | $t_a$ | – | 167 | – | |
| | | $t_b$ | – | 32 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.63 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 13 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

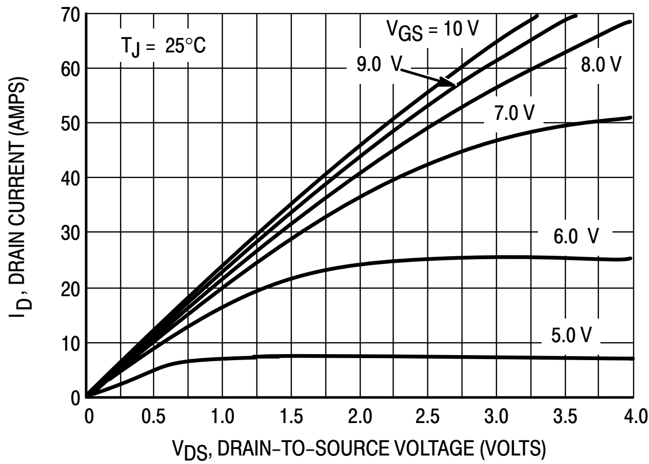



**Figure 1. On–Region Characteristics**

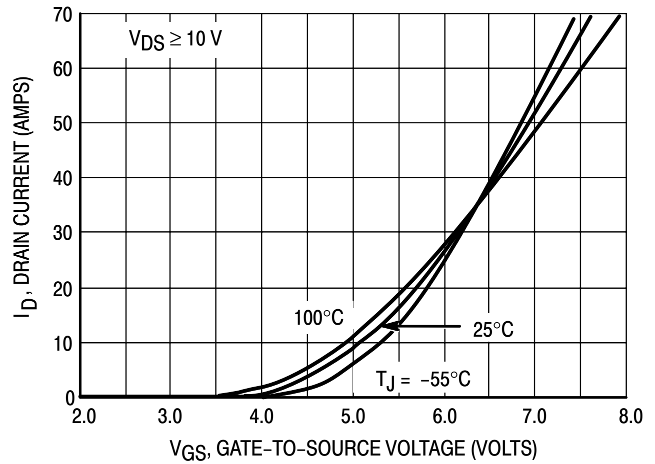



**Figure 2. Transfer Characteristics**

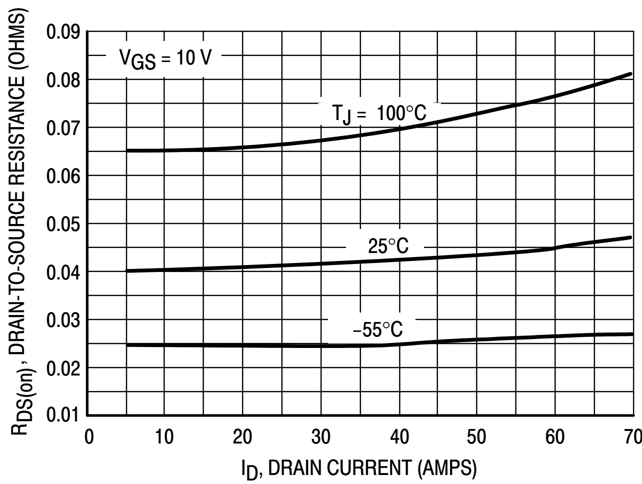



**Figure 3. On–Resistance versus Drain Current and Temperature**

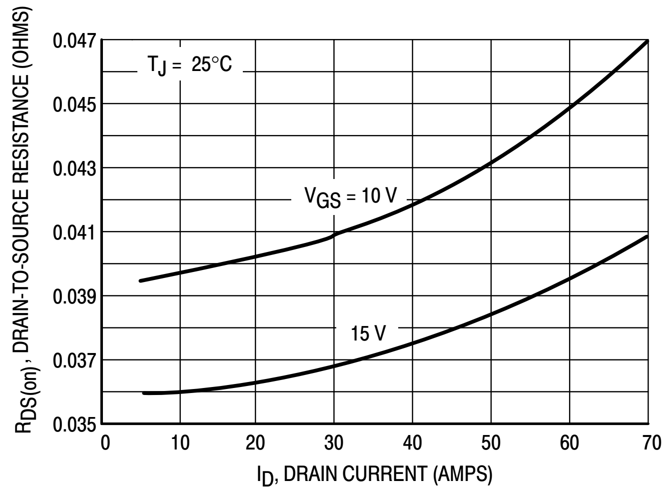



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

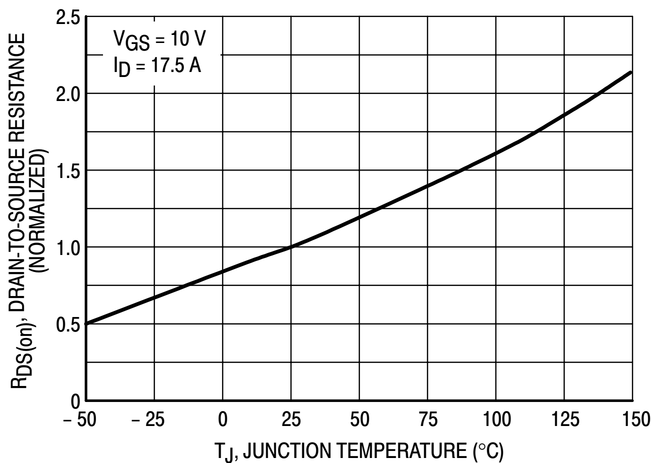



**Figure 5. On–Resistance Variation with Temperature**

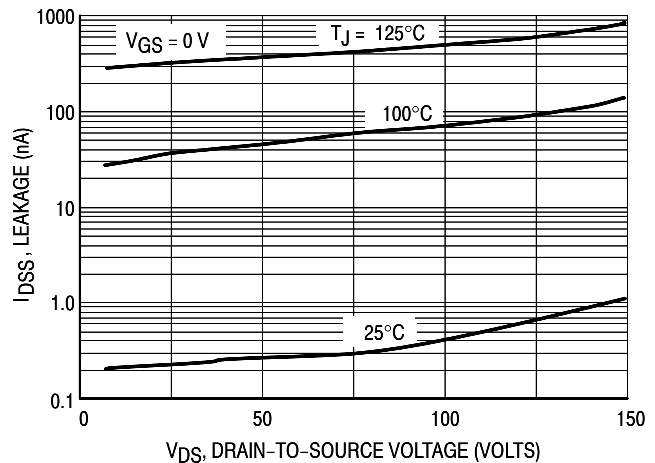



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G\ C_{iss}\ In\ [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G\ C_{iss}\ In\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

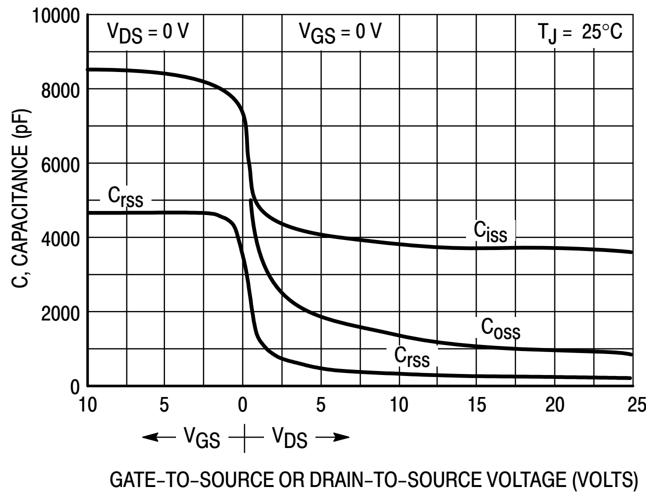



**Figure 7. Capacitance Variation**

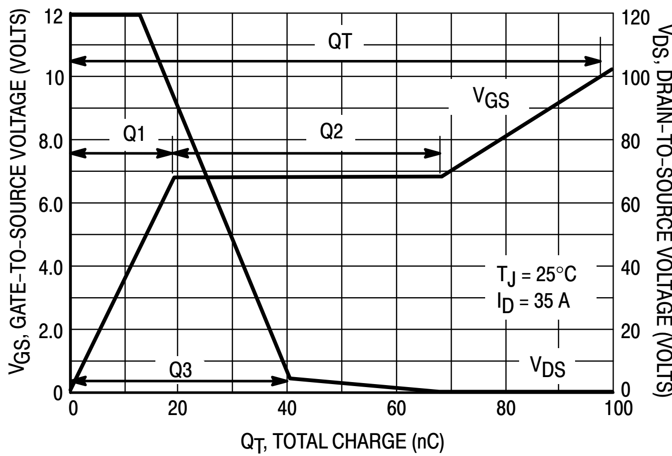



Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge

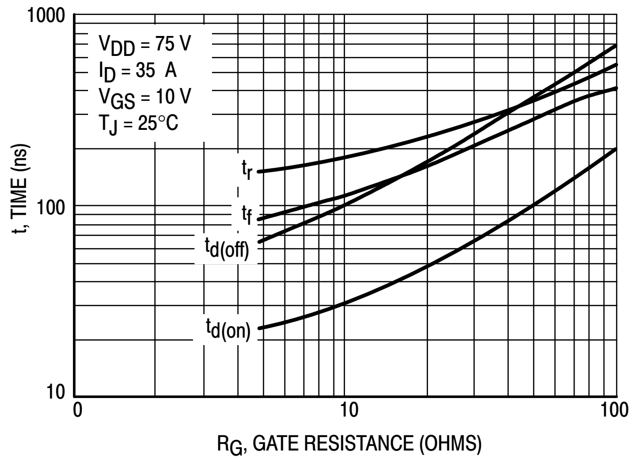



Figure 9. Resistive Switching Time Variation versus Gate Resistance

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

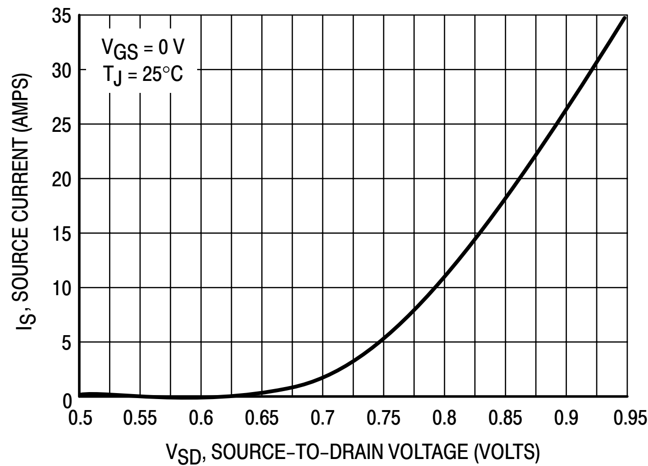



Figure 10. Diode Forward Voltage versus Current

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, "Transient Thermal Resistance–General Data and Its Use."

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

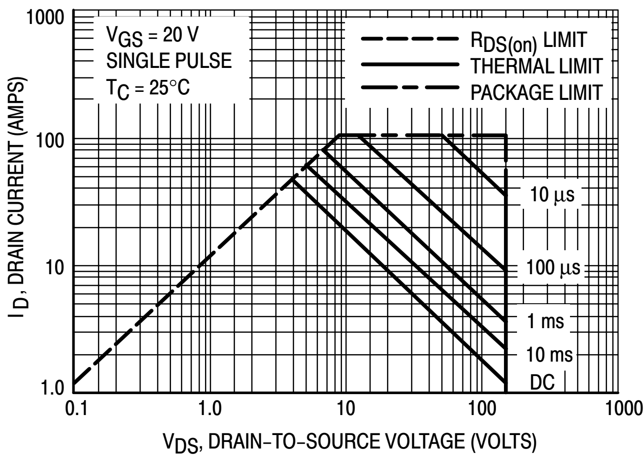



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

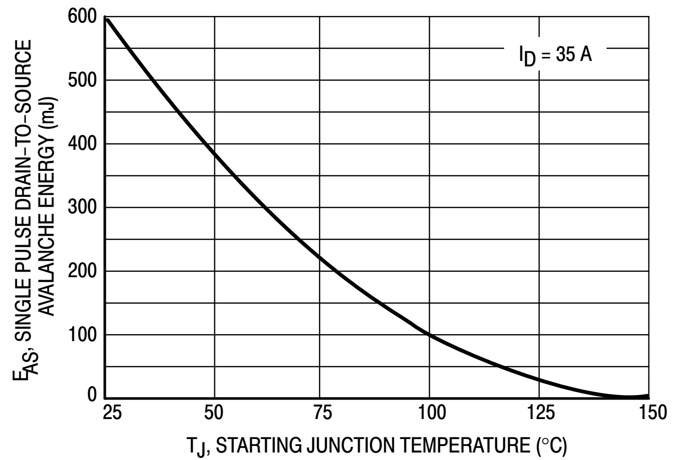



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

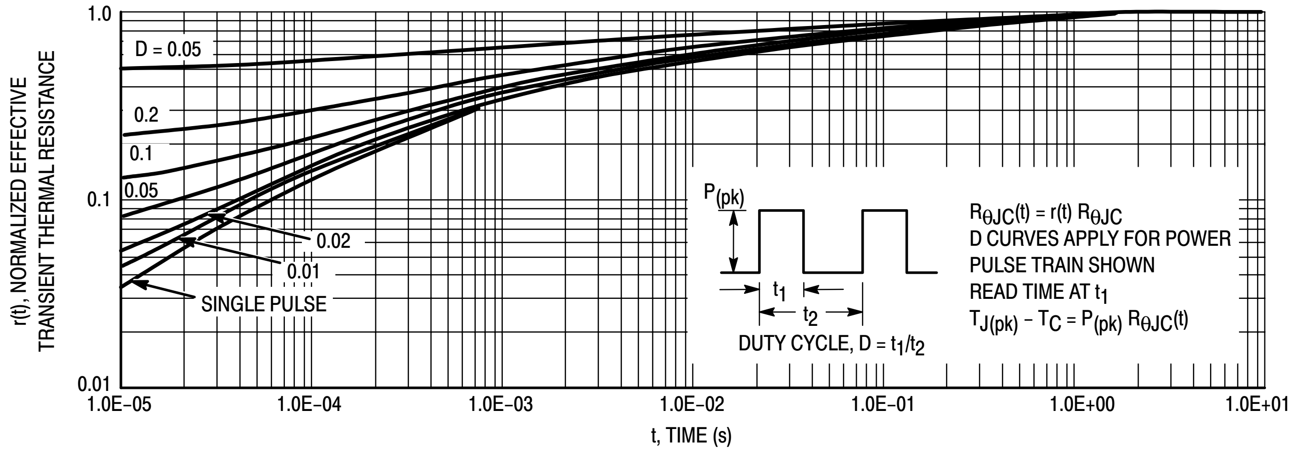



**Figure 13. Thermal Response**

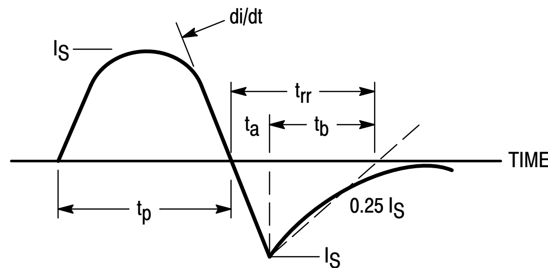



**Figure 14. Diode Reverse Recovery Waveform**

# MTW45N10E

Preferred Device

# Power MOSFET 45 Amps, 100 Volts

## N–Channel TO–247

This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for low voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature
- Isolated Mounting Hole Reduces Mounting Hardware

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

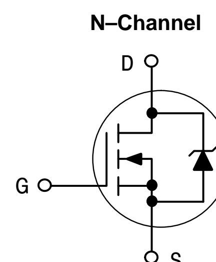
| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 100 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 100 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous<br>– Continuous @ 100°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_D$<br>$I_{DM}$ | 45<br>34.6<br>135 | Adc<br><br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 180<br>1.44 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 Vdc, $V_{GS}$ = 10 Vdc, $I_L$ = 45 Apk, L = 0.8 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 810 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.70<br>62.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

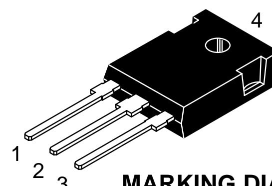
**ON Semiconductor™**

http://onsemi.com

**45 AMPERES**
**100 VOLTS**
**$R_{DS(on)}$ = 35 mΩ**

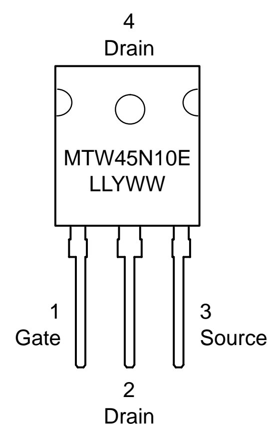
**N–Channel**




**TO–247AE**
**CASE 340K**
**Style 1**

**MARKING DIAGRAM & PIN ASSIGNMENT**




LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTW45N10E | TO–247 | 30 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0 Vdc, $I_D$ = 250 μAdc) | | $V_{(BR)DSS}$ | 100 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 116 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 100 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 100 | |
| Gate–Body Leakage Current ($V_{GS}$ = ± 20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2.0 | – | 4.0 | Vdc |
| Temperature Coefficient (Negative) | | | – | 7.0 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 22.5 Adc) | | $R_{DS(on)}$ | – | 0.027 | 0.035 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 45 Adc) | | $V_{DS(on)}$ | – | 1.13 | 2.16 | Vdc |
| ($I_D$ = 22.5 Adc, $T_J$ = 125°C) | | | – | – | 1.53 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 22.5 Adc) | | $g_{FS}$ | 12 | – | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1.0 MHz) | $C_{iss}$ | – | 3480 | 5000 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1240 | 2000 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 315 | 650 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$= 50 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 9.1 Ω) | $t_{d(on)}$ | – | 25 | 50 | ns |
| Rise Time | | $t_r$ | – | 234 | 470 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 83 | 170 | |
| Fall Time | | $t_f$ | – | 116 | 240 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 80 Vdc, $I_D$ = 45 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 106 | 220 | nC |
| | | $Q_1$ | – | 26 | – | |
| | | $Q_2$ | – | 54 | – | |
| | | $Q_3$ | – | 44 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage (Note 1.) | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 1.09 | 1.635 | Vdc |
| | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 1.04 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 45 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 166 | – | ns |
| | | $t_a$ | – | 118 | – | |
| | | $t_b$ | – | 48 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 1.1 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
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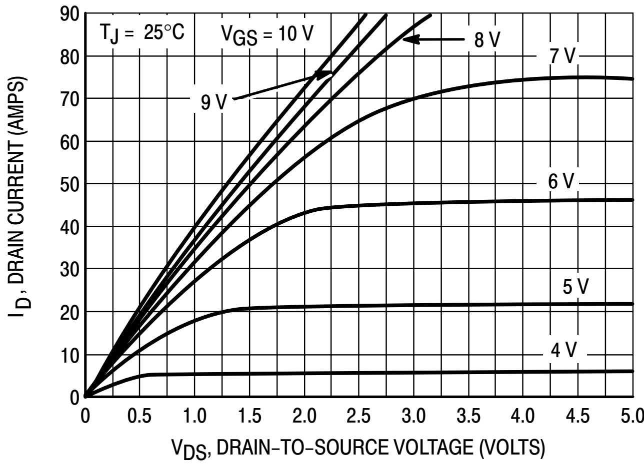
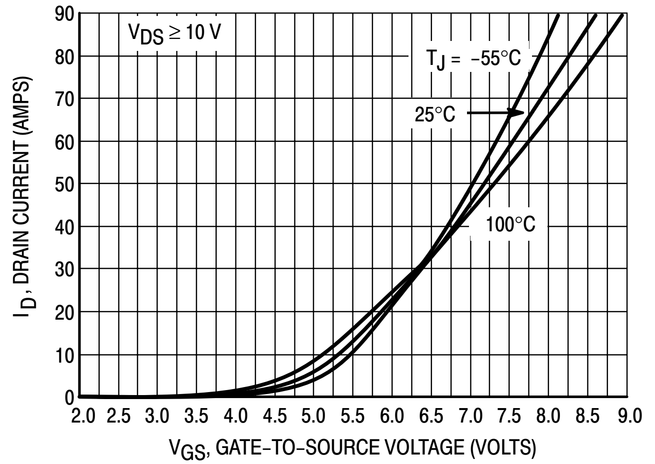



**Figure 1. On–Region Characteristics**

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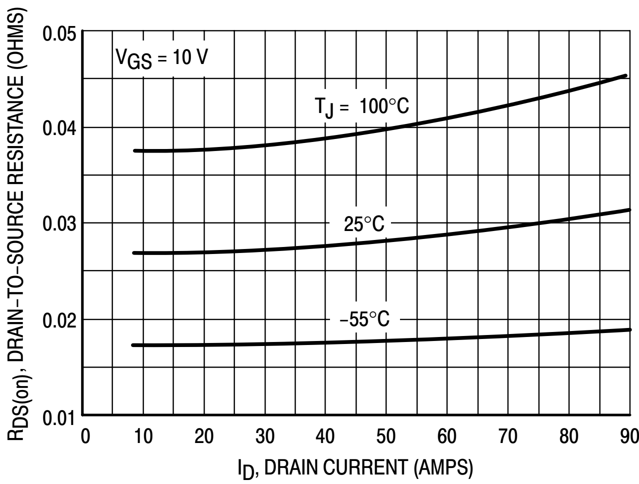



**Figure 3. On–Resistance versus Drain Current and Temperature**

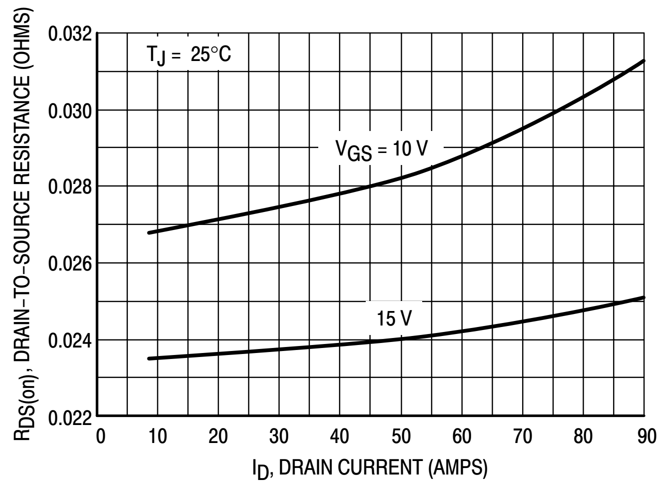
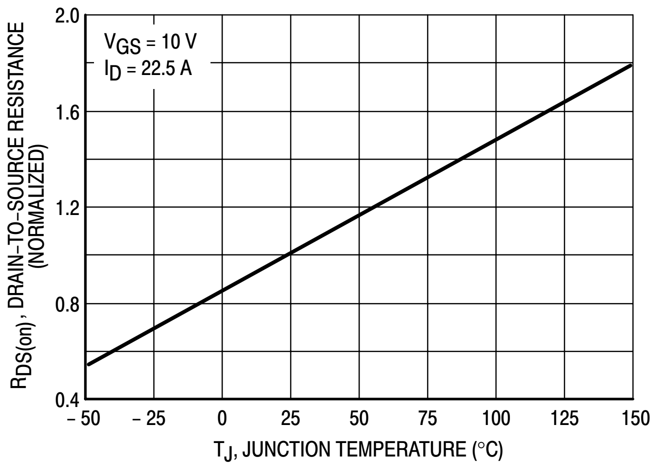



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

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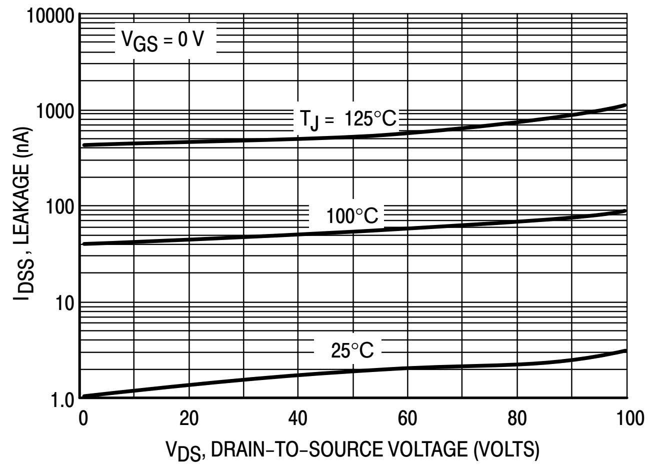


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$t_{d(off)} = R_G\ C_{iss}\ \text{In}\ (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

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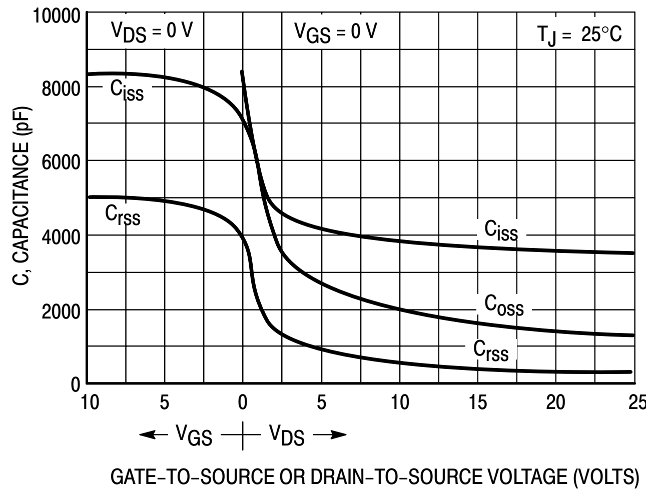


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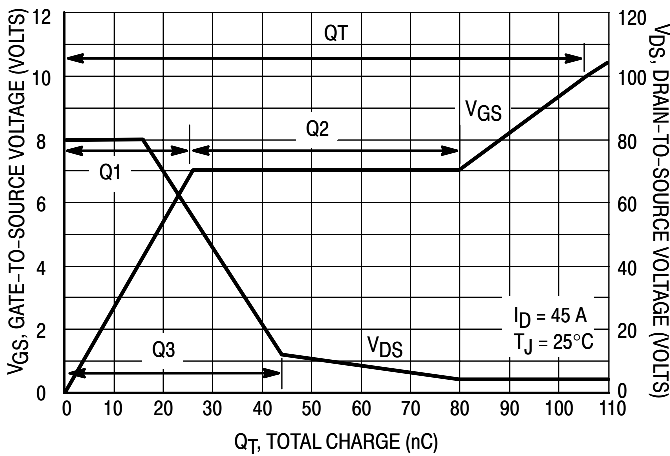



**Figure 8. Gate–To–Source and Drain–To–Source Voltage versus Total Charge**

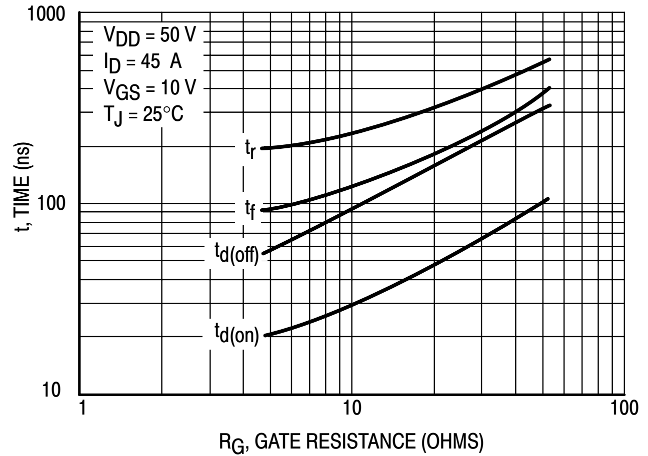
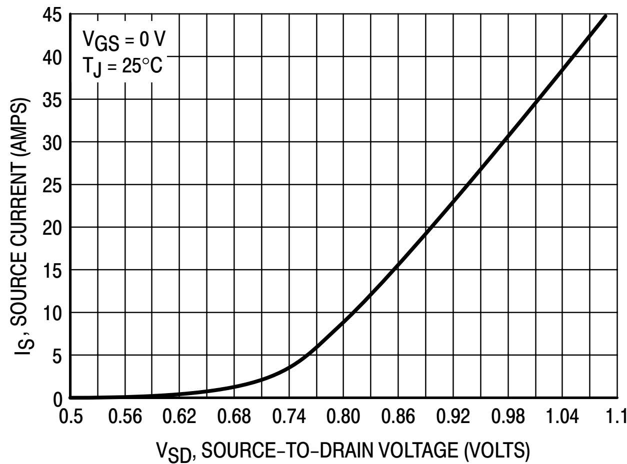



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

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The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 μs. In addition the total power averaged over a complete switching cycle must not exceed $(T_{J(MAX)} - T_C)/(R_{\theta JC})$.

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

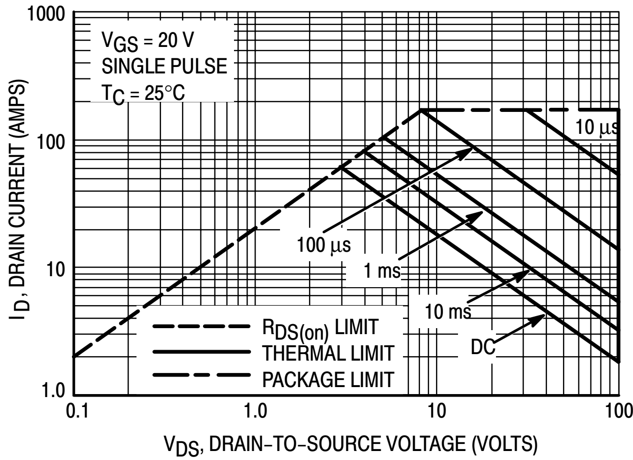



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

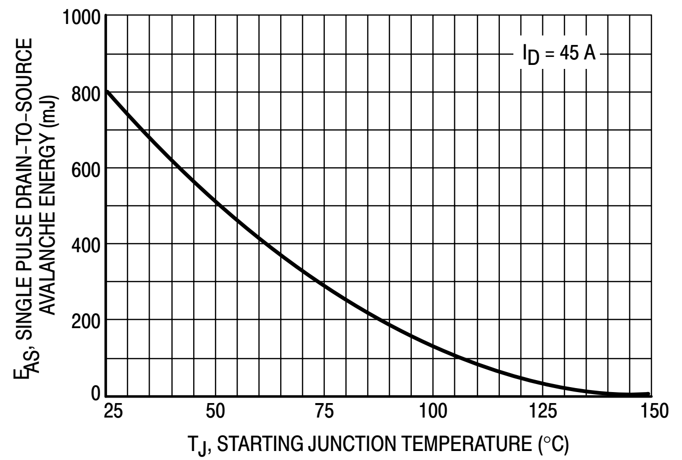



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

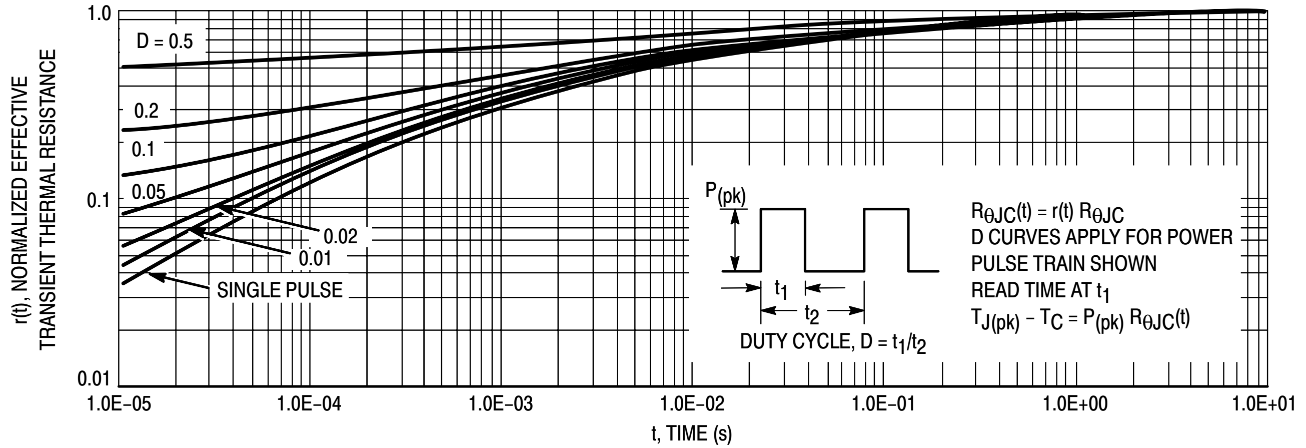



**Figure 13. Thermal Response**

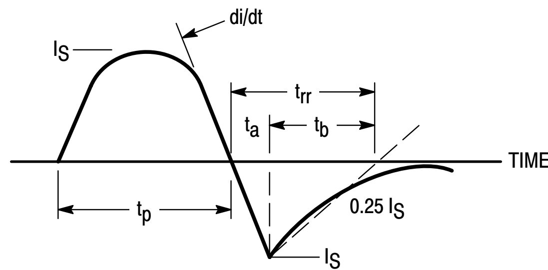



**Figure 14. Diode Reverse Recovery Waveform**

# MTY55N20E

**Preferred Device**

# Power MOSFET
# 55 Amps, 200 Volts

## N–Channel TO–264

**ON Semiconductor™**

**http://onsemi.com**

**55 AMPERES**
**200 VOLTS**
**$R_{DS(on)}$ = 28 mΩ**

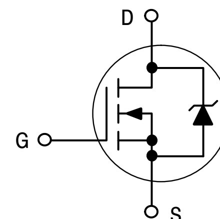
This advanced Power MOSFET is designed to withstand high energy in the avalanche and commutation modes. This new energy efficient design also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters, PWM motor controls, and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

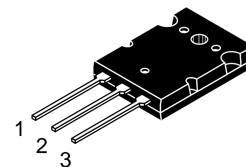
- Avalanche Energy Specified
- Diode is Characterized for Use in Bridge Circuits
- $I_{DSS}$ and $V_{DS(on)}$ Specified at Elevated Temperature

**MAXIMUM RATINGS** ($T_C$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 200 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1 MΩ) | $V_{DGR}$ | 200 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p$ ≤ 10 ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current – Continuous @ $T_C$ = 25°C<br>– Single Pulse ($t_p$ ≤ 10 μs) | $I_D$<br>$I_{DM}$ | 55<br>165 | Adc<br>Apk |
| Total Power Dissipation<br>Derate above 25°C | $P_D$ | 300<br>2.38 | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to 150 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 80 Vdc, $V_{GS}$ = 10 Vdc, Peak $I_L$ = 110 Apk, L = 0.3 mH, $R_G$ = 25 Ω ) | $E_{AS}$ | 3000 | mJ |
| Thermal Resistance – Junction to Case<br>– Junction to Ambient | $R_{\theta JC}$<br>$R_{\theta JA}$ | 0.42<br>40 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds | $T_L$ | 260 | °C |

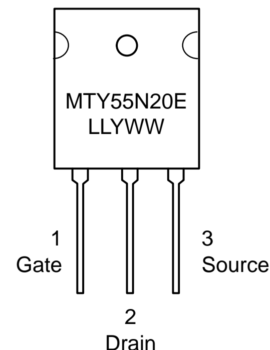
**N–Channel**




**TO–264**
**CASE 340G**
**Style 1**

**MARKING DIAGRAM & PIN ASSIGNMENT**




LL = Location Code
Y = Year
WW = Work Week

**ORDERING INFORMATION**

| Device | Package | Shipping |
|---|---|---|
| MTY55N20E | TO–264 | 25 Units/Rail |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_J$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 250 μA) | | $V_{(BR)DSS}$ | 200 | – | – | Vdc |
| Temperature Coefficient (Positive) | | | – | 250 | – | mV/°C |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc) | | $I_{DSS}$ | – | – | 10 | μAdc |
| ($V_{DS}$ = 200 Vdc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | | – | – | 200 | |
| Gate–Body Leakage Current ($V_{GS}$ = ±20 Vdc, $V_{DS}$ = 0) | | $I_{GSS}$ | – | – | 100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 250 μAdc) | | $V_{GS(th)}$ | 2 | – | 4 | Vdc |
| Threshold Temperature Coefficient (Negative) | | | – | 7 | – | mV/°C |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 27.5 Adc) | | $R_{DS(on)}$ | – | – | 0.028 | Ohm |
| Drain–Source On–Voltage ($V_{GS}$ = 10 Vdc) ($I_D$ = 55 Adc) | | $V_{DS(on)}$ | – | 1.3 | 1.6 | Vdc |
| ($I_D$ = 27.5 Adc, $T_J$ = 125°C) | | | – | – | 1.8 | |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 27.5 Adc) | | $g_{FS}$ | 30 | 37 | – | mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0 Vdc, f = 1 MHz) | $C_{iss}$ | – | 7200 | 10080 | pF |
| Output Capacitance | | $C_{oss}$ | – | 1800 | 2520 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 460 | 920 | |
| **SWITCHING CHARACTERISTICS** (Note 2.) | | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 100 Vdc, $I_D$ = 55 Adc, $V_{GS}$ = 10 Vdc, $R_G$ = 4.7 Ω) | $t_{d(on)}$ | – | 33 | 66 | ns |
| Rise Time | | $t_r$ | – | 200 | 400 | |
| Turn–Off Delay Time | | $t_{d(off)}$ | – | 150 | 300 | |
| Fall Time | | $t_f$ | – | 170 | 340 | |
| Gate Charge (See Figure 8) | ($V_{DS}$ = 160 Vdc, $I_D$ = 55 Adc, $V_{GS}$ = 10 Vdc) | $Q_T$ | – | 245 | 343 | nC |
| | | $Q_1$ | – | 33 | – | |
| | | $Q_2$ | – | 128 | – | |
| | | $Q_3$ | – | 79 | – | |
| **SOURCE–DRAIN DIODE CHARACTERISTICS** | | | | | | |
| Forward On–Voltage | ($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc) | $V_{SD}$ | – | 0.75 | 1.2 | Vdc |
| | ($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc, $T_J$ = 125°C) | | – | 1.1 | – | |
| Reverse Recovery Time (See Figure 14) | ($I_S$ = 55 Adc, $V_{GS}$ = 0 Vdc, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | – | 310 | – | ns |
| | | $t_a$ | – | 220 | – | |
| | | $t_b$ | – | 90 | – | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | – | 4.6 | – | μC |
| **INTERNAL PACKAGE INDUCTANCE** | | | | | | |
| Internal Drain Inductance (Measured from the drain lead 0.25″ from package to center of die) | | $L_D$ | – | 4.5 | – | nH |
| Internal Source Inductance (Measured from the source lead 0.25″ from package to source bond pad) | | $L_S$ | – | 13 | – | nH |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
2. Switching characteristics are independent of operating junction temperature.

## TYPICAL ELECTRICAL CHARACTERISTICS

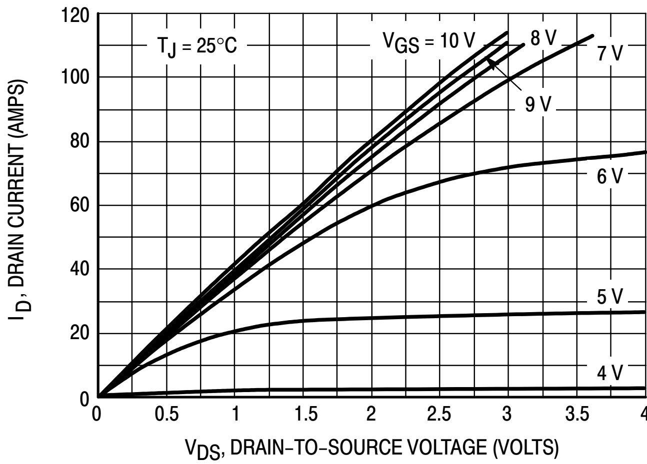



**Figure 1. On–Region Characteristics**

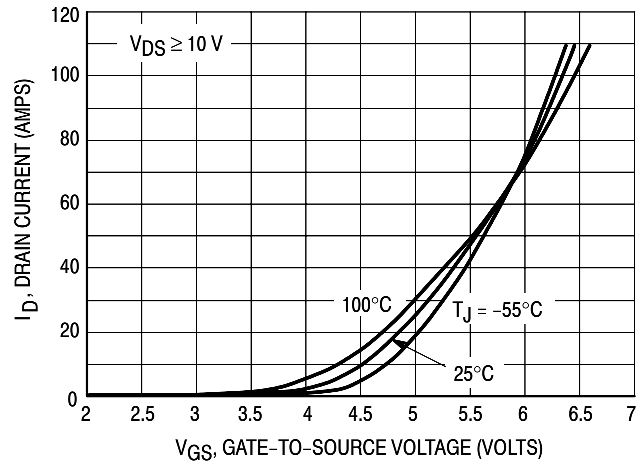



**Figure 2. Transfer Characteristics**

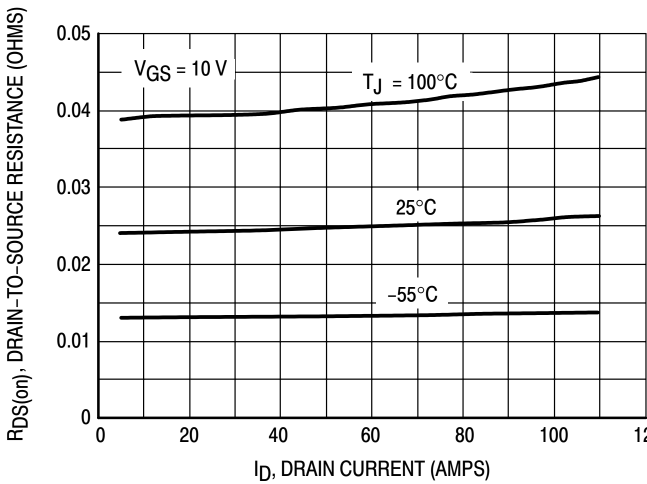



**Figure 3. On–Resistance versus Drain Current and Temperature**

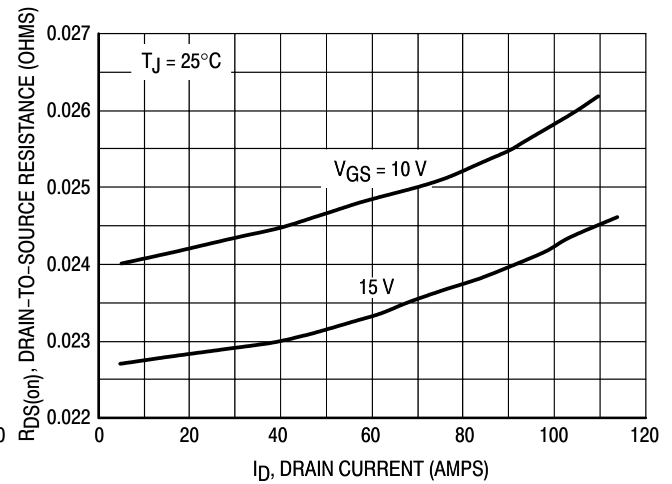



**Figure 4. On–Resistance versus Drain Current and Gate Voltage**

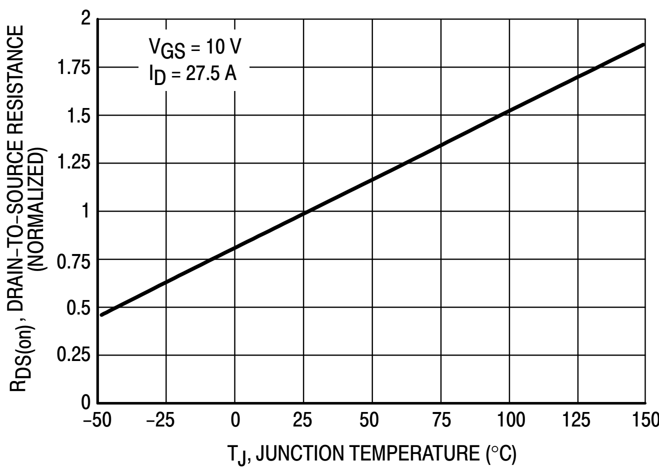



**Figure 5. On–Resistance Variation with Temperature**

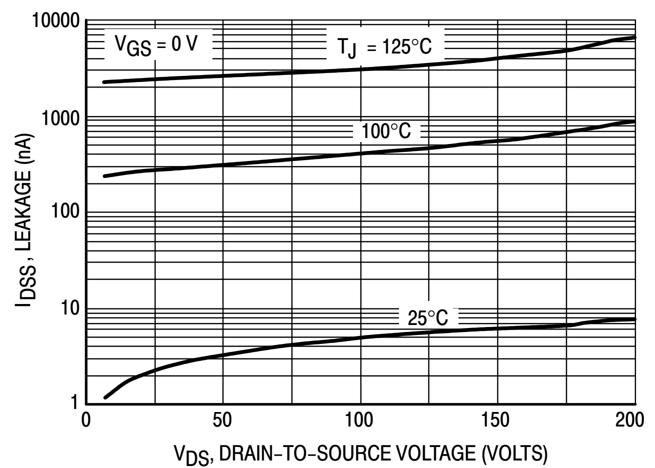



**Figure 6. Drain–To–Source Leakage Current versus Voltage**

## POWER MOSFET SWITCHING

Switching behavior is most easily modeled and predicted by recognizing that the power MOSFET is charge controlled. The lengths of various switching intervals ($\Delta t$) are determined by how fast the FET input capacitance can be charged by current from the generator.

The published capacitance data is difficult to use for calculating rise and fall because drain–gate capacitance varies greatly with applied voltage. Accordingly, gate charge data is used. In most cases, a satisfactory estimate of average input current ($I_{G(AV)}$) can be made from a rudimentary analysis of the drive circuit so that

$t = Q/I_{G(AV)}$

During the rise and fall time interval when switching a resistive load, $V_{GS}$ remains virtually constant at a level known as the plateau voltage, $V_{SGP}$. Therefore, rise and fall times may be approximated by the following:

$t_r = Q_2 \times R_G/(V_{GG} - V_{GSP})$
$t_f = Q_2 \times R_G/V_{GSP}$

where

$V_{GG}$ = the gate drive voltage, which varies from zero to $V_{GG}$
$R_G$ = the gate drive resistance
and $Q_2$ and $V_{GSP}$ are read from the gate charge curve.

During the turn–on and turn–off delay times, gate current is not constant. The simplest calculation uses appropriate values from the capacitance curves in a standard equation for voltage change in an RC network. The equations are:

$t_{d(on)} = R_G \; C_{iss} \; In \; [V_{GG}/(V_{GG} - V_{GSP})]$
$t_{d(off)} = R_G \; C_{iss} \; In \; (V_{GG}/V_{GSP})$

The capacitance ($C_{iss}$) is read from the capacitance curve at a voltage corresponding to the off–state condition when calculating $t_{d(on)}$ and is read at a voltage corresponding to the on–state when calculating $t_{d(off)}$.

At high switching speeds, parasitic circuit elements complicate the analysis. The inductance of the MOSFET source lead, inside the package and in the circuit wiring which is common to both the drain and gate current paths, produces a voltage at the source which reduces the gate drive current. The voltage is determined by Ldi/dt, but since di/dt is a function of drain current, the mathematical solution is complex. The MOSFET output capacitance also complicates the mathematics. And finally, MOSFETs have finite internal gate resistance which effectively adds to the resistance of the driving source, but the internal resistance is difficult to measure and, consequently, is not specified.

The resistive switching time variation versus gate resistance (Figure 9) shows how typical switching performance is affected by the parasitic circuit elements. If the parasitics were not present, the slope of the curves would maintain a value of unity regardless of the switching speed. The circuit used to obtain the data is constructed to minimize common inductance in the drain and gate circuit loops and is believed readily achievable with board mounted components. Most power electronic loads are inductive; the data in the figure is taken with a resistive load, which approximates an optimally snubbed inductive load. Power MOSFETs may be safely operated into an inductive load; however, snubbing reduces switching losses.

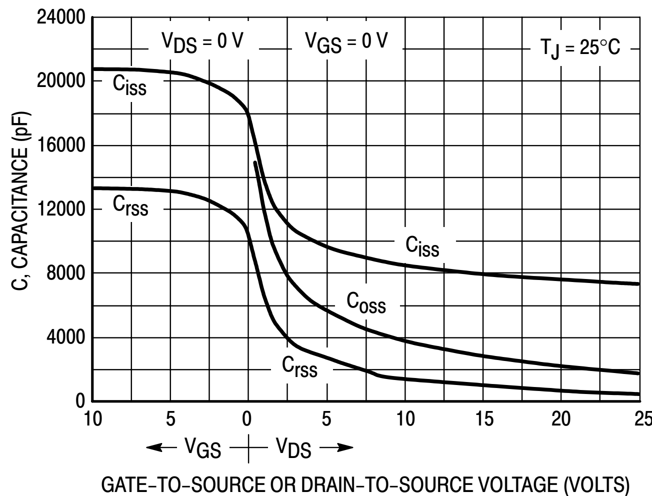



**Figure 7. Capacitance Variation**

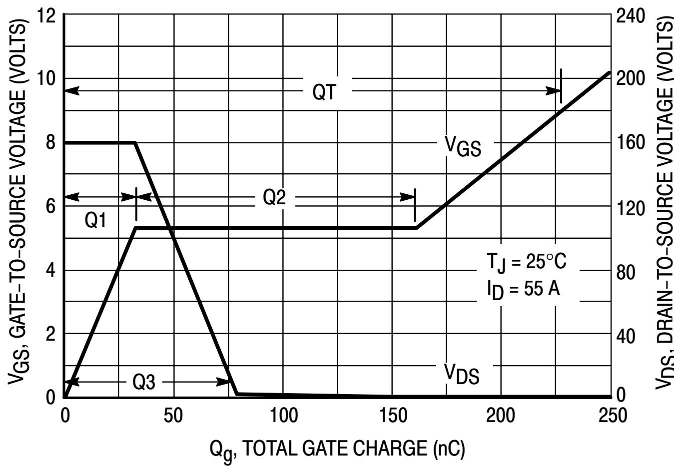



**Figure 8. Gate Charge versus Gate–to–Source Voltage**

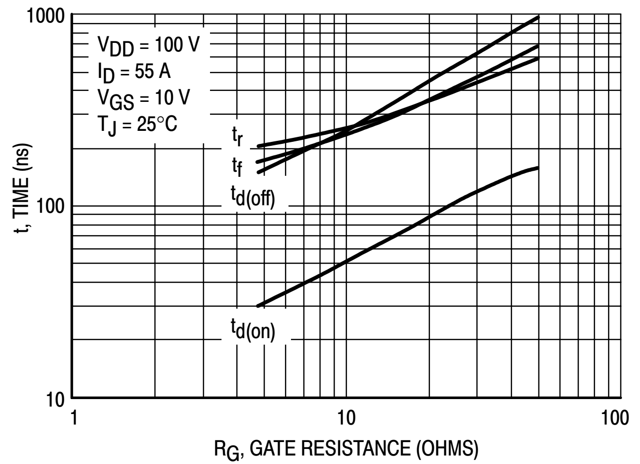



**Figure 9. Resistive Switching Time Variation versus Gate Resistance**

## DRAIN–TO–SOURCE DIODE CHARACTERISTICS

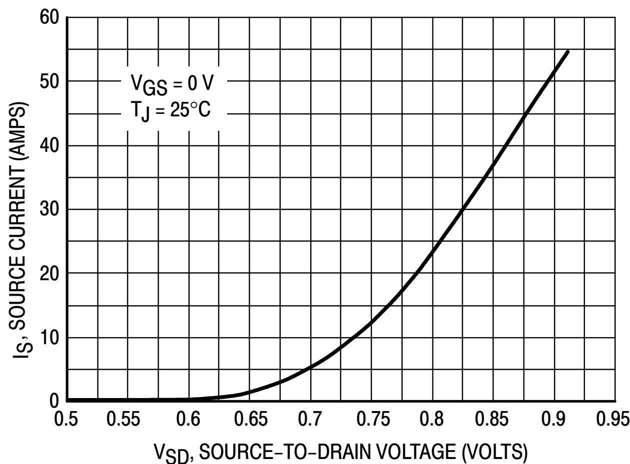



**Figure 10. Diode Forward Voltage versus Current**

## SAFE OPERATING AREA

The Forward Biased Safe Operating Area curves define the maximum simultaneous drain–to–source voltage and drain current that a transistor can handle safely when it is forward biased. Curves are based upon maximum peak junction temperature and a case temperature ($T_C$) of 25°C. Peak repetitive pulsed power limits are determined by using the thermal response data in conjunction with the procedures discussed in AN569, “Transient Thermal Resistance–General Data and Its Use.”

Switching between the off–state and the on–state may traverse any load line provided neither rated peak current ($I_{DM}$) nor rated voltage ($V_{DSS}$) is exceeded and the transition time ($t_r$,$t_f$) do not exceed 10 µs. In addition the total power averaged over a complete switching cycle must not exceed ($T_{J(MAX)} - T_C$)/($R_{\theta JC}$).

A Power MOSFET designated E–FET can be safely used in switching circuits with unclamped inductive loads. For reliable operation, the stored energy from circuit inductance dissipated in the transistor while in avalanche must be less than the rated limit and adjusted for operating conditions differing from those specified. Although industry practice is to rate in terms of energy, avalanche energy capability is not a constant. The energy rating decreases non–linearly with an increase of peak current in avalanche and peak junction temperature.

Although many E–FETs can withstand the stress of drain–to–source avalanche at currents up to rated pulsed current ($I_{DM}$), the energy rating is specified at rated continuous current ($I_D$), in accordance with industry custom. The energy rating must be derated for temperature as shown in the accompanying graph (Figure 12). Maximum energy at currents below rated continuous $I_D$ can safely be assumed to equal the values indicated.

## SAFE OPERATING AREA

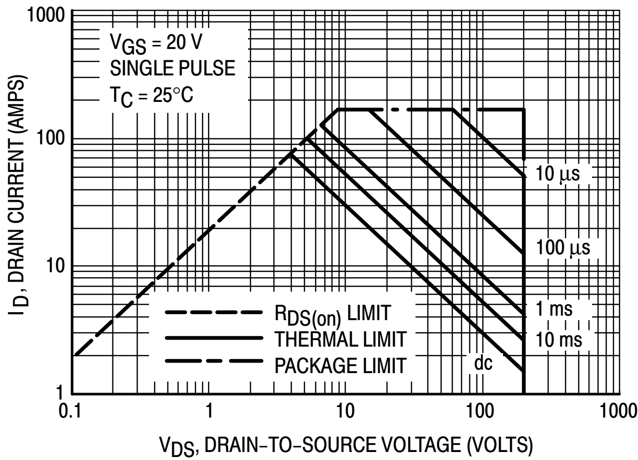



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

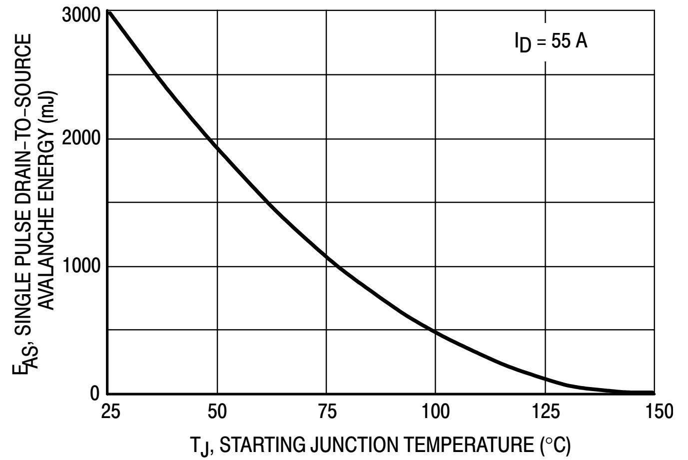



**Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature**

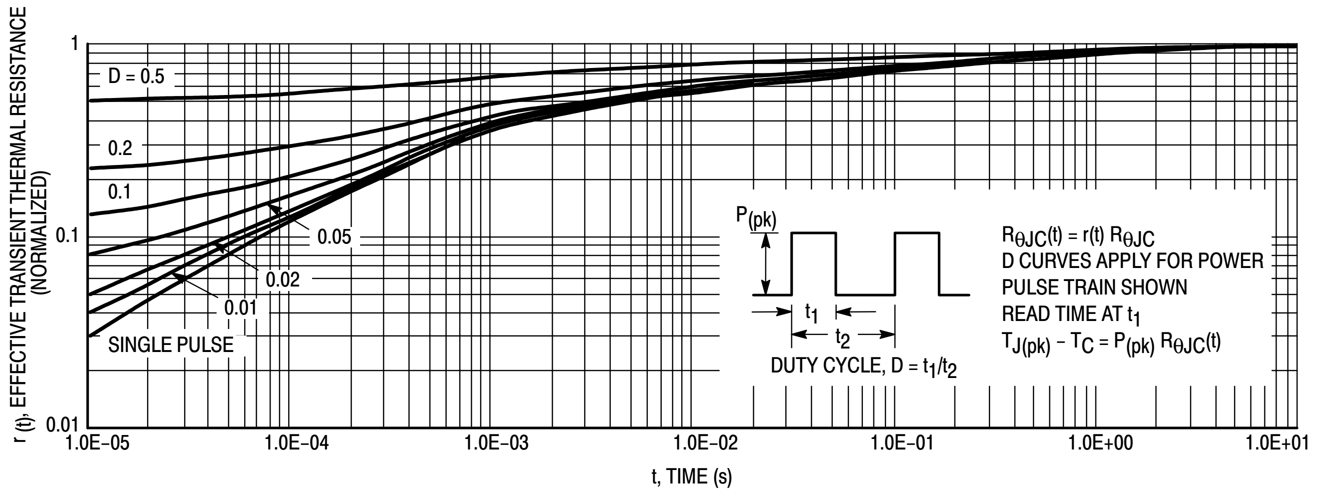



**Figure 13. Thermal Response**

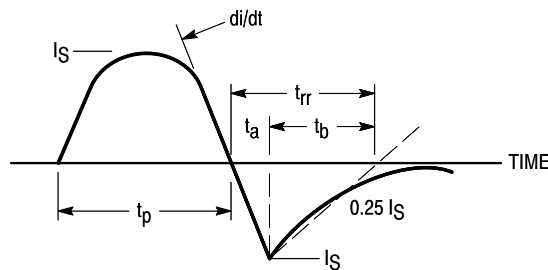



**Figure 14. Diode Reverse Recovery Waveform**

# VN0300L

**Preferred Device**

# Small Signal MOSFET 200 mAmps, 60 Volts

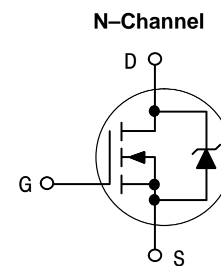
## N–Channel TO–92

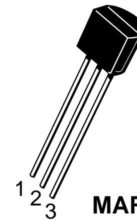
**ON Semiconductor™**

**http://onsemi.com**

**200 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 1.2 Ω**

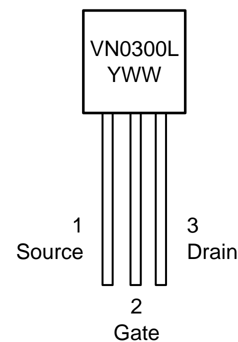
**N–Channel**




**TO–92**
**CASE 29**
**Style 22**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | V |
| Drain–Gate Voltage | $V_{DGR}$ | 60 | V |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq 50\ \mu s$) | $V_{GS}$<br>$V_{GSM}$ | ± 20<br>± 40 | Vdc<br>Vpk |
| Continuous Drain Current | $I_D$ | 200 | mA |
| Pulsed Drain Current | $I_{DM}$ | 500 | mA |
| Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 350<br>2.8 | mW<br>mW/°C |
| Operating and Storage Temperature | $T_J$, $T_{stg}$ | – | °C |

### THERMAL CHARACTERISTICS

| Characteristics | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 312.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/16” from case for 10 seconds | $T_L$ | 300 | °C |

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| VN0300L | TO–92 | 1000 Units/Box |
| VN0300LRLRA | TO–92 | 2000 Tape & Reel |
| VN0300LRLRE | TO–92 | 2000 Tape & Reel |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | |
| Drain–Source Breakdown Voltage ($V_{DS}$ = 0, $I_D$ = 10 μA) | $V_{(BR)DSS}$ | 30 | – | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | | | μA |
| ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0) | | – | 10 | |
| ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0, $T_A$ = 125°C) | | – | 500 | |
| Gate–Body Leakage ($V_{DS}$ = 0, $V_{GS}$ = ±30 V) | $I_{GSS}$ | – | ±100 | nA |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | $V_{GS(th)}$ | 0.8 | 2.5 | V |
| On–State Drain Current (Note 1.) ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | $I_{D(on)}$ | 1.0 | – | A |
| Drain–Source On Resistance (Note 1.) | $r_{DS(on)}$ | | | Ω |
| ($V_{GS}$ = 5.0 V, $I_D$ = 0.3 A) | | – | 3.3 | |
| ($V_{GS}$ = 10 V, $I_D$ = 1.0 A) | | – | 1.2 | |
| Forward Transconductance (Note 1.) ($V_{DS}$ = 10 V, $I_D$ = 0.5 A) | $g_{fs}$ | 200 | – | mS |
| **DYNAMIC CHARACTERISTICS** | | | | |
| Input Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 100 | pF |
| Output Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{oss}$ | – | 95 | pF |
| Reverse Transfer Capacitance ($V_{DS}$ = 15 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{rss}$ | – | 25 | pF |
| **SWITCHING CHARACTERISTICS** | | | | |
| Turn–On Time ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 A, $R_L$ = 24 Ω, RG = 25 Ω) | $t_{on}$ | – | 30 | ns |
| Turn–Off Time ($V_{DD}$ = 25 Vdc, $I_D$ = 1.0 A, $R_L$ = 24 Ω, RG = 25 Ω) | $t_{off}$ | – | 30 | ns |

1. Pulse Test; Pulse Width < 300 μs, Duty Cycle ≤ 2.0%.

# VN2222LL

**Preferred Device**

# Small Signal MOSFET 150 mAmps, 60 Volts

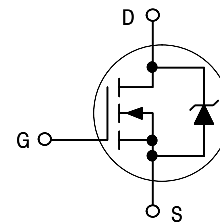
## N–Channel TO–92

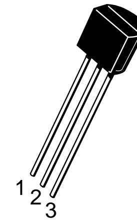
**ON Semiconductor**™

**http://onsemi.com**

**150 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 7.5 Ω**

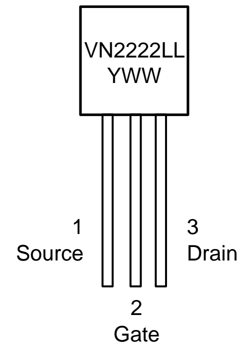
**N–Channel**




**TO–92**
**CASE 29**
**Style 22**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 60 | Vdc |
| Drain–Gate Voltage ($R_{GS}$ = 1.0 MΩ) | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le 50\ \mu s$) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±20<br>±40 | <br>Vdc<br>Vpk |
| Drain Current<br>– Continuous<br>– Pulsed | <br>$I_D$<br>$I_{DM}$ | <br>150<br>1000 | mAdc |
| Total Power Dissipation @ $T_A$ = 25°C<br>Derate above 25°C | $P_D$ | 400<br>3.2 | mW<br>mW/°C |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +150 | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 312.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds | $T_L$ | 300 | °C |

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 1393 of this data sheet.

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 μAdc) | | $V_{(BR)DSS}$ | 60 | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0)<br>($V_{DS}$ = 48 Vdc, $V_{GS}$ = 0, $T_J$ = 125°C) | | $I_{DSS}$ | –<br>– | 10<br>500 | μAdc |
| Gate–Body Leakage Current, Forward ($V_{GSF}$ = 30 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | – | –100 | nAdc |
| **ON CHARACTERISTICS** (Note 1.) | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mAdc) | | $V_{GS(th)}$ | 0.6 | 2.5 | Vdc |
| Static Drain–Source On–Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 0.5 Adc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 0.5 Vdc, $T_C$ = 125°C) | | $r_{DS(on)}$ | –<br>– | 7.5<br>13.5 | Ω |
| Drain–Source On–Voltage ($V_{GS}$ = 5.0 Vdc, $I_D$ = 200 mAdc)<br>($V_{GS}$ = 10 Vdc, $I_D$ = 500 mAdc) | | $V_{DS(on)}$ | –<br>– | 1.5<br>3.75 | Vdc |
| On–State Drain Current ($V_{GS}$ = 10 Vdc, $V_{DS} \geq 2.0 V_{DS(on)}$) | | $I_{D(on)}$ | 750 | – | mA |
| Forward Transconductance ($V_{DS}$ = 10 Vdc, $I_D$ = 500 mAdc) | | $g_{fs}$ | 100 | – | μmhos |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 60 | pF |
| Output Capacitance | | $C_{oss}$ | – | 25 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 5.0 | |
| **SWITCHING CHARACTERISTICS** (Note 1.) | | | | | |
| Turn–On Delay Time | ($V_{DD}$ = 15 Vdc, $I_D$ = 600 mA, $R_{gen}$ = 25 Ω, $R_L$ = 23 Ω) | $t_{on}$ | – | 10 | ns |
| Turn–Off Delay Time | | $t_{off}$ | – | 10 | |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

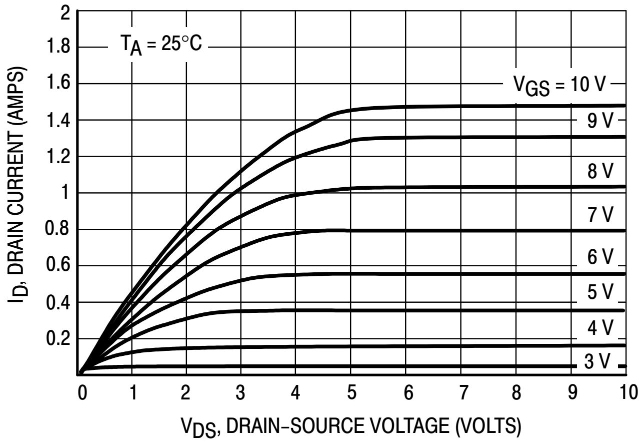



**Figure 1. Ohmic Region**

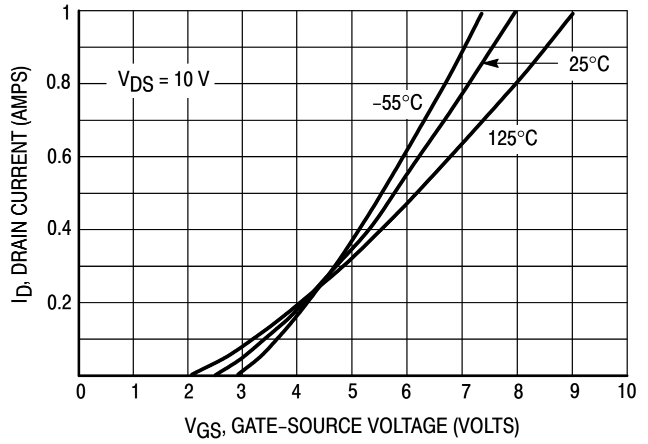



**Figure 2. Transfer Characteristics**

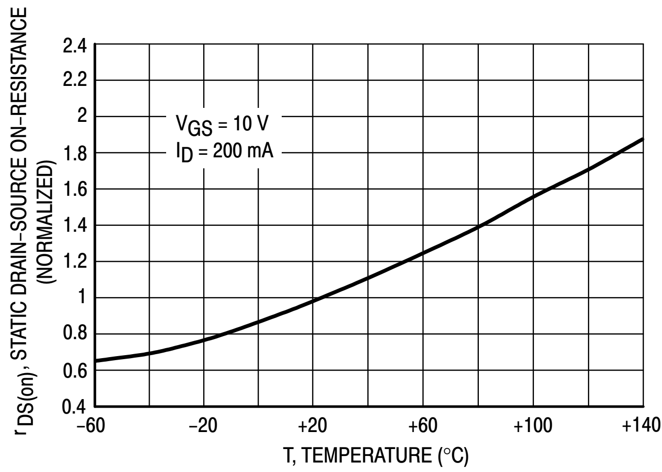



**Figure 3. Temperature versus Static Drain–Source On–Resistance**

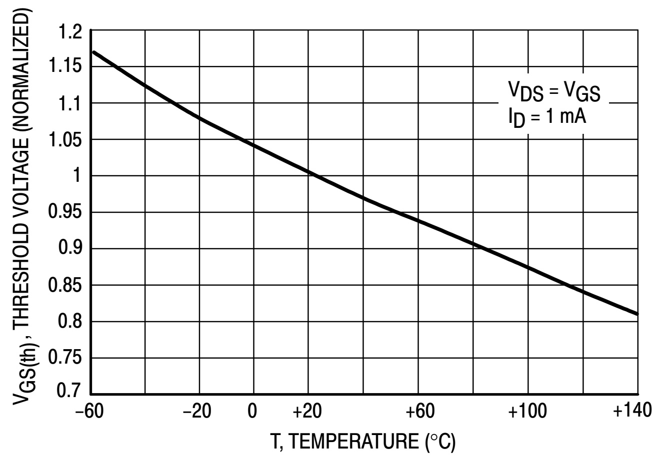



**Figure 4. Temperature versus Gate Threshold Voltage**

## ORDERING INFORMATION

| Device | Package | Shipping |
| --- | --- | --- |
| VN2222LL | TO–92 | 1000 Unit/Box |
| VN2222LLRL | TO–92 | 2000 Tape & Reel |
| VN2222RLRA | TO–92 | 2000 Tape & Reel |
| VN2222RLRM | TO–92 | 1000 Unit/Box |

# VN2406L

**Preferred Device**

# Small Signal MOSFET 200 mAmps, 240 Volts

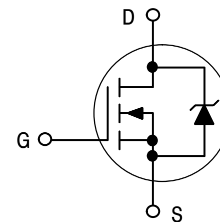
## N–Channel TO–92

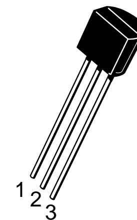
**ON Semiconductor™**

**http://onsemi.com**

**200 mAMPS**
**240 VOLTS**
**$R_{DS(on)}$ = 6 Ω**

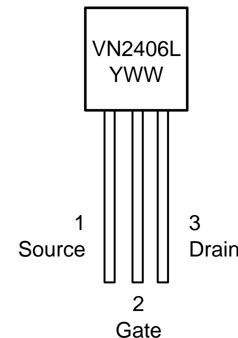
**N–Channel**




**TO–92**
**CASE 29**
**Style 22**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 240 | Vdc |
| Drain–Gate Voltage | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \le 50$ µs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Continuous Drain Current | $I_D$ | 200 | mAdc |
| Pulsed Drain Current | $I_{DM}$ | 500 | mAdc |
| Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 350<br>2.8 | mW<br>mW/°C |
| Operating and Storage Temperature | $T_J$, $T_{stg}$ | – | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 312.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds | $T_L$ | 300 | °C |

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| VN2406L | TO–92 | 1000 Units/Box |
| VN2406LZL1 | TO–92 | 2000 Ammo Pack |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 μA) | $V_{(BR)DSS}$ | 240 | – | Vdc |
| Zero Gate Voltage Drain Current<br>($V_{DS}$ = 120 Vdc, $V_{GS}$ = 0)<br>($V_{DS}$ = 120 Vdc, $V_{GS}$ = 0, $T_A$ = 125°C) | $I_{DSS}$ | <br>–<br>– | <br>10<br>500 | μAdc |
| Gate– Body Leakage ($V_{DS}$ = 0, $V_{GS}$ = ±15 V) | $I_{GSS}$ | – | ±100 | nAdc |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | $V_{GS(th)}$ | 0.8 | 2.0 | Vdc |
| On–State Drain Current (Note 1.) ($V_{GS}$ = 10 V, $V_{DS}$ ≥ 2.0 $V_{DS(on)}$) | $I_{D(on)}$ | 1.0 | – | Adc |
| Drain–Source On Resistance (Note 1.)<br>($V_{GS}$ = 2.5 V, $I_D$ = 0.1 A)<br>($V_{GS}$ = 10 V, $I_D$ = 0.5 A) | $r_{DS(on)}$ | <br>–<br>– | <br>10<br>6.0 | Ω |
| Forward Transconductance (Note 1.) ($V_{DS}$ = 10 V, $I_D$ = 0.5 A) | $g_{fs}$ | 300 | – | mS |

**DYNAMIC CHARACTERISTICS**

| Characteristic | Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 125 | pF |
| Output Capacitance | | $C_{oss}$ | – | 50 | pF |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 20 | pF |

**SWITCHING CHARACTERISTICS**

| Characteristic | Conditions | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| Turn–On Time | ($V_{DD}$ = 60 Vdc, $I_D$ = 0.4 A, $R_L$ = 150 Ω, $R_G$ = 25 Ω) | $t_{(on)}$ | – | 8.0 | ns |
| | | $t_{(r)}$ | – | 8.0 | ns |
| Turn–Off Time | | $t_{(off)}$ | – | 23 | ns |
| | | $t_{(f)}$ | – | 34 | ns |

1. Pulse Test; Pulse Width < 300 μs, Duty Cycle ≤ 2.0%.

# VN2410L

**Preferred Device**

# Small Signal MOSFET 200 mAmps, 240 Volts

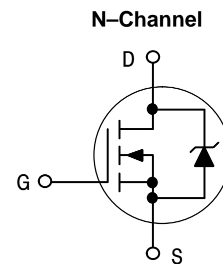
## N–Channel TO–92

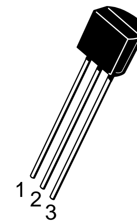
**ON Semiconductor™**

**http://onsemi.com**

**200 mAMPS**
**60 VOLTS**
**$R_{DS(on)}$ = 10 Ω**

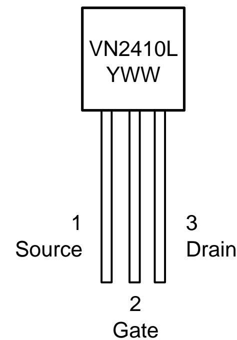
**N–Channel**




**TO–92**
**CASE 29**
**Style 22**

**MARKING DIAGRAM & PIN ASSIGNMENT**




Y = Year
WW = Work Week

### MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–Source Voltage | $V_{DSS}$ | 240 | Vdc |
| Drain–Gate Voltage | $V_{DGR}$ | 60 | Vdc |
| Gate–Source Voltage<br>– Continuous<br>– Non–repetitive ($t_p \leq 50$ μs) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>± 20<br>± 40 | <br>Vdc<br>Vpk |
| Continuous Drain Current | $I_D$ | 200 | mAdc |
| Pulsed Drain Current | $I_{DM}$ | 500 | mAdc |
| Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 350<br>2.8 | mW<br>mW/°C |
| Operating and Storage Temperature | $T_J$, $T_{stg}$ | – | °C |

### THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| Thermal Resistance, Junction to Ambient | $R_{\theta JA}$ | 312.5 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, 1/16″ from case for 10 seconds | $T_L$ | 300 | °C |

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| VN2410L | TO–92 | 1000 Units/Box |
| VN2410LZL1 | TO–92 | 2000 Ammo Pack |

**Preferred** devices are recommended choices for future use and best overall value.

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**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | |
| Drain–Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 100 µA) | | $V_{(BR)DSS}$ | 240 | – | Vdc |
| Zero Gate Voltage Drain Current ($V_{DS}$ = 120 Vdc, $V_{GS}$ = 0) ($V_{DS}$ = 120 Vdc, $V_{GS}$ = 0, $T_A$ = 125°C) | | $I_{DSS}$ | –<br>– | 10<br>500 | µAdc |
| Gate– Body Leakage ($V_{DS}$ = 0, $V_{GS}$ = ±15 V) | | $I_{GSS}$ | – | ±100 | nAdc |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | | $V_{GS(th)}$ | 0.8 | 2.0 | Vdc |
| On–State Drain Current (Note 1.) ($V_{GS}$ = 10 V, $V_{DS}$ ≥ 2.0 $V_{DS(on)}$) | | $I_{D(on)}$ | 1.0 | – | Adc |
| Drain–Source On Resistance (Note 1.) ($V_{GS}$ = 2.5 V, $I_D$ = 0.1 A) ($V_{GS}$ = 10 V, $I_D$ = 0.5 A) | | $r_{DS(on)}$ | –<br>– | 10<br>10 | Ω |
| Forward Transconductance (Note 1.) ($V_{DS}$ = 10 V, $I_D$ = 0.5 A) | | $g_{fs}$ | 300 | – | mS |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 Vdc, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | – | 125 | pF |
| Output Capacitance | | $C_{oss}$ | – | 50 | pF |
| Reverse Transfer Capacitance | | $C_{rss}$ | – | 20 | pF |
| **SWITCHING CHARACTERISTICS** | | | | | |
| Turn–On Time | ($V_{DD}$ = 60 Vdc, $I_D$ = 0.4 A, $R_L$ = 150 Ω, $R_G$ = 25 Ω) | $t_{(on)}$ | – | 8.0 | ns |
| | | $t_{(r)}$ | – | 8.0 | ns |
| Turn–Off Time | | $t_{(off)}$ | – | 23 | ns |
| | | $t_{(f)}$ | – | 34 | ns |

1. Pulse Test; Pulse Width < 300 µs, Duty Cycle ≤ 2.0%.

# CHAPTER 2
# MOSFET Application Note Abstracts

**AN1040 – Mounting Considerations for Power Semiconductors**

The operating environment is a vital factor in setting current and power ratings of a semiconductor device. Reliability is increased considerably for relatively small reductions in junction temperature. Faulty mounting not only increases the thermal gradient between the device and its heat sink, but can also cause mechanical damage. This comprehensive note shows correct and incorrect methods of mounting all types of discrete packages, and discusses methods of thermal system evaluation.

**AN1083 – Basic Thermal Management of Power Semiconductors**

Switching audio amplifiers were impractical before the availability of complementary Power MOSFETs. Now, gate drive circuitry is simpler than for bipolar transistors, and the MOS devices operate more efficiently at higher frequencies. This detailed discussion of switching amplifier design is supported by a 72W Class D circuit.

**AN1090 – Understanding and Predicting Power MOSFET Switching Behavior**

SPICE is a user–friendly, general–purpose circuit simulation program for non–linear DC, non–linear transient and linear AC analysis. It is now available in various commmercial versions for use on personnel computers. ON and LAAS–CNRS Research Laboratory have bult a TMOS Power MOSFET library to simplify power dissipation simulation using SPICE. This note describes how to use the library; the physics of the Power MOSFET; the implementation of the model within SPICE; the method of extracting the parameters for the library; and a comparison of practical and simulated characteristics.

**AN1102 – Interfacing Power MOSFETs to Logic Devices**

Most popular power MOSFETs need 10 volts of gate drive to support their maximum drain current. This creates problems when attempting to drive from 5V logic. The new logic level power MOSFETs solve some but not all of the problems. This note discusses easy methods of directly interfacing both types of MOSFET to TTL and CMOS logic, and to microprocessors such as the M68HC11. Discusses a method of calculating switching times, to minimize switching losses, and stresses the significance of logic power supply variations.

**AN1317 – High–Current DC Motor Drive Uses Low On–Resistance Surface Mount MOSFETs**

Surface mount technology have often been used in controllers for small disk drive motors with peak currents of 1 or 2 amps. Now the availability of low ON–resistance, surface mount power MOSFETs has increased the current handling capability of surface mount technology. This application note presents a 5 amp DC motor drive board (DEVB148) using all surface mount components apart from the filter capacitor. It features a cycle–by–cycle current limit and is intended for direct control from a microcontroller.

**AN1319 – Design Considerations for a Low Voltage N–Channel H–Bridge Motor Drive**

Complementary MOSFET half–bridges are commonly used in low voltage motor drives to simplify gate drive design. However, the P–channel FET in the half–bridge usually has higher ON–resistance or is larger and more expensive then the N–channel half–bridge, which uses silicon more efficiently and minimizes cost and conduction losses. The trade–off is usually a more complex gate drive; this note looks at ways of minimizing gate drive complexity, and also discusses diode snap, shoot–through current and general design considerations. A design is implemented in the dEVB151 development board.

**AN1520 – HDTMOS POWER MOSFETs Excel in Synchronous Rectifier Applications**

The new HDTMOS technology combines VLSI techniques with the ruggedness of vertical power structures to obtain increased cell density and to provide devices with lower overall on–resistance. The reverse recovery characteristic of the parasitic body diode is also faster than in MOSFETs that use conventional technologies. This note examines the advantages of using HDTMOS transistors as synchronous rectifiers in a high power buck converter, and in a 5V DC to 3.3V DC buck converter, in order to increase circuit performance and efficiency while minimizing parts count.

**AN1541/D – Introduction to insulated Gate Bipolar Transistors**

The ideal switch for use in power conversion applications would have zero voltage drop in the ON state, infinite resistance in the OFF state, would switch with infinite speed and not need any power to make it operate. IN practice, the designer must make a compromise and choose a device that suits the application with minimal loss of efficiency. Combining the low conduction losses of a BJT with the switching speed of a power MOSFET would create an optimal solid state switch. The insulated Gate Bipolar Transistor (IGBT) offers a combination of these attributes. This note explains how it is made, how it works, and how it compares with BJTs and power MOSFETs.

**AN1570 – Basic Semiconductor Thermal Measurement**

This application note provides basic information about power semiconductor thermal parameters, how they are measured, and how they are used. The intention is to enable the reader to better describe power semiconductors and to answer many common questions relating to their power handling capability. Four key topics are covered: Understanding basic semiconductor thermal parameters; Semiconductor thermal test equipment; Thermal parameter test procedures; Using thermal parameters to solve frequently asked thermal questions.

**AN211A – Field Effect Transistors in Theory and Practice**

There are two types of field–effect transistor: the Junction Field–Effect Transistor (JFET) and the Metal Oxide Semiconductor Field–Effect Transistor (MOSFET). The principles on which these devices operate are very similar, the main difference being in the method by which the control element is made. This difference, however, results in a considerable difference in device characteristics and necessitates different approaches in circuit design.

**AN220 – FETs in Chopper and Analog Switching Circuits**

The author's discussion begins with elementary chopper and analog switch characteristics, explores fully the considerations required for conventional and FET chopper and anlog switch design, and finishes with specific FET circuit examples.

**AN861 – Power Transistor Safe Operating Area: Special Considerations for Motor Drives**

Motor drives present a unique set of safe operating area conditions for power output transistors. Starting with the basics of forward and reverse safe operating area, considerations unique to motor drives are discussed. The industrial motor drive application is sufficiently different from the electronics uses of power transistors that a new safe operating area specification has been developed. It is called overload safe operating area (OSLOA). The concept and that data sheet curves that go with it are presented.

**AN873 – Understanding Power Transistor Dynamic Behavior: dv/dt Effects on Switching RBSOA**

Power transistor dynamic behavior can be affected to a large extent by dv/dt limitations. A look at the internal workings of the transistor readily shows how these limitations arise. A simple circuit model is developed which reproduces the behavior of power transistors in dv/dt–limited modes of operation. Experience with the model gives some guidelines for minimizing dv/dt limitations in practical circuits.

**AN875 – Power Transistor Safe Operating Area: Special Considerations for Switching Power Supplies**

The purpose of this application note is to take a look at some of the more subtle aspects of how stress imposed by the power supply relates to transistor safe operating area, and to differentiate those stresses that the transistor can handle from those it cannot. In order to provide a proper foundation, special considerations are preceded by a review of forward bias safe operating area.

**AN876 – Using Power MOSFETs in Stepping Motor Control**

Stepping Motor control techniques and circuits utilizing Power MOSFETs driven from CMOS Integrated Circuits are discussed. The techniques described are shift register phase generation, comparator switched current limiting, utilization of synchronous rectification, transient current suppression by use of the Power FET transfer characteristic, and the transient voltage protection requirements of the Power FET. The techniques are presented as components for an 88% efficient stepping motor drive circuit; however they are also applicable to other power control tasks.

**AN913 – Designing with TMOS Power MOSFETs**

Clearly, the advantages and disadvantages that the power MOSFET gives technology are its specific realm of usefulness. Some designers also favor the power MMOSFET because of its extended FBSOA or its other more subtle advantages. The most common considerations that designers should be aware of when designing with TMOS power MOSFETs are outlined and explained here.

**AN918 – Paralleling Power MOSFETs in Switching Applications**

The present TDT series of application notes are updated in this note with a more detailed analysis and design guide for TMOS power MOSFET parallel applications to account for device–to–device parameter

### AN929 – Insuring Reliable Performance from Power MOSFETs

Due to their many unique advantages, power MOSFETs are being used in an increasing number of applications. To aid the circuit designer in developing reliable power MOSFET circuits, this application note examines six potential problem areas and offers suggestions for eliminating or minimizing problems in each area. In addition, as an aid to the many designers who are using power MOSFETs in switched–mode power supplies, this note includes a section on improving switching power supply circuits.

### EB125 – Testing Power MOSFET Gate Charge

Most power MOSFET manufacturers now specify Gate Charge, as well as Input Capacitance, as an indication of the drive current required to turn on the device. The data can be useful in predicting switching speeds and drive losses. Commercially available gate charge test equipment is not yet widely used, and this simple tester for both N and P–channel devices is a practical alternative for smaller users.

### EB131 – Curve Tracer Measurement Techniques for Power MOSFETs

Most curve tracers are designed to measure the parameters of bipolar transistors, but because of similarities in their characteristics, the same techniques can also be used to measure the parameters of power MOSFETs. This bulletin explains how, with particular reference to the Tektronix 370A Curve Tracer.

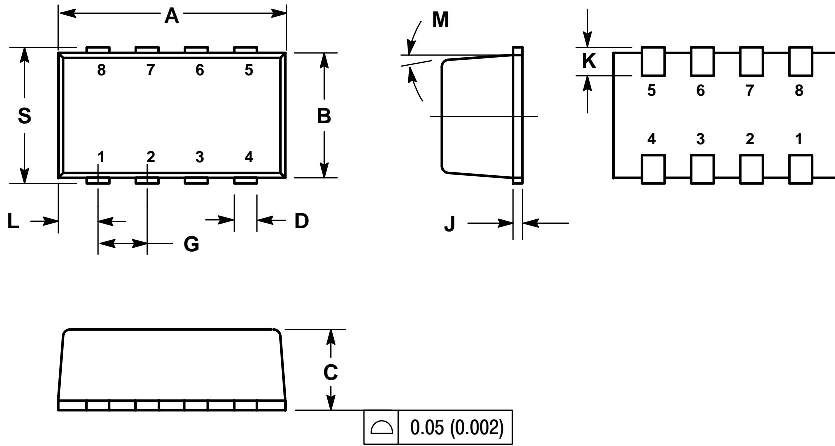
### EB201 – High Cell Density MOSFETs

HDTMOS technology brings high cell density with additional advantages such as greatly improved body diode performance. The technological advances are sufficiently great that they are fundamentally changing low voltage power transistor technology. This bulletin discusses high cell density technology and its benefits for the end user.

# CHAPTER 3
# MOSFET Case Outlines and Package Dimensions

# CASE OUTLINE AND PACKAGE DIMENSIONS

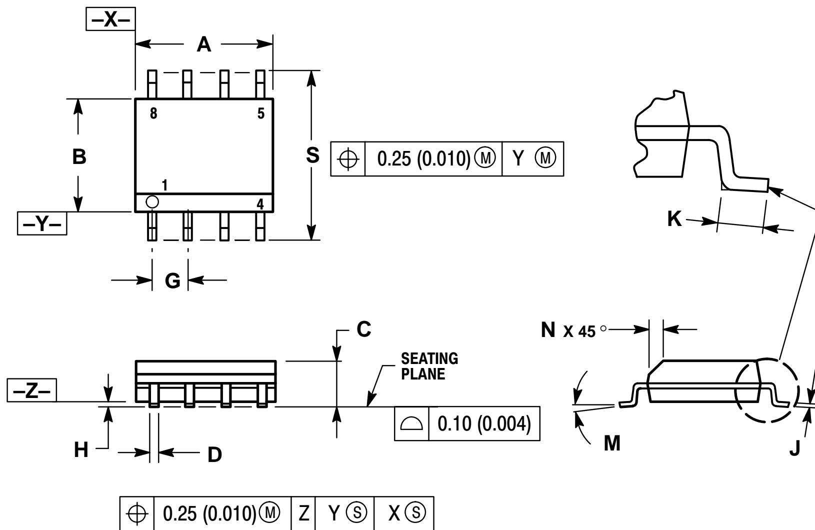
## CHIPFET
CASE 1206A–01
ISSUE A




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MOLD GATE BURRS SHALL NOT EXCEED 0.13 MM PER SIDE.
4. LEADFRAME TO MOLDED BODY OFFSET IN HORIZONTAL AND VERTICAL SHALL NOT EXCEED 0.08 MM.
5. DIMENSIONS A AND B EXCLUSIVE OF MOLD GATE BURRS.
6. NO MOLD FLASH ALLOWED ON THE TOP AND BOTTOM LEAD SURFACE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.95 | 3.10 | 0.116 | 0.122 |
| B | 1.55 | 1.70 | 0.061 | 0.067 |
| C | 1.00 | 1.10 | 0.039 | 0.043 |
| D | 0.25 | 0.35 | 0.010 | 0.014 |
| G | 0.65 BSC | | 0.025 BSC | |
| J | 0.10 | 0.15 | 0.004 | 0.008 |
| K | 0.30 | 0.45 | 0.012 | 0.018 |
| L | 0.55 BSC | | 0.022 BSC | |
| M | 5° NOM | | 5° NOM | |
| S | --- | 1.80 | --- | 0.071 |

## SO–8
CASE 751–07
ISSUE W

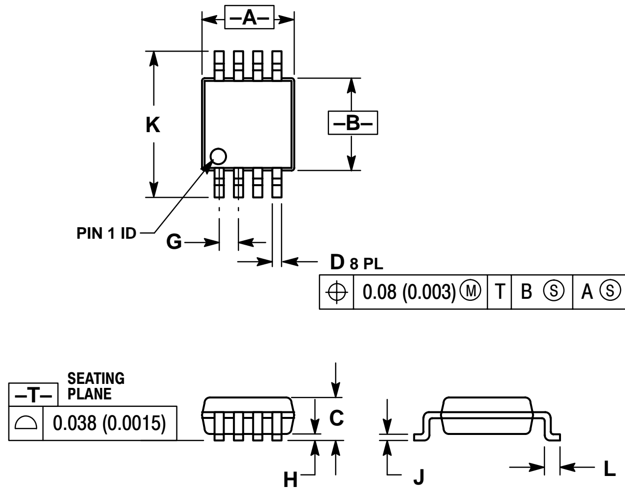



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0° | 8° | 0° | 8° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

# CASE OUTLINE AND PACKAGE DIMENSIONS

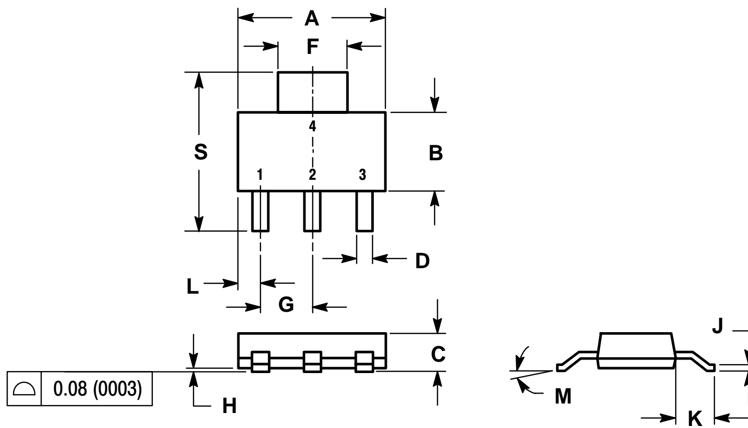
**Micro8**
CASE 846A–02
ISSUE E




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 2.90 | 3.10 | 0.114 | 0.122 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.25 | 0.40 | 0.010 | 0.016 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.05 | 0.15 | 0.002 | 0.006 |
| J | 0.13 | 0.23 | 0.005 | 0.009 |
| K | 4.75 | 5.05 | 0.187 | 0.199 |
| L | 0.40 | 0.70 | 0.016 | 0.028 |

**SOT–223 (TO–261)**
CASE 318E–04
ISSUE K

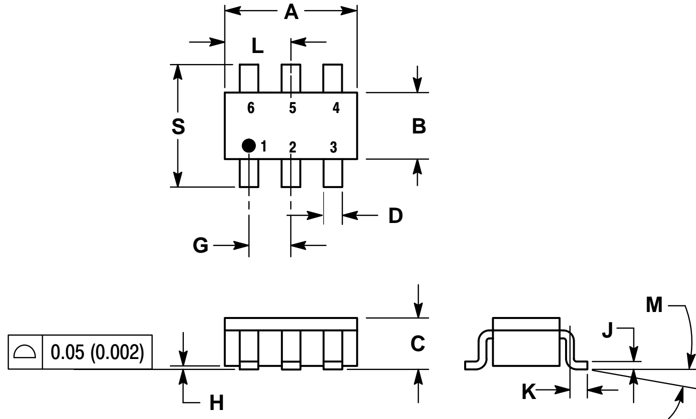



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.249 | 0.263 | 6.30 | 6.70 |
| B | 0.130 | 0.145 | 3.30 | 3.70 |
| C | 0.060 | 0.068 | 1.50 | 1.75 |
| D | 0.024 | 0.035 | 0.60 | 0.89 |
| F | 0.115 | 0.126 | 2.90 | 3.20 |
| G | 0.087 | 0.094 | 2.20 | 2.40 |
| H | 0.0008 | 0.0040 | 0.020 | 0.100 |
| J | 0.009 | 0.014 | 0.24 | 0.35 |
| K | 0.060 | 0.078 | 1.50 | 2.00 |
| L | 0.033 | 0.041 | 0.85 | 1.05 |
| M | 0° | 10° | 0° | 10° |
| S | 0.264 | 0.287 | 6.70 | 7.30 |

## CASE OUTLINE AND PACKAGE DIMENSIONS

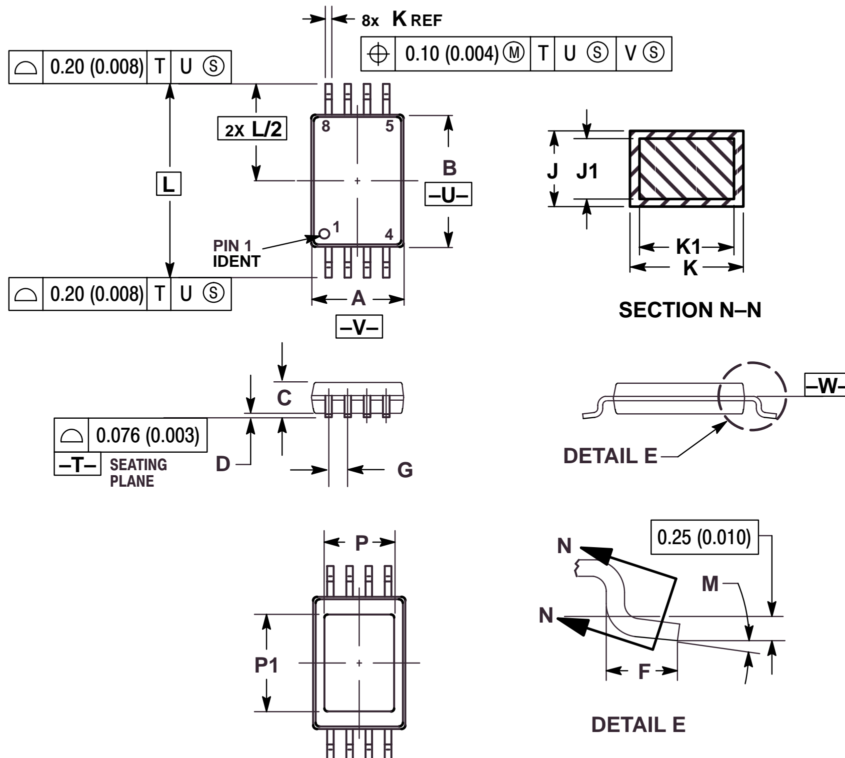
### TSOP–6
CASE 318G–02
ISSUE G




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.1142 | 0.1220 |
| B | 1.30 | 1.70 | 0.0512 | 0.0669 |
| C | 0.90 | 1.10 | 0.0354 | 0.0433 |
| D | 0.25 | 0.50 | 0.0098 | 0.0197 |
| G | 0.85 | 1.05 | 0.0335 | 0.0413 |
| H | 0.013 | 0.100 | 0.0005 | 0.0040 |
| J | 0.10 | 0.26 | 0.0040 | 0.0102 |
| K | 0.20 | 0.60 | 0.0079 | 0.0236 |
| L | 1.25 | 1.55 | 0.0493 | 0.0610 |
| M | 0 ° | 10 ° | 0 ° | 10 ° |
| S | 2.50 | 3.00 | 0.0985 | 0.1181 |

### TSSOP–8
CASE 948S–01
ISSUE O

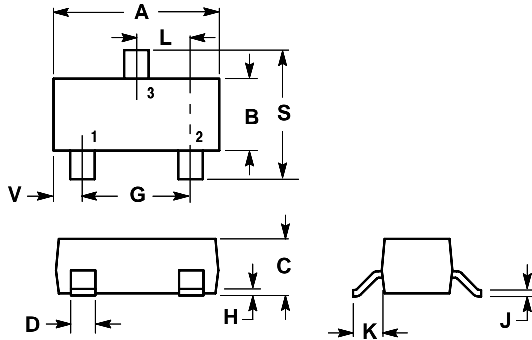



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 2.90 | 3.10 | 0.114 | 0.122 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.10 | --- | 0.043 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.70 | 0.020 | 0.028 |
| G | 0.65 BSC | | 0.026 BSC | |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| P | --- | 2.20 | --- | 0.087 |
| P1 | --- | 3.20 | --- | 0.126 |

# CASE OUTLINE AND PACKAGE DIMENSIONS

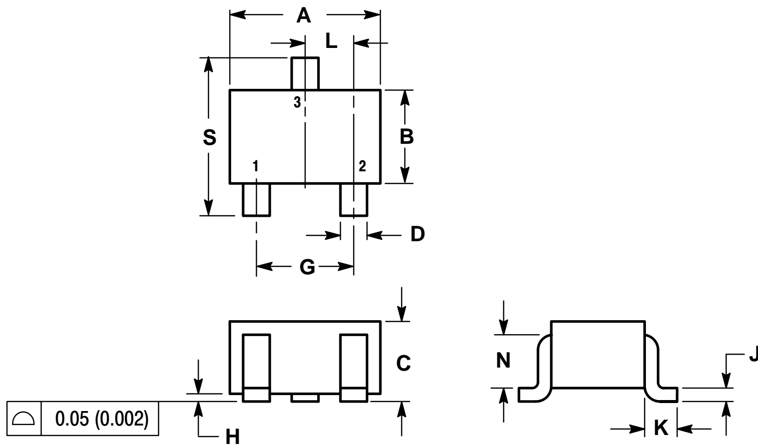
**SOT–23 (TO–236)**
CASE 318–08
ISSUE AF




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.1102 | 0.1197 | 2.80 | 3.04 |
| B | 0.0472 | 0.0551 | 1.20 | 1.40 |
| C | 0.0350 | 0.0440 | 0.89 | 1.11 |
| D | 0.0150 | 0.0200 | 0.37 | 0.50 |
| G | 0.0701 | 0.0807 | 1.78 | 2.04 |
| H | 0.0005 | 0.0040 | 0.013 | 0.100 |
| J | 0.0034 | 0.0070 | 0.085 | 0.177 |
| K | 0.0140 | 0.0285 | 0.35 | 0.69 |
| L | 0.0350 | 0.0401 | 0.89 | 1.02 |
| S | 0.0830 | 0.1039 | 2.10 | 2.64 |
| V | 0.0177 | 0.0236 | 0.45 | 0.60 |

**SC–70/SOT–323**
CASE 419–04
ISSUE L

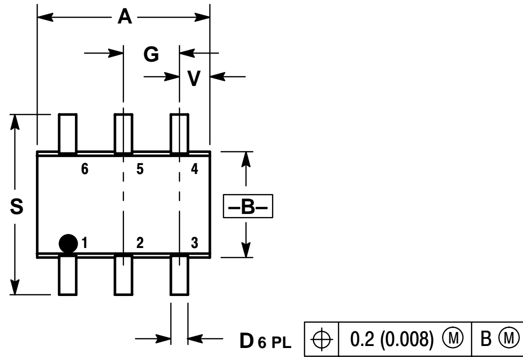



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.032 | 0.040 | 0.80 | 1.00 |
| D | 0.012 | 0.016 | 0.30 | 0.40 |
| G | 0.047 | 0.055 | 1.20 | 1.40 |
| H | 0.000 | 0.004 | 0.00 | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.017 REF | | 0.425 REF | |
| L | 0.026 BSC | | 0.650 BSC | |
| N | 0.028 REF | | 0.700 REF | |
| S | 0.079 | 0.095 | 2.00 | 2.40 |

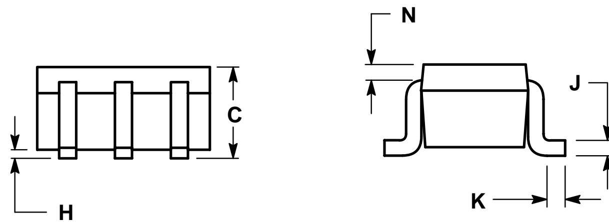
# CASE OUTLINE AND PACKAGE DIMENSIONS

## SC–88 (SOT–363)
CASE 419B–01
ISSUE G

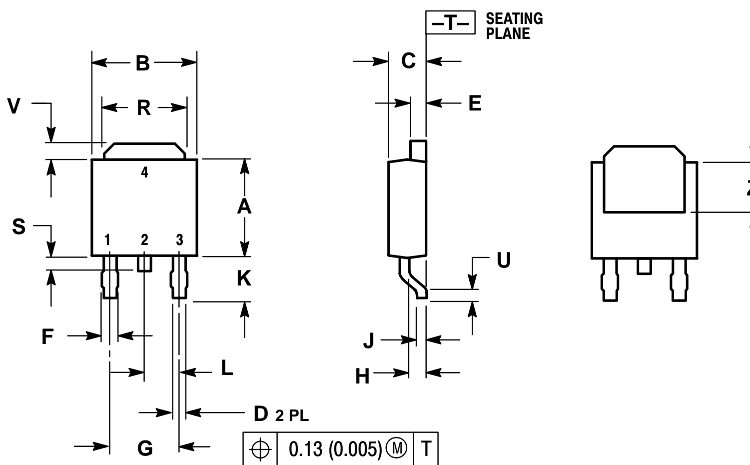



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.071 | 0.087 | 1.80 | 2.20 |
| B | 0.045 | 0.053 | 1.15 | 1.35 |
| C | 0.031 | 0.043 | 0.80 | 1.10 |
| D | 0.004 | 0.012 | 0.10 | 0.30 |
| G | 0.026 BSC | | 0.65 BSC | |
| H | --- | 0.004 | --- | 0.10 |
| J | 0.004 | 0.010 | 0.10 | 0.25 |
| K | 0.004 | 0.012 | 0.10 | 0.30 |
| N | 0.008 REF | | 0.20 REF | |
| S | 0.079 | 0.087 | 2.00 | 2.20 |
| V | 0.012 | 0.016 | 0.30 | 0.40 |




## DPAK
CASE 369A–13
ISSUE AA

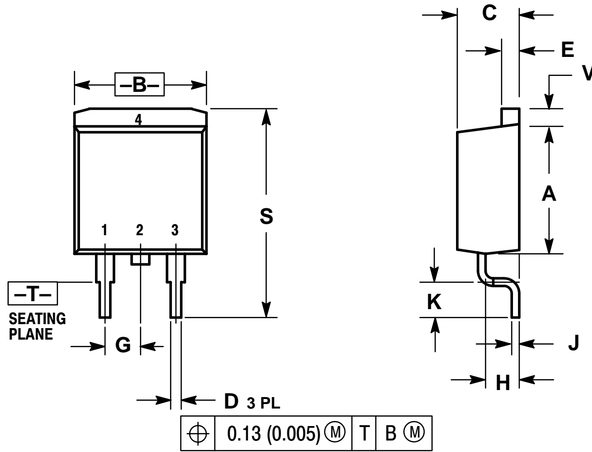



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.235 | 0.250 | 5.97 | 6.35 |
| B | 0.250 | 0.265 | 6.35 | 6.73 |
| C | 0.086 | 0.094 | 2.19 | 2.38 |
| D | 0.027 | 0.035 | 0.69 | 0.88 |
| E | 0.033 | 0.040 | 0.84 | 1.01 |
| F | 0.037 | 0.047 | 0.94 | 1.19 |
| G | 0.180 BSC | | 4.58 BSC | |
| H | 0.034 | 0.040 | 0.87 | 1.01 |
| J | 0.018 | 0.023 | 0.46 | 0.58 |
| K | 0.102 | 0.114 | 2.60 | 2.89 |
| L | 0.090 BSC | | 2.29 BSC | |
| R | 0.175 | 0.215 | 4.45 | 5.46 |
| S | 0.020 | 0.050 | 0.51 | 1.27 |
| U | 0.020 | --- | 0.51 | --- |
| V | 0.030 | 0.050 | 0.77 | 1.27 |
| Z | 0.138 | --- | 3.51 | --- |

# CASE OUTLINE AND PACKAGE DIMENSIONS

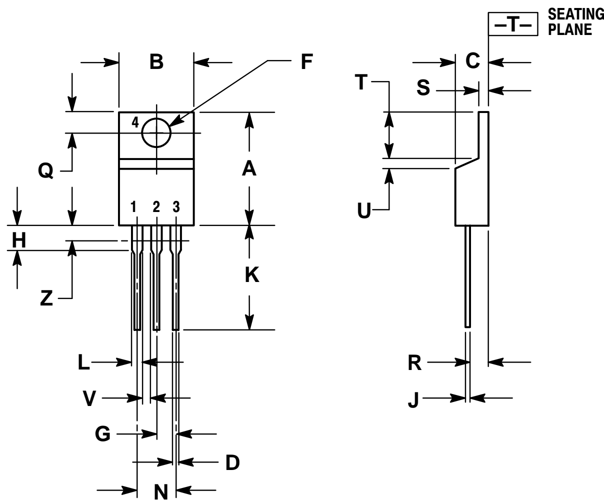
## D2PAK
CASE 418B–03
ISSUE D




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.035 | 0.51 | 0.89 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.080 | 0.110 | 2.03 | 2.79 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |

## TO–220 THREE–LEAD
## TO–220AB
CASE 221A–09
ISSUE AA

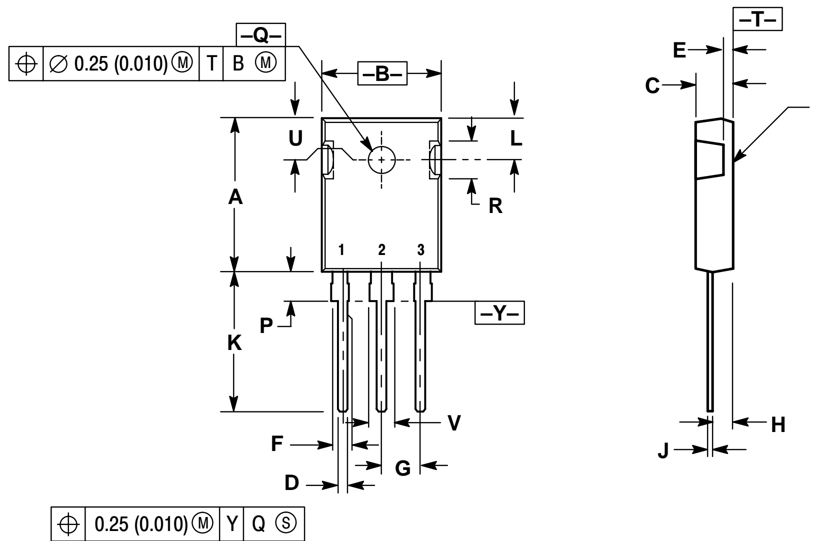



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

| DIM | INCHES MIN | INCHES MAX | MILLIMETERS MIN | MILLIMETERS MAX |
|---|---|---|---|---|
| A | 0.570 | 0.620 | 14.48 | 15.75 |
| B | 0.380 | 0.405 | 9.66 | 10.28 |
| C | 0.160 | 0.190 | 4.07 | 4.82 |
| D | 0.025 | 0.035 | 0.64 | 0.88 |
| F | 0.142 | 0.147 | 3.61 | 3.73 |
| G | 0.095 | 0.105 | 2.42 | 2.66 |
| H | 0.110 | 0.155 | 2.80 | 3.93 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.500 | 0.562 | 12.70 | 14.27 |
| L | 0.045 | 0.060 | 1.15 | 1.52 |
| N | 0.190 | 0.210 | 4.83 | 5.33 |
| Q | 0.100 | 0.120 | 2.54 | 3.04 |
| R | 0.080 | 0.110 | 2.04 | 2.79 |
| S | 0.045 | 0.055 | 1.15 | 1.39 |
| T | 0.235 | 0.255 | 5.97 | 6.47 |
| U | 0.000 | 0.050 | 0.00 | 1.27 |
| V | 0.045 | --- | 1.15 | --- |
| Z | --- | 0.080 | --- | 2.04 |

## CASE OUTLINE AND PACKAGE DIMENSIONS

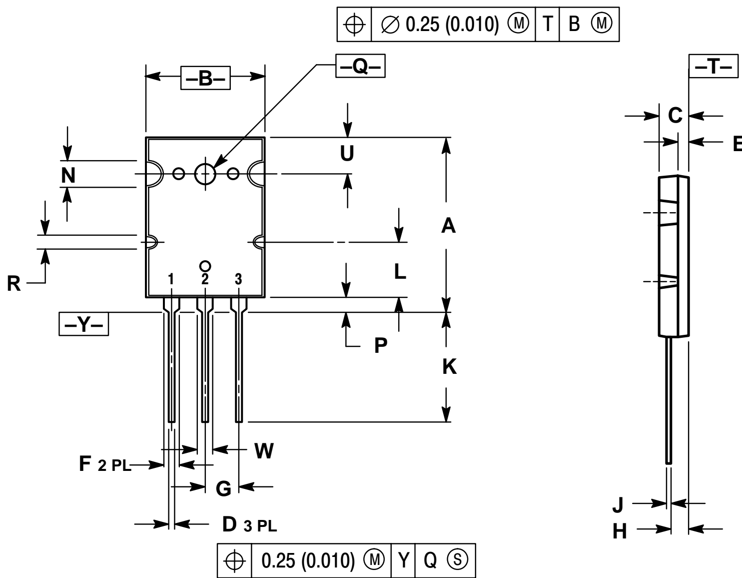
### TO–247
CASE 340K–01
ISSUE C




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 19.7 | 20.3 | 0.776 | 0.799 |
| B | 15.3 | 15.9 | 0.602 | 0.626 |
| C | 4.7 | 5.3 | 0.185 | 0.209 |
| D | 1.0 | 1.4 | 0.039 | 0.055 |
| E | 1.27 REF | | 0.050 REF | |
| F | 2.0 | 2.4 | 0.079 | 0.094 |
| G | 5.5 BSC | | 0.216 BSC | |
| H | 2.2 | 2.6 | 0.087 | 0.102 |
| J | 0.4 | 0.8 | 0.016 | 0.031 |
| K | 14.2 | 14.8 | 0.559 | 0.583 |
| L | 5.5 NOM | | 0.217 NOM | |
| P | 3.7 | 4.3 | 0.146 | 0.169 |
| Q | 3.55 | 3.65 | 0.140 | 0.144 |
| R | 5.0 NOM | | 0.197 NOM | |
| U | 5.5 BSC | | 0.217 BSC | |
| V | 3.0 | 3.4 | 0.118 | 0.134 |

### TO–264
CASE 340G–02
ISSUE H

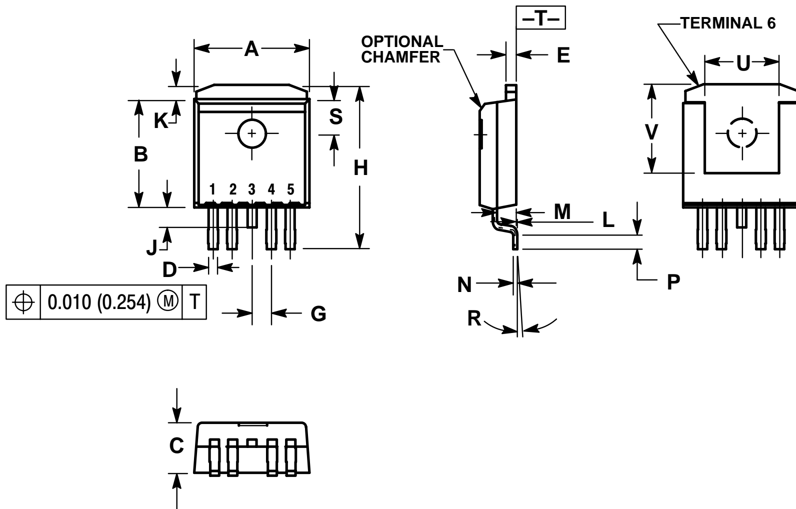



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 28.0 | 29.0 | 1.102 | 1.142 |
| B | 19.3 | 20.3 | 0.760 | 0.800 |
| C | 4.7 | 5.3 | 0.185 | 0.209 |
| D | 0.93 | 1.48 | 0.037 | 0.058 |
| E | 1.9 | 2.1 | 0.075 | 0.083 |
| F | 2.2 | 2.4 | 0.087 | 0.102 |
| G | 5.45 BSC | | 0.215 BSC | |
| H | 2.6 | 3.0 | 0.102 | 0.118 |
| J | 0.43 | 0.78 | 0.017 | 0.031 |
| K | 17.6 | 18.8 | 0.693 | 0.740 |
| L | 11.0 | 11.4 | 0.433 | 0.449 |
| N | 3.95 | 4.75 | 0.156 | 0.187 |
| P | 2.2 | 2.6 | 0.087 | 0.102 |
| Q | 3.1 | 3.5 | 0.122 | 0.137 |
| R | 2.15 | 2.35 | 0.085 | 0.093 |
| U | 6.1 | 6.5 | 0.240 | 0.256 |
| W | 2.8 | 3.2 | 0.110 | 0.125 |

# CASE OUTLINE AND PACKAGE DIMENSIONS

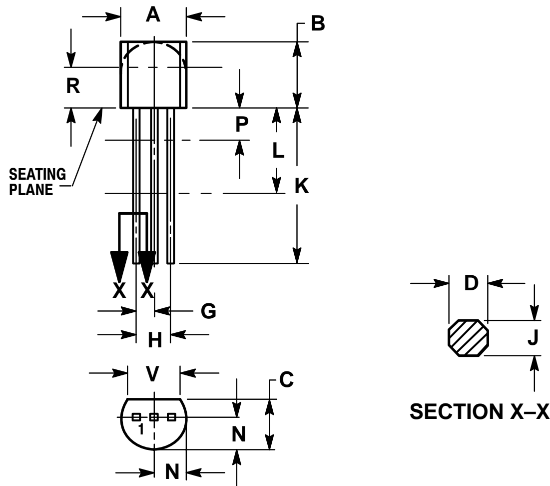
**DPAK**
CASE 936D–03
ISSUE B




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. TAB CONTOUR OPTIONAL WITHIN DIMENSIONS A AND K.
4. DIMENSIONS U AND V ESTABLISH A MINIMUM MOUNTING SURFACE FOR TERMINAL 6.
5. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH OR GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.025 (0.635) MAXIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.386 | 0.403 | 9.804 | 10.236 |
| B | 0.356 | 0.368 | 9.042 | 9.347 |
| C | 0.170 | 0.180 | 4.318 | 4.572 |
| D | 0.026 | 0.036 | 0.660 | 0.914 |
| E | 0.045 | 0.055 | 1.143 | 1.397 |
| G | 0.067 BSC | | 1.702 BSC | |
| H | 0.539 | 0.579 | 13.691 | 14.707 |
| J | 0.125 MAX | | 3.175 MAX | |
| K | 0.050 REF | | 1.270 REF | |
| L | 0.000 | 0.010 | 0.000 | 0.254 |
| M | 0.088 | 0.102 | 2.235 | 2.591 |
| N | 0.018 | 0.026 | 0.457 | 0.660 |
| P | 0.058 | 0.078 | 1.473 | 1.981 |
| R | 5° REF | | 5° REF | |
| S | 0.116 REF | | 2.946 REF | |
| U | 0.200 MIN | | 5.080 MIN | |
| V | 0.250 MIN | | 6.350 MIN | |

**TO–92**
CASE 29–11
ISSUE AL




D
J
SECTION X–X

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.175 | 0.205 | 4.45 | 5.20 |
| B | 0.170 | 0.210 | 4.32 | 5.33 |
| C | 0.125 | 0.165 | 3.18 | 4.19 |
| D | 0.016 | 0.021 | 0.407 | 0.533 |
| G | 0.045 | 0.055 | 1.15 | 1.39 |
| H | 0.095 | 0.105 | 2.42 | 2.66 |
| J | 0.015 | 0.020 | 0.39 | 0.50 |
| K | 0.500 | --- | 12.70 | --- |
| L | 0.250 | --- | 6.35 | --- |
| N | 0.080 | 0.105 | 2.04 | 2.66 |
| P | --- | 0.100 | --- | 2.54 |
| R | 0.115 | --- | 2.93 | --- |
| V | 0.135 | --- | 3.43 | --- |

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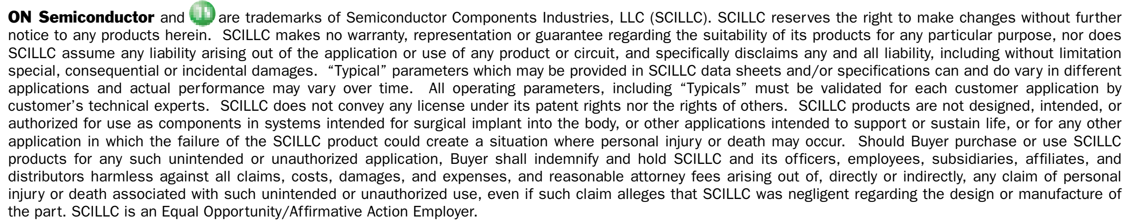
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